

The document and process conversion measures necessary to comply with this revision shall be completed by 31 December 1997.

INCH-POUND

MIL-PRF-55110F  
31 May 1997  
SUPERSEDING  
MIL-PRF-55110E  
31 December 1993  
(See 6.6)

PERFORMANCE SPECIFICATION  
PRINTED WIRING BOARD, RIGID  
GENERAL SPECIFICATION FOR

Inactive for new design after 31 December 1997.  
For new design use MIL-PRF-31032.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the performance and qualification requirements for rigid single-sided, double-sided, and multilayer printed wiring boards with or without plated through holes (see 6.1). Verification is accomplished through the use of one of two methods of product assurance (appendix A or appendix B). Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use are specified in the applicable master drawing.

1.2 Classification. Printed wiring boards are classified by 1.2.1 and 1.2.2.

1.2.1 Type. Printed wiring boards are of the types shown, as specified

- Type 1 - Single-sided printed wiring board (see A.6.4.6.1).
- Type 2 - Double-sided printed wiring board (see A.6.4.6.2).
- Type 3 - Multilayer printed wiring board (see A.6.4.6.3).

1.2.2 Base material type. The printed wiring board base material type should be identified by the base material designators of the applicable base material specification (see 6.6.5) as required by the master drawing (see 3.1.1).

1.3 Description of this specification. The main body contains general provisions and is supplemented by detailed appendices. Appendices A and B describe the two product assurance programs that can be implemented by the manufacturer. Appendix A contains the traditional QPL product assurance program. Appendix B is an optional quality management approach using a quality review board concept addressed in MIL-PRF-31032, to modify the generic verification criteria provided in this specification. Appendix C provides statistical sampling, and basic test and inspection procedures. Appendix D is optional and can be used when producing printed wiring boards designed to superseded design standards (see 6.4.1). Appendix D may also be used as a guide in developing a test plan for legacy or existing designs based on the tests and inspections of appendix A. Appendix E is optional and describes an alternative procedure used to evaluate oxidation levels on solderable surfaces. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center Columbus ATTN: DSCC-VAC, 3990 East Broad Street, Columbus, OH 43213-1152 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5998

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see 6.2).

### INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS

IPC-T-50 - Terms and Definitions. (DoD adopted)

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General requirements. The manufacturer of printed wiring boards, in compliance with this specification, shall use or have access to production and verification facilities adequate to assure successful compliance with the provisions of this specification and the associated master drawing. Only printed wiring boards which are verified and meet all the applicable performance requirements and the design, construction, and material requirement of the associated master drawing shall be certified as compliant and delivered.

3.1.1 Master drawing. Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing.

3.1.2 Conflicting requirements. In the event of conflict between the requirements of this specification and other requirements of the applicable master drawing, the precedence in which documents shall govern, in descending order, is as follows:

- a. The applicable master drawing (see 3.1.1). Additional acquisition requirements (see 6.2) may be provided in the purchase order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the qualifying activity, will result in the printed wiring board being deemed noncompliant with this specification.
- b. This specification.
- c. The applicable design standard (see A.3.3).
- d. Specifications, standards, and other documents referenced in section 2.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC-T-50 and those contained herein (see 6.4, and appendices A, B, C, D, and E).

3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see 4.5 and 6.3). In addition, the manufacturer shall certify (for QPL) or receive certification from the qualifying activity (for QPL/QML) that the product assurance requirements of 3.3 have been met and are being maintained.

3.2.1 QPL. The qualification requirements for the QPL product assurance level shall be in accordance with appendix A.

3.2.2 QPL/QML. The qualification requirements for the QPL/QML product assurance level shall be in accordance with appendix B.

3.3 Product assurance requirements. This document contains two different methods of product assurance for printed wiring board compliance. The two levels of printed wiring product assurance are QPL (see 3.3.1) and QPL/QML (see 3.3.2) as defined below.

3.3.1 QPL product assurance. Product assurance procedures (see A.4.5.5.2) shall be made available to the qualifying activity no later than 6 months after the date of this specification in order for the manufacturer to be retained on QPL No. 55110. The product assurance procedures shall, as a minimum, consist of the items outlined in appendix A.

3.3.2 QPL/QML product assurance. A product assurance program for QPL/QML printed wiring board furnished under this specification shall satisfy the requirements of appendix B.

3.4 Letters of interpretation and policy. Letters of interpretation and policy applicable to this document shall be approved in writing by the preparing activity. All letters of interpretation and policy applicable to MIL-P-55110 or MIL-PRF-55110, written prior to the current date of this document are not applicable to this revision. All subsequent letters of interpretation and policy letters are valid only until the next document change action (amendment or revision).

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.3).
- b. Inspection of product for delivery (see A.4.6 or B.5.1).
- c. Periodic conformance inspection (see A.4.7 or B.5.1).

#### 4.2 Printed wiring board performance verification.

4.2.1 QPL. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and the quality conformance test circuitry or test coupons referenced in appendix A.

4.2.2 QPL/QML. The minimum requirements for printed wiring board performance verification to the QPL/QML product assurance level shall satisfy the guidelines of appendix B.

4.3 Qualification inspection (see 6.3). Qualification is possible by two different methods based on the product assurance level used, QPL (see 4.3.1) or QPL/QML (see 4.3.2).

4.3.1 QPL. Qualification inspection for the QPL product assurance level shall be performed at a laboratory acceptable to the Government (see A.6.6) on qualification test specimens produced with material, equipment, and procedures that will be used in subsequent production. The requirements concerning the qualification test specimens, number of specimens to be tested, and the test routines they shall be subjected to, and the extent of qualification shall be as specified in appendix A.

4.3.2 QPL/QML. The minimum requirements for qualification to the QPL/QML product assurance level shall be as specified in appendix B.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with the purchase order or contract (see 6.2).

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Printed wiring boards are intended primarily for use in electronic and electrical equipment to eliminate high density hand wiring, where space is limited and where compact packaging is desirable.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.
- b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1 and 2.2).
- c. Appropriate type (see 1.2.1) and base material designation (see 1.2.2).
- d. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see 3.1).
- e. Levels of preservation and packing required.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Products List (QPL) No. 55110 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. The activity responsible for QPL No. 55110 is the Defense Supply Center Columbus (DSCC-VQE), 3990 East Broad Street, Columbus, Ohio 43216-5000. Application procedures should conform to the guidelines of SD-6, "Provisions Governing Qualification" (see 6.3.3).

6.3.1 Transference of qualification. Manufacturers currently qualified to MIL-PRF-55110E will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL-PRF-55110E as applicable. New applications for qualification (after the date of this document) must be performed to the requirements of this revision.

6.3.2 Discussion. MIL-P-55110C certification program (CML-1 through CML-11) was not governed by the policies and procedures of the Defense Standardization Program as defined by DoD 4120.3-M and therefore does not exist within the QPL program of MIL-P-55110D and beyond. For additional information concerning this issue, see MIL-P-55110C, paragraph 60.1. Verification Conformance Inspection (VCI, see 6.4.3.4) option 1 (see appendix D) is offered in this document as an alternative to MIL-P-55110C. Manufacturer's are encouraged to examine and compare appendix D and its various VCI options.

6.3.3 "Provisions Governing Qualification". Copies of SD-6, "Provisions Governing Qualification", may be obtained upon application to Commanding Officer, Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.

#### 6.4 Terms and definitions.

6.4.1 Design standard. A document that establishes the baseline parameters (default values), standard practices and guidelines for the design of printed wiring boards. Within this document, the term "design standard" is used to describe the document (other than the master drawing) that contains these design, construction, material, and test coupon requirements and guidelines used to produce panels of printed wiring boards.

6.4.3 Product assurance. The method of complying with the two different levels of this document using either the QPL method (that has been internal to this document since MIL-P-55110D) or the new method QPL/QML (introduced by this revision).

6.4.3.1 QML (Qualified Manufacturers List). A list of manufacturers, by name and plant address, who have met the certification and qualification requirements stated in MIL-PRF-31032. A QML focuses on qualifying an envelope of materials and processes rather than individual product(s). That envelope is qualified by carefully selecting representative worst case test vehicles or representative samples from production that contain all potential combinations of materials and processes that may be subsequently used during production. A QML is normally appropriate for items of supply that have very rapid technological advancement or a myriad of variations or custom designs that make individual product qualifications impractical or excessively expensive.

6.4.3.2 QPL (Qualified Products List). A QPL focuses on qualifying individual products or families of products. A QPL will normally be appropriate for items of supply that are stable and will be continually available for extended period of time.

6.4.3.3 QPL/QML. A transitional program that allows a manufacturer that is certified and qualified to the QML program of MIL-PRF-31032 to fabricate, test and supply products to this revision of this document.

6.4.3.4 Verification Conformance Inspection (VCI). See D.3.4.

6.5 Compliant printed wiring boards. For a printed wiring board to be compliant with this document, it must be produced by a manufacturer qualified for listing on QPL No. 55110 or reciprocal listing as described in appendix B, and must be obtained from a lot which was subjected to and passed all inspection of product for delivery using the applicable Verification Conformance Inspection (VCI) option.

#### 6.6 Supersession.

6.6.1 Design, construction and verification. Design, construction and verification supersession information is included in appendix D of this document.

6.6.2 Reference to superseded specifications. All the requirements of this document can be interchangeable with those documents identified as MIL-P-55110. Therefore, existing documents (master drawings or OEM documents) referencing MIL-P-55110 need not be revised, updated or changed to make reference to MIL-PRF-55110 in order for this document to be used.

6.6.3 Design detail. This document does not contained detailed design requirements such as minimum annular ring, minimum dielectric spacing, minimum coating or plating (copper or finish) thickness, etc., as previous revisions of MIL-P-55110. A majority of these design specific requirements were a duplication of the information already contained in MIL-STD-275 (canceled April 21, 1995), the legacy design standard for previous revisions of this document, or IPC-D-275.

6.6.4 Diagrams and figures. Most diagrams and figures that were in previous revisions of MIL-P-55110 have been eliminated from this document. See Appendix A for guidance concerning diagrams and figures.

6.6.5 Base material identifiers and designators. Within this document, certain base material identifiers and designators associated with MIL-S-13949 have been used in the past for standardization purposes. These same MIL-S-13949 identifiers and designators are currently used on QPL-55110. Since the issuance of MIL-PRF-55110, base material not conforming to MIL-S-13949 can be used to supply (once qualified), printed wiring board designs to this document. These non-standard base material identifiers and designators will be listed on QPL-55110 and or cross-referenced to MIL-S-13949 as needed.

6.6.6 Performance specifications and design solutions. The removal of all design, material and construction detail from this document was not undertaken to shift design responsibility from printed wiring board designers onto printed wiring board manufacturers. Under the requirements for DoD performance specifications, no design solutions are to be contained within the DoD performance document, only critical form, fit or function parameters. Design solutions are dictated by the design activity by detailed drawing such as the master drawing.

6.7 Design standards. This document contains guidelines for the testing or printed wiring boards that were designed to and or use test coupons conforming to either IPC-D-275 or various revisions of MIL-STD-275. See appendix D for additional guidance regarding the verification of panels using different design standards.

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

6.9 Subject term (key word) listing.

- Design standard
- Master drawing
- Qualified Manufacturer List (QML)
- Qualified Product List (QPL)
- Test coupon
- Verification conformance inspection

APPENDIX A

PRODUCT ASSURANCE (QUALIFICATION AND VERIFICATION) REQUIREMENTS  
FOR QUALIFIED PRODUCTS LIST (QPL) PROGRAMS

A.1. SCOPE

A.1.1 Scope. This appendix contains the requirements and procedures for manufacturers using the traditional QPL method of product assurance (qualification and verification inspection) for printed wiring boards covered by this specification. The process for extending and retaining qualification is also herein. This appendix is a mandatory part of this specification for non-QML manufacturers and the information contained herein is intended for compliance.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see A.6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-S-13949 - Sheet, Printed Wiring Board, General Specification for.

(Unless otherwise indicated, copies of Department of Defense documents are available from the Defense Printing Services Detachment Office, Building 4D (Customer Services), 700 Tabor Avenue, Philadelphia, PA 19111-5094.)

A.2.2 Non-Government publications. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issue of the documents cited in the solicitation (see A.6.2).

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

J-STD-003 - Solderability Tests for Printed Boards.  
IPC-D-275 - Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies. (DoD adopted)  
IPC-A-600 - Acceptability of Printed Boards.  
IPC-TM-650 - Test Methods Manual. (DoD Adopted)  
IPC-100041 - Master Drawing for Single Sided Printed Boards.  
IPC-100042 - Master Drawing for Double Sided Printed Boards.  
IPC-100043 - Master Drawing for 10 Layer Multilayer Printed Boards.  
IPC-100046 - Composite Test Pattern Basic Dimension Drawing (One/Two Layers).  
IPC-100047 - Composite Test Pattern Basic Dimension Drawing (Ten Layers).

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135.)

NATIONAL CONFERENCE OF STANDARDS LABORATORIES

NCSL Z540 - General Requirements for Calibration Laboratories and Measuring and Test Equipment.

(Application for copies should be addressed to the National Conference of Standards Laboratories, 1800 30th Street, Suite 305B, Boulder, CO 80301-1032.)

## APPENDIX A

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

**A.2.3 Order of precedence.** In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

**A.3 REQUIREMENTS**

**A.3.1 General.** The performance requirements contained in this section, although determined by examination of sampled printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

**A.3.1.1 Master drawing (see A.6.2.1d).** Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing. For the purposes of this appendix, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable master drawing.

**A.3.2 Qualification.** Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see A.4.5 and 6.3). In addition, the manufacturer shall certify that the product assurance requirements of A.4.5.5.2 have been met and are being maintained.

**A.3.3 Design standard (see A.6.2.1e).** Unless otherwise specified (see A.3.1.1), if individual design details are not specified on the applicable master drawing, then the baseline design parameters shall be as specified in the design standard that was used to design the printed wiring board. If no design standard is specified on the master drawing or the appropriate design standard cannot be determined, use IPC-D-275, class 3.

**A.3.4 Material.** The printed wiring boards shall be constructed of material as specified (see A.3.1.1). When a definite material is not specified (see A.3.1.1), a material shall be used that will enable the printed wiring board to meet the performance requirements of this specification. Acceptance or approval of any material shall not be construed as a guarantee of the acceptance of the finished printed wiring board.

**A.3.5 Visual and dimensional requirements.** IPC-A-600 contains figures and illustrations that can be useful in visualizing the accept/reject requirements listed below.

**A.3.5.1 Base material defects.**

**A.3.5.1.1 Edges of base material.** Defects such as burrs, nicks, and haloing along the edges of printed wiring boards shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1).

**A.3.5.1.2 Surface imperfections.** Surface imperfections (such as scratches, pits, dents, cuts or exposed reinforcement material fibers and weave texture) shall be acceptable providing the imperfection meets the following:

- a. The imperfection does not bridge between conductors (weave texture may bridge conductors).
- b. The dielectric spacing between the imperfection and conductors is not reduced below the specified minimum requirements (see A.3.1.1).

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A.3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

- a. The imperfection is translucent.
- b. The imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.
- c. The imperfection does not reduce conductor spacing below the minimum requirements specified (see A.3.1.1).
- d. The imperfection does not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).

Note: Color variations or mottled appearance in bond enhancement treatments shall be acceptable.

A.3.5.1.3.1 Foreign inclusions. Foreign inclusions shall be permitted when they meet the following:

- a. The inclusions are translucent or are located no less than the minimum spacing from or at least .010 inch (0.25 mm) from the nearest conductor, whichever is less.
- b. The inclusion does not reduce conductor spacing by more than 50 percent.
- c. The longest dimension is no greater than .032 inch (0.81 mm) in non-circuitry areas.

A.3.5.1.3.2 Subsurface spots. Subsurface spots shall be permitted when they meet any of the following:

- a. The spots are translucent.
- b. The spots are known to be weave texture other than delamination or disbonding.
- c. The spots are isolated white spots that are at least .010 inch (0.25 mm) from the nearest conductor or that do not propagate as a result of any soldering operation (gelation particles are acceptable regardless of location).

A.3.5.2 Conductive pattern.

A.3.5.2.1 Annular ring, external. The minimum external annular ring shall be as specified (see A.3.1.1). Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the minimum external annular ring specified (see A.3.1.1), due to defects such as pits, dents, nicks, and pinholes.

A.3.5.2.2 Conductor spacing. The conductor spacing(s) shall be as specified (see A.3.1.1).

A.3.5.2.3 Conductor width. The conductor width(s) shall be as specified (see A.3.1.1).

A.3.5.2.4 Conductive pattern imperfections. The conductive pattern shall contain no cracks, splits or tears. Unless otherwise specified (see A.3.1.1), any combination of edge roughness, nicks, pinholes, cuts or scratches exposing the base material shall not reduce each conductor width more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than .50 inch (12.70 mm) or 10 percent of a conductor length, whichever is less.

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A.3.5.2.5 Conductor finish coverage. The conductor finish plating or coating shall completely cover the basis metal of the conductive pattern. Complete conductor coverage by solder does not apply to the vertical conductor edges. There shall be no evidence of any lifting or separation of conductor finish plating or coating from the surface of the conductive pattern. There shall be no whiskers of solder or plating on the surface of the conductive pattern. For designs using solder resist over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder resist and the basis metal conductor finish. For design requiring unfused tin-lead plating as a final conductor finish coverage, the thickness shall be as specified (see A.3.1.1 and A.3.3).

A.3.5.3 Dimensions. The finished printed wiring board shall meet the dimensional (such as cutouts, overall thickness, periphery, etc.) requirements specified (see A.3.1.1).

A.3.5.4 Hole pattern accuracy. The accuracy of the hole pattern (size and location) on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.5 Lifted lands. There shall be no lifted lands on the deliverable (non-stressed) printed wiring board.

A.3.5.6 Registration external (method I)(types 1 and 2). Layer-to-layer misregistration shall not reduce the minimum external annular ring below its specified (see A.3.1.1) limits.

A.3.5.7 Solder resist. Unless otherwise specified, the solder resist conditions below shall apply.

A.3.5.7.1 Coverage. Solder resist coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the imperfection meets all of the following:

- a. The solder resist imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.
- b. In areas containing parallel conductors, the solder resist imperfection shall not expose two isolated conductors whose spacing is less than .020 inch (0.5 mm) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.
- c. The exposed conductor shall not be bare copper.
- d. The solder resist imperfection does not expose tented via holes.

A.3.5.7.2 Discoloration. Discoloration of metallic surfaces under the cured solder resist is acceptable.

A.3.5.7.3 Registration. The solder resist shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If no requirements are specified, the following apply:

- a. For surface mount lands with no plated-through holes, the following shall apply:
  - 1) For lands with a pitch of .050 inch (.125 mm) or greater, solder resist encroachment onto the land shall not exceed .002 inch (0.050 mm).
  - 2) For lands with a pitch less than .050 inch (.125 mm), solder resist encroachment is on one side of land only and shall not exceed .001 inch (0.025 mm).

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b. For plated-through holes and vias, the following shall apply:

- 1) Solder resist misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.
- 2) Solder resist shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers or lands of unplated holes) to which solder connections will be made.
- 3) Solder resist is permitted in plated-through vias or holes in which no lead is to be soldered.

c. Edge board connectors and test points which are intended for assembly testing shall be free of solder resist unless a partial coverage allowance is specified.

A.3.5.7.4 Thickness. The solder resist thickness shall be as specified (see A.3.1.1).

A.3.6 Plated-through hole requirements. IPC-A-600 contains figures and illustrations that can be useful in visualizing the accept/reject requirements listed below.

A.3.6.1 Annular ring, internal (type 3). The minimum annular ring for functional internal lands on type 3 printed wiring boards shall be as specified (see A.3.1.1).

A.3.6.2 Conductor thickness. The conductor thickness shall be as specified (see A.3.1.1). When a copper foil weight requirement is specified, a reduction in thickness up to 10 percent below the minimum allowable foil thickness specified by the applicable material specification shall be considered acceptable in order to accommodate a processing allowance for cleaning either by chemical or mechanical means.

A.3.6.3 Dielectric layer thickness. The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1).

A.3.6.3.1 Thermal planes. The minimum lateral spacing between adjacent conductive surfaces (nonfunctional pads) or plated-through hole and the thermal plane shall be as specified (see A.3.1.1).

A.3.6.4 Delamination. Printed wiring boards shall have no delaminations in excess of that allowed in A.3.5.1.3.

A.3.6.5 Etchback or smear removal (type 3).

A.3.6.5.1 Etchback (when specified, see A.3.1.1). When specified (see A.3.1.1), printed wiring boards shall be etched back for the lateral removal of resin and reinforcement material (woven glass or other media) from the internal conductors of the hole walls prior to plating. The etchback shall be effective on the vertical face and at least the top or bottom (horizontal) surface of each internal conductor. Negative etchback is not acceptable when etchback is specified (see A.3.1.1).

A.3.6.5.1.1 Etchback limits. Unless otherwise specified (see A.3.1.1), the etchback shall be .0002 inch (0.005 mm) minimum and .003 inch (0.08 mm) maximum when measured at the internal copper contact area protrusion with a preferred depth of .0005 inch (.013 mm).

NOTE: Etchback greater than .002 inch (0.05 mm) may cause fold or voids in the plating.

A.3.6.5.2 Smear removal (hole cleaning). When etchback is not specified (see A.3.1.1), the vertical faces of the internal conductors of the plated-through hole shall be cleaned to be free of resin smear. Lateral removal of base material from the hole wall shall not exceed .001 inch (0.03 mm). When etchback is not specified (see A.3.1.1), a negative etchback of .0005 inch (0.013 mm) maximum shall be acceptable.

## APPENDIX A

**A.3.6.6 Laminate voids.**

A.3.6.6.1 As received condition. Laminate voids with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable.

A.3.6.6.2 After rework simulation, thermal shock or thermal stress testing. Laminate voids are not evaluated in zone A. Laminate voids in zone B with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified (see A.3.1.1).

**A.3.6.7 Lifted lands.**

A.3.6.7.1 As received condition. There shall be no lifted lands on the as received specimen (see A.3.5.5). When inspected in accordance with A.4.8.2 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with A.4.8.1 for separation of the lands from the base material.

A.3.6.7.2 After rework simulation, thermal shock or thermal stress testing. After undergoing rework simulation, thermal shock or thermal stress testing (see A.3.7.4.4, A.3.7.4.8, and A.3.7.6.2), the maximum allowed distance from the base material surface to the bottom of the edge of the land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and copper plating on that land.

**A.3.6.8 Plating and coating thickness.**

A.3.6.8.1 Conductor finish thickness. The conductor finish plating or coating thickness shall be as specified (see A.3.1.1)(Also see A.3.5.2.5).

A.3.6.8.2 Copper plating thickness (when applicable). The copper plating thickness (in plated-through holes and on the surface) shall be as specified (see A.3.1.1).

A.3.6.9 Copper plating defects. Unless otherwise specified (see A.3.1.1), a 20 percent reduction of the specified copper plating thickness (see A.3.6.8.2) shall be acceptable. Any 20 percent thickness reduction shall be isolated (non-continuous). Any copper plating less than 80 percent of the specified thickness shall be treated as a void.

A.3.6.9.1 Copper plating voids. The copper plating in the plated-through holes shall not exhibit any void in excess of the following:

- a. There shall be no more than one plating void per panel, regardless of length or size.
- b. There shall be no plating void in excess of 5 percent of the total printed wiring board thickness.
- c. There shall be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

A.3.6.9.2 Separations. Except for along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable. Anomalies resulting from this separation shall not be cause for rejection (see A.6.4.3).

A.3.6.10 Hole wall deficiencies. Nodules, plating folds, or plated glass fiber protrusions that project into the plated-through hole shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below their specified limits (see A.3.1.1).

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A.3.6.11 Metallic cracks.

A.3.6.11.1 External layers. Cracks in outer layer metal foil shall be acceptable if the crack(s) do not propagate into the plated copper. Cracks shall not be acceptable in the outer copper plating.

A.3.6.11.2 Internal layers. There shall be no cracks in the internal layer conductive foils, platings, or coatings.

A.3.6.12 Nail-heading. Nail-heading of conductors shall not exceed 1.5 times the copper foil thickness.

A.3.6.13 Resin recession.

A.3.6.13.1 As received condition. Resin recession at the outer surface of the plated-through hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (0.08 mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

A.3.6.13.2 After rework simulation, thermal shock or thermal stress testing. Resin recession at the outer surface of the plated-through hole barrel shall be permitted and is not cause for rejection.

A.3.6.14 Wicking. Wicking of copper plating extending .003 inch (0.08 mm) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1).

A.3.6.15 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.7 Inspection requirements. The detailed requirements contained in this section, although determined by examination of sample printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.7.1 Acceptability (of printed wiring boards). When examined as specified in A.4.8.1, the printed wiring boards shall be in accordance with the design and construction specified in A.3.1.1 (master drawing) and A.3.4 (material), and meet the acceptance requirements specified in A.3.5 (visual and dimensional), A.3.8 (marking), and A.3.11 (workmanship), as applicable.

A.3.7.2 Microsection evaluation (of printed wiring test specimens). When printed wiring board test specimens (finished printed wiring boards, supporting test coupons, or qualification test specimens) are microsectioned and examined as specified in A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.7.2.1 As received. After meeting the requirements of A.3.8 and A.3.11 when inspected in accordance with A.4.8.1, the as received printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.6.

A.3.7.2.2 Registration internal (type 3).

A.3.7.2.2.1 By microsection (method II). Unless otherwise specified (see A.3.1.1), when inspected as specified in A.4.8.2.2, the layer-to-layer pattern misregistration shall not reduce the minimum internal annular ring below its specified (see A.3.1.1) limits.

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A.3.7.2.2.2 By registration test coupons (method III). Registration test coupons may have been designed into the printed wiring board by the design activity, or may be added to the panel by the manufacturer to enhance testability (see A.4.8.2.2.2 and appendix D). To be usable for acceptance purposes, registration test coupons must relate the actual grid location of each circuitry layer to all other circuitry layers and to the hole pattern accuracy required (see A.3.5.4) in each printed wiring board.

A.3.7.3 Chemical requirements.

A.3.7.3.1 Cleanliness. When printed wiring boards are tested in accordance with A.4.8.3.1, the levels of cleanliness shall be in accordance with the requirements of A.3.7.3.1.1 or A.3.7.3.1.2, as applicable.

A.3.7.3.1.1 Prior to the application of solder resist. Unless otherwise specified, prior to the application of solder resist, the level of ionic contamination shall not exceed 1.56 micrograms/square centimeter (10.06 micrograms/square inch) using either a or b below:

- a. Resistivity of solvent extract. When printed wiring boards are tested as specified in A.4.8.3.1.1, the resistivity of the alcohol-water wash solution shall be greater than  $2 \times 10^6$  ohms-cm.
- b. Sodium chloride salt equivalent ionic contamination test (see A.6.5). The sodium chloride salt equivalent ionic contamination test equipment specified in A.6.5.1 may be used in lieu of the method specified in A.4.8.3.1.1. When printed wiring boards are tested using the sodium chloride salt equivalent ionic contamination test equipment specified in A.6.5.1, the final value shall be less than equivalents of sodium chloride specified in table A-V for the printed wiring board surface area tested.

A.3.7.3.1.2 Completed printed wiring boards (when specified, see A.3.1.1 and A.6.2.2g). The levels of cleanliness for completed printed wiring boards shall be as specified.

A.3.7.3.2 Resistance to solvents (marking inks or paints). After marking is tested in accordance with A.4.8.3.2, any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

A.3.7.4 Physical requirements.

A.3.7.4.1 Bow and twist. When tested as specified in A.4.8.4.1, the maximum allowable bow and twist shall be as specified (see A.3.1.1).

A.3.7.4.2 Conductor edge outgrowth.

A.3.7.4.2.1 Solder covered conductors. When the printed wiring board test specimen is examined as specified in A.4.8.1, there shall be no outgrowth of the solder coating on the conductor edges.

A.3.7.4.2.2 Conductors covered with metals other than solder. After undergoing the test as specified in A.4.8.4.2, the printed wiring board test specimen shall be examined as specified in A.4.8.1 and the maximum permissible outgrowth on conductors shall be .001 inch (0.03 mm).

A.3.7.4.3 Plating adhesion. When tested as specified in A.4.8.4.3, there shall be no plating particles or conductive patterns removed from the printed wiring board test specimen except for outgrowth.

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A.3.7.4.4 Rework simulation. Rework simulation is not applicable for printed wiring board designs that do not use holes for component attachment.

A.3.7.4.4.1 Type 1 with unsupported holes (bond strength). After undergoing the test specified in 4.8.4.4.1, the unsupported land shall withstand 5 pounds (2.27 Kg) pull or 500 lb/in<sup>2</sup> (3.4 MPa), whichever is less.

A.3.7.4.4.2 Types 2 and 3 with plated-through holes. After undergoing the test specified in A.4.8.4.4.2, the type 2 or 3 printed wiring board test specimens shall meet the following requirements:

- a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of blistering, crazing, or delamination in excess of that allowed in A.3.5.
- b. Internal visual and dimensional inspection (plated-through hole): The printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.7.4.5 Solderability. Solderability testing is applicable only on printed wiring board designs that require soldering during circuit card assembly processes. Printed wiring board designs that use compliant pin technology only for component attachment do not require solderability testing. Printed wiring board designs that use surface mount components only shall be tested for surface solderability, not hole solderability.

A.3.7.4.5.1 Hole solderability. After undergoing the test specified in A.4.8.4.5.1, the printed wiring board test specimen shall conform to the criteria specified in J-STD-003 class 3 or appendix E, as applicable.

A.3.7.4.5.2 Surface solderability. After undergoing the test specified in A.4.8.4.5.2, the printed wiring board test specimen shall conform to the criteria specified in J-STD-003 class 3 or appendix E, as applicable.

A.3.7.4.6 Solder resist cure and adhesion. When tested as specified in A.4.8.4.6, the cured solder resist coating shall not exhibit tackiness, blistering, or delamination and the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall be in accordance with the following:

- a. Bare copper or base material: Maximum percentage of lifting 0 percent.
- b. Gold or nickel plating: Maximum percentage of lifting 5 percent.
- c. Tin-lead plating or solder coating: Maximum percentage of lifting 10 percent.

A.3.7.4.7 Surface peel strength (type 3 foil laminated printed wiring boards). After undergoing the test specified in A.4.8.4.7, the surface conductor shall withstand a minimum peel strength greater than or equal to the "after thermal stress" values for the corresponding copper foil type, profile and weight specified by the base material specification. This requirement is only applicable to foil laminated type 3 printed wiring boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

A.3.7.4.8 Thermal stress.

A.3.7.4.8.1 Type 1. After undergoing the test specified in A.4.8.4.8, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and shall not exhibit any cracking or separation of plating and conductors, blistering or delamination shall not exceed the limits allowed in A.3.5.1.3 and lands shall not lift in excess of that allowed in A.3.5.5.

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A.3.7.4.8.2 Types 2 and 3. After undergoing the test specified in A.4.8.4.8, the printed wiring board test specimen shall be examined in accordance with A.4.8.1 and shall exhibit no blistering or delamination in excess of that allowed in A.3.5.1.3. After meeting the visual and dimensional requirements of A.3.5, the printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.6.

A.3.7.5 Electrical requirements.

A.3.7.5.1 Continuity. The circuit continuity test shall be in accordance with A.4.8.5.1. For qualification inspection there shall be no open circuits whose resistance exceeds 5 ohms. For production testing, there shall be no open circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum per inch of circuit length shall apply.

A.3.7.5.2 Circuit shorts (type 3 only). When tested as specified in A.4.8.5.2, the resistance between mutually isolated conductors shall be greater than 2 megohms.

A.3.7.5.3 Dielectric withstanding voltage. When inspected as specified in A.4.8.5.3, there shall be no flashover, sparkover, or breakdown.

A.3.7.6 Environmental requirements.

A.3.7.6.1 Moisture and insulation resistance.

A.3.7.6.1.1 Component printed wiring boards. When tested as specified in A.4.8.6.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.1.2 Non-component (flush conductor) printed wiring boards. When inspected as specified in A.4.8.6.1.1, non-component printed wiring board test specimens shall have a minimum of 50 megohms resistance between conductors. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the requirements specified in A.3.5.1.3 shall be met.

A.3.7.6.1.3 Thermal planes. The insulation material used for hole-fill dielectric shall provide an insulation resistance between the thermal plane and insulated plated-through holes greater than 100 megohms.

A.3.7.6.2 Thermal shock.

A.3.7.6.2.1 Thermoplastic resin base material types (see A.6.4.7.1). After undergoing the test specified in A.4.8.6.2, the requirements of A.3.7.5.1 shall be met.

A.3.7.6.2.2 Thermosetting resin base material types (see A.6.4.7.2). While undergoing the test specified in A.4.8.6.2, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, the printed wiring board test specimens shall meet the following requirements:

- a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, crazing, or delamination in excess of that allowed in A.3.5.1.3.
- b. Internal visual and dimensional inspection: When the printed wiring board test specimen is microsectioned and inspected in accordance with 4.8.2, the requirements specified in A.3.6 shall be met.

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A.3.8 Marking. Unless otherwise specified (see A.6.2), each production printed wiring board, each qualification test specimen, and each set of quality conformance test circuit strips (as opposed to each individual test coupon) shall be marked as specified (see A.3.1.1) and in accordance with herein. As a minimum, each production printed wiring board, qualification test specimen or quality conformance test circuit strip shall reference the printed wiring board manufacturers' CAGE (Commercial and Government Entity), lot date, and printed wiring board traceability code. The marking shall be produced by the same process used in producing the conductive pattern; or by the use of a nonconductive, fungistatic ink or paint applied to the printed wiring board or to a label which is applied to the printed wiring board; or by mechanical pencil marking on a metallic area provided for marking purposes may also be used. All marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards, shall remain legible after all tests, and in no manner affect printed wiring board performance.

A.3.9 Traceability. Unless otherwise specified, traceability shall be available for review by the qualifying or contracting activity for a minimum of 3 years after delivery of the printed wiring boards.

A.3.9.1 Quality conformance test circuitry and test coupons. Each quality conformance test circuitry (QCTC) shall be identifiable with those corresponding production printed wiring boards produced on the same panel that also produced the QCTC. All individual test coupons separated from its QCTC or qualification test specimen shall have its traceability maintained back to the QCTC or qualification test specimen from which the test coupons were separated.

A.3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

A.3.10 Repair. When inspected in accordance with 4.8.1, printed wiring boards shall not reveal any evidence of repair.

A.3.11 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality (except for slight color variations of the base material) and shall be free of defects in excess of those allowed herein that could affect life or serviceability.

#### A.4 QPL VERIFICATION

A.4.1 Classification of inspections. The inspections requirements specified herein are classified as follows:

- a. Qualification inspection (see A.4.5).
- b. Inspection of product for delivery (see A.4.6).
- c. Periodic conformance inspection (see A.4.7).

A.4.2 Test and measuring equipment. Test and measuring equipment of sufficient accuracy, quality, and quantity to permit performance of the required inspection shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with NCSL Z540, or equivalent.

A.4.3 Inspection conditions. Unless otherwise specified in the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

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**A.4.4 Printed wiring board performance verification.** Printed wiring board performance verification shall consist of inspections on the production printed wiring boards and the QCTC or test coupons referenced in tables herein for in-process, groups A and B inspections. Selection of test coupons for testing shall be in accordance with the applicable inspection table (see A.4.4.1). Each production printed wiring board or panel of printed wiring boards shall include sufficient test coupons to completely verify the applicable performance requirements specified. The design of test coupons shall be as specified on the applicable master drawing or by the applicable design standard (see A.3.1.1 and appendix D). The minimum number of test coupons on the production panel and the requirements for positioning shall be in accordance with the requirements of the applicable design standard (see A.3.1.1 and appendix D). NOTE: The design standard used to design the printed wiring boards influences the Verification Conformance Inspection (VCI) option used to perform the verification. See appendix D for additional guidance concerning VCI option selection.

**A.4.4.1 Verification Conformance Inspection (VCI) options (see D.5).** This document contains four VCI options that are available for group A (see tables A-II, D-IIc, D-IIId, or D-IIe) and group B (tables A-III, D-IIIC, D-IIId, or D-IIIE) testing. Unless otherwise specified, the VCI option to be used shall be determined using the guidelines of Appendix D. If a VCI option cannot be determined, the default VCI option VCI-4 contained in tables A-II, A-III, and A-IV shall be used.

**A.4.5 Qualification inspection (see A.6.3).**

**A.4.5.1 Qualification eligibility.** The fabrication of the qualification test vehicles may begin before authorization to test is granted, however before the start of qualification testing, the manufacturer must receive authorization from the qualifying activity.

**A.4.5.2 Samples.**

**A.4.5.2.1 Qualification test specimens.** Qualification test specimens shall conform to the following for the type of printed wiring boards for which qualification is sought:

- a. Type 1: The qualification test specimens for type 1 shall meet the requirements specified in master drawing IPC-100041.
- b. Type 2: The qualification test specimens for type 2 shall meet the requirements specified in master drawing IPC-100042.
- c. Type 3: The qualification test specimens for type 3 shall meet the requirements specified in master drawing IPC-100043.

**A.4.5.2.2 Sample size.** A sample of at least six qualification test specimens shall be produced by the manufacturer. Unless otherwise specified on the qualifying activity approved authorization, the qualification test specimens shall be serialized 1 through 6.

**A.4.5.2.3 Modifications to qualification test specimens.** Requests for the modification (the design or materials used) of qualification test specimens shall be prior to or at the time of the request for qualification testing. As an option, qualification test specimens can be fabricated to comply with master drawing IPC-100046 or IPC-100047, as applicable.

**A.4.5.3 Inspection routines.** Qualification inspection shall consist of the inspections specified in A.4.5.3.1 and A.4.5.3.2. The following details shall apply:

- a. Qualification test specimens serial numbers 1 and 2 shall be tested by the manufacturer.
- b. Qualification test specimens serial numbers 3 and 4 shall be tested at a laboratory acceptable to the Government.
- c. The two unused qualification test specimens (serial numbers 5 and 6) shall be retained as reference samples by the manufacturer for a period of 12 months.

## APPENDIX A

TABLE A-I. Qualification inspection.

Inspection	Requirement paragraph	Method paragraph	Qualification test specimen number <u>1/</u>	Test specimen <u>2/</u>				Notes
				TC1	TC2	TC3	PWB	
<b>Acceptability:</b>								
Design and construction <u>3/</u>	A.3.1.1	A.4.8.1	3 and 4				X	<u>3/</u>
Material	A.3.4	A.4.6.1.4	3 and 4				X	
Visual and Dimensional <u>3/</u>	A.3.5	A.4.8.1	3 and 4				X	<u>3/</u>
Registration (method I) <u>4/</u>	A.3.5.6	A.4.8.1.2	3 and 4			<u>4/</u>	X	<u>4/</u>
Marking	A.3.8	A.4.8.1	3 and 4				X	
Workmanship	A.3.11	A.4.8.1	3 and 4				X	
<b>Microsection requirements:</b>								
As received	A.3.7.2.3	A.4.8.2.1	3 and 4		A-3	A-3		
Registration (method II)	A.3.7.2.2	A.4.8.2.2.1	3 and 4			A,B		<u>5/</u>
<b>Chemical requirements:</b>								
Cleanliness	A.3.7.3.1	A.4.8.3.1	3 and 4				X	
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	3 and 4				X	
<b>Physical requirements:</b>								
Bow and twist	A.3.7.4.1	A.4.8.4.1	3 and 4				X	
Plating adhesion	A.3.7.4.3	A.4.8.4.3	3 and 4	C	C	C		<u>6/</u>
Rework simulation	A.3.7.4.4	A.4.8.4.4	3 and 4	A-2	A-2	A-2		
Solderability								
Hole	A.3.7.4.5.1	A.4.8.4.5.1	3 and 4		B	B		<u>7/</u>
Surface	A.3.7.4.5.2	A.4.8.4.5.2	3 and 4	C				<u>6/</u>
Thermal stress	A.3.7.4.8	A.4.8.4.8	3 and 4	B-4	B-4	B-4		
<b>Electrical requirements:</b>								
Continuity	A.3.7.5.1	4.8.5.1	3 and 4	D-3	D-3	D-3		
Circuit shorts	A.3.7.5.2	4.8.5.2	3 and 4	E-1	E-1	E-1		
Dielectric withstanding voltage (DWV)	A.3.7.5.3	4.8.5.3	3	E-1	E-1	E-1		<u>8/</u>
<b>Environmental requirements:</b>								
Moisture and insulation resistance (MIR)	A.3.7.6.1	A.4.8.6.1	3	E-1	E-1	E-1		
Thermal shock	A.3.7.6.2	A.4.8.6.2	3 and 4	D-3	D-3	D-3		

1/ See A.4.5.2 for qualification test specimen description and identification numbers.

2/ TC1 designates test coupons from a type 1 specimen; TC2 designates test coupons from a type 2 specimen; TC3 designates test coupons from type 3 specimens; panel means inspect the entire specimen. See qualification test specimen master drawing for test coupon design.

3/ Conductor spacing and width on test coupon E-5 shall not be evaluated in zone C.

4/ Not applicable for type 3.

5/ Combination of test coupons A-3 and B-6 (see A.4.6.2.2d for details and information).

6/ Test coupon C-1, C-4 and C-5.

7/ Test coupons A-1 and B-2.

8/ Dielectric withstanding voltage shall be performed only once before the moisture and insulation resistance test.

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A.4.5.3.1 Manufacturer test routine. The manufacturer shall perform the inspections specified in tables A-II and A-III (in-process and group A inspection).

A.4.5.3.2 Acceptable qualification laboratory test routine. The qualification laboratory acceptable to the Government shall subject the qualification test specimens to the inspections specified in table A-I. The order of the inspections and tests is optional; however, the cleanliness test shall be performed first.

A.4.5.3.3 Contract services. Manufacturers wanting to use an external subcontracted service for production of printed wiring board shall first qualify using their own internal equipment/processes within its facility. Once qualified internally, a manufacturer may qualify using the subcontracted service. This additional subcontracted qualification will not be listed separately on the QPL. The subcontract service shall not be extended to another external subcontracted service or manufacturer.

NOTE: For the purposes of this appendix, the internal equipment/process condition applies only to those processes used to manufacture the qualification test specimen. When applying for qualification of sub-contracted services, the process and the company performing the sub-contracted service shall be identified. If the manufacturer does not have any internal capability to perform a certain production step (either used during qualification or only used during production) this shall be identified on the application for authorization to test. If the sub-contracted service is changed, the manufacturer shall requalify.

A.4.5.3.4 Qualification rejection. Qualification approval will not be granted if any of the qualification test specimens tested in accordance with table A-I fail to meet the specified requirements.

A.4.5.4 Extent of qualification.

A.4.5.4.1 Printed wiring board type. Qualification of a particular printed wiring board type shall be extended to cover all conductive patterns of that same printed wiring board type produced. Qualification of type 3 printed wiring boards shall be extended to cover type 1 and type 2 printed wiring boards. Qualification of type 2 printed wiring boards shall be extended to cover type 1 printed wiring boards.

A.4.5.4.2 Base material types. Extension of qualification using base laminate materials in accordance with MIL-S-13949 shall be as follows:

- a. Qualification with type GF base materials shall be extended to cover types GB and GH base materials.
- b. Qualification with type GR base materials shall be extended to cover type GP base materials.
- c. Qualification with type GY base materials shall be extended to cover types GT and GX base materials.
- d. Qualification with type GX base materials shall be extended to cover type GT base material.
- e. Qualification with type SC base materials shall be extended to cover type GC base material.
- f. Qualification with types AF, BF, BI, GB, GC, GH, GI, GM, GP, GT, or QI shall cover that base material only.

A.4.5.4.3 Mass lamination (see A.6.4.4.1). Qualification of a contract lamination (ten conductor layers) shall be extended to cover a contract lamination of three or more conductor layers. The test specimens for ten layer contract lamination shall meet the requirements specified in master drawing IPC-100043.

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A.4.5.4.4 Processes.

A.4.5.4.4.1 Etchback. Qualification using etchback shall be extended to cover non-etchback.

A.4.5.4.4.2 Process changes. Any changes to a manufacturers qualified base material type, equipment, or processes must be reviewed by the qualifying activity for determination if partial or full requalification is necessary.

A.4.5.5 Retention of qualification. To retain qualification, the manufacturer shall certify to the qualifying activity that they still have the capability of manufacturing and verifying printed wiring boards which meet the performance requirements of this document. Refer to the qualifying activity for any additional guidelines necessary to retain qualification to this document. The manufacturer shall immediately notify the qualifying activity at any time that the inspection data indicates failure of the qualified product to meet the performance requirements, of this document.

A.4.5.5.1 Requalification (see A.6.3.2). Qualifications expire 36 months from the date of initial qualification. In order to maintain a QPL listing, manufacturers shall complete requalification before the end of its current 36 month qualification.

A.4.5.5.2 Product assurance information. The manufacturer shall make available to qualifying activity an approved quality manual or procedures that as a minimum addresses the following information:

- a. In-process and group A verification procedures.
- b. Test coupon quantity, design, placement and usage procedures.
- c. The definition of complexity used to select samples for group B verification testing.

A.4.6 Inspection of product for delivery. Inspection of product for delivery shall consist of in-process and group A inspection. Except as specified in A.4.7.1.4, delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of the periodic inspection. Anomalies or defects noted on sample printed wiring boards or test coupons (or both) defined herein shall be recorded and the proper corrective action shall be initiated. Manufacturers that are qualified to use subcontract services are still responsible for in-process and groups A inspections and shall be subject to loss of qualification if the results of in-process and group A inspections indicate failure to meet the applicable requirements.

A.4.6.1 In-process inspection. Each inspection lot of printed wiring boards or panels, as applicable shall be inspected in accordance with table A-II, as applicable. When permanent solder resist is specified (see A.3.1.1), the in-process inspections specified in subgroups 1, 2 and 3 of table A-II shall be performed prior to solder resist application. Prior to lamination of type 3 printed wiring boards, the in-process inspections specified in subgroup 2 of table A-II shall be performed.

A.4.6.1.1 Inspection lot.

A.4.6.1.1.1 Subgroup 1. An inspection lot shall correspond to each change of shift or work force, whichever occurs first. Production lots may be grouped based on same materials, same type or types of interfacial connections and terminations, and same processing requirements.

A.4.6.1.1.2 Subgroups 2 and 3. An inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

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TABLE A-II. In-process inspection.

Inspection	Requirement paragraph	Method paragraph	Sample size <u>1/</u>
<u>Subgroup 1</u>			
Material Cleanliness <u>2/</u>	A.3.4 A.3.7.3.1.1	A.4.8.1 A.4.8.3.1	See A.4.6.1.4 Plan *L
<u>Subgroup 2</u>			
Conductor spacing <u>2/</u> <u>3/</u>	A.3.5.2.2	A.4.8.1	Plan BH
Conductor width <u>2/</u> <u>3/</u>	A.3.5.2.3	A.4.8.1	Plan BH
Conductive pattern imperfections	A.3.5.2.4	A.4.8.1	Plan BH
<u>Subgroup 3</u>			
Plating adhesion <u>2/</u> <u>4/</u>	A.3.7.4.3	A.4.8.4.3	Plan BH

1/ See appendix C, table C-I for C = 0 sampling plans and C.4.5 for examples.

2/ Performed prior to solder resist application.

3/ Performed prior to lamination on each production lot.

4/ A Non-reflowed test coupon prior to reflow may be required (see A.6.2).

A.4.6.1.2 Sample size. The number of printed wiring boards or panels to be selected from each inspection lot shall be in accordance with table A-II.

A.4.6.1.3 Rejected lots. If an inspection lot is rejected as a result of a failure to pass the subgroup 1 test specified, the manufacturer shall withdraw the lot, take corrective action in connection with the cleaning materials and procedures, reclean the lot and resubmit the lot for inspection prior to application of permanent solder resist coating. Printed wiring boards are not acceptable if the permanent solder resist coating has been applied to a contaminated surface. If an inspection lot is rejected for subgroup 2 or 3 tests, the manufacturer may screen (100 percent inspection) out the defective units (printed wiring boards or panels). Defective printed wiring boards shall not be shipped.

A.4.6.1.4 Materials inspection. Materials inspection shall consist of certification supported by verifying data that the materials used in fabricating the printed wiring boards are in accordance with the applicable referenced specifications or requirements specified (see A.3.1.1), prior to such fabrication. Unless otherwise specified (see A.3.1.1), verifying data need not be submitted to the qualifying activity or acquiring activity, but must be made available upon request.

A.4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in table A-III. The qualified manufacturer shall be responsible for completion of all group A inspections and shall be subject to loss of qualification for failure not to complete or to have completed all group A test and inspections (see appendix D for group A VCI options).

A.4.6.2.1 Inspection lot. A group A inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.2.2 Sampling procedures. Statistical sampling and inspection shall be in accordance with appendix C. For 100 percent inspection, all rejected units (printed wiring boards or panels of printed wiring boards) shall not be supplied as compliant. The following details on panel/test coupon sampling shall apply:

- a. Solderability: For SERA, samples shall be selected in accordance with appendix E; For J-STD-003, samples shall be selected in accordance with appendix C, table C-I, plan L.

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b. As received:

- 1) Types 1 and 2: The number of test coupons to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with appendix C, plan L.
- 2) Type 3: A minimum of one test coupon per panel shall be microsectioned.

c. Thermal stress:

- 1) Types 1 and 2: The number of test coupons to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with appendix C, plan L.
- 2) Type 3: A minimum of two test coupons (A's, B's or combination of both) per panel shall be microsectioned. One of the test coupon shall be microsectioned in the panel's length direction and the other shall be microsectioned along the panel's width direction.

- d. Registration (method II, type 3 only): When method II is to be used, registration shall be evaluated using any combination of two microsectioned test specimens taken from diagonal corners of the panel. Both test coupons shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X) direction and the other representing the panel's width (Y) direction. Test coupons from the AS RECEIVED (see A.3.7.2.1), THERMAL STRESS (see A.3.7.4.8.2) or when available, HOLE SOLDERABILITY (see A.3.7.4.5) verifications may be used.

A.4.6.2.3 Rejected lots. If an inspection lot is rejected, the manufacturer may rework it to correct the defects and resubmit the lot for reinspection, or screen out the defective units (if possible). Resubmitted lots shall be inspected using tightened inspection (plan T or Q of table VII, as applicable). Such lots (reworked or screened) shall be clearly identified as reinspected lots. Products which have failed any group A inspection and have not been reworked and have not passed reinspection (as specified in this appendix) may not be delivered as compliant printed wiring boards.

A.4.6.2.4 Disposition of sample units and test coupons. Sample printed wiring boards which have passed all of group A inspection may be delivered if the inspection lot is accepted. Test coupons which have been subjected to group A shall be retained as specified in A.3.9.

A.4.7 Periodic inspection. Periodic inspection shall consist of group B inspection. Except where these inspections show noncompliance (see A.4.7.1.4) with the applicable requirements of this document and the master drawing, delivery of printed wiring boards which have passed group A shall not be delayed pending the results of these periodic inspections. Periodic inspections shall be performed at a laboratory acceptable to the Government (see A.6.6).

A.4.7.1 Group B inspection. Group B inspection shall consist of the inspections specified in table A-IV (see appendix D for group B VCI options).

A.4.7.1.1 Inspection lot. The sample units (test coupons) shall be randomly selected from the most complex (see A.6.4.2) inspection lot that has passed all in-process and group A inspections during that production month. The most complex printed wiring boards shall be as determined by the manufacturer using its definition of complex (see A.6.4.2), subject to approval by the qualifying activity.

A.4.7.1.2 Sampling procedures. The selection of sample units and testing shall be on a monthly basis. Samples for each extent of qualification base material type family (see A.4.1.2) produced during that reporting period shall be subjected to group B inspection. Because of the performance nature of this document, the design details of the test coupons will need to be supplied with the sample units (see A.6.8).

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TABLE A-III. Group A inspection (VCI option 4). 1/

Inspection	Requirement paragraph	Method paragraph	Test specimen 2/				Sample plans 3/
			PWB	TC1	TC2	TC3	
<u>Visual and dimensional</u>							
Acceptability 4/	A.3.7.1	A.4.8.1	X				Plan BH 4/
Visual & dimensional	A.3.5	A.4.8.1	X				Plan BH
Solder mask thickness	A.3.5.7.2	A.4.8.1.3	X	E	E	E	Plan BH/TJ 5/
Registration (method I)	A.3.5.6	A.4.8.1.2	X				Plan BH
Registration (method III)	A.3.7.2.2.2	A.4.8.2.2.2				F/R	See 6/
Marking	A.3.8	A.4.8.1	X				Plan BH
Workmanship	A.3.11	A.4.8.1	X				Plan BH
<u>Microsection requirements</u>							
As received	A.3.7.2.1	A.4.8.2		B	B	B	See 7/
Registration (method II)	A.3.7.2.2.1	A.4.8.2.2.1	X			A/B	See 7/
<u>Chemical requirements</u>							
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	8/	8/	8/	8/	See 8/
<u>Physical requirements</u>							
Bow and twist	A.3.7.4.1	A.4.8.4.1	X				Plan BH
Conductor edge outgrowth	A.3.7.4.2	A.4.8.4.2	X				Plan BH
Plating adhesion	A.3.7.4.3	A.4.8.4.3	X	C	C	C	Plan BH/TJ 4/ 7/
Solderability 9/							
Hole 9/	A.3.7.4.5.1	A.4.8.4.5.1			A/S	A/S	See 7/ 10/
Surface	A.3.7.4.5.2	A.4.8.4.5.2	X	C		M	Plan BH/TJ 7/
Solder mask adhesion	A.3.7.4.6	A.4.8.4.6		G	G	G	Plan TJ
Thermal stress	A.3.7.4.8	A.4.8.4.8		B	B	B	See 7/
<u>Electrical requirements 11/</u>							
Continuity 12/	A.3.7.5.1	A.4.8.5.1	X				100 percent 12/
Circuit shorts 12/	A.3.7.5.2	A.4.8.5.2	X				100 percent 12/
Registration (method III)	A.3.7.2.2.2	A.4.8.2.2.2				F/R	See 6/

- 1/ See A.4.4.1 and appendix D for Verification Conformance Inspection options. Sufficient quantity of test coupons need to be present on the panel to complete group A and possibly group B verification.
- 2/ PWB is a production printed wiring board; TC1 is a type 1 test coupon; TC2 is a type 2 test coupon; TC3 is a type 3 test coupon. See appendix D herein for test coupon identification (name) translation to the applicable design standard.
- 3/ See appendix C, table C-I for C = 0 sampling plans and C.4.5 for examples.
- 4/ Some attributes may need to be inspected prior to lamination or solder resist application.
- 5/ Test coupon or production printed wiring board, manufacturer's option.
- 6/ See A.4.8.2.2 for test specimen description and sample size.
- 7/ See A.4.6.2.2 for sample size and/or test specimen description.
- 8/ See A.4.8.3.2.1 for test specimen description and sample size.
- 9/ For printed wiring boards using only surface mount lands for component attachment, the surface solderability test can be used in lieu of the hole solderability test.
- 10/ A or S test coupon, manufacturers option.
- 11/ Type 3 printed wiring boards only.
- 12/ If the printed wiring assembly drawing requires 100 percent circuitry test inspection on the printed wiring assembly, a sampling plan based on appendix C, table C-I, plan F, can be used.

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A.4.7.1.2.1 Sample unit selection. Unless otherwise specified in A.4.8.3.2 (resistance to solvents) or 4.8.4.7 (surface peel strength), the following criteria shall be used in selecting samples for group B testing:

- a. The sample units shall be from the most complex (see A.6.4.2) printed wiring board design produced that calendar month.
- b. The sample units shall be selected from lots which have passed group A inspection during that calendar month.
- c. Sample units shall be randomly selected from panels which have passed group A inspection.
- d. The sample units can be either:
  1. Two sets of quality conformance test circuitry, or
  2. Two test coupons for each test to be performed.

A.4.7.1.3 Frequency. The frequency of group B testing shall be monthly. The sample units shall be submitted for testing within 30 calendar days after the end of each month in which production occurred.

TABLE A-IV. Group B inspection (VCI option 4). 1/

Inspection	Requirement paragraph	Method paragraph	Test coupon by type <u>2/</u>		
			Type 1	Type 2	Type 3
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	<u>3/</u>	<u>3/</u>	<u>3/</u>
Rework simulation	A.3.7.4.4	A.4.8.4.4	A	A	A
Surface peel strength	A.3.7.4.7	A.4.8.4.7			P <u>4/</u>
Dielectric withstanding voltage <u>5/</u> Moisture and insulation resistance	A.3.7.5.3 A.3.7.6.1	A.4.8.5.3 A.4.8.6.1	E	E	E

1/ See appendix D for other VCI options.

2/ See 1.2, A.3.1.1, and A.6.4.6 herein.

3/ Test coupon identification strip or production board, manufacturers option.

4/ See A.4.8.4.7.1 for test specimen description and number of samples required.

5/ Dielectric withstanding voltage shall be performed only once (before the moisture and insulation resistance test).

A.4.7.1.4 Failures. If one or more sample units fail to pass group B inspection, the sample shall be considered to have failed. The qualifying activity shall be notified of any group B failure within 3 business days. Group B inspection shall be repeated on additional sample units (either all group B inspections or just the group B inspections which the original sample failed, at the option of the qualifying activity) from the next most complex (see A.6.4.2) inspection lot from the same month that the failure occurred. Group A testing and shipment of the product represented by the failed group B sample shall be discontinued.

A.4.7.1.4.1 Corrective actions. Corrective actions shall be taken on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, etc.), and which are considered subject to the same failure.

A.4.7.1.4.2 Noncompliance. If the lot or lots directly represented by the group B failure have been shipped, the manufacturer must notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group B sample are considered noncompliant until a sample from the next most complex (see A.6.4.2) inspection lot passes group B inspection.

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A.4.7.1.4.3 Reinstitution of Group A inspection. After successful completion of group B reinspection, group A inspection of product represented by the group B failure may be reinstated.

A.4.7.1.5 Disposition of sample units. Test coupons which have been subjected to group B shall be retained as specified in A.3.9.

A.4.8 Methods of inspection. The following identified tests and test methods assure printed wiring board integrity with typical operating conditions. Alternate commercial or industry standard test methods may be allowed, however if an alternate method is to be used, the qualifying activity must be notified prior to the performance of the test. The following verification test methods described herein are proven methods and shall be the referee method in case of dispute.

A.4.8.1 Acceptability inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using either an optical apparatus or aid which provides a minimum magnification of 1.75x (3 diopters) or by using automated inspection techniques. Referee inspection of the specimen features shall be accomplished at a magnification of 10X.

A.4.8.1.1 Annular ring, external (see A.3.5.2.1). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board (see IPC-TM-650, method 2.2.1 for illustration).

A.4.8.1.2 Registration (method I)(Types 1 and 2)(see A.3.5.6). Layer-to-layer registration of type 1 and type 2 printed wiring boards shall be satisfied if the outer layers meet the external annular ring (see 3.1 and A.3.5.2.1) and hole pattern accuracy (see A.3.1.1 and A.3.5.4) requirements.

A.4.8.1.3 Solder resist thickness (see A.3.5.7.4). Solder resist thickness shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.2 Microsection inspection. Microsection inspections (to evaluate characteristics such as plated-through holes, plating thickness, or foil thickness) shall be accomplished by using methods in accordance with either IPC-TM-650, method 2.1.1 or 2.1.1.2. The following details shall apply:

- a. Number of holes per specimen. A minimum of one microsection containing at least three plated-through holes shall be made for each test specimen required. Each side of the plated hole shall be viewed independently.
- b. Accuracy. Plated-through holes shall be microsectioned in the vertical plane at the center of the hole  $\pm 10$  percent.
- c. Magnifications. The specimens shall be inspected for foil and plating integrity at a magnification of 100X  $\pm 5$  percent. Referee inspections shall be accomplished at a magnification of 200X  $\pm 5$  percent.
- d. Evaluations. Evaluations for items such as base material thickness, metal foil thickness, plating thickness, lay-up orientation, resin smear, and plating voids shall be accomplished at magnifications specified above. If resin smear is detected or suspected on a vertical microsection, a referee microsection shall be prepared and evaluated in the annular (horizontal) direction.
- e. Measurements. Measurements shall be averaged from at least three determinations for each side of the plated-through hole. Isolated thick or thin sections shall not be used for averaging, however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified herein.

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A.4.8.2.1 Plated-through hole inspection (see A.3.6). When inspected in accordance with 4.8.2, the following details shall apply:

- a. Annular ring (internal) (see A.3.6.1). This measurement shall apply to all internal lands for all three holes.
- b. Dielectric layer thickness (see A.3.6.3). The dielectric layer thickness shall be inspected between all conductor layers present in the test specimen.
- c. Plating and coating thickness (see A.3.6.8). Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured for compliance with the requirements of A.3.6.8.
- d. Copper plating voids (see A.3.6.9.1). Any plated-through hole in the microsection failing the plating void criteria A.3.6.9.1 subparagraphs a, b or c, shall be cause for the entire panel of printed wiring boards associated with the microsection to be rejected. The following details apply if a single plating void is found:
  - (1) Type 2: If the plating void does not exceed the conditions of A.3.6.9.1, the entire lot (100 percent panel inspection) shall be microsectioned and inspected for voids. If a plating void is present on any panel, a referee microsection shall be performed using an A or B test coupon from the opposite corner of that panel. If the referee has no plating voids, that panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.
  - (2) Type 3: If the plating void does not exceed the conditions of A.3.6.9.1, a referee microsection shall be performed using an A or B test coupon from the opposite corner of the panel. If the referee has no plating voids, the panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.
- e. Thermal planes (see A.3.6.3.1). The lateral dielectric spacing between the heat sinking planes and adjacent conducting surfaces (nonfunctional lands) or plated-through holes shall be measured at the closest point between these surfaces or the plated-through hole.

A.4.8.2.2 Registration (internal). Internal layer-to-layer registration shall be determined by either evaluating microsectioned test coupons (method II, see A.4.8.2.2.1) or the use of registration test coupons and techniques (method III, see A.4.8.2.2.2).

A.4.8.2.2.1 Method II (by microsectioned sample units). The two microsectioned test coupons shall be evaluated by computing the difference in centerline location of the two lands found to be most eccentric to one another within each cross-section (see IPC-TM-650, method 2.2.11 for illustration).

A.4.8.2.2.2 Method III (by registration test coupons). Registration test coupons and techniques, when provided by the printed wiring board fabricator, shall be evaluated in accordance with methods approved by the qualifying activity and when applicable, the acquiring activity. Unapproved methods of measurement using registration test coupons shall be backed up by method II of A.4.8.2.2.1 using the appropriate test coupons (see table A-III) from the same panel. Two non-destructive methods for determining registration are available using the following test coupon designs:

- a. Test coupon F (etch factor not needed).
- b. Test coupon R (etch factor of each layer needed).

If other registration test coupon designs and requirements are provided as an element of the design documentation set, registration can be evaluated in accordance with the criteria specified on the applicable master drawing.

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**A.4.8.3 Chemical inspection.**

A.4.8.3.1 Cleanliness (by resistivity of solvent extract) (see A.3.7.3.1 and 6.5). The printed wiring board shall be inspected for cleanliness in accordance with IPC-TM-650, method 2.3.25.

A.4.8.3.2 Resistance to solvents (marking ink or paint) (see A.3.7.3.2). Marking ink or paint resistance to solvents shall be inspected in accordance with IPC-TM-650, method 2.3.4. The following details apply:

- a. The marked portion of the test specimen shall be brushed.
- b. After the test, the test specimen shall be visually inspected in accordance with A.4.8.1 for legibility of marking.

A.4.8.3.2.1 Sampling procedures and test specimens. The resistance to solvents test shall be performed either during group A (every lot) or during group B (monthly). The test specimens can be either production printed wiring boards or quality conformance test circuitry strip identification areas (see appendix D) containing ink or paint marking. For either group A or group B, the minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

**A.4.8.4 Physical inspections.**

A.4.8.4.1 Bow and twist (see A.3.7.4.1). The printed wiring board shall be inspected for bow and twist in accordance with IPC-TM-650, method 2.4.22.

A.4.8.4.2 Conductor edge outgrowth (see A.3.7.4.2). The extent of outgrowth, on conductors covered with metals other than fused tin-lead or solder coating, shall be determined by measuring the conductor width before and after mechanically removing the overhang metal. If a referee test is required, cross-sectioning of the conductor shall be performed. The procedure for removing overhang metal, for this test, shall be as follows:

- a. Wet the printed wiring board specimen in tap water at approximately room temperature.
- b. While wet, brush the printed wiring board specimen with a brass wire brush to remove the overhang metal. Brush in the direction of the functional line, using moderate pressure.

A.4.8.4.3 Plating adhesion (see A.3.7.4.3). The printed wiring board shall be inspected in accordance with IPC-TM-650, method 2.4.1, with the following details and exceptions. When edge board contacts are part of the pattern, at least one pull must be on the contacts. Fresh tape shall be used for each pull. If overhang metal breaks off (slivers) and adheres to the tape, it is evidence of outgrowth (see A.3.7.4.2), but not a plating adhesion failure.

**A.4.8.4.4 Rework simulation.**

A.4.8.4.4.1 Type 1 (unsupported hole) (see A.3.7.4.4.1). The printed wiring board test specimen shall be inspected in accordance with IPC-TM-650, method 2.4.21 with the following details and exceptions: Three holes per test coupon shall be tested. Insert wires in holes in selected lands and solder to lands by machine or hand, as applicable. The insert wire lead shall have a diameter so that the diameter of the hole will be at a maximum of .020 inch (0.51 mm) greater than the diameter of the inserted wire lead. The wires shall not be clinched. It shall be considered a failure when a land around an unsupported hole is loosened.

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A.4.8.4.4.2 Types 2 and 3 (see A.3.7.4.4.2). Rework simulation of plated-through holes shall be tested in accordance with IPC-TM-650, method 2.4.36, except that the rework simulation shall be performed after stabilizing the test coupons at temperatures of 15°C to 35°C and relative humidity of 40 to 85 percent for a period of 24 hours.

A.4.8.4.4.3 Surface mount land. The surface mount lands on the printed wiring board test specimen shall be inspected in accordance with IPC-TM-650, method 2.4.21.1.

A.4.8.4.5 Solderability (see A.3.7.4.5).

A.4.8.4.5.1 Hole (plated-through hole)(Types 2 and 3)(see A.3.7.4.5.1). The printed wiring board test specimens shall be inspected in accordance with J-STD-003 class 3 or appendix E.

A.4.8.4.5.2 Surface (Type 1 or surface mount land)(see A.3.7.4.5.2). The printed wiring board test specimens shall be inspected in accordance with J-STD-003 class 3 or appendix E.

A.4.8.4.6 Solder resist adhesion (see A.3.7.4.6). The permanency and adhesion of cured solder resist shall be determined in accordance with IPC-TM-650, method 2.4.28.1.

A.4.8.4.7 Surface peel strength (type 3 using foil lamination)(see A.3.7.4.7). The peel strength shall be inspected in accordance with IPC-TM-650, method 2.4.8, except that the after thermal stress condition and after exposure to processing chemicals tests shall not be performed. Plated tin-lead, solder coating, or other plated metallic resist shall be chemically removed prior to test or shall be prevented from being deposited during manufacturing. The test specimen shall not be coated with any organic coating for test. All peel strength readings obtained shall meet the minimum requirement.

A.4.8.4.7.1 Test specimens. The specimen shall consist of conductors that provide a minimum test length of 2 inches (50.8 mm) and a conductor width of .125 inch (3.3 mm).  
NOTE: This test coupon is described in the design standard for VCI option 4 (test coupon "P") or IPC-TM-650, section 5.8.3. At least one test coupon per foil laminated side shall be placed on the panel where space is available. Eight peel strength specimens shall be selected from two different production lots; four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is submitted/passes group A inspection in a calendar month, then only the test coupon(s) from that lot shall be submitted.

A.4.8.4.8 Thermal stress (see A.3.7.4.8). The printed wiring board test specimen shall be inspected for thermal stress in accordance with IPC-TM-650, method 2.6.8.

A.4.8.5 Electrical inspection.

A.4.8.5.1 Continuity (see A.3.7.5.1). A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard (see A.3.1.1 and appendix D) for the smallest conductor in the circuit.

A.4.8.5.2 Circuit shorts (see A.3.7.5.2). A test voltage shall be applied between all common portions of each conductive pattern and all adjacent common portions of each conductive pattern. The voltage shall be applied between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer. For manual testing the voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be as specified on the applicable master drawing. If a test voltage of the printed wiring board is not specified on the applicable master drawing, the test voltage shall be the maximum rated voltage of the printed wiring board or 40 volts minimum, whichever is less.

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A.4.8.5.3 Dielectric withstanding voltage (see A.3.7.5.3). The printed wiring board test specimen shall be tested in accordance with IPC-TM-650, method 2.5.7. The following details and exceptions apply:

- a. Magnitude of test voltage: 1,000 V dc +25 V dc, -0 V dc.
- b. Duration of application of test voltage: 30 seconds +3, -0 seconds.
- c. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductive pattern and all adjacent common portions of each conductive pattern. The voltage shall be applied between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.8.6 Environmental inspection.

A.4.8.6.1 Moisture and insulation resistance (see A.3.7.6.1). The printed wiring board test specimen shall be tested in accordance with IPC-TM-650, method 2.6.3, class 3.

A.4.8.6.1.1 Non-component (flush conductor) printed wiring boards (see A.3.7.6.1.1). The specimens shall be inspected in accordance with A.4.8.6.1, except the insulation resistance measurement shall be taken within 1 minute after the removal of the specimen from the humidity chamber after 100 V dc,  $\pm 15$  percent has been applied between all conductors for a minimum of 60 seconds.

A.4.8.6.2 Thermal shock (see A.3.7.6.2). The printed wiring board test specimen shall be tested in accordance with IPC-TM-650, method 2.6.7.2, with the following exceptions:

- a. The printed wiring board test specimens shall be subjected to 100 temperature cycles in accordance with the table A-V following:
- b. Transfer time between chambers shall be less than 2 minutes. The thermal capacity of the test chambers used shall be such that the ambient temperature shall reach the specified temperature within 2 minutes after the specimen has been transferred to the appropriate chamber.
- c. The following measurements shall be made:
  1. Before test: Resistance.
  2. During the test: Resistance during the first and last high temperature cycle:
  3. After the test: Resistance.

TABLE A-V. Thermal shock, temperatures and times.

Low temperature +0°C/-5°C	Time (minutes) +2/-0	High temperature +5°C/-0°C	Time (minutes) +2/-0	Base material type(see appendix D)
-65	15	85	15	GR, GP, GT, GY, GX
-65	15	125	15	AF, BF, BI, GC, GF, GH, SC
-65	15	150	15	GB, GM,
-65	15	175	15	AI, GI, QI

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A.5 PACKAGING

A.5.1 Packaging requirements. The requirements for packaging shall be in accordance with the purchase order or contract (see A.6.2).

A.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. This appendix is intended to be used by manufacturer's not certified to the QML printed board specification, MIL-PRF-31032. This appendix is not a duplicate or look-alike of any MIL-PRF-31032 associated specification, most of the historic performance and verification requirements are still contained in this appendix. However, many of the "enhanced" acceptance criteria or methods developed for MIL-PRF-31032 associated specifications have been added as the baseline or are available as an option.

A.6.2 Acquisition requirements.

A.6.2.1 Acquisition documents. Acquisition documents should specify the following:

- a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.
- b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.2, A.2.1 and A.2.2).
- c. Appropriate type (see 1.2.1) and base material designation (see 1.2.2).
- d. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see A.3.1.1).
- e. Title, number, revision letter (with any notice number when applicable), and date of the applicable design standard (see A.3.3).
- f. Part identification (if applicable), and marking instructions including size, location and application method (see A.3.1.1 and A.3.8).
- g. Whether microsectioned test specimens, samples or photographs are required to be delivered with the order.
- h. Levels of preservation and packing required (see A.5.1).

A.6.2.2 Additional acquisition requirements. Acquisition documents should also specify the following data, if applicable:

- a. Verification Conformance Inspection option (if other than option 4)(see appendix D).
- b. Design related if different than the applicable design standard (see appendix D).
  1. Minimum annular ring (external or internal)(see A.3.1.1), if different than the applicable design standard.
  2. Minimum conductor width (see A.3.1.1), if different than the applicable design standard.
  3. Minimum conductor spacing (see A.3.1.1), if different than the applicable design standard.

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4. Minimum dielectric thickness (see A.3.1.1), if different than the applicable design standard.
  5. Minimum edge spacing requirement (see A.3.1.1), if different than the applicable design standard.
  6. Copper plating thickness (see A.3.1.1), if different than the applicable design standard.
  7. Conductor finish plating (see A.3.1.1), if other than solder coating or tin-lead.
- c. Conductor edge overhang, if applicable (see A.3.7.4.2).
  - d. Insulation resistance requirements (see A.3.7.5.2).
  - e. Foil lamination peel strength, if applicable (see A.3.7.4.7).
  - f. Nondelivery of sample units which have not been subjected to the continuity test and have passed all other tests to groups A and B inspection.
  - g. Cleanliness (organic)(see A.3.7.3.1.2 and A.6.5.3).
  - h. If special or other identification marking is required (see A.3.8).

A.6.3 Qualification notes. Although the qualification test specimen master drawings specified in A.4.5.2.1 requires the use of base material compliant to MIL-P-13949 (now MIL-S-13949), manufacturer's can qualify base material not addressed by MIL-S-13949 by specifying the base material on the application for qualification.

A.6.3.1 Transference of QPL qualification. Manufacturers currently qualified to MIL-PRF-55110E will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL-PRF-55110E with amendment 1. New applications for qualification (after the date of this document) must be performed to the requirements of this revision.

A.6.3.2 Qualification expiration and QPL-55110. Qualification listings within QPL-55110 for manufacturers qualified under this appendix (QPL product assurance level) includes the qualification expiration date as the last six digits of the test reference number. This date, formatted as month/day/year, is the actual qualification expiration date and represents the date that the company is no longer qualified (unless notified in writing by the qualifying activity) whether or not that individual listing has been removed the QPL. If the company has not requalified before the next issue of the QPL is updated, then the listing will be stricken from the QPL.

#### A.6.4 Terms and definitions.

A.6.4.1 Board thickness. The overall printed wiring board thickness includes metallic depositions, fusing, and solder mask. The overall thickness is measured across the printed wiring board extremities (thickest part), unless a critical area, such as an edge card connector or card guide mounting location, is identified on the master drawing.

A.6.4.2 Complex (or Complexity, as it relates to group B inspection). Complexity of printed wiring boards will usually depend on the base materials used; dielectric layer thickness; overall printed wiring board thickness; number of conductor layers; conductor widths and spacings; intricacy of patterns; size, quantity, aspect ratio and positioning of plated holes; tolerancing of any or all of the above; the presence of internal thermal planes or heat sinks, and all combinations of the above with respect to their manufacturing difficulty, and their effects upon the consistent ability of the printed wiring boards to meet the requirements of the periodic testing, unless otherwise specified by the contracting activity.

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**A.6.4.3 Conductive interfaces.** The term conductive interfaces is used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of metal foil. The interface between platings and coating (electroless copper, direct metallization copper and non-electroless electroless copper substitutes, etc., and electrolytic copper, whether panel or pattern plated), are also considered a conductive interface.

**A.6.4.3.1 External conductive interfaces.** An external conductive interface is considered to be the junction between the surface copper foil and the deposited or plated copper.

**A.6.4.3.2 Internal conductive interfaces.** An internal conductive interface is considered to be the junction between the internal layers (copper foil posts or internal layers) and the deposited or plated copper.

**A.6.4.4 Contract service(s).** Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include verification testing including electrical function tests.

**A.6.4.4.1 Mass lamination.** Manufacturers requesting to use contract services lamination (mass lamination) must be qualified to type 3 of the same base material type requested. The qualification test specimens and sample size must be as specified in A.4.5.2.1. The qualification test specimens must be produced by the QPL manufacturer and the mass laminator and must be representative of the subsequent production process. Printed wiring board manufacturers using contract services are subject to the conditions of A.4.5.5.

**A.6.4.5 Printed wiring board test specimen.** The term printed wiring board test specimen is used to describe all of the following; production printed wiring boards, qualification test specimens, or test coupons.

**A.6.4.6 Printed wiring board types.** The printed wiring board types are as specified in both MIL-STD-275 and IPC-D-275. This document does not address many of the performance or verification routines associated with types 4, 5, and 6 printed wiring boards described by IPC-D-275.

**A.6.4.6.1 Type 1.** Type 1 printed wiring boards are usually single sided conductive pattern with no plating in the component holes (base material with metal foil on only one side). Both MIL-STD-275 and IPC-D-275 detail the default design parameter of type 1 printed wiring boards.

**A.6.4.6.2 Type 2.** Type 2 printed wiring boards are printed wiring boards with conductive patterns on both sides of the board (double sided). In addition, holes through the base material are plated with copper (plated-through holes) to connect the conductive patterns on both sides together. Both MIL-STD-275 and IPC-D-275 detail the default design parameter of type 2 printed wiring boards.

**A.6.4.6.3 Type 3.** Type 3 printed wiring boards are printed wiring boards with conductive patterns on the outer layers of the board and contains internal conductive layers (multilayer). In addition, holes through the base material are plated with copper (plated-through holes) to connect the conductive patterns, external and internal, together. Both MIL-STD-275 and IPC-D-275 detail the default design parameter of type 3 printed wiring boards.

**A.6.4.7 Resin systems families.**

**A.6.4.7.1 Thermoplastic resins (see IPC-T-50).** For the purposes of this document, the following base material types are classified as containing thermoplastic resin: GR, GP, GT, GX, and GY.

**A.6.4.7.2 Thermosetting resins (see IPC-T-50).** For the purposes of this document, the following base material types are classified as containing thermosetting resins: AF, BF, BI, GB, GC, GF, GH, GI, GM, QI, and SC.

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A.6.5 Cleanliness.

A.6.5.1 Flux removal. Selection of procedures for flux removal is at the manufacturer's discretion. A procedure should be chosen which will enable the printed wiring board fabricator to produce results enabling compliance with this document. Both polar and nonpolar solvents may be required to effect adequate flux removal.

A.6.5.2 Resistivity of solvent extract (see A.4.8.3.1). This test procedure, including solution preparation and a laboratory ware cleaning procedure, was documented in Materials Research Report No. 3-72, "Printed-Wiring Assemblies; Detection of Ionic Contaminants on" published by the Naval Air Warfare Center, Indianapolis, IN.

A.6.5.2.1 Alternate cleanliness methods. The following methods of determining the cleanliness of printed wiring boards have been shown to be equivalent to the resistivity of the solvent extract method:

- a. The Kenco Alloy and Chemical Company, Incorporated, "Omega Meter™, Model 200."
- b. Alpha Metals Incorporated, "Ionograph™."
- c. Zero Systems, Incorporated, "Zero Ion™, Model ZI-100."
- d. Westek, "ICOM 5000™."

Test procedures and calibration techniques for these methods are documented in Materials Research Report No. 3-78, "Review of Data Generated With Instruments Used to Detect and Measure Ionic Contaminants on Printed-Wiring Assemblies". Table A-VI lists the equivalence factors for these methods in terms of microgram equivalents of sodium chloride per unit area.

TABLE A-VI. Equivalence factors.

Method	Equivalence factors	Equivalents of sodium chloride		Related IPC-TM-650 test method
		Micrograms per square inch	Micrograms per square cm	
Resistivity of solvent extract	1.00	10.06	1.56	2.3.5
Omega meter™	1.39	14.00	2.20	2.3.26
Ionograph™	2.01	20.00	3.10	2.3.26.1
Zero ion™	3.68	37.00	5.80	N/A
ICOM 5000™	2.20	22.00	3.40	N/A

A.6.5.3 Organic. When noncoated printed wiring boards are inspected in accordance with A.6.5.3.1 and organic surface contaminants are detected, it should be established that the levels are insufficient to cause measling, delamination, or surface insulation resistance degradation when samples of the coated assembly or test coupon are tested in accordance with A.4.8.6.1.

A.6.5.3.1 Organic contaminant removal. Organic surface contaminants of this type, responsible for documented surface insulation resistance failures, have been removed successfully from circuit card assemblies by a procedure using a two-step fluorocarbon followed by 2-propanol cleaning process.

A.6.6 Acceptable to the Government test laboratories (suitable laboratory). Government accepted test laboratories are those facility that have demonstrated their ability to perform the verification test required by this document. Levels of acceptance include group A, group B and qualification testing.

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A.6.7 Alternate test methods. Other test methods may be substituted for those specified herein provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification.

A.6.8 Group B sample critical design details. Past non-performance versions of this document contained default design details that were assumed to apply to all test coupons subjected to group B inspection, regardless of the master drawing design requirements. With the issuance of the performance version of this document (MIL-PRF-55110E and later), the design details which were universally used to determine acceptance or failure of the group B samples, are no longer present in this document. These needed design details are now relegated to the master drawing or the applicable design standard.

Therefore, additional design information, such as the critical design parameters of the printed wiring board design (plating thickness, dielectric separation, external and internal annular ring, etc.) or the default design standard that applies to the test coupons, must be submitted along with test coupons so that a proper group B evaluation can be completed.

Example, the master drawing of the most complex design selected for group B testing requires .003 inch (.08 mm) of copper plating thickness, .006 inch (.15 mm) of dielectric spacing, and .005 inch (.13 mm) internal annular ring. These design details are considerably different than the baseline design parameters found in either IPC-D-275 or MIL-STD-275. If on these same group B samples, the laboratory acceptable to the Government found that the samples exhibited .002 inch (.05 mm) of copper plating thickness, .005 inch (.13 mm) of dielectric spacing and .005 inch (.13 mm) internal annular ring, they could not state that the results of group B testing met the specification requirement.

APPENDIX B

OPTIONAL QPL/QML PRODUCT ASSURANCE REQUIREMENTS  
FOR QUALIFIED MANUFACTURER LIST PROGRAMS

B.1. SCOPE

B.1.1 Scope. This appendix contains optional requirements concerning the QPL/QML product assurance level for printed wiring boards covered by this specification. The process for extending qualification is also outlined herein. This appendix is an optional part of this specification that can be used only by manufacturers qualified for listing on QML-31032. The information contained herein is intended for guidance.

B.2. APPLICABLE DOCUMENTS

B.2.1 Government specifications. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-31032 - Printed Circuit Board/Printed Wiring Board, General Specification for.

(Unless otherwise indicated, copies of the above document are available from the Defense Printing Services Detachment Office, Building 4D (Customer Services), 700 Tabor Avenue, Philadelphia, PA 19111-5094.)

B.2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 PERFORMANCE REQUIREMENTS ISSUES

B.3.1 Performance requirements. The performance requirements of the applicable MIL-PRF-31032 associated specification shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.2 Accept/reject criteria. The accept/reject criteria of the applicable MIL-PRF-31032 associated specification shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.3 QML brand. At the option of the manufacturer, the QML brand specified in MIL-PRF-31032 may be placed on printed wiring boards that comply with the product assurance requirements of this appendix.

B.4 QUALIFICATIONS ISSUES

B.4.1 Reciprocal qualification (from MIL-PRF-31032). A reciprocal qualification listing (i.e., from a technology qualified to a MIL-PRF-31032 associated specification) to this document will depend on the level of QML technology qualified. Unless otherwise detailed in MIL-PRF-31032 qualification test plan, following guidelines will apply:

- a. Printed board type (see A.4.5.4.1, 6.4.6 and D.3.5). The extent of qualification for base materials types defined in A.4.5.4 will apply. Example; a type 2 qualification under a MIL-PRF-31032 associated specification will not justify a type 3 qualification listing to this document.

## APPENDIX B

- b. Printed board material (see A.4.5.4.2). The extent of qualification for base materials types defined in A.4.5.4 will apply. Example; a BF base material qualification under a MIL-PRF-31032 associated specification will justify a BF base material qualification listing to this document.
- c. Complexity. The manufacturer can only supply QPL/QML technology equal to or less than their QML capability (unlike the QPL product assurance level with its unlimited multilayer capability qualification). Example; a type 3, 6 conductor layer GF base material qualification under a MIL-PRF-31032 associated specification will allow a type 3, GF base material reciprocal qualification listing to this document, however, the manufacturer could certify up to 7.5 layers as compliant (25 percent extension of qualification as allowed by MIL-PRF-31032). In order to supply a 10 conductor layer GF base material QPL/QML printed wiring board, the QML manufacturer would need to extend its QML qualification listing. This could be done by using the add-on provisions of MIL-PRF-31032.

B.4.1.1 Concurrent qualification. Manufacturers already qualified to the QPL level of this document will retain that listing after transitioning to the QPL/QML level. The 3 year expiration time will not apply to the QPL/QML product assurance level.

B.4.1.2 Retention (see B.6.3). The QML status report described in MIL-PRF-31032 will cover the QPL/QML retention requirements to this document.

## B.5 VERIFICATION ISSUES

B.5.1 QPL/QML product assurance. The product assurance requirements for the QPL/QML level of printed wiring board furnished under this specification shall be satisfied by certification to MIL-PRF-31032. All printed wiring boards manufactured and delivered in compliance with this appendix should be produced in accordance with the approved Quality Management plan.

B.5.2 Printed wiring board performance verification. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and test coupons specified in the applicable MIL-PRF-31032 associated specification. The following details are applicable to the QPL/QML product assurance level:

- a. Lot conformance inspection (LCI) product acceptance testing should be based on the applicable verification flows (in-process and group A) offered by this document (see 4.4 and appendix D) or the routine from a similar technology described by a MIL-PRF-31032 associated specification. The various verification flows should be based upon the design standard used to design the printed wiring boards and the available panel test coupons.
- b. MIL-PRF-31032 periodic conformance inspection (PCI) program can be used in lieu of groups B inspection of this document.
- c. Test optimization is applicable to this appendix and can be applied to any verification flow detailed in this document.

## B.6 NOTES

B.6.1 Intended use. This appendix is intended to be used by manufacturer's certified to MIL-PRF-31032 to reduce the complexity of maintaining multiple product/process and testing flows (both MIL-P-55110 or MIL-PRF-55110 and MIL-PRF-31032) within a the manufacturing and testing facility.

B.6.2 Application of the QPL/QML product assurance level to existing requirements.

B.6.2.1 Use of existing master drawings. The QPL/QML printed wiring board manufacturer can use pre-existing master drawing and production artwork without any modifications (existing production masters test coupons and requires no additional or new ones).

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**B.6.2.2 Form, fit and function.** The form, fit and function of the printed wiring boards, whether the QPL/QML product assurance level or the QPL product assurance level is used, will be the same.

**B.6.2.3 Certification.** The printed wiring boards can be certified as being compliant to this document (MIL-PRF-55110).

**B.6.3 Benefits of the QPL/QML product assurance level.** Printed wiring boards produced by QML manufacturers using the provisions of this appendix in lieu of previous revisions would be compliant to this document (MIL-PRF-55110) via the QPL/QML product assurance level with the added benefits as follows:

- a. The QPL/QML manufacturer can use pre-existing master drawing and production artwork without any modifications needed (can use existing production masters test coupons and requires no additional or new ones).
- b. The printed wiring boards, whether the QPL/QML option or the QPL option is used, will be the same.
- c. The level of quality will be the same or higher than the QPL product assurance level.
- d. When using the correct (for the design) Verification Conformance Inspection option, the cost should be the same or less due to enhancements made to accept/reject criteria.
- e. Customers will be more confident that a QPL/QML manufacturer has demonstrated the capabilities to build its design dues to its QML certification and qualification rather the generic standardized qualification test vehicle of the QPL quality assurance level portion of this document.

**B.6.4 Retention issues.** The manufacturer need only to keep the qualifying activity apprised of its total QML program, i.e., MIL-PRF-31032 QML and this document's QPL/QML product assurance level. This means that the manufacturer does not have to maintain two separate compliance programs, (i.e., no need for a QPL compliance program for this document and a QML program for MIL-PRF-31032).

**B.6.5 Certificates of compliance issues.** The manufacturer can certify QPL/QML printed wiring boards process under their QML program as compliant to this document. The certificate of compliance should reference the QPL/QML product assurance level to differentiate the compliant product from printed wiring boards verified using the QPL product assurance level offered in this document.

**B.6.6 Past specification revisions (see appendix D for more details).** Printed wiring boards procured to this document meets and/or exceeds all quality and reliability requirements of previous revisions of MIL-P-55110 or MIL-PRF-55110.

APPENDIX C

C = 0 (ZERO DEFECT) SAMPLING

C.1. SCOPE

C.1.1 Scope. This appendix details the statistical sampling procedures to be used with the QPL product assurance level of this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

C.2. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

C.3. DEFINITIONS AND SYMBOLS.

C.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

- a. C = 0 sample plan: The C = 0 sample plans are defined as a combination of a test specimen usage identifier (see b below) and a sample size series (see c below). The resulting C = 0 sample plan will be a two character designator combination that identifies the sample size series that is to be with a type of test specimen for a particular verification (see C.4.5).
- b. Test specimen usage identifier: The following usage modifiers are used to differentiate when a particular plan is to be used for a particular test specimen: (B) shall be used to identify production printed boards, (T) shall be used for test coupons and an asterisk (\*) for either printed boards or test coupons (see C.4.5 for examples).
- c. Sample size series: The sample size series is defined as the following series of letters: B, D, F, H, J, L, and N that are listed in table C-I (see C.4.5 for examples).
- d. Tightened inspection: Tightened inspection is defined as inspection performed using the next sample size value in the sample size series lower than that specified.
- e. Acceptance number (C): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.
- f. Rejection number (R): Rejection number is defined as one plus the acceptance number.

C.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

- a. C: Acceptance number.
- b. R: Rejection number.

C.4. STATISTICAL SAMPLING PROCEDURES AND SAMPLE PLAN TABLE

C.4.1 General. Statistical sampling shall be conducted using the C = 0 method. The C = 0 method as specified herein is a sampling plan that provides a high degree of assurance that a lot having a proportion defective greater than the specified acceptance number (C = 0) will not be accepted. For all situations, the acceptance number (C) shall be equal to 0 (C = 0) and the rejection number (R) shall be 1 or greater ( $R \geq 1$ ). For reevaluation purposes, see C.4.3.

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**C.4.2 Acceptance and procedure.**

C.4.2.1 Acceptance number (C = 0). Acceptance of inspection lots shall be based on an acceptance number of zero (C = 0).

C.4.2.2 Rejection number (R ≥ 1). Failure of a sample unit for one or more tests of a subgroup shall be charged as a single failure. One or more sample rejects shall be cause for failure of the lot or subplot, as applicable. Any failure on any of the sample units shall constitute a failure of the entire inspection lot or subplot.

C.4.3 Tightened inspection. Tightened inspection shall be performed by sampling using double the sample size as specified in table C-I or 100 percent with zero failures allowed.

C.4.4 Sample size. The sample size for each subgroup shall be determined from table C-I. If lot size is smaller than sample size, test all of the units. The manufacturer may, at his option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number.

C.4.5 C = 0 sample plan construction (selection and usage of the sample size series). The sample size series of table C-I to be used will be directed from the appropriate inspection table. The inspection table will specify the C = 0 sample plan (test specimen identifier and sample size series) or plans (test printed wiring board, test coupons, or either one) to use.

Examples: If an inspection table specified that "Plan BF or TL" be used when verifying test specimens, it is specifying that sample size series "F" of table C-I must be used for selecting printed wiring boards and sample size series "L" must be used for selecting test coupons. If the same inspection table specified that "Plan \*H" be used, then sample size series "H" of table C-I can be used for either printed wiring boards or test coupons.

TABLE C-I. C = 0 (zero defect) sampling.

Lot size	Sample size (number of test specimens to be inspected) <u>1/</u>						
	Series B	Series D	Series F	Series H	Series J	Series L	Series N
1 to 8	All	All	All	5	3	2	1
9 to 15	All	All	13	5	3	2	1
16 to 25	All	All	13	5	3	2	1
26 to 50	All	32	13	5	5	3	1
51 to 90	50	32	13	7	6	4	2
91 to 150	50	32	13	11	7	5	2
151 to 280	50	32	20	13	10	6	2
281 to 500	50	48	29	16	11	7	3
501 to 1200	75	73	34	19	15	8	4
1201 to 3200	116	73	42	23	18	9	5

1/ If lot size is smaller than sample size test all of the units.

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C.5. TEST EQUIPMENT AND INSPECTION FACILITIES

C.5.1 Calibration. All tests and measurements for process control, qualification testing, lot conformance inspection or periodic conformance inspection shall be made with capable instruments whose accuracy has been verified. Calibration of measurement and test equipment and test standards that control the accuracy of inspection and test equipment and facilities shall be in accordance with NCSL Z540, or equivalent.

C.5.2 Inspection facilities. The inspection facility used to perform qualification testing and periodic conformance inspection shall be approved by the qualifying activity for the performance of the tests and inspection requirements of compliant printed wiring boards.

C.5.3 Acquiring activity or manufacturer imposed tests. Acquiring activity or manufacturer imposed tests shall be in accordance with the requirements specified in the master drawing. If any additional imposed tests detect a problem, the manufacturer shall submit all panels/printed wiring boards in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure.

C.5.4 Test method alternatives. Alternate test methods are allowed provided that it is demonstrated to the qualifying activity that such alternatives in no way relax the requirements of the test method referenced by this specification (see appendix D).

C.5.5 Procedure in case of test equipment malfunction or operator error. When it has been established that a improper test is due to test equipment malfunction or operator error, the inspection facility shall document the results of its investigations and corrective actions, if required, and shall make this information available to the qualifying activity and the acquiring activity, as applicable.

APPENDIX D

SUPERSESSSION, VERIFICATION CONFORMANCE INSPECTION OPTIONS,  
AND USAGE OF PAST DESIGN STANDARDS

D.1. SCOPE.

D.1.1 Scope. This appendix contains information and guidance concerning the supersession of legacy Department of Defense documents such as MIL-P-55110 revision C, D, and E and MIL-STD-275 revision D and E. In addition, it contains the alternative Verification Conformance Inspection (VCI) options 1, 2, and 3 that have been structured around the test flows and test coupons of these legacy documents. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

D.2. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

D.3 DEFINITIONS

D.3.1 Design standard. A document that establishes the standard practices, guidelines and default values for the design of printed wiring boards. Within this document, the term "design standard" is used to describe those documents that contains the design, construction, material, and test coupon requirements and guidelines.

D.3.2 Legacy designs or documents (superseded standards). See D.4.2.

D.3.3 Supersession. The act of replacing an legacy document that no longer exists or is no longer supported with a currently supported document.

D.3.4 Verification Conformance Inspection (VCI). A method of allowing printed wiring boards that were designed to or had test coupons applied in accordance with various legacy Department of Defense design standards to be tested to this document.

D.3.5 Quality conformance test circuitry. See IPC-T-50.

D.3.6 Printed wiring board types. The printed wiring board types shall be as specified in either MIL-STD-275 and IPC-D-275. This appendix does not address design rules associated with printed board types 4, 5, and 6 described by IPC-D-275.

D.4 SUPERSESSSION

D.4.1 Superseded specifications. Appendix A of this document includes the essential requirements of the previous revision and can be used to supersede the following specifications:

- a. MIL-P-55110C, dated 26 April 1978.
  1. MIL-P-55110C with Amendment 1, dated 18 July 1978.
  2. MIL-P-55110C with Amendment 2, dated 27 August 1979.
  3. MIL-P-55110C with Amendment 3, dated 16 October 1980.
  4. MIL-P-55110C with Amendment 4, dated 28 June 1982.
  5. MIL-P-55110C with Amendment 5, dated 28 March 1984.
- b. MIL-P-55110D, dated 31 December 1984.
  1. MIL-P-55110D with Amendment 1, dated 6 March 1987.
  2. MIL-P-55110D with Interim Amendment 2(USAF), dated 22 April 1988.
  3. MIL-P-55110D with Amendment 3, dated 18 May 1989.
  4. MIL-P-55110D with Amendment 4, dated 2 December 1990.
- c. MIL-P-55110E, dated 22 December 1993.
- d. MIL-PRF-55110E, dated 22 December 1993 with Amendment 1, dated 29 September 1995.

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D.4.1.1 Reference to superseded specifications. All the requirements of this document (MIL-PRF-55110F) can be interchangeable with those of MIL-P-55110. Therefore, existing procurement documents (master drawings or OEM documents) referencing MIL-P-55110 need not be revised, updated or changed to make reference to MIL-PRF-55110 in order for this document to be used.

D.4.2 Superseded standards. The following design standards have been superseded by IPC-D-275.

MIL-STD-275D dated 26 April 1978.  
MIL-STD-275D with Notice 1 dated 19 January 1979.  
MIL-STD-275D with Notice 2 dated 10 October 1979.  
MIL-STD-275D with Notice 3 dated 5 October 1981.  
MIL-STD-275D with Notice 4 dated 28 May 1982.  
MIL-STD-275D with Notice 5 dated 7 February 1984.  
MIL-STD-275E dated 31 December 1984.  
MIL-STD-275E with Notice 1 dated 8 July 1986.

D.4.3 Testing.

D.4.3.1 Group A testing. Group A testing should be performed to the specific revision, and amendment if applicable, called out by the acquisition documents. For example, if printed wiring boards are produced to MIL-P-55110D with amendment 1, MIL-P-55110D with amendment 3 and MIL-P-55110E, a manufacturer would be expected to perform group A testing, for the applicable lot, to the requirements of the revision specified. In those 3 different revisions (D w/amendment 1, D w/amendment 3, and E) a requirement for an acceptability criteria or test procedure may be the same or it might be significantly different. Retention of qualification summaries for group A should list the lots produced for each, grouped by revision and amendment.

D.4.3.1.1 Group A VCI options. The VCI options associated with group A testing are covered in tables D-II-c, D-II-d, and D-II-e.

D.4.3.2 Group B sample selection and testing. Samples to be selected for group B testing should be based on the most complex compliant printed wiring boards produced that month. For example, if printed wiring boards are produced to MIL-P-55110D, MIL-P-55110D with amendment 4 and MIL-PRF-55110E with amendment 1 during a given month, and the most complex printed wiring boards produced that month were in the lot ordered to MIL-P-55110D with amendment 3, then that should be that lot from which the group B sample should be selected. The samples should be tested in accordance with MIL-P-55110D with amendment 3. If during that same month, printed wiring boards were produced to MIL-P-55110B and MIL-P-55110C, group B tests to those specific revisions would also be required in order to be compliant to those revisions, unless specifically specified in the contract.

D.4.3.2.1 Group B VCI options. The VCI options associated with group B testing are covered in tables D-III-c, D-III-d, and D-III-e.

D.4.3.3 Revisions. Printed wiring boards tested to this document (and using the correct VCI option) generally would meet or exceed the performance requirements of past revisions, however, due to various changes in acceptability and evaluation criteria, testing procedures and test coupon sampling, an exact duplication of a previous revision cannot be claimed or made in all areas of concern. Manufacturers should not pick-and-choose or mix acceptability requirements and/or test procedures from one revision of MIL-P-55110 or MIL-PRF-55110 to another. Compliance should be either to MIL-P-55110C, MIL-P-55110D, MIL-P-55110E (with a specific amendment, if applicable) or this document entirely, unless the manufacturer documents a direct correlation between the revisions (with any amendments, if applicable) under consideration.

D.4.4 Updating master drawing (retooling). Printed wiring board that were designed using superseded Department of Defense design standards do not require conversion to IPC-D-275.

## APPENDIX D

## D.5 VERIFICATION CONFORMANCE OPTIONS

**D.5.1 Verification flow options.** The following is a general description of the Verification Conformance Inspection (VCI) Options that are available for groups A and B testing. Unless otherwise specified, VCI option usage shall be determined using the guidelines contained in this appendix. If a VCI flow cannot be determined, use the default VCI flow option (VCI-4) contained in appendix A this document.

- a. VCI-1: The verification flow using tables D-Id, D-IIId, and D-IIId.
- b. VCI-2: The verification flow using tables D-Ic, D-IIc, and D-IIc.
- c. VCI-3: The verification flow using tables D-Ib, D-IIb, and D-IIb.
- d. VCI-4: The default verification flow using tables A-II, A-III and A-IV (see appendix A of this document).

**D.5.1 Verification conformance options.** This document, unlike past revisions, was developed with the intent that printed wiring boards designed to various design standard (current and legacy) and various revisions of a design standard could be verified using the testing options detailed with this document.

**D.5.1.1 Description.** A description of the verification conformance options are as follows:

- a. VCI Option 1 verification flow (VCI-1) uses test coupons from MIL-STD-275D and is intended to emulate the test routines of MIL-P-55110C with amendment 5.
- b. VCI Option 2 verification flow (VCI-2) uses test coupons from MIL-STD-275E and is intended to emulate the test routines of MIL-P-55110D and MIL-P-55110D with amendments 1, 2, or 3.
- c. VCI Option 3 verification flow (VCI-3) uses test coupons from MIL-STD-275E and is intended to emulate the test routines of MIL-P-55110D with amendment 4 or MIL-P-55110E.
- d. VCI Option 4 verification flow (VCI-4) uses test coupons from IPC-D-275 and is the most current testing plan for printed wiring boards.

**NOTE:** VCI-1 (flow 1) of this document is a close representation of the quality conformance flow of MIL-P-55110C with amendment 5, however, because some of the accept/reject criteria will not closely cross reference

## D.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

**D.6.1 Intended use and intent of this appendix.** This appendix was developed to allow the OPL product assurance level manufacturer the option to minimize the need to maintain numerous permutations of groups A and B test routines. These group A/B test routines include all the different performance requirements, accept/reject criteria, sampling plans, and testing procedures to be used to verify pre-existing (i.e., older) printed wiring board designs to a particular revision of this document. By applying this appendix and using the correct VCI of this document, the many permutations of reference documents, performance requirements, accept/reject criteria, sampling schemes, and testing procedures necessary to be entirely complaint with a previous revision of this document would not be needed.

**IMPORTANT:** This appendix is not a mandatory part of this specification. USE OF THIS APPENDIX IS STRICTLY OPTIONAL. This appendix was not constructed or included in this document to increase the complexity or cost of testing printed wiring boards.

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**D.6.1.1 Background.** The lack of supersession information or guidance regarding the changes in test coupon quantity and usage within MIL-P-55110 and MIL-STD-275 were studied in 1993 as a result of a meeting of representatives of the military services held at the Defense Electronics Supply Center on 25 March 1993 concerning procurement of printed wiring boards designed using legacy revisions of MIL-STD-275. The concept of adding multiple verification tables which emulate the group A and B testing routines of past revisions (calling out the tests and using sample sizes, test coupons, etc.) was judged the best alternative method of all of the options studied.

**D.6.2 Supporting documents.** The documents in this section may be used as guidelines for the development of a multiple Verification Conformance Inspection program and are not mandatory for this specification.

**D.6.2.1 Canceled Government standards (for legacy designs).** The following canceled Department of Defense standard forms a part of this appendix to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

## DEPARTMENT OF DEFENSE

MIL-STD-275 - Printed Wiring for Electronic Equipment.

(MIL-STD-275 was canceled on April 21, 1995. Unless otherwise indicated, copies of the cancellation notice are available from the Defense Printing Services Detachment Office, in Philadelphia, PA. Copies of past revision of this standard are no longer available from the Defense Printing Services Detachment Office but might be available from other informational services.)

**D.6.2.2 Active design standards (for current designs).** The active design standard to current printed wiring board designs is IPC-D-275 "Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies". Information concerning obtaining copies is detailed in appendix A of this document.

**D.6.3 History of MIL-P-55110 and MIL-STD-275.** The method in which MIL-P-55110C, MIL-P-55110D and MIL-P-55110E were written, only particular revisions of MIL-STD-275 test coupons could be used to test printed wiring boards tested to a particular revision of MIL-P-55110 without complications or deviations from the specification. This made the "Superseding" statement on the first page of previous MIL-P-55110's (and MIL-STD-275 also) somewhat untrue in regards to how previous printed wiring board designs could be tested, because the revisions (55110 and its corresponding 275) were really stand alone documents (MIL-STD-275D with MIL-P-55110C and MIL-STD-275E with MIL-P-55110D and MIL-P-55110E). The supersession information that was necessary for the documents to transition the legacy printed wiring board designs to the next or newer document were either ignored, left out, or never even considered for inclusion in previous revisions of either this document or of MIL-STD-275.

TABLE D-I. Verification Conformance Inspection (VCI) options cross reference.

VCI Option	Specification	Design Standard	Group A table	Group B table
1	MIL-P-55110C with Amendment	MIL-STD-275D	D-II-d	D-III-c
2	MIL-P-55110D	MIL-STD-275E	D-II-d	D-III-c
3	MIL-P-55110D with Amendment 4 and MIL-P-55110E	MIL-STD-275E	D-II-e	D-III-e
4	Appendix A of MIL-PRF-55110	IPC-D-275	A-III	A-IV

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TABLE D-II-c. Group A inspection for VCI option 1 (TABLE V of MIL-P-55110C w/amendment 5).

Inspection	Requirement paragraph	Method paragraph	Test specimen <u>c1</u> /				Sample plan <u>c2</u> /
			PWB	TC1	TC2	TC3	
Visual:							
Incoming material	A.3.4	A.4.8.1					Plan BH <u>c3</u> /
Surface examination	A.3.5	A.4.8.1	X				Plan BH <u>c3</u> /
Plated-through hole <u>c4</u> / Etchback	A.3.6 A.3.6.5	A.4.8.2 A.4.8.2.1			A	A A	See <u>c4</u> / See <u>c5</u> /
Marking	A.3.8	A.4.8.1	X				Plan BH
Workmanship	A.3.11	A.4.8.1	X				Plan BH
Dimensional:							
Plating <u>c8</u> / Annular ring (external)	A.3.6.8.2 A.3.5.2.1	A.4.8.2 A.4.8.1	X X				Plan BH See <u>c6</u> /
Hole pattern location	A.3.5.4	A.4.8.1	X				
Dielectric layer thickness	A.3.6.3	A.4.8.2	X			<u>c8</u> /	
Undercutting <u>c8</u> / Conductive pattern <u>c7</u> / Conductor overhang <u>c8</u> / Conductor spacing Bow and twist	A.3.6.17 A.3.5.2.4 A.3.7.4.2 A.3.5.2.2 A.3.7.4.1	A.4.8.2 A.4.8.1 A.4.8.2 A.4.8.1 A.4.8.4.1	X X X X X				See <u>c7</u> /
Plating adhesion	A.3.7.4.3	A.4.8.4.3	X				Plan BH
Hole solderability	A.3.7.4.2	A.4.8.4.5.1			C	B	Plan BH
Surface solderability	A.3.7.4.3	A.4.8.4.5.2		D			Plan BH
Thermal stress	A.3.7.4.8	A.4.8.4.8			C	B	See <u>c4</u> / <u>c9</u> /
Plated-through hole	A.3.7.2.1	A.4.8.2.1					
Layer-to-layer	A.3.7.2.2	A.4.8.2.2					
Annular ring (internal)	A.3.6.1	A.4.8.2.1a					See <u>c7</u> /
Circuitry:							
Continuity	A.3.7.5.1	A.4.8.5.1	X				100 percent <u>c5</u> /
Circuit shorts	A.3.7.5.2	A.4.8.5.2	X				100 percent <u>c5</u> /

c1/ See MIL-STD-275D and 1.2.1. PWB is a production printed wiring board; TC1 is a type 1 test coupon; TC2 is a type 2 test coupon; TC3 is a type 3 test coupon. See appendix D herein for test coupon identification (name) translation to the applicable design standard.

c2/ See appendix C, table C-I for C=0 sampling plans.

c3/ One coupon per panel shall be microsectioned for type 3 boards; the number of coupons to be microsectioned for type 2 boards shall be based on sampling plan BH of table C-I for the number of panels in the lot.

c4/ For type 3 boards, microsection 1 coupon per panel 100 percent of the time in any one direction, and microsection perpendicular to that direction on using sampling plan BH of table C-I. Type 2 boards shall be microsectioned in only one direction.

c5/ If the printed wiring assembly drawing requires 100 percent circuitry test inspection on the printed wiring assembly, a sampling plan based on appendix C, table C-I, plan F, shall be used.

c6/ Attributes may need to be inspected prior to lamination or solder resist application.

c7/ See A.4.6.2.2 for test specimen sampling and description.

c8/ May be inspected by examination of microsectioned coupon associated w/production board.

c9/ See A.4.8.2.2 for test specimen description.

## APPENDIX D

TABLE D-II-d. Group A inspection for VCI option 2 (TABLE VII from MIL-P-55110D).

Inspection	Requirement paragraph	Method paragraph	Test specimen <u>d1</u> /				Sample plan <u>d2</u> /
			PWB	TC1	TC2	TC3	
Material Visual: <u>d7</u> / Edges of printed boards Surface imperfections Subsurface imperfections Marking Resistance to solvents Traceability Workmanship Hole solderability Surface solderability <u>d3</u> / Repair	A.3.4 A.3.5.1.1 A.3.5.1.2 A.3.5.1.3 A.3.8 A.3.7.3.2 A.3.9 A.3.11 A.3.7.4.5.1 A.3.7.4.5.2 A.3.7.10	A.4.6.1.4 4.8.1.1 4.8.1.2 4.8.1.3 4.8.1 4.8.3.2 4.8.1 4.8.1 A.4.8.4.5.1 A.4.8.4.5.2 A.4.8.1					See A.4.6.1.4 Plan BH Plan BH/TJ <u>d7</u> / Plan BH/TJ <u>d7</u> / See <u>d8</u> / Plan BH Plan BH Plan BH Plan BH 100 percent
Dimensional: Hole pattern Bow and twist Conductor spacing Conductive pattern Layer-to-layer registration Annular ring (external) Solder mask thickness Plating & coating thickness	A.3.5.4 A.3.7.4.1 A.3.5.2.2 A.3.5.2.4 A.3.5.6 A.3.5.2.1 A.3.5.8 A.3.6.8	A.4.8.2 A.4.8.4.1 A.4.8.1 A.4.8.1 A.4.8.1 A.4.8.1 A.4.8.1 A.4.8.2	X X X X X X X X				Plan BH Plan BH Plan BH Plan BH See <u>d9</u> / See <u>d3</u> / See <u>d3</u> /
Physical requirements: Solder mask cure & adhesion Plating adhesion <u>d3</u> / Conductor edge outgrowth Thermal stress	A.3.7.4.6 A.3.7.4.3 A.3.7.4.2 A.3.7.4.8	A.4.8.4.6 A.4.8.4.3 A.4.8.4.2 A.4.8.4.8	X X X	J C B	J C B	J C B	Plan BH/TJ <u>d3</u> / Plan BH/TJ <u>d7</u> / Plan BH See <u>d6</u> /
Construction integrity: Plated copper thickness Plating voids Conductor thickness Resin smear and etchback Hole cleaning Etchback Undercutting Annular ring (internal) Dielectric layer thickness Laminate voids Resin recession Lifted lands	A.3.7.2.1 A.3.6.8.2 A.3.6.9.1 A.3.6.2 A.3.6.5 A.3.6.5.2 A.3.6.5.1 A.3.6.17 A.3.6.1 A.3.6.3 A.3.6.6.1 A.3.6.14.1 A.3.6.7.1	A.4.8.2 A.4.8.4.2 A.4.8.4.3 A.4.8.4.4 A.4.8.4.6 A.4.8.4.7 A.4.8.4.9 A.4.8.2 A.4.8.2 A.4.8.2 A.4.8.2 A.4.8.2		B	B	B	Plan BH*
Electrical requirements: Continuity Circuit shorts	A.3.7.5.1 A.3.7.5.2	A.4.8.5.1 A.4.8.5.2	X X				100 percent <u>d10</u> / 100 percent <u>d10</u> /

d1/ See MIL-STD-275E and 1.2.1. PWB is a production printed wiring board; TC1 is a type 1 test coupon; TC2 is a type 2 test coupon; TC3 is a type 3 test coupon.

d2/ See table C-I for C = 0 plans.

d3/ Test coupon or production printed wiring board, manufacturer's option.

d4/ One coupon per panel shall be microsectioned for type 3 boards; the number of coupons to be microsectioned for type 2 boards shall be based on sampling plan BH of table C-I for the number of panels in the lot.

d5/ For type 3 boards, microsection 1 coupon per panel 100 percent of the time in any one direction, and microsection perpendicular to that direction on using sampling plan BH of table C-I. Type 2 boards shall be microsectioned in only one direction.

d6/ See A.4.6.2.2 for test specimen sampling.

d7/ Some attributes may need to be inspected prior to lamination or solder mask application.

d8/ See A.4.8.3.2.1 for test specimen description and sample size.

d9/ See A.4.8.2.2 for test specimen description.

d10/ Type 3 boards only. If the printed wiring assembly drawing requires 100% electrical testing on the assembly, a sampling based on an table C-I, plan F, shall be used.

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APPENDIX D

TABLE D-II-e. Group A inspection for VCI option 3 (TABLE VI from MIL-PRF-55110E).

Inspection	Requirement paragraph	Method paragraph	Test specimen <u>e1/</u>				Sample plan <u>e2/</u>
			PWB	TC1	TC2	TC3	
Visual & dimensional reqs.:							
Acceptability	A.3.7.1	A.4.8.1	X				Plan BH <u>e3/</u>
Solder mask thickness	A.3.5.7.4	A.4.8.1.3	X	E	E	E	Plan BH/TJ <u>e4/</u>
Tin-lead plating thickness	A.3.6.1.3	A.4.8.2.1c	X	C	C	C	Plan BH/TJ <u>e4/</u>
Registration (method II)	A.3.6.2.2	A.4.8.2.2				A/B	See <u>e5/</u>
Repair	A.3.10	A.4.8.1	X				100 percent
Marking	A.3.8	A.4.8.1	X				Plan BH
Workmanship	A.3.11	A.4.8.1	X				Plan BH
Microsection requirements:							
As received	A.3.7.2.1	A.4.8.2		B	B	B	See <u>e6/</u>
Chemical requirements:							
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	<u>e7/</u>	<u>e7/</u>	<u>e7/</u>	<u>e7/</u>	See <u>e7/</u>
Physical requirements:							
Bow and twist	A.3.7.4.1	A.4.8.4.1	X				Plan BH
Conductor edge outgrowth	A.3.7.4.2	A.4.8.4.2	X				Plan BH
Plating adhesion	A.3.7.4.3	A.4.8.4.3	X	C	C	C	Plan BH/TJ <u>e3/ e4/</u>
Solderability							
Hole	A.3.7.4.5.1	A.4.8.4.5.1			A	A	Plan TJ
Surface	A.3.7.4.5.2	A.4.8.4.5.2	X	C			Plan BH/TJ <u>e4/</u>
Solder mask adhesion	A.3.7.4.6	A.4.8.4.6		J	J	J	Plan TJ
Thermal stress	A.3.7.4.8	A.4.8.4.8		B	B	A/B	See <u>e8/</u>
Electrical requirements:							
Continuity <u>e9/</u>	A.3.7.5.1	A.4.8.5.1	X				100 percent <u>e10/</u>
Circuit shorts <u>e9/</u>	A.3.7.5.2	A.4.8.5.2	X				100 percent <u>e10/</u>

e1/ See MIL-STD-275E with notice 1 and 1.2.1. PWB is a production printed wiring board; TC1 is a type 1 test coupon; TC2 is a type 2 test coupon; TC3 is a type 3 test coupon.

e2/ See table C-I in appendix C for C = 0 sampling plans.

e3/ Some attributes may need to be inspected prior to lamination or solder mask application.

e4/ Test coupon or production printed wiring board, manufacturer's option.

e5/ See A.4.8.2.2 for test specimen description (destructive).

e6/ See A.4.6.2.2b for sampling and/or test specimen description.

e7/ See A.4.8.3.2.1 for test specimen description and sample size.

e8/ See A.4.6.2.2c for sampling and/or test specimen description.

e9/ Type 3 printed wiring boards only.

e10/ If the printed wiring assembly drawing required the circuitry test to be run with 100 percent inspection on the printed wiring assembly, a sampling plan based on an table VII, plan F, shall be used.

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APPENDIX D

TABLE D-III-c. Group B inspection for VCI option 1 (TABLE VII from MIL-P-55110C).

Inspection	Requirement paragraph	Method paragraph	Test coupon by type <u>c1/</u>		
			1	2	3
Cleanliness	A.3.7.3.2	A.4.8.3.2	<u>c2/</u>	<u>c2/</u>	<u>c2/</u>
Bond strength (terminal pull)	A.3.7.4.4.1	A.4.8.4.4.1	B	B	B
Rework simulation (Plated-through hole)	A.3.7.4.4.2	A.4.8.4.4.2			<u>c3/</u>
Interconnection resistance	A.3.7.4.8	A.4.8.4.8	E	E	E
Moisture and insulation resistance	A.3.7.5.3	A.4.8.5.3			
Dielectric withstanding voltage	A.3.7.6.1	A.4.8.6.1	E	E	E

c1/ See MIL-STD-275D and 1.2 herein.

c2/ See A.4.8.3.1 for test specimen description and number of samples required.

c3/ See A.4.8.4.8 for test specimen description and number of samples required.

TABLE D-III-d. Group B inspection for VCI option 2 (TABLE IX from MIL-P-55110D).

Inspection	Requirement paragraph	Method paragraph	Test coupon by type <u>d1/</u>		
			1	2	3
Bond strength	A.3.7.4.4.1	A.4.8.4.4.1	B		
Surface peel strength <u>d2/</u> <u>d3/</u>	A.3.7.4.5	A.4.8.4.5			<u>d2/</u> <u>d3/</u>
Rework simulation	A.3.7.4.4.2	A.4.8.4.4.2		B	B
Dielectric withstanding voltage	A.3.7.5.3	A.4.8.5.3	E	E	E
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1	E	E	E

d1/ See MIL-STD-275E and 1.2 herein.

d2/ See A.4.8.4.5 for test coupon description and number of samples required.

d3/ For MIL-P-55110D with Amendment 4 emulation only.

TABLE D-III-e. Group B inspection for VCI option 3 (TABLE VIII from MIL-PRF-55110E).

Inspection	Requirement paragraph	Method paragraph	Test coupon by type <u>e1/</u>		
			Type 1	Type 2	Type 3
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	<u>e2/</u>	<u>e2/</u>	<u>e2/</u>
Bond strength	A.3.7.4.4.1	A.4.8.4.4.1	B		
Rework simulation	A.3.7.4.4.2	A.4.8.4.4.2		B	B
Surface peel strength	A.3.7.4.8	A.4.8.4.8			<u>e3/</u>
Dielectric withstanding voltage	A.3.7.5.3	A.4.8.5.3	E	E	E
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1	E	E	E

e1/ See MIL-STD-275E with notice 1 and 1.2 herein.

e2/ See 4.8.3.2.1 for test specimen description and number of samples required.

e3/ See 4.8.4.8 for test specimen description and number of samples required.

## APPENDIX D

TABLE D-IV. Optional qualification inspection for IPC-100046 and IPC-100047.

Inspection	Requirement paragraph	Method paragraph	Qualification test specimen number 1/	Test specimen 2/				Notes
				TC1	TC2	TC3	PWB	
<b>Acceptability:</b>								
Design and construction 3/ Material	A.3.1.1 A.3.4	A.4.8.1 A.4.6.1.4	1, 2, 3 and 4 1, 2, 3 and 4				X X	3/
Visual and Dimensional Registration (I) Registration (III) Marking Workmanship	A.3.5 A.3.5.6 A.3.5. A.3.8 A.3.11	A.4.8.2.2 A.4.8.1 A.4.8.1	1 and 4 1, 2, 3 and 4 1, 2, 3 and 4			4/ R	X X X	4/
<b>Microsection requirements:</b>								
As received Registration (method II)	A.3.7.2.3 A.3.7.2.2	A.4.8.2.1 A.4.8.2.2	1 and 4 1 and 4		A-3	A-3 5/		5/
<b>Chemical requirements:</b>								
Cleanliness Resistance to solvents	A.3.7.3.1 A.3.7.3.2	A.4.8.3.1 A.4.8.3.2	1, 2 and 4 1, 2 and 4				X X	
<b>Physical requirements:</b>								
Bow and twist Plating adhesion Rework simulation Solderability Hole Surface Thermal stress	A.3.7.4.1 A.3.7.4.3 A.3.7.4.4 A.3.7.4.5.1 A.3.7.4.5.2 A.3.7.4.8	A.4.8.4.1 A.4.8.4.3 A.4.8.4.4 A.4.8.4.5.1 A.4.8.4.5.2 A.4.8.4.8	1, 2 and 4 1, 2, 3 and 4 1 and 2 1 and 4 1 and 4 1 and 4	M A-4 A-4 M B-5	M A-4 A-4 S B-6	M A-4 A-4 S B-6	X	6/ 7/ 6/
<b>Electrical requirements:</b>								
Continuity Circuit shorts Dielectric withstanding voltage (DWV)	A.3.7.5.1 A.3.7.5.2 A.3.7.5.3	4.8.5.1 4.8.5.2 4.8.5.3	1 and 2 1 and 2 2	D-4 E-4 E-2	D-4 E-4 E-2	D-4 E-4 E-2		8/
<b>Environmental requirements:</b>								
Moisture and insulation resistance (MIR) Thermal shock	A.3.7.6.1 A.3.7.6.2	A.4.8.6.1 A.4.8.6.2	2 1 and 2	E-2 D-4	E-2 D-4	E-2 D-4		

1/ A.4.5.2 for qualification test specimen description and identification numbers.

2/ TC1 designates test coupons from a type 1 specimen; TC2 designates test coupons from a type 2 specimen; TC3 designates test coupons from type 3 specimens; panel means inspect the entire specimen. See qualification test specimen master drawing for test coupon design.

3/ Conductor spacing and width on test coupons E-5 and E-6 shall not be evaluated in zone C.

4/ Not applicable for type 3.

5/ See A.4.8.2.2.1 for registration sample units.

6/ Test coupon M-2 and M-5.

7/ Test coupons S-1 and S-6.

8/ Dielectric Withstanding Voltage shall be performed only once before the Moisture and Insulation Resistance test.

APPENDIX E

SEQUENTIAL ELECTROCHEMICAL REDUCTION ANALYSIS (SERA)  
SOLDERABILITY TEST

E.1. SCOPE.

E.1.1 Scope. This test method describes the method and procedure used to evaluate oxidation levels on solderable surfaces. The type and quantity of oxides on copper, tin, and lead surfaces have a significant impact on solderability. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes, attachment lands, and printed wiring board surface conductors. The SERA solderability test method is offered as an alternative to other solderability test methods required by this document. This test method shall not be contractually imposed upon either the contractor or sub-contractor. This appendix is not a mandatory part of the specification. The information contained herein is intended for compliance only when volunteered as an alternative to the other solderability test methods detailed.

E.2. APPLICABLE DOCUMENTS.

E.2.1 Government documents.

E.2.1.1 Specifications. The following specifications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

FEDERAL

O-C-265 - Chemicals, Analytical; General Specification for.

(Unless otherwise indicated, copies of federal specifications are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

E.2.2 Non-Government publications. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issue of the documents cited in the solicitation (see 6.2).

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

J-STD-004 - Requirements for Soldering Fluxes.

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

E.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## APPENDIX E

## E.3. DEFINITIONS.

E.3.1 Sequential Electrochemical Reduction Analysis (SERA). A chronopotentiometric reduction method for assessing tin-lead finish solderability.

## E.4. TESTING.

E.4.1 Apparatus (see figure E1).

E.4.1.1 Reservoir (see detail A). The reservoir shall be a container constructed of a nonmetallic, nonreactive material with a minimum volume of 500 ml. The reservoir shall have an inlet/outlet port, test head chamber port, and a SCE reference electrode port. The inlet/outlet port shall be connected to a vacuum trap tube. The inlet/outlet port shall incorporate a diffuser to aid in the effectiveness of the inert gas purging. Polypropylene tubing may be used for connection tubing. All connection fittings shall be of a nonreactive material. The reservoir shall have the capability of maintaining a positive pressure environment. The reservoir shall be emptied and rinsed with deionized water for every 16 hours of testing.

E.4.1.2 Test head (see detail B). The test head shall be constructed of a nonmetallic, nonreactive material. The test head shall have ports to allow inert gas purging and intake/expulsion of borate buffer solution. The test head shall have either an optical or mechanical means of aligning the test head chamber over the test plated-through hole. The test head shall use Vitron or equivalent o-rings for the test head to test surface interface seals. These o-rings shall be replaced after every 8 hours of testing unless integrity of the o-rings can be documented for extended periods. The test head shall have the capability of maintaining a positive pressure environment.

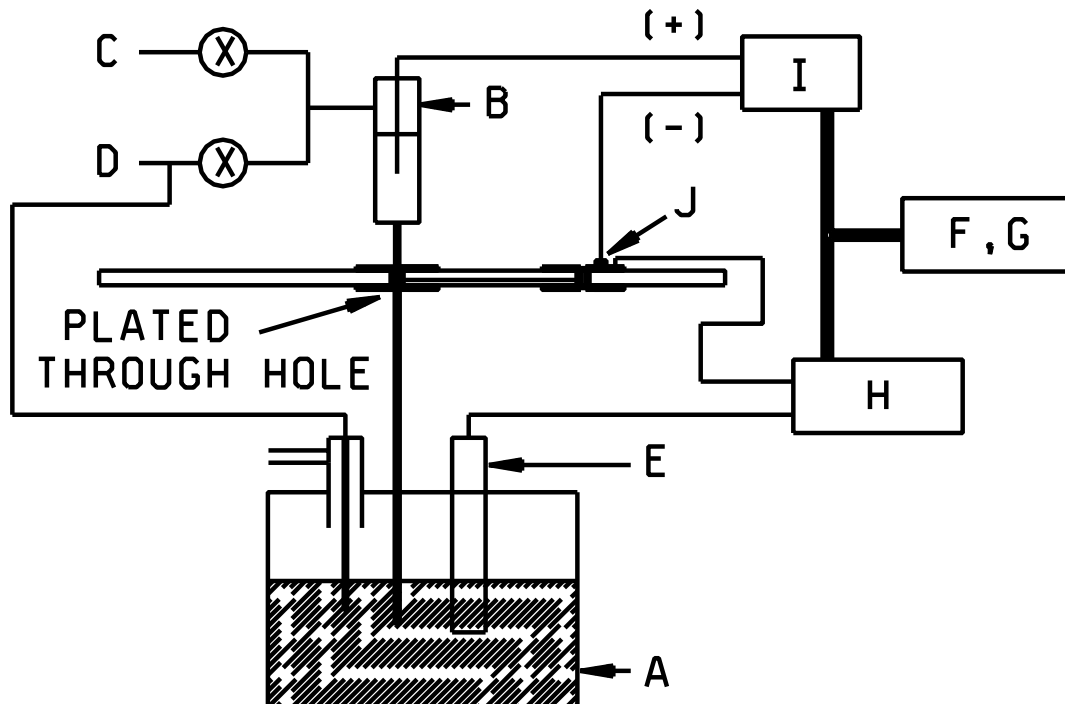


FIGURE E1. Schematic of SERA plated through hole apparatus.

## APPENDIX E

E.4.1.3 Vacuum pump (see detail C). A vacuum pump shall be used to draw buffer solution into and out of the test head compartment. The vacuum pump shall be able to draw minimum vacuum of 5 inches of Hg (15 kPa).

E.4.1.4 Gas regulator (see detail D). An in-line gas regulator shall be used to monitor the flow of the inert purging gas. The gas regulator shall be able to measure a minimum of 1 cubic foot per hour (0.02832 cubic meters per hour) at standard temperature and pressure.

E.4.1.5 SCE reference electrode (see detail E). The reference electrode shall be a saturated calomel electrode (SCE) with a temperature range of  $-5^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$  and a Ph range of 0-14. The SCE reference electrode shall be stored in such a manner as to prevent drying out (either in a saturated KCl solution or in accordance with the manufacturer's instructions). The SCE reference electrode shall be calibrated in accordance with the manufacturer's instructions once every 30 days.

E.4.1.6 Computer (see detail F). The computer shall be equivalent to or better than a MS-DOS compatible, 80286-12MHz, with 512 Kbyte of internal memory and floppy and hard disk drives.

E.4.1.7 IEEE-488 interface card (see detail G). An IEEE-488 interface card is required for data acquisition between the computer, the digital multimeter, and the programmable current source.

E.4.1.8 Digital multimeter (see detail H). A digital multimeter is required to measure the voltage changes during the SERA reduction. The digital multimeter shall have the following characteristics:

- a. A measurable voltage range of 0 V to -2.0 V.
- b. A voltage measurement tolerance of  $\pm 5$  mV.
- c. Voltage measurement RMS noise level should not exceed 10 mV.
- d. Input impedance should be greater than 1 G-Ohm.

E.4.1.9 Programmable current source (see detail I). A programmable current source is required to apply a constant current during the SERA reduction. The programmable current source shall have the following minimum characteristics:

- a. The applied current should be variable in 0.1  $\mu\text{amp}$  steps between 1.0  $\mu\text{amps}$  and 10  $\mu\text{amps}$ .
- b. The applied current should remain constant within  $\pm 5$  percent.

E.4.1.10 Printed wiring board (PWB) contact pin (see detail J). A contact pin is required to complete the electrical circuit with the test plated-through hole. The contact pin shall not exert a force of greater than .5 pounds (0.23 Kg) nor alter the plated-through hole form, fit, or function.

#### E.4.2 Materials.

E.4.2.1 Borate buffer solution. The SERA test requires the use of a borate buffer solution. This solution uses reagent grade boric acid, sodium borate ( $\text{Na}_2\text{B}_4\text{O}_7 \cdot 10 \text{H}_2\text{O}$ ), and deionized water. The recipe is 6.18 grams/liter boric acid and 9.55 grams/liter of sodium borate. The Ph of the borate buffer solution shall range in the range of 8.3 to 8.4. Adjustments to the buffer Ph shall be made using either boric acid or sodium borate additions.

E.4.2.2 Inert gas. An inert gas is required to purge oxygen from the system. Either argon or ultra high purity (99.998%) dry nitrogen shall be used.

E.4.2.3 Deionized water. Deionized water comprises a portion of the borate buffer solution and shall be used to rinse the test plated-through hole after completion of the SERA analysis. The deionized water shall be 1 Megohm conductivity or better.

## APPENDIX E

E.4.2.4 Isopropyl alcohol. Isopropyl alcohol is used to rinse the test plated-through hole after the completion of the SERA analysis. Reagent grade isopropyl alcohol, in accordance with O-C-265, shall be used.

E.4.2.5 Potassium chloride solution (KCI). The SCE reference electrode may be stored in a saturated KCI solution. This solution uses reagent grade potassium chloride, in accordance with O-C-265, in a saturated solution form.

## E.5. PROCEDURES.

E.5.1 General. The test procedure shall be performed on three plated-through holes randomly chosen on the printed wiring board or representative test coupon. The SERA test shall be performed just prior to packaging for storage or shipment or immediately upon removal from the manufacturer's protective package. During handling, care shall be exercised to prevent the surfaces being tested from being abraded or contaminated by grease, perspirants, abnormal atmosphere, etc. The test procedure consists of the following operations:

- a. Proper preparation of SERA system (See B.5.2).
- b. Application of test method (see B.5.3).
- c. Evaluation of test data (see B.5.4).
- d. Proper post test preparation of SERA system (see B.5.5).

E.5.2 Preparation of SERA systems.

- a. Initiate inert gas flow into system and allow a minimum of 10 minutes to elapse prior to testing.
- b. Turn on digital multimeter and programmable current source and allow a minimum of 10 minutes to elapse prior to testing.
- c. Remove reference electrode port and rinse with deionized water. Replace reference electrode port and add sufficient quantity of borate buffer solution to immerse the SCE reference electrode a minimum of 1 inch (25.4 mm).
- d. Remove SCE reference electrode from storage container. Rinse with deionized water, wipe with clean soft cloth, and place into reference electrode port. Attach system electrical connections in accordance with figure E1.
- e. Remove and replace test head o-ring seals as required (see B.4.1.2).
- f. Close SERA test head together thus seating o-rings together on a representative sample plated-through hole and perform vacuum check on system. No visible air bubbles shall be detected in the test head chamber which would indicate improper sealing.

E.5.3 Application of test method.

- a. The test operator shall record the specimen lot date code and manufacturer for each individual printed wiring board. An individual printed wiring board reference chart for the test plated-through holes and PWB contact pin locations shall be maintained for each test specimen configuration.
- b. Insert test specimen onto SERA test head and allow a minimum of 4 seconds for inert gas purging of the test head. Ensure inert gas bubbling is occurring in the reservoir tube.
- c. Attach PWB contact pin.
- d. Attach electrical source leads.

## APPENDIX E

- e. Draw borate buffer solution into test head chamber a minimum of 75 percent of chamber height. Visually monitor test head chamber for leaks.
- f. Partially flush test head chamber to 50 percent height to dislodge any gas bubbles which could be trapped in test hole.
- g. Input computer data for test specimen and test hole identification. Set current density at 30  $\mu$ amp per centimeter squared (plated-through hole area shall be calculated as specified in 50.3.1), test duration at a minimum of 400 seconds, the number of open circuit samples to be measured, and the number of systems measurements at one reading per second. The minimum test duration may be reduced provided complete plated-through hole reduction has been achieved.
- h. Perform SERA test to test duration completion.
- i. Remove electrical source leads.
- j. Remove PWB contact clamp.
- k. Flush borate buffer solution from test hole.
- l. Remove test specimen from SERA test head.
- m. Rinse test plated-through hole with deionized water saturated cotton swab for a minimum of 3 seconds, then rinse test plated-through hole with isopropyl alcohol saturated cotton swab for a minimum of 3 seconds. Allow test plated-through hole to air dry. The rinsing operations may be conducted for all test holes as a one time operation provided the rinsing operation is completed within 10 minutes of completion of the last test hole on that individual printed wiring board specimen. Other documented rinsing operations may be used provided their effectiveness is as good as or better than the cotton swab rinse process.

E.5.3.1 Plated-through hole area calculation. The area of plated-through holes shall be determined using:

$$\text{Area} = (2)(\Pi)(R1)(H) + [(2)(\Pi)(R2^2) - (2)(\Pi)(R1^2)]$$

where H = Printed wiring specimen thickness.  
 R1 = Plated-through hole radius.  
 R2 = O-ring internal radius.

An example of the calculation is as follows:

H = See table E-I for H  
 R1 = Plated-through hole radius = 0.018 inches nominal (0.046 cm)  
 R2 = O-ring internal radius = 0.075 cm

$$\begin{aligned} \text{Area} &= (2)(\Pi)(0.046)(H) + [(2)(\Pi)(0.075^2) - (2)(\Pi)(0.046^2)] \\ &= (0.22890)(H) + [0.03534 - 0.013295] \\ &= 0.2890 \text{ cm (H cm)} + [0.022045 \text{ cm}^2] \end{aligned}$$

## APPENDIX E

TABLE E-I. SERA plated-through hole example calculation data.

Printed wiring board thickness (inches)	H (centimeters)	Area (centimeters <sup>2</sup> )
.020	0.0508	0.0367
.030	0.0762	0.0441
.040	0.1016	0.0514
.050	0.1270	0.0587
.060	0.1524	0.0661
.070	0.1778	0.0734
.080	0.2032	0.0808
.090	0.2286	0.0881
.100	0.2540	0.0955
.110	0.2794	0.1028

**E.5.4 Evaluation of test data.** The change in reduction voltage shall be plotted versus the charge density (current density x time). This SERA curve generated shall be differentiated and then incorporate the following moving window average, curve smoothing function:

$$V(n) = \text{SUM} [V(n-5) \text{ through } V(n+5)] / 11$$

The following 8 SERA parameters shall be calculated from the differentiated and smoothed SERA curve using the following threshold limits listed below. Figure E2 illustrates these parameters and threshold limits on an example SERA curve.

1.  $V_{oc}$  = The final open circuit voltage measured for the SERA differentiated/smoothed curve.
2.  $Q_1$  = The area under the curve defined by  $N_{min1}$  threshold value (defined constant value).
3.  $V_2$  = The voltage on the differentiated/smoothed curve defined by:  $(N_{min3} + N_{min1}$  threshold values)/2.
4.  $Q_2$  = The area under the curve defined by:  $N_{min3}$  threshold value -  $N_{min1}$  threshold value.
5.  $V_3$  = The voltage on the differentiated/smoothed curve defined by:  $(N_{min5} + N_{min3}$  threshold value)/2.
6.  $Q_3$  = The area under the curve defined by:  $N_{min5}$  threshold value -  $N_{min3}$  threshold value.
7.  $V_f$  = Most negative reduction voltage measured for the SERA differentiated/smoothed curve.
8.  $Q_t$  = Total reduction charge (summation of  $Q_1+Q_2+Q_3$ ) for the SERA differentiated/smoothed curve.
9. Threshold constraints:
  - a. Constant = First point on curve for measured voltage before applying current.
  - b.  $N_{min1}$  = First point on curve where measured voltage < -0.85 Volts.
  - c.  $N_{min3}$  = Minimum calculated dVoltage between  $N_1$  and  $N_2$ .
   
 $N_1$  = First point between  $N_{min1}$  and  $N_2$  where calculated Dvoltage < -0.003 volts.
   
 $N_2$  = Last point on curve where measured voltage < -1.3 volts.
  - d.  $N_{min5}$  = Last point on curve where calculated Dvoltage < -1.3 volts.

## APPENDIX E

Unless otherwise agreed upon by the printed wiring board fabricator and user, the SERA parameter for V2 shall meet the minimum acceptable value listed in table E-II. The other seven (7) SERA parameters shall be within the ranges listed in table E-III for a RMA flux per J-STD-004. The printed wiring board soldering performance in the manufacturing process will be directly related to the specific flux used in the soldering process. It is the printed wiring board users responsibility to document the critical SERA parameter levels for other specific flux systems.

TABLE E-II. Minimum acceptable V2 value.

SERA parameter	Minimum acceptable value
V2	Equal to or more positive than -1.07 v

TABLE E-III. SERA values for RMA flux per J-STD-004.

SERA parameter	Minimum acceptable value
Voc	-0.461 to -0.613 V
Q1	0.0 to +1.312 Mc/cm <sup>2</sup>
Q2	0.0 to +3.823 Mc/cm <sup>2</sup>
Q3	0.0 to +3.299 Mc/cm <sup>2</sup>
V3	-1.29 to -1.412 V
Vf	-1.365 to -1.466 V
Qt	+2.005 to +5.985 Mc/cm <sup>2</sup>

E.5.5 Proper post test preparation of SERA system.

- a. Shut off inert gas flow into system.
- b. Shut off digital multimeter and programmable current source.
- c. Remove SCE reference electrode, rinse with deionized water and wipe clean with clean soft cloth. Place SCE reference electrode in storage container.
- d. Remove reference electrode port and dump out borate buffer solution. Rinse inner and outer surfaces of reference electrode port with deionized water. Replace reference electrode port into system.
- e. Remove o-rings and dispose of as required (see B.4.1.2). Rinse test head o-ring seal with deionized water and wipe dry with clean soft cloth.
- f. Empty reservoir of borate buffer solution, rinse with deionized water, and refill with buffer solution as required (see B.4.1.1).

## E.6. NOTES

E.6.1 The equipment described herein is a result of a United States Army MANTECH program investment. For further information, contact Mr. Mike Plott, US Army Research Laboratory, Attn: AMSRL-EP-RC, Adelphi, MD 20783-1145 or by phone at (301) 394-4340.

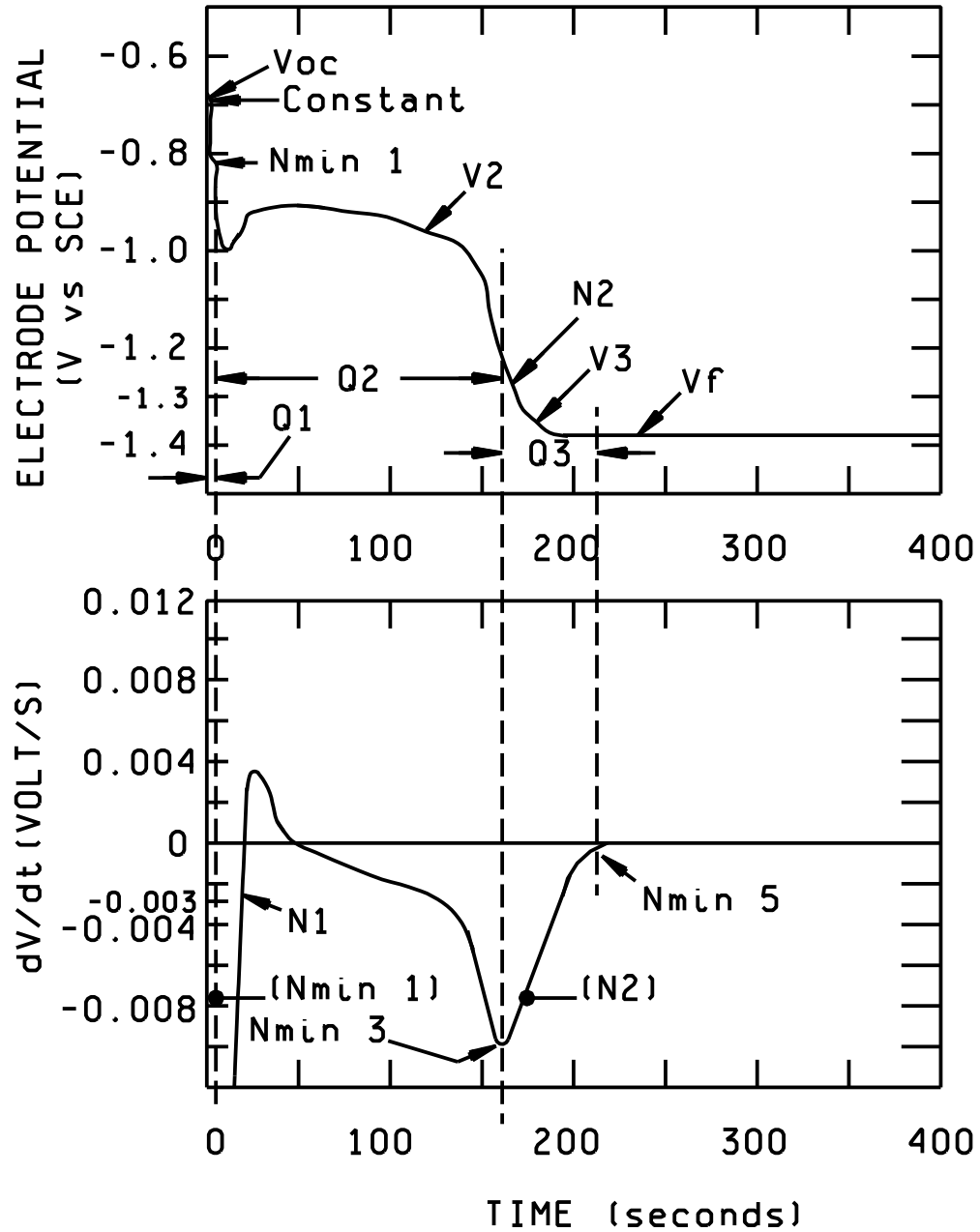


FIGURE E2. Example SERA differentiated/smoothed curve.

MIL-PRF-55110F

CONCLUDING MATERIAL

Custodians:

Army - CR  
Navy - EC  
Air Force - 85

Preparing activity:

DLA - CC

(Project 5998-0083)

Review activities:

Army - AR, MI  
Navy - AS, CG, MC, OS, SH, TD  
Air Force - 11, 16, 17, 19, 99  
NSA - NS

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1. DOCUMENT NUMBER  
MIL-PRF-55110F

2. DOCUMENT DATE (YYMMDD)  
97-05-31

3. DOCUMENT TITLE: PRINTED WIRING BOARD, RIGID, GENERAL SPECIFICATION FOR

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

#### 5. REASON FOR RECOMMENDATION

#### 6. SUBMITTER

a. NAME (Last, First, Middle initial)

b. ORGANIZATION

c. ADDRESS (Include Zip Code)

d. TELEPHONE (Include Area Code)

7. DATE SUBMITTED (YYMMDD)

- (1) Commercial
- (2) AUTOVON (If applicable)

#### 8. PREPARING ACTIVITY

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