

## A VIDEO PRE/POST-PROCESSING LSI FOR VIDEO CAPTURE

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### Abstract

A video processing LSI which converts video signals to digital YUV signals in various image formats was successfully developed for a video capture system. This LSI is suitable for PC cameras, camera/recorders and PC video capture boards.

### Introduction

In addition to non-compressed pictures, compressed pictures such as MPEG and/or

JPEG encoded pictures have become to be handled on PCs<sup>(1)</sup> as the performance of personal computers (PC) has improved impressively. So we developed a video pre/post-processing LSI for a simple video capture system.

The system concept is shown in Figure 1. The PC camera is performed with the camera head and the camera/recorder is performed with the video codec and the storage device in addition to the PC camera. The PC board which is put on a PC is performed with the video codec.

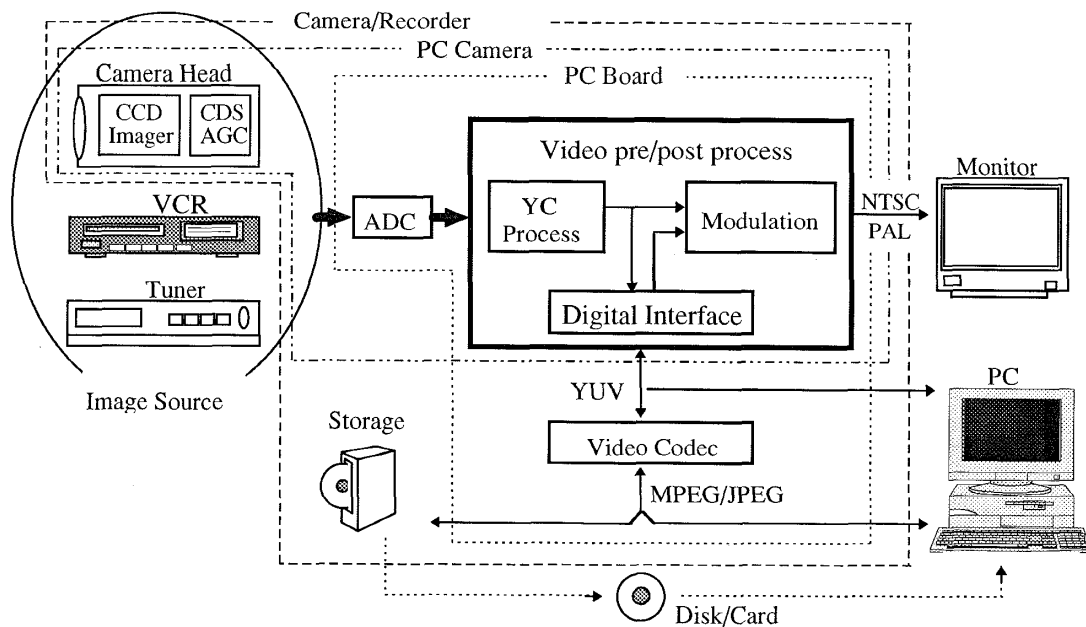


Figure 1 Video capture system

**Table 1 Specifications of input/output signals**

Block	Input signal	Output signal
YC process	CCD imager NTSC/PAL composite	QCIF~Rec.601 YUV4:2:0/4:2:2
Modulation	QCIF~Rec.601 YUV4:2:0/4:2:2	NTSC/PAL YC

The design concept and the technology used in the LSI are described in this paper.

**LSI design concept**

In order to correspond with PC camera use, camera/recorder use and PC board use, a YC process block and a modulation block are included for video pre-processing and post-processing respectively as shown in figure 1 and the input signal and the output signal of above blocks are set as shown in table 1.

The input signal of the YC process block is designed to correspond with an image signal from CCD imagers for PC camera use and camera/recorder use. NTSC and/or PAL composite signals are also designed to be acceptable for PC board use. An image signal from CCD imagers is similar to the composite video signal because a modulated color signal is superimposed on a luminance signal. So the

YUV signals are generated by the YC process block in a similar way. As the CDS/AGC output is chosen as an analog interface, the scale of the YC process block is able to be designed compactly.

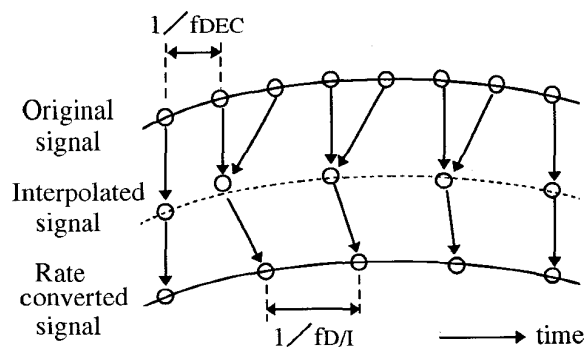
The image format of YUV signals which are output from the YC process block and/or are input to the modulation block are designed to be selectable in order to correspond with various applications such as video phone use, MPEG compression, VGA-PC camera use and so on.

**Circuit block diagram**

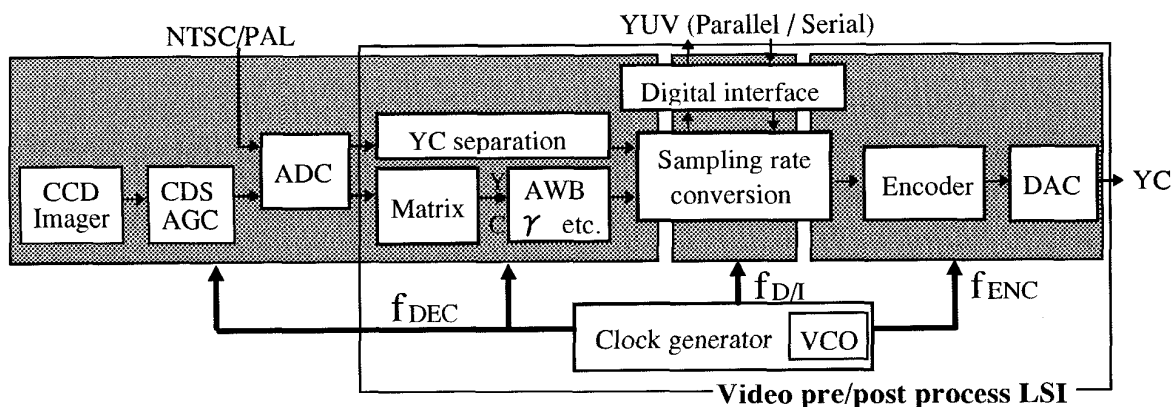
The newly developed technology used in this LSI are following two processing methods.

*(a) Dot number and/or line number conversion*

Figure 2 shows a block diagram of the signal processing for dot number and/or line number



**Figure 3 Sampling rate conversion**



**Figure 2 Block diagram of signal processing system**

conversion. The frequencies of the operating clocks such as  $f_{DEC}$ ,  $f_{D/I}$  and  $f_{ENC}$  are selectable for various image formats. The composite video signal or CDS/AGC output signal is transformed to YUV signals using  $f_{DEC}$  operating clock by the YC separation block or matrix block and the sampling rate is converted to  $f_{D/I}$  by the sampling rate conversion block.

Figure 3 shows the sequence of sampling rate conversion. The rate converted signal is generated by linear interpolation with spatially adjacent two original signals. The linear interpolated signals are written to included FIFO memory at the  $1/f_{DEC}$  interval and are read from the FIFO memory at the  $1/f_{D/I}$  interval.

The output sequence of YUV signals is selectable in following two condition by the digital interface block. (1) parallel : 8bit Y and 8bit UV. The UV signals are dot-interlaced. (2) serial : 8bit YUV

The acceptable input sequence of YUV signals is above mentioned parallel and/or serial. The input digital YUV signals are encoded to YC signals using  $f_{ENC}$  operating clock which is generated by digital VCO including in the LSI and encoded YC signals are converted to analog YC signals by also included D/A converter.

#### (b) Jitter compensation

Figure 4 shows the signal process for NTSC and/or PAL video input. When the composite video signal is input,  $f_{DEC}$  operating clock is

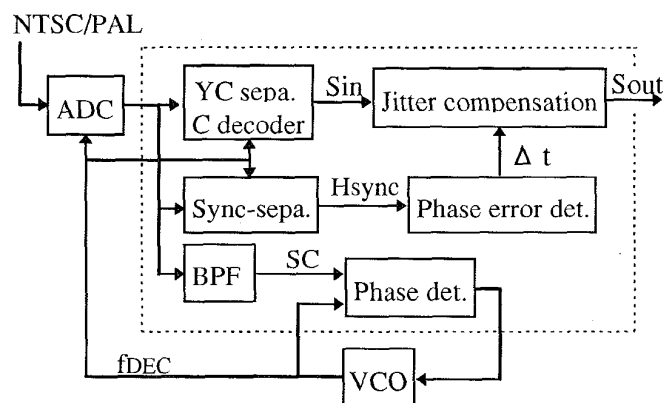
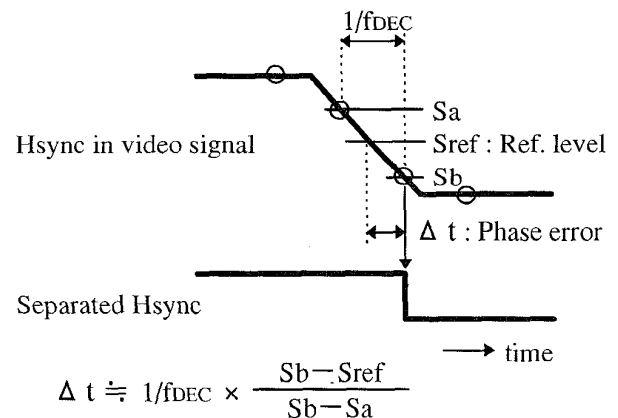
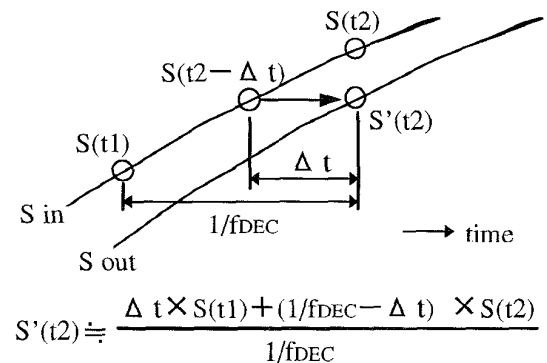


Figure 4 Signal process for video input



(a) Phase error detection



(b) Compensation method

Figure 5 Jitter compensation

phase-locked with the sub-carrier (SC) of the input signal.

A sampled digital video image is converted to base-band YUV signals by YC separation and C decoder block.

In order to make the system common as possible, a VCR's reproduced image which has jitter must be able to be processed. In the above case, a horizontal synchronous pulse (Hsync shown in figure 4) which is separated from the reproduced image has a digitized jitter caused by the  $f_{DEC}$  sampling.

Though the phase shift width of the digitized jitter becomes small in proportion to the increase of the sampling frequency, power consumption and circuit scale become large. So a jitter compensation is developed as shown in figure 4

**Table 1 Example of applications**

CCD imager (pixel)	Output format (dots × lines)	Applications
768 × 485	Rec.601 (720 × 480)	MPEG2 camera
500 × 485	VGA (640 × 480)	PC camera
	SIF (360 × 240)	MPEG1 camera
768 × 576	CIF (360 × 288)	Video phone
500 × 576	QCIF (180 × 144)	Video phone

and 5.

The Hsync in the input video signal ( $S_{in}$ ) should be digitized at a reference level ( $S_{ref}$ ) in every horizontal period. In the case of VCR's reproduced image, horizontal period changes about a few hundred nano-second range. So the phase error ( $\Delta t$ ) occurs and changes in  $1/f_{DEC}$  range.

The phase error is able to be approximated from signal levels of  $S_a$ ,  $S_b$  and  $S_{ref}$  as shown in figure 5(a) because the Hsync is able to be regarded as linear in the short range  $1/f_{DEC}$ .

The phase error  $\Delta t$  is detected by the phase error detection block and is supplied to the jitter compensation block.

In the jitter compensation block, the input video signal ( $S_{in}$ ) is interpolated as shown in figure 5(b). The signals  $S(t_1)$  and  $S(t_2)$  are sampled input video signals at the timing  $t_1$  and  $t_2$  respectively. Using those two signals, a signal  $S(t_2 - \Delta t)$  at the timing  $(t_2 - \Delta t)$  is able to be approximated by linear interpolation. The calculated signal  $S(t_2 - \Delta t)$  is output from the jitter compensation block at the timing  $t_2$  instead of the signal  $S(t_2)$ .

By repeating above signal shift in every horizontal period, the digitized jitter is able to be suppressed. This signal shift method is similar to the image swing suppression method we have reported<sup>(2)</sup>.

### Applications

As the developed LSI includes a pulse generator for CCD imager scanning, a compact PC camera,

camera/recorders and video capture boards are able to be realized in low cost with a video codec LSI which was developed in parallel.

The example of applications for PC camera and camera/recorders is shown in table 1.

### Conclusion

We have developed a pre/post-processing LSI for video capture. Video signals are converted to digital YUV signals with various dot number. With a video codec LSI which was developed in parallel, a simple video codec system was realized.

The specification of the pre/post-processing LSI is shown in table 2. The process is  $0.6 \mu m$  CMOS and power consumption is about 400mW.

**Table 2 Specification of video pre/post-processing LSI**

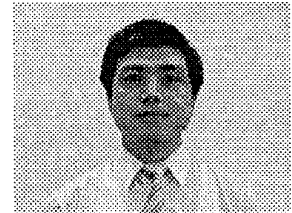
Process	0.6 $\mu m$ CMOS
Logic	140 k gates
RAM	81 k bits
DAC	2 ch
Package	120 TQFP

### Reference

- (1) Imaide et.al."A multimedia color camera providing multi-format digital images", IEEE trans. on CE, Vol.39, No.3, pp467-473, 1993
- (2) Kinugasa et. al."Electronic image stabilizer for video camera use", IEEE trans. on CE, Vol.36, No.3, pp520-525, 1990

## Biographies

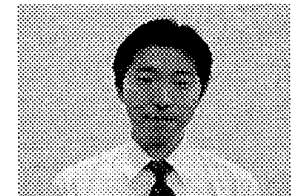
Toshiro Kinugasa received B.S. and M.S. degree from Kobe University in 1977, 1979 respectively. In 1979 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and development of solid-state color video cameras. He is a member of the Institute of Television Engineers of Japan (ITEJ).



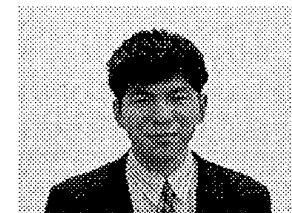
Akihito Nishizawa received B.S. degree from Tokyo Denki University in 1985 respectively. In 1985 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and development of solid-state color video cameras. He is a member of the ITEJ.



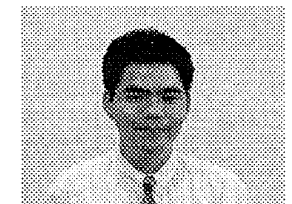
Kazuhiro Koshio received the B.S. degree from University of Electro-Communications in 1987. In 1987 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and the development of solid-state color video cameras. He is a member of the ITEJ.



Takuya Iguchi received B.S. degree from Ritsumeikan University in 1991. In 1991 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and development of solid-state color video cameras. He is a member of the ITEJ.



Junji Kamimura was graduated from Hamamatsu technical high-school in 1986. In 1986 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and development of solid-state color video cameras. He is a member of the ITEJ.



Hiroyuki Marumori received B.S. degree from Chiba University in 1993. In 1993 he joined Multimedia Systems R&D Division, Hitachi Ltd., where he has been engaged in the research and development of solid-state color video cameras. He is a member of the ITEJ.

