

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CITADEL SECURITIES LLC,

Petitioner

v.

HFT SOLUTIONS, LLC,

Patent Owner

Case No. IPR2026-00151

Patent No. 11,575,381

PATENT OWNER'S PRELIMINARY RESPONSE

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No.	Description
Ex. 2001	<i>HFT Solutions, LLC v. Jump Trading LLC</i> , 1:24-cv-13214, Dkt. 30-1 (N.D. Ill.) - Agreed Schedule
Ex. 2002	<i>HFT Solutions, LLC v. Optiver US LLC et al</i> , Case No. 7:25-cv-00415, Dkt. 24 (W.D. Tex.) - Scheduling Order
Ex. 2003	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 30 (N.D. Ill.) – Motion to Dismiss
Ex. 2004	<i>HFT Solutions, LLC v. Citadel Securities LLC</i> , 1:24-cv-13214, Dkt. 57 (N.D. Ill.) – Order Denying Motion to Dismiss
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Ex. 2009	U.S. Patent No. 10,931,286
Ex. 2010	Email title “HFT v. Citadel – deadlines” from Meg Fasulo to Dale Chang dated May 2, 2025
Ex. 2011	Declaration of Dale Chang In Support of Patent Owner’s Preliminary Response
Ex. 2012	Internet Archive Redirect Failure from Website Identified in Ex. 1009

I. INTRODUCTION

The present Petition fails to establish a reasonable likelihood of success on the merits for numerous reasons. First and as a threshold matter, the Petition fails to establish that either Altera or Lockwood qualifies as prior art. Second, to show the “wherein” clause, the Petition assumes all of Altera’s components operate in the same clock domain without providing any evidence of such; the Petition’s lack of evidence on this point is unsurprising because Altera’s components operate in *different* clock domains. Third, the Petition fails to show that Altera teaches using computational circuitry with the parallel data streams to perform any set of operations as claimed. Fourth, the Petition offers divergent claim construction positions¹ from the district court with no explanation.

Any one of these failures shows the Petition cannot succeed and justifies denial of institution. Together, they make it clear there is no likelihood of success on the merits. Because the Petition does not present any grounds that can be instituted, much less any that present a reasonable likelihood of success, institution should be denied.

¹ *Revvo Technologies* explains divergent claim construction positions without explanation is a failure to comply with 37 CFR § 42.104(b)(3), which specifies what “the petition *must* set forth” as opposed to any discretionary issues. As such, Patent Owner addresses it here rather than as a discretionary denial factor.

II. BACKGROUND

A. Citadel's Petition

Petitioner Citadel Securities LLC (“Citadel” or “Petitioner”) challenges claims 1–4 and 6-12 of U.S. Patent No. 11,575,381 (the “’381 Patent”). Petitioner structures its asserted grounds for unpatentability as follows:

- Ground 1: Altera Anticipates Claims 1, 4, 6-10
- Ground 1A: Altera in view of Stratix Handbook and SI5345 Manual Render Obvious Claims 1, 4, 6-10
- Ground 2: Altera and Lockwood Render Obvious Claims 1-4 and 6-12

Because all challenged dependent claims across all grounds depend from claim 1, this Preliminary Response need only address the Petition’s arguments concerning claim 1. If the Petition does not show a reasonable likelihood of prevailing on claim 1, then it cannot prevail on any other challenged claim.

B. Overview of the ’381 Patent

At a high level, the ’381 Patent is directed to addressing a need for phase control to minimize latency in high-speed FPGA systems. Ex. 1001 at 1:43-47, Abstract. Latency reduction is important “in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.” *Id.* at 1:42-43. Contrary to the prior art method of using a clock domain crossing circuit to synchronize clock

signals, which adds delay, the invention teaches a technique that avoids clock domain crossings. *Id.* at 1:47-52.

In particular, the '381 Patent teaches utilizing an external phase-locked loop to avoid the need for clock domain crossings. *Id.* 1:31-35. This solution is reflected, for example, in claim 1 of the '381 Patent, which recites:

1. A method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream, wherein the method comprises the steps of:
 - (a) receiving, by a deserializer in a field programmable array, a clock signal;
 - (b) receiving, by the deserializer, the first serial data stream;
 - (c) generating, by the deserializer, a receiver side clock signal;
 - (d) converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams;
 - (e) transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams;
 - (f) transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within the field programmable gate array, the receiver side clock signal;
 - (g) generating, using the phase lock loop, a second clock signal;
 - (h) generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal;

(i) performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams; and

(j) transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams,

wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.

Ex. 1001 at claim 1.

All other challenged claims (2–4 and 6–12) depend from claim 1.

III. LEVEL OF ORDINARY SKILL IN THE ART

The Petition proposes that a person of ordinary skill in the art in the field of the '381 Patent “would have a bachelor’s degree in electrical or computer engineering and 3-5 years of academic or industry experience working with clocking techniques for FPGAs with high-speed transceivers.” Paper 1 (“Petition” or “Pet.”) at 23. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. THE PETITION DOES NOT DEMONSTRATE A LIKELIHOOD OF SUCCESS ON THE MERITS

The Petition fails on multiple independent counts. First, the Petition fails to make the threshold showing that either Altera or Lockwood are prior art. Second, the Petition assumes from Altera’s silence on the matter that it provides only a single clock domain, and thus no clock domain crossings, but the Petition never shows this

to be the case either directly or inherently and indeed it is not. Third, the Petition fails to show performing a set of operations using computational circuitry is taught by, inherent to, or obvious in light of Altera whether in combination with Stratix or Lockwood. Finally, Citadel's divergent claim construction positions mandate denial of institution. For these myriad reasons, there is no likelihood of success and institution should be denied.

A. The Asserted Grounds Are Not Based On Prior Art

Before addressing the technical shortcomings of the Petition, Citadel fails even to establish that either Altera or Lockwood is prior art. Neither reference is a patent or patent application, as such the Petition must show that they were publicly available, i.e., that each reference was “disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1350 (Fed.Cir.2008). “[T]he burden is on the petitioner to identify with particularity evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent, and therefore that there is a reasonable likelihood that it qualifies as a printed publication.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 16 (PTAB Dec. 20, 2019) (precedential). Here, the Petition fails to meet this burden as to Altera or Lockwood.

The Petition does not show Altera to have been available “long before November 2018” as it claims. Neither of the two pieces of evidence raised by the Petition, the white paper itself and a declaration by the internet archive, establish when or even if Altera was ever publicly available. Without showing Altera was publicly available before November 2018, neither of the Petition’s two grounds have a reasonable likelihood of success and institution should be denied.

The Petition first contends that the date on the face of Altera, November 2015, suggests it was publicly available by that date. Pet. at 9-11. However, such a position has been repeatedly rejected as not actually showing when a document was distributed. *See e.g. Navico Inc. v. Garmin Int’l, Inc.*, No. 216CV00190JRGRSP, 2017 WL 3750252, at *3 (E.D. Tex. July 28, 2017), *report and recommendation adopted*, No. 216CV00190JRGRSP, 2017 WL 3764213 (E.D. Tex. Aug. 29, 2017) (copyright and revision dates insufficient to show date of distribution); *Finjan, Inc. v. Sophos, Inc.*, No. 14-CV-01197-WHO, 2016 WL 2988834, at *26 (N.D. Cal. May 24, 2016) (copyright date and screen shot from decades later showing “Published/distributed” in 1995 insufficient to show date of distribution); *ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015- 00716, slip op. at 17 (Paper 13) (PTAB Aug. 26, 2015) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication). Moreover, looking at Altera itself, there is no statement that the November 2015 relates to publication or other

distribution. *See* Ex. 1004. Rather, “November 2015” is found at the bottom of every page with no context and then at the end of the document as part of the “Document Revision History.” *See id.* A date lacking context, as at the bottom of each page, certainly does not suggest public dissemination much less the kind of public dissemination to the interested public that is required. Indeed, this date could represent the date of authorship or the date of internal circulation or any number of other relevant dates than public dissemination. Likewise, a “Document Revision History” is just that, a history of revision, not a history of dissemination or publication.

Further and contrary to the Petition, Altera is entirely different in nature to those characteristics relied upon by *Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1067 (Fed. Cir. 2024). Altera is not an operating manual and is not clearly “created for dissemination to the interested public to provide instructions about how to assemble, use, clean, and maintain” a product. *See id.* Rather, Altera merely describes a potential functionality, one that the Petition makes no effort to show was ever sold or used by anyone. *See* Ex. 1004 at 1 (“This paper describes a multiple-port 1G/10Gbps Ethernet SyncE synchronization solution....”). Rather, the portion cited by the Petition urging action by customers is part of a copyright notice with nothing to do with the actual substance of Altera. *Id.* By contrast, in *Weber* public accessibility was shown by testimony corroborated by delivery notes, invoices, price

lists, declarations, and emails exchanged with customers. *Weber*, 92 F.4th at 1068. This showed both when and to whom distribution was made. Neither is present here.

Here, the only corroboration offered by the Petition is an Internet Archive declaration for a website, not Altera itself, where Altera is *not* available. The Petition contends Ex. 1009 shows “that the Altera White Paper was available online no later than October 18, 2016.” Pet. at 10. But examining Ex. 1009 does nothing to demonstrate the website shown was indexed, accessible, or well known to the community interested in the subject matter of Altera and moreover does not even show the Altera cited was ever available at the website.

First, and as noted above, to be publicly accessible “persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence” must be able to locate the reference. *See Kyocera*, 545 F.3d at 1350. Here, even if Ex. 1009 showed a website offering Altera for download (as explained below, it does not) it does not show that website was known or findable to the community interested in the subject matter of the reference. Indeed, the Affidavit of Mina Ching provides only how the Internet Archive and the Wayback Machine operate and does not even nominally authenticate Altera. Ex. 1009 at 1. Notably, it provides no suggestion that the underlying website was indexed or that an interested member of the public would or even could find the website shown in Ex. 1009. Neither does Dr. Stanton’s declaration. All Dr. Stanton provides is that “Altera and Silicon Labs made

specifications and data sheets available for download from their respective websites...,” Ex. 1002 at ¶118, not that the website was accessible via an internet search or otherwise known by the interested public. Addressing a similar situation and a similar Internet Archive affidavit, the Board found reliance on the Internet Archive to show a reference was publicly available failed. *See First Solar, Inc. v. Rovshan Sade*, IPR2023-00827, Paper 13 at 18 (PTAB Nov. 16, 2023) (explaining the Internet Archive affidavit “only indicates that the Wayback Machine is searchable ‘by URL,’” same as Ex. 1009, and “not by a query of a search engine before the critical date”). The Petition and Ex. 1009 fail to show Altera was publicly accessible given they do not show the underlying website could be found or was otherwise known.

Second, the website shown in Ex. 1009 does not allow access or download of the relevant entry. Visiting the cited Internet Archive website and attempting to select the relevant entry returns an error. Ex. 2011, Ex. 2012 (showing the error resulting from following the link in the Ex. 1009 website). As far as Ex. 1009 shows, the relevant entry could have led to a different document or indeed have been broken from the beginning and never allowed an interested member of the public to access Altera. As such there is no evidence in the Petition that the listing in Ex. 1009 refers to the same document as Ex. 1004. Indeed, the Board addressed such a situation where the included Internet Archive affidavit was directed to a *different document*

of the same name as the reference used throughout the petition and denied institution. *See First Solar, Inc. v. Rovshan Sade*, IPR2023-00827, Paper 13 at 24 (PTAB Nov. 16, 2023). Given Ex. 1009 does not even show Ex. 1004, much less when or if it was available, it does nothing to corroborate any date for Altera.

Similarly, the Petition fails to show Lockwood was publicly available prior to the critical date. Rather, the Petition merely points to a current website, not even an exhibit, to suggest when Lockwood was published. *See* Pet. at 20. This is improper, because the website only demonstrates Lockwood is *now* available, not that it was available prior to the critical date. Rather, the date provided on Lockwood itself and the cited website are hearsay. *See e.g. ServiceNow, Inc. v. Hewlett-Packard Co.*, Case IPR2015-00716, slip op. at 17 (PTAB Aug. 26, 2015) (Paper 13) (finding a copyright notice unreliable hearsay for purposes of establishing the date of a printed publication). With no evidence of distribution such as an archived version of an indexed website, the Petition cannot meet its burden to show Lockwood is prior art. As the Petition and its expert declaration offer no other support for the proposed date of Lockwood, the Petition fails to demonstrate Lockwood is prior art to the '381 Patent.

Because the Petition has not established that Altera is prior art, grounds 1, 1A, and 2 do not demonstrate any likelihood of success on the merits. Similarly, because

the Petition has not established that Lockwood is prior art, ground 2 fails. As none of the asserted grounds rely on prior art, institution should be denied.²

B. The Wherein Limitation Is Not Taught And Is Indeed Directly Contrary To Altera’s Disclosure

Next, not only does the Petition fail to demonstrate the wherein clause is taught, i.e. that there is no clock-domain-crossing, but also Altera affirmatively must have a clock domain crossing. The Petition argues there is only a single clock domain in Altera (such that there *cannot* be any clock domain crossing). Pet. at 47-48. This apparent inherency assertion is not only unsupported but also directly inconsistent with Altera’s disclosure.

Rather, a Petitioner must explain *with particularity* how the prior art would have rendered the challenged claims unpatentable. 35 U.S.C. § 312(a)(3); 37 CFR § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”). “The IPR petition, thus, must provide an understandable explanation of the element-by-element specifics of the patentability challenges, including the identification of particular portions of prior art on which the petitioner is relying.” *Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1001 (Fed. Cir. 2023). Because, as detailed below, the Petition does not

² Should the Director find that these issues can or should be addressed through further discovery after institution, Patent Owner urges discretionary denial given the volume and nature of discovery that would be required as explained in its Request for Discretionary Denial.

even address its proposed operation of Altera, it has not shown the wherein clause is met. *See, e.g., Apple, Inc. v. Ginko LLC*, IPR2025-01388, Paper 14, slip op. at 3 (PTAB Mar. 2, 2026) (Squires).

The Petition’s argument that because Altera supports “[g]eneration of all system clock frequencies from a single recovered clock frequency” all clock frequencies must be the same, is nonsensical. First, Altera itself immediately disproves this by having the Silicon Labs PLL generate at least four different frequencies from a single input. Ex. 1004 at Fig. 1. Second, Figure 1 shows a myriad of frequencies used throughout Altera. *Id.* It shows rx_recov_ckN is at 125/156.25 MHz while tx_ref_clk can be at 125, 644.53125, 322.265625, or 156.25MHz. *See id.* Moreover, the incoming data rx_dataN and the outgoing data tx_dataN are at 10.3125GHz. *See* Ex. 1005 at 228. Accordingly, far from disclosing or suggesting that all of its clock frequencies are the same, Altera explicitly teaches that it makes use of numerous different clock frequencies.

Furthermore, this only accounts for the clocks that Altera actually shows. As explained *infra* §IV.C, Altera does not show computational circuitry or what clock frequency it might use to perform the claimed set of operations, or rather the unclaimed noise making functions. *See* Ex. 1004 at Fig. 1, 3 (“[t]he FPGA core is filled with instances of a digital noise-maker design...”). Even accepting the Petition’s inclusion of computational circuitry from Stratix and assuming the

performance of a set of operations, the Petition offers no showing regarding what clock domain these operations are performed on. Indeed, the Petition points to page 256 of Stratix for the computational circuitry, Pet. at 44 (referencing logic array block), but this portion of Stratix explains that those logic array blocks have “two unique clock sources and three clock enable signals,” Ex. 1005 at 256, 260. The Petition offers no explanation for how these clock sources and clock signals would not create different domains needing to be crossed.

Beyond the Petition failing to prove its own position, Altera discloses not only multiple clock domains, but *also* expressly teaches clock domain crossings. Altera teaches receiving data at 10.3125 Gbps or GHz. Ex. 1004 at 2. This is the speed at which 10Gbps Ethernet is delivered. *See e.g.* Ex. 1005 at 228 (providing the “Lane Data rate” for 10 Gigabit Ethernet is 10.3125Gbps). Altera labels this rx_dataN. Ex. 1004 at 2. Rx_data is deserialized and eventually sent out as rx_data_out. Pet. at 37-39. The frequency rx_data has immediately after being deserialized is a function of the bit width of the new parallel data stream and rx_data’s original frequency. *See e.g.* Ex. 1001 at 9:66-10:2. Here, the Stratix FPGA has a limited number of choices for bit width: only 8, 10, 16, 20, 32, 40, 64, and 80. *See* Ex. 1005 at 231. The clock that is recovered from the deserializer is 125 or 156.25MHz. *See* Ex. 1004 at 2. To reach those from 10.3125 GHz requires a divisor of 82.5 or 66 bits, *neither* of which

is a width offered by the Stratix hardware used.³ A POSITA would therefore understand that the incoming signal is necessarily deserialized and then crossed into the 125/156.25MHz domain to better align with the goal of Altera to maintain synchronicity with the broader network. As such, one of skill would understand that Altera has a clock domain crossing that would delay the processing of the parallel data stream.

At a minimum, the Petition simply assumes that all components operate in a single clock domain but never explains how Altera's disclosed frequencies and hardware constraints could produce such an architecture. Indeed, nothing in the Petition explains how the deserialized parallel data streams could be clocked directly at 125 or 156.25 MHz given the supported Stratix parallel widths identified above.

Indeed, both Ground 1 and Ground 2 offer the same explanation for the wherein clause. *See* Pet. at 68 (Ground 2 relying on Ground 1's discussion of claim one except as to Limitations 1(e) and 1(i)). Because the Petition both fails to demonstrate its contentions that all components use the same clock and that Altera does not have a clock domain crossing, the Petition fails to demonstrate a likelihood of success as to the wherein clause limitation. Institution should be denied.

³ Indeed, for this 10G ethernet operations, Stratix provides the width should be 40. Ex. 1005 at 228.

C. Limitation 1(i) Is Not Anticipated, Inherent, or Obvious

Here, the Petition attributes much to its seven-page primary reference which is never actually disclosed. Tellingly, the Petition has to affirmatively add the subject of limitation 1(i), computational circuitry, to Altera's Figure 1 and presume it must perform a set of operations. Pet. at 44-46. But even the Petition's secondary references cannot justify adding so entirely foreign a concept to Altera, one that Altera itself never depicted in its figures. The Petition does not show that Altera teaches, inherently discloses, or renders obvious performing a set of operations on the parallel data streams on computational circuitry to generate a second plurality of parallel data streams. Without showing limitation 1(i) is met, the Petition cannot show any claim is invalid and institution should be denied.

Limitation 1(i) requires "performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams." For Ground 1, the Petition proposes "[l]ike all FPGAs, the Stratix FPGA used in Altera includes computational circuitry" and points to the Stratix handbook and a single mention of "FPGA core" in Altera itself. Pet. at 44-45. This is not enough to establish inherency. First, Stratix only provides the computational circuitry is composed of "adaptive logic modules (ALMs) that you *can* configure to implement logic functions, arithmetic functions, and register functions." Ex. 1005 at 256; *see also* Pet. at 45. Can is not must. *PAR Pharm.*,

Inc. v. TWI Pharms., Inc., 773 F.3d 1186, 1195 (Fed. Cir. 2014) (“Inherency, however, may not be established by probabilities or possibilities.”). Second, Altera explains what its “FPGA core” does, it “is filled with instances of a digital noise-maker design...,” it does not perform operations on the serial data. Ex. 1004 at 3. But the Petition still concludes Altera “must also use the computational circuitry.” Such a conclusion fails as it is counter to Altera’s explicit teaching and lacks a rationale. Thus, the petition has not met its burden of establishing inherency or obviousness.

First, Altera itself does not show *any* computational circuitry is used to analyze the serial data stream. Indeed, the only alleged mention of such is the single reference to the “FPGA core” that is only provided as a noisemaker, not performing operations on any data. *See* Ex. 1004 at 3 (“The FPGA core is filled with instances of a digital noise-maker design to create a real-world scenario for measuring the clock parameters.”). The Petition concedes as much when it adds the computational circuitry into the data stream shown in Figure 1. Pet. at 39. Without the computational circuitry being expressly present in this data stream and performing the claimed set of operations, Altera does not anticipate limitation 1(i).

Moreover, the Petition has not shown 1(i) is inherent to Altera. A party suggesting inherency “must show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function.” *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (emphasis original;

internal citations and quotations omitted). The Petition does not attempt to show performing operations on the parallel data streams is inherent to Altera. While the Stratix FPGA used in Altera includes computational circuitry, the Petition makes no effort to show it would be “the natural result flowing from the operation” of Altera to use it in any way, much less in the claimed manner. Indeed, Stratix only provides computational circuitry *can* be configured to perform operations and Altera only teaches using such circuitry as a noise maker. *See* Ex. 1005 at 256, Ex. 1004 at 3. Rather, the Petition identifies computational circuitry and assumes it to be used in a particular manner. Pet. at 45 (“any useful application of an FPGA that uses the transceivers (the RX and TX blocks) *must* also use the computational circuitry.” (emphasis added)). But the Petition offers no explanation, not even a citation, for why this *must* be the case. Instead, the Petition notes Altera mentions “voice, data, and video” applications but it cannot tie that disclosure to any use of computational circuitry much less any set of operations. *See* Pet. at 45. Indeed, Altera does not teach hosting any such operations on the FPGA, instead Altera merely mentions “[e]thernet networks can be used to transport voice, data, and video.” Ex. 1004 at 1. Neither Altera nor the Petition demonstrate transporting such data requires the performance of any functions, much less that it must be on the claimed computational circuitry. Likewise, while the Petition cites Ex. 1013 mentioning Ethernet and application logic

needed for its implementation, there is no attempt to show this makes anything in Altera inherent.

Second, the Petition fails to show limitation 1(i) is obvious under either ground. First, under Ground 1, at best the Petition contends it would be obvious that “in order to use the FPGA-based solution of Altera, the parallel data streams received from the deserializer must go through the computational circuitry and undergo operations.” Pet. at 45 (citing Ex. 1002 at ¶¶150-51 and Ex. 1013 at 2). But all Dr. Stanton adds is that because Altera “was used for ‘voice, data, and video’ applications,” again it was not, “computational circuitry performs operations ... that such computational circuitry constructs, modifies, or triggers transmission of zero, one, or more packet(s) through each of one or more parallel interface(s) to the associated serializer as a consequence.” Ex. 1002 at ¶150. Beyond this being based on a false premise, i.e., that Altera was used for voice, data, or video applications when Altera only provides ethernet may *transport* such data, Dr. Stanton fails to explain why such applications would require the computational circuitry, as opposed to other circuitry whether on or off the FPGA, to perform any particular operations. Altera already explains what the FPGA core does, it is *filled* with noise makers, not voice, data, or video applications. Ex. 1004 at 3. As to Ex. 1013, it is not part of any ground. Moreover, it offers a completely different approach to Ex. 1004.⁴ While both

⁴ Patent Owner refers to Altera here as Ex. 1004 to avoid confusion as Ex. 1013 is

white papers show very similar figure 1's, where Ex. 1004 explains "Figure 1 illustrates ... multiple 1G/10Gb Ethernet media access control (MAC) and physical coding sublayer (PCS) and physical medium attachment (PMA) (PHY) intellectual property (IP) instances," Ex. 1013 provides "the programmable logic ... includes one or more Ethernet cores" and these Ethernet cores contain the MAC and PCS. *See* Ex. 1004 at 2; Ex. 1013 at 2. Because Ex. 1013 uses computational circuitry to perform operations that Ex. 1004 has different components to perform, a POSITA would not have looked to Ex. 1013 for any suggestion that using computational in Ex. 1004 would be obvious. As such, Ex. 1013 says nothing as to what is obvious in a completely different system.

Ground 2 is no better. Again, the Petition contends using the computational circuitry to perform operations as claimed would be obvious by pointing to Ex. 1013 as well as Ex. 1016. But as explained above, because Ex. 1013 describes a completely different solution as to the computational circuitry, it is irrelevant and it would be illogical to implement its teachings on Ex. 1004. Ex. 1016 only offers a generalized description of an FPGA's capability and makes no suggestion that those capabilities would be useful in Ex. 1004 or Lockwood. *See* Pet. at 69 (citing Ex. 1016 with no analysis).

likewise an Altera white paper that could logically also be given the Altera shorthand.

Likewise, Lockwood does not suggest implementing Altera to perform limitation 1(i). To the extent Lockwood suggests performing operations (i.e., trading algorithms), a POSITA would not seek to perform time-sensitive operations on the FPGA taught by Altera. As explained below, Altera is not a low latency solution, Altera is not compatible with Lockwood, and Lockwood suggests other tools, nearly teaching away from Altera. First, the Petition recognizes that Lockwood requires a low latency FPGA, but never actually shows this is consistent with the FPGA disclosed in Altera. Altera having “high reliability” or being “high performance” is not equivalent to low latency. *See* Pet. at 64-65. Rather, “reliability” relates to synchronizing a frequency across an ethernet network. Ex. 1004 at 2 (reliability “is essential for telecommunications data transmission”). Likewise, “performance” here is directly tied with this same “frequency synchronization.” *Id.* at 6 (the white paper demonstrates “a high-performance and flexible solution for frequency synchronization of telecom and data communication networks...”). Neither has anything to do with speed or low latency. Moreover, as explained above, Altera requires multiple latency adding clock domain crossings. *Supra* §IV.B. Even Stratix shows significant latency when using the FPGA for ethernet. Ex. 1005 at 230 (showing a latency of 23 to 46 additional clock cycles for the 10G Ethernet configuration used by Altera in comparison to lower latencies available for other configurations). Second, Altera is not compatible with Lockwood. Lockwood’s

repeated mention of “Smart NICs” as a possible implementation does not suggest Altera. Indeed, Altera is never referred to as a “Smart NIC.” Altera lacks key functionality, notably a PCIe host interface is never mentioned in Altera, nor any suggestion one could be implemented with the functionality taught by Altera. *See* Ex. 1004; *see also* Pet. at 65-67, Ex. 1002 at ¶¶193-97 (never considering if Altera would be considered a Smart NIC or that Altera could implement Lockwood’s PCIE). Indeed, Lockwood relies on this interface and the computational circuitry that Altera provides is “filled with instances of a digital noise-maker design” in its proposed trading set up. *See* Ex. 1007 at Fig. 3. Third, Lockwood identifies available smart NICs a POSITA can use, with no mention of Altera or Stratix. *See id.* Table I. A POSITA would have believed Altera to be incompatible with Lockwood’s trading algorithm and would have never considered Altera to implement Lockwood.

Lastly and in addition to all of the above, the Petition offers no analysis as to “to generate a second plurality of parallel data streams” at all. Instead, all of the Petition’s analysis is directed to adding computational circuitry and a set of operations without even nominally addressing the generation of the second plurality of parallel data streams. *See* Pet. at 44-46. Even assuming “computational circuitry [that] constructs, modifies, or triggers transmission of zero, one, or more packet(s)” neither the Petition nor Dr. Stanton offer an explanation that this generates a second plurality rather than simply retransmitting the first plurality or the like. *See* Ex. 1002

at ¶150; *see also* Pet. at 45-46. Likewise, as to Ground 2, the Petition fails to even identify what it contends would be the “second plurality of parallel data streams.” *See* Pet. at 63-70.

Because neither Ground 1 nor Ground 2 demonstrate Limitation 1(i) is anticipated, inherent, or obvious, institution should be denied.

D. The Petition Does Not Comply with Rule 104(b)(3)

“The Board’s claim construction rules are designated to ensure that the Board correctly construes claim terms and to minimize inconsistency in claim construction between forums.” *Revvo Tech., Inc. v. Cerebrum Sensor Tech., Inc.*, IPR2025-00632, Paper 20 at 4 (November 3, 2025) (Precedential). As such while inconsistent claim construction positions are not barred, under 37 CFR §42.104(b)(3) a petitioner is required to “explain sufficiently why the different positions are warranted, even in instances that do not implicate Section 112(f).” *Id.* at 4-5. Despite this guidance,⁵ Citadel has taken inconsistent constructions and offered no explanation for why such is warranted. Institution should be denied.

Here, except as to “deserializer,” the Petition “interprets the claims ‘in accordance with the ordinary and customary meaning,’” though “[w]ithout conceding that the ’381 patent’s claims are supported under 35 U.S.C. § 112.” Pet. at 25. Citadel offers no further explanation regarding the terms “a first plurality of

⁵ Indeed, *Revvo* was designated precedential a month before the petition was filed.

parallel data streams,” “the first set of parallel data streams,” “the first plurality of data streams,” “the second plurality of parallel data streams,” “the second plurality of data streams,” or the term “delay processing.” *See id.* Despite this, Citadel contends each of these terms render claim 1 indefinite in the district court. *See Ex. 2005 at 39-40.*

Clearly, indefinite and “the ordinary and customary meaning” are inconsistent, yet the Petition offers no explanation for why such inconsistent positions are warranted. There is no justification for these inconsistencies. *See Tesla v. Intellectual Ventures II LLC*, IPR2025-00340, Paper 18, at 3 (Nov. 5, 2025) (Informative) (Squires) (“that it cannot raise indefiniteness challenges in an *inter partes* review is not a sufficient explanation.”). As to the first and second data stream terms, Citadel contends “[i]t is indefinite whether these three different terms represent the same or different data streams because all three different terms are recited throughout the claims of the ’381 patent.” *Ex. 2005 at 39-40.* If that is true, there is no basis for Citadel to now contend it can determine that the prior art teaches these streams. Likewise, Citadel contends “delay processing” is a term of degree with “no standard for measuring such degree.” Again, Citadel offers no explanation for why it can now determine what might fall within the alleged degree.

Because Citadel has taken inconsistent claim construction positions, offered no explanation for its inconsistent positions, and none exist, the Petition fails to

comply with Rule 104 and institution should be denied. *See Revvo*, IPR2025-00632, Paper 20 at 4.

V. CONCLUSION

Because of the failures noted above, Patent Owner respectfully asks the Director to find the Petition has failed to establish any likelihood of success on the merits and deny institution.

Date: March 5, 2026

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on March 5, 2026 by filing this document through the Patent Trial and Appeal Case Tracking System (PTACTS) as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioner:

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