PHASELOCK TECHNIQUES

Third Edition

FLOYD M. GARDNER
Consulting Engineer
Palo Alto, California

WILEY-
INTERSCIENCE

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Published by John Wiley & Sons, Inc., Hoboken, New Jersey.
Published simultaneously in Canada.

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Library of Congress Cataloging-in-Publication Data:

Gardner, Floyd Martin, 1929–
Phaselock techniques / Floyd M. Gardner.—3rd ed.
p. cm.
Includes bibliographical references and index.
ISBN-13 978-0-471-43063-6 (cloth)
ISBN-10 0-471-43063-3 (cloth)
1. Phase-locked loops. I. Title.
TK7872.P38G37 2005
621.3815′364—dc22
2004065041

Printed in the United States of America.

10 9 8 7 6 5 4 3 2 1

To Benjamin

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PREFACE

The first edition of this book was published in 1966 and the second in 1979. Phaselock was an unimaginably exotic subject in 1966, with limited applications and few practitioners. Now phaselock is a mature subject: myriads of phaselock loops are ensconced in the world's electronic devices; numerous applications include phaselock loops; large numbers of practitioners deal with phaselock. No other books on phaselock loops existed when the first edition was published, but more than 20 exist today. Why is a third edition justified at this time?

In 1966, a simple, short introduction to the basics of the subject was needed for an audience for whom phaselock was strange and new. Today, phaselock loops are firmly established in the mainstream of electronics engineering. Much new information on phaselock loops has accumulated over the years, and several topics once thought important have proved to be ephemeral. Experience has taught me that certain explanations would be better presented from revised viewpoints.

There is no need for another introductory text; that function is well served by a number of the books listed in Section 1.3 and probably others as well. Instead, this book reexamines the traditional phaselock topics in greater depth than previously. In addition, much new material has been included, some of it never before published. Examples of additions include revised and expanded material on transfer functions, two chapters related to phase noise, two chapters related to digital phaselock loops, a chapter on charge-pump phaselock loops, expanded material on phase detectors, and a chapter on anomalous phaselocking.

As in the earlier editions, only minimal space has been devoted to circuits. The book is concerned with underlying principles, which remain valid despite technology advances, not with implementations, which change drastically as technology changes. Several parts of the second edition have been omitted: the chapters on optimization and synchronization, and the mathematical appendix. Formal optimization has not proved to be as important to design as was earlier anticipated; instead, a designer is much more likely to perform a trade-off among the few parameters available in a practical phaselock loop. The mathematical appendix has been omitted on the premise that the level of mathematics presented here should be comfortable for all electrical engineering graduates. Synchronization (recovery of carrier and clock from data signals), a major discipline of its own, was deemed to have grown too large to cover adequately in a book on phaselock loops. See Section 17.1 for a brief guide to synchronization.

Simulation is another absent topic. Information presented in several chapters is based on simulations, certain kinds of new data can be gathered only by simulation, and simulation is crucial for design and verification of integrated circuits. Nonetheless, the book does not tell how to conduct simulations of phaselock loops. That topic deserves a separate book of its own; it is too extensive to include here.

Many thousands of articles and books on phaselock have appeared worldwide over the years, far too many to cite individually. Although many pertinent references have been cited in the individual chapters of the book, it is not possible to discover every valuable publication written on each topic. Nor, after many years of work on the subject, is it possible always to remember who originated every technique that is presented. I apologize in advance to anyone who may have been slighted; the omission is not deliberate.

Several guidelines have been followed in selecting reference citations for each chapter: The reference is to an original work; wherever possible, the reference appeared in a public, archival publication; the reference treats lasting principles rather than transitory details of implementation. A reader will observe a preponderance of citations to IEEE publications and to books published in the United States. This choice reflects the omnipresence of IEEE publications and also the contents of my personal library.

I want to thank my many clients over the years who have afforded me the opportunities to learn so much about such a fascinating subject.

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October 2004

NOTATION

A	Amplitude
B_i	Bandwidth (Hz) of an input bandpass filter
B_L	Noise bandwidth (Hz) of a PLL
b	Number of bits in a digital word
b	Ratio of frequency of a pole to frequency of a zero
f	Frequency (Hz)
f	Transform variable of Fourier transforms
f_c	Comparison frequency (Hz) at a phase detector
f_{ck}	Clock frequency (Hz)
f_m	Frequency (Hz) of modulation
f_s	Sampling frequency (Hz), $= 1/t_s$
Δf	Peak frequency deviation (Hz)
Δf	Frequency offset (Hz) from a carrier
δf	Frequency increment (Hz) in a quantized-tuning oscillator
D	Delay (sample intervals)
$E(f)$	$= E(s)\vert_{s=j2\pi f}$
$E(s)$	Closed-loop error transfer function of a PLL
$F(s)$	Transfer function of a loop filter
$\mathrm{FP}[x]$	Fractional part of x
$G(s)$	Open-loop transfer function of a PLL
$H(f)$	$= H(s)\vert_{s=j2\pi f}$
$H(s)$	Closed-loop system transfer function of a PLL
$\mathrm{Im}[x]$	Imaginary part of x
$\mathrm{IP}[x]$	Integer part of x
i	Subscript denoting “input”

i	An integer
$J_n(x)$	Bessel function of the first kind, order n, and argument x
j	$\sqrt{-1}$
K	Loop gain (rad/sec) of a PLL
K'	Normalized (dimensionless) loop gain, $= K\tau_2$
K_d	Gain (V/rad or A/rad) of a phase detector
K_{DC}	DC gain (rad/sec) of a PLL
K_i	Gain coefficient in analog PLL, $i = 1, 2, \ldots$
K_m	Gain (V^{-1}) of a multiplier
K_o	Gain (rad/sec·V) of a VCO
K_p	Gain (V/cycle) of a phase detector $= 2\pi K_d$
K_v	Gain (Hz/V) of a VCO, $= K_o/2\pi$
k	An integer
$L\{x\}$	Laplace transform of x
$\mathcal{L}(f)$	Normalized one-sided RF spectrum of a signal
m, M	An integer
$m(t)$	Modulation waveshape
N_0	One-sided spectrum (V^2/Hz) of white noise
n, N	An integer
$n(t)$	Noise voltage (V)
$n_c(t)$, $n_s(t)$	Baseband quadrature components of bandpass noise (V)
o	Subscript denoting “output” or “oscillator”
$P_{\mathrm{RF}}(f)$	Spectrum analyzer representation of the one-sided spectral density of an RF signal
P_s	Signal power (W)
p	Normalized Laplace variable, $= s\tau_2$
Q	Quality factor of a resonator
Q	Number of quantization levels
Q	Division ratio
$\mathrm{Re}[x]$	Real part of x
$r(t)$	Received signal
$s = \sigma + j\omega$	Transform complex variable of a Laplace transform
SNR	Signal-to-noise ratio
SNR_L	Signal-to-noise ratio in PLL noise bandwidth $2B_L$
t	Time (sec)
t_s	Sampling interval (sec), $= 1/f_s$
$u_c[n]$	Sample-n control input (dimensionless) to an NCO
$u_d[n]$	Sample-n output (dimensionless) of a digital phase detector
V_o	Peak output voltage (V) of a VCO
V_s	Peak voltage (V) of an input signal
$v_c(t)$, $V_c(s)$	VCO control voltage (V)
$v_d(t)$, $V_d(s)$	Phase detector output (V)
$W_{n'}(f)$	One-sided spectral density (rad^2/Hz) of the equivalent noise out of a phase detector

$W_{\theta no}(f)$	One-sided spectral density of the VCO phase (rad^2/Hz) due to the noise input to a PLL
$W_{\mathrm{RF}}(f)$	Measured one-sided spectral density (V^2/Hz) of an RF signal
$W_{vo}(f)$	Theoretical one-sided spectral density (V^2/Hz) of an oscillator output
$W_{\phi}(f)$	One-sided baseband spectrum (rad^2/Hz) of phase noise
z	Transform variable of z-transforms

Greek Symbols

α	Signal suppression factor (dimensionless) in a limiter
β	Modulation index (rad) of angle modulation
γ	Crest factor of a signal
$\varepsilon[n]$	Sample n of phase (cycles)
ζ	Damping factor of a second-order PLL
θ	Phase angle (rad)
θ_a	Steady-state phase error (rad) due to frequency-ramp input
θ_e	Phase error (rad) between an input signal and a VCO, $= \theta_i - \theta_o$
θ_i	Phase angle (rad) of an input signal
θ_{no}	Fluctuation of VCO phase (rad) caused by noise
θ_o	VCO phase (rad)
θ_v	Steady-state phase error (static phase error; loop stress) due to frequency offset
$\Delta\theta$	Phase deviation (rad)
$\Delta\theta$	Amplitude (rad) of phase step
κ	Loop gain (dimensionless) in a digital PLL
κ_d	Gain (rad^{-1}) of a digital phase detector
κ_i	Gain coefficient in a digital PLL, $i = 1, 2, \ldots$
κ_o	Gain (rad) of a NCO
κ_p	Gain (cycle^{-1}) of a digital phase detector, $= 2\pi\kappa_d$
κ_v	Gain (cycles) of an NCO, $= \kappa_o/2\pi$
Λ	Rate of change (rad/sec^2) of frequency, $= d\omega/dt$
ρ	Signal-to-noise ratio
σ_x	Standard deviation of x
τ	Timing error (sec)
τ	Delay (sec)
τ_i	Time constant (sec), $i = 1, 2, \ldots$
τ_2	Time constant (sec) of stabilizing zero in a type 2 PLL
$\phi(t)$	Phase noise (rad)
ψ	Angle (rad) around a unit circle
ψ	Normalized frequency (dimensionless), $= \omega t_s$
$\psi(s)$	Phase (rad) of a transfer function
ψ_{gc}	Normalized unity-gain crossover frequency $\omega_{gc}t_s$ of open-loop transfer function of sampled PLL, $\lvert G(e^{j\psi_{gc}})\rvert = 1$

ω	Angular frequency (rad/sec), $= 2\pi f$
ω_c	Comparison frequency (rad/sec) at a phase detector, $= 2\pi f_c$
ω_{gc}	Unity-gain crossover frequency (rad/sec) of open-loop transfer function, $\lvert G(j\omega_{gc})\rvert = 1$
ω_m	Modulating frequency (rad/sec)
ω_n	Natural frequency (rad/sec) of a second-order PLL
ω_π	Phase crossover frequency (rad/sec), $\mathrm{Arg}[G(j\omega_\pi)] = -\pi$
$\Delta\omega$	Frequency offset or frequency step (rad/sec)
$\Delta\omega_H$	Hold-in limit (rad/sec) of a PLL
$\Delta\omega_L$	Lock-in limit (rad/sec) of a PLL
$\Delta\omega_P$	Pull-in limit (rad/sec) of a PLL

CHAPTER 1

INTRODUCTION

A *phaselock loop* (PLL) contains three essential elements (Fig. 1.1): (1) a phase detector (PD), (2) a loop filter (LF), and (3) a voltage-controlled oscillator (VCO). A phase detector compares the phase of a periodic input signal against the phase of the VCO signal; the output of the PD is a measure of the phase error between its two inputs. The error voltage is then filtered by the loop filter, whose control output is applied to the VCO. Control voltage changes the VCO frequency in a direction that reduces the phase error between the input signal and the VCO.

When the loop is *locked*, the control voltage sets the average frequency of the VCO *exactly* equal to the average frequency of the input signal. For each cycle of input there is one and only one cycle of oscillator output. Phaselock does not

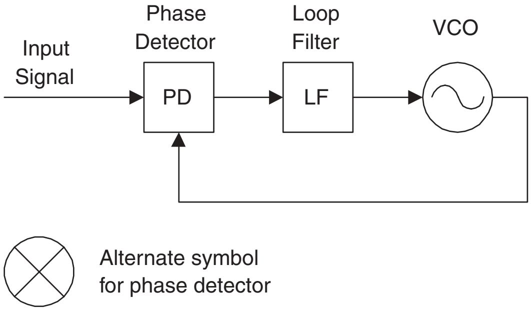

Figure 1.1 Basic phaselock loop.

Phaselock Techniques, Third Edition, by Floyd M. Gardner imply zero phase error; steady phase errors and fluctuating phase errors can both be present. Excessive phase error causes loss of lock.

1.1 SALIENT PROPERTIES OF PLLs

Certain fundamental properties of phaselock loops are outlined here, properties that arise repeatedly throughout the book.

1.1.1 Bandwidth

Bandwidth is one crucial property; PLLs with a narrow bandwidth are employed quite differently from PLLs with a wide bandwidth.

Narrow Bandwidth Suppose that the input signal carries information in its phase or frequency and that the signal is corrupted by additive noise. The task of a phaselock receiver is to reproduce the original signal adequately while removing as much of the noise as possible. To reproduce the signal, the receiver makes use of a local oscillator whose frequency is very close to that expected in the signal. Waveforms of the local oscillator and incoming signal are compared with one another in the phase detector. Error output from the PD indicates instantaneous phase difference. To suppress noise, the PLL averages the error over some length of time, and the average is used to set the frequency and phase of the oscillator.

If the original signal is well behaved (stable in frequency), the local oscillator will need very little information to be able to track, and that information can be obtained by averaging for a long period of time, thereby eliminating noise that could be very large. The input to the PLL is a noisy signal, whereas the output of the VCO is a cleaned-up version of the input. Therefore, the PLL can be regarded as a kind of filter that passes signals and rejects noise.

Two important characteristics of the PLL as a filter are that (1) its bandwidth can be very small and (2) it tracks the signal frequency automatically. These features, automatic tracking and narrow bandwidth, are the primary reasons for using phaselock in receivers. A narrow bandwidth is capable of rejecting large amounts of noise; it is not at all unusual for a PLL to recover a signal that is deeply embedded in the noise at the input to the PD.

Wide Bandwidth Consider an oscillator with desirable features such as power output or high frequency but with poor stability of frequency. Its frequency can be stabilized by phaselocking that oscillator to a reference oscillator of lesser power, perhaps at a lower frequency but with superior frequency stability. The PLL acts as an electronic servomechanism to suppress unwanted frequency or phase fluctuations in the locked oscillator. The PLL should have fast response—wide bandwidth—to suppress the oscillator fluctuations to the greatest extent possible.

1.1.2 Linearity

Every PLL is nonlinear. Tools for analysis of nonlinear systems are exceedingly cumbersome and provide meager benefits compared to the powerful analytical tools available for linear systems. Fortunately, most (but not all) PLLs of interest can be analyzed by linear techniques when in their locked condition. This book argues throughout that linear methods are sufficient for the bulk of analysis and initial design of most PLLs. Therefore, linear approximations are employed wherever feasible.

Several important instances of inescapably nonlinear PLLs are examined in later chapters. The relative simplicity of linear analysis is vividly emphasized by the obstacles that are encountered when trying to understand nonlinear operations.

1.2 ORGANIZATION OF THE BOOK

The book is divided into several parts. The first part, consisting of Chapters 2 through 8, explains fundamental principles of PLLs. The second part covers the elements within a PLL: oscillators (Chapter 9), phase detectors (Chapter 10), loop filters (Chapter 11), and charge pumps (Chapter 12). Chapters 13 (on digital PLLs) and 14 (on PLL misbehavior) each stand alone. The last part, Chapters 15 through 17, describes various applications of PLLs.

A word on the explanations that follow: The first introduction of a topic is usually simplified, if not oversimplified, with little or no regard for rigor or any warning about complicating factors. Where necessary, complexities are addressed later, after a reader has had a chance to absorb the fundamentals. The essential elements of PLLs are not particularly abstruse even though analysis of many aspects can be formidable. A reader is more likely to be put off by the sheer mass of detail rather than by finding any single topic impenetrable. A system as illustrated in Fig. 1.1 initially appears so simple as to be trivial: How can its treatment fill so many pages? Read the book and find out.

1.3 ANNOTATED BIBLIOGRAPHY

This section lists books, reprint volumes, and journal special issues devoted to PLLs. Items within a heading are entered chronologically. The items listed cover mainly the general topic of PLLs; no claim is made for completeness. More specialized publications are cited in later chapters.

1.3.1 Books

A. J. Viterbi, *Principles of Coherent Communications*, McGraw-Hill, New York, 1966, Chaps. 2–4. (An account of the contributions on PLLs by a noted pioneer in the electronics community.)

W. C. Lindsey, *Synchronization Systems in Communications and Control*, Prentice Hall, Englewood Cliffs, NJ, 1972. (Massive exposition on PLLs in noise. Includes deep theory of stochastic processes and nonlinear analysis.)

W. C. Lindsey and M. K. Simon, *Telecommunication Systems Engineering*, Prentice Hall, Englewood Cliffs NJ, 1973. (High-level presentation of application of PLLs in deep-space receivers.)

A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design*, Wiley, New York, 1976. (Contains data not found elsewhere on the performance of PLL receivers.)

H. Meyr and G. Ascheid, *Synchronization in Digital Systems: Phase-, Frequency-Locked Loops, and Amplitude Control*, Wiley, New York, 1990. (A wealth of material, invaluable to any serious worker on PLLs.)

D. H. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice Hall, Englewood Cliffs, NJ, 1991. (A practical introduction to PLLs. Offers numerous shortcut approximations.)

J. Encinas, *Phase Locked Loops*, Kluwer Academic, Boston, MA, 1993.

P. V. Brennan, *Phase-Locked Loops: Principles and Practice*, McGraw-Hill, New York, 1996.

J. L. Stensby, *Phase-Locked Loops: Theory and Applications*, CRC Press, Cleveland, OH, 1997. (Includes coverage not found elsewhere on nonlinear operations.)

W. Egan, *Phase-Lock Basics*, Wiley, New York, 1998. (Outgrowth of university courses on PLLs. Affords online access to simulations of PLLs.)

D. R. Stephens, *Phase-Locked Loops for Wireless Communications*, Kluwer Academic, Boston, MA, 2001.

R. E. Best, *Phase-Locked Loops*, 5th ed., McGraw-Hill, New York, 2003. (A popular introductory text, profusely illustrated, with accompanying software.)

V. F. Kroupa, *Phase Lock Loops and Frequency Synthesis*, Wiley, Chicester, West Sussex, England, 2003. (Painstaking tour through the fundamentals.)

N. I. Margaris, *Theory of the Non-linear Analog Phase Locked Loop*, Springer-Verlag, Berlin, 2004.

W. H. Tranter, *Phase-Locked Loops and Synchronization Systems: A Matlab-Based Simulation Library*, Prentice Hall, Englewood Cliffs, NJ, 2005.

1.3.2 Reprint Volumes

These volumes are collections of selected papers on the general subject of PLLs. Many of the papers are classic expositions of their subjects. Additional reprint volumes, covering more specialized areas, are cited in later chapters.

W. C. Lindsey and M. K. Simon, eds., *Phase-Locked Loops and Their Applications*, IEEE Press, New York, 1978.

W. C. Lindsey and C. M. Chie, eds., *Phase-Locked Loops*, IEEE Press, New York, 1986.

B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, New York, 1996.

B. Razavi, *Phase-Locking in High-Performance Systems*, IEEE Press, New York, and Wiley, Hoboken, NJ, 2003.

1.3.3 Journal Special Issues

Two entire issues of IEEE journals were devoted to phaselock loops.

W. C. Lindsey and C. M. Chie, guest eds., *IEEE Transactions on Communications* ***COM-30***, Oct. 1982.

M. H. Perrott and G.-Y. Wie, guest eds., *IEEE Transactions on Circuits and Systems II* ***50***, Nov. 2003.

CHAPTER 2

TRANSFER FUNCTIONS OF ANALOG PLLs

Although PLLs are inherently and inescapably nonlinear circuits, the main operations of many can be approximated very well by linear models. A linear model typically will be applicable if phase error is small, a condition normally attained when the loop is locked. Most analysis and design of PLLs can be based on the linear approximations; analysis becomes far more challenging when the linear approximations fail.

Among the tools of linear analysis, the Laplace and Fourier transforms—and various concepts derived therefrom—stand out as being particularly valuable. The related concept of a *transfer function*, describing a transform-domain relation between the input and output of a linear circuit, is an extremely powerful tool for dealing with PLLs. Analytical design of PLLs is carried out almost entirely through transfer functions. Take heed that only linear circuits have transfer functions; no such property exists for nonlinear circuits.

Transfer functions of analog PLLs are introduced in this chapter and the next, and transfer functions of digital PLLs are treated in Chapter 4. Results are employed throughout the rest of the book.

2.1 BASIC TRANSFER FUNCTIONS

In ordinary electrical circuits, a transfer function relates voltages or currents of the input and output signals. But in a PLL, the input or output variables of most interest are phases of the signals, not the voltages or currents. The transfer

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Phaselock Techniques, Third Edition, by Floyd M. Gardner