

Filed: December 3, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CITADEL SECURITIES LLC,  
Petitioner

v.

HFT SOLUTIONS, LLC,  
Patent Owner

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Case No. IPR2026-00155

U.S. Patent No. 11,575,381

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**PETITION FOR INTER PARTES REVIEW**  
**OF CLAIMS 1-4 AND 6-12 OF U.S. PATENT NO. 11,575,381**

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1001	U.S. Patent No. 11,575,381
1002	Expert Declaration of Kevin B. Stanton, Ph.D.
1003	File History of U.S. Patent No. 11,575,381
1004	Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs (“Altera”)
1005	Altera Stratix V Handbook (“Stratix Handbook”)
1006	Any-Frequency, Any-Output Jitter-Attenuators/Clock Multipliers Si5345, Si5344, Si5342 Family Reference Manual, August 2015 (“Si5345 Manual”)
1007	A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT) by John W. Lockwood et al., 2012 IEEE 20th Annual Symposium on High-Performance Interconnects (September 2012), <a href="https://doi.org/10.1109/HOTI.2012.15">https://doi.org/10.1109/HOTI.2012.15</a> (“Lockwood”)
1008	Plaintiff HFT Solutions’ Response in Opposition to Defendant Citadel Securities’ Motion to Dismiss
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1013	Altera and IDT Synchronous Ethernet Solution for ITU-T G.8262
1014	“The Race to Zero Latency for High Frequency Trading” by Saul Sahoo

EXHIBIT NO.	DESCRIPTION
1015	U.S. Patent No. 10,169,814
1016	High-Frequency Trading, A Practical Guide to Algorithmic Strategies and Trading Systems by Irene Aldridge (2013)
1017	Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig Megafunctions, Application Note AN-661-3.0, Altera Corporation, November 2013
1018	Exploring Algorithmic Trading in Reconfigurable Hardware by Stephen Wray (2010)
1019	HDL Chip Design, A practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog by Douglas J. Smith, Doone Publications (1999)
1020	UltraScale Architecture Clocking Resources – User Guide, Xilinx, April 9, 2018
1021	Chip Hall of Fame: XC2064 FPGA, IEEE Spectrum, June 30, 2017
1022	List and comparison of FPGA companies by Jeff Johnson, FPGA Developer, July 15, 2011
1023	Understanding Clock Domain Crossing (CDC) Checks and Techniques by Saurabh Verna, <i>et al.</i> , EE Times, December 24, 2007
1024	Phaselock Techniques by Floyd Gardner, Third Edition (2005)
1025	Interactive Brokers’ Founder Changed Trading Forever. What He Sees Next by David Wignall, Barrons (October 2, 2025)
1026	Wall Street’s Quest to Process Data at the Speed of Light by Richard Martin, Rubinow (April 21, 2017)
1027	FPGA accelerated low-latency market data feed processing by Gareth W. Morris, <i>et al.</i> , 17 <sup>th</sup> IEEE Symposium on High Performance Interconnects (2009)
1028	The Once and Future Internet by Daniel Svensson, Design Lines (May 1, 2001)

EXHIBIT NO.	DESCRIPTION
1029	An Introduction to Synchronized Internet, Embedded (March 3, 2009)
1030	Design of Control Systems by A. Frank D'Souza, Prentice-Hall (1988)
1031	Clock Networks and PLLs in Stratix V Devices, Altera (May 6, 2013)

## I. INTRODUCTION

Citadel Securities challenges claims 1-4 and 6-12 of U.S. Patent No. 11,575,381 as unpatentable. Although lengthy and couched in complicated-seeming language, the challenged claims describe nothing more than a preexisting method that—at the time these claims were filed—had long been in use for keeping clock signals in sync on a programmable chip called a field programmable gate array (FPGA), using an external system called a phase-locked loop (PLL), which keeps the timing of one signal matched with another.

No aspect of the challenged claims is new. PLLs have been around since the 1930s, and FPGAs have been commercially available since the 1980s. Ex. 1002 at ¶ 39. The prior art cited on the face of the '381 patent confirms as much. *See* Ex. 1001 at 1-2 (citing FPGA user guides and handbooks and articles about PLLs). Patent Owner has admitted that the '381 patent “do[es] not claim to invent FPGAs or any other individual component.” Ex. 1008 at 17. Indeed, the '381 patent itself acknowledges the well-established prior use of FPGAs in the financial industry. Ex. 1001 at 1:42-44.

Despite this, the '381 patent suggests that it solved a problem in the field and asserts that using a PLL that is external to the FPGA in order to provide “phase synchronization” without “introduc[ing] unwanted latency” caused by “clock domain crossing circuits” is novel. *Id.* at 1:49-52. Patent Owner has emphasized its

position that what is supposedly new here is “using an external PLL to synchronize” clock signals. Ex. 1008 at 17. That is not right.

In November of 2018, when the initial application leading to the '381 patent was first filed, there was nothing new about using an external PLL to synchronize clock signals to minimize latency. Skilled artisans in this space knew by 2018 that using clock-domain crossing circuitry requires additional time to properly synchronize clock signals and therefore adds additional latency. Ex. 1002 at ¶ 42. And they had also long understood that, as an alternative, clocks can be synchronized using a PLL. *Id.* at ¶ 47. Skilled artisans therefore understood the design choice that Patent Owner claims to have invented—the use of a PLL to synchronize clocks. Patent Owner cannot invent something that was already understood and in use.

The use of an external PLL was also nothing new. Years before the '381 patent, Altera (a top FPGA manufacturer) gave skilled artisans a clear map to ensuring proper synchronization in an FPGA with a commonly used external PLL through a white paper, the prior art cited here. Ex. 1004. Altera therefore accomplished exactly what the '381 patent later claimed—an FPGA and external PLL system for synchronizing a receiver-side clock and transmitter-side clock such that clock-domain crossing circuitry was not needed, thus anticipating the majority of the claims of the '381 patent.

To the extent Patent Owner claims there are any differences between what Altera disclosed and the claims of the '381 patent, those differences are trivial and would have been obvious to a skilled artisan. For example, while the use case Altera describes was not specific to financial instrument trading, which is referenced in claims 2 and 3, a skilled artisan would have been motivated to use its teachings in such a setting. Indeed, the '381 patent acknowledges that, well before its filing, FPGAs were being “used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.” Ex. 1001 at 1:41-43. This is because high-frequency trading, which involves profiting from small price movements, requires low latency in the delivery of information to identify and capitalize on short-lived market opportunities. *See, e.g.*, Ex. 1007 at 1 (As early as 2012, “FPGAs [we]re being used in electronic trading to approach the goal of zero latency.”). A skilled artisan would have therefore looked to how FPGAs are used in computer networking and recognized that Altera’s synchronization approach avoided using clock-domain crossing circuitry, thereby eliminating the latency cost associated with such circuits.

For these reasons, as more fully detailed below, Citadel Securities requests that the Board institute review of claims 1-4 and 6-12 of the '381 patent and cancel all challenged claims as unpatentable.

## **II. MANDATORY NOTICES**

### **A. Real Parties in Interest**

Petitioner identifies itself, Citadel Securities LLC, as the real party-in-interest. Additionally, while Petitioner does not believe that the following entities must be disclosed as real parties-in-interest because these entities (or any of them) have not exercised control and could not have exercised control over Petitioner's participation in this IPR, out of an abundance of caution, Petitioner discloses the following entities as additional real parties-in-interest who will be bound by the outcome of this IPR to the same extent as Petitioner:

Citadel Securities GP LLC

Citadel Securities Holdings LP

CSIPTRS LP

Citadel Securities Global Holdings LLC

Citadel Securities Group LP

Citadel Securities Group Holdings LLC

CSHC US LLC

Citadel ENTP Services Group LLC

Citadel Enterprise Americas LLC

Citadel Enterprise Americas Services LLC

Citadel Securities Americas Services LLC

Citadel Securities Americas LLC

Board of Citadel Securities Group LP

**B. Related Matters**

Patent Owner has asserted the '381 patent in two actions currently pending in the United States District Court for the Northern District of Illinois and another action currently pending in the United States District Court for the Western District of Texas:

*HFT Solutions, LLC v. Citadel Securities LLC*, 1:24-cv-13213 (N.D. Ill.)

*HFT Solutions, LLC v. Jump Trading, LLC*, 1:24-cv-13214 (N.D. Ill.)

*HFT Solutions, LLC v. Optiver US LLC*, 7:25-cv-00415 (W.D. Tex.)

**C. Identification of Counsel and Service Information**

Petitioner designates the following counsel as Lead and Back-up Counsel. A power of attorney is filed concurrently with this petition.

<b>Lead Counsel</b>	<b>Back-Up Counsel</b>
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### **III. REQUIREMENTS FOR REVIEW**

Standing: Petitioner certifies under 37 C.F.R. § 42.104(a) that the '381 patent is eligible for inter partes review and that Petitioner is not barred or estopped from requesting inter partes review on the grounds set forth below.

Petitioner requests cancellation of the challenged claims under the following grounds:

<b>Ground</b>	<b>Claims</b>	<b>Basis</b>	<b>References</b>
1	1, 4, 6-10	§ 102	Altera
1A	1, 4, 6-10	§ 103	Altera, Stratix Handbook, Si5345 Manual
2	1-4, 6-12	§ 103	Altera, Lockwood

### **IV. DISCRETIONARY DENIAL NOT WARRANTED**

The Director should not exercise discretion to deny the present petition. The '381 patent issued less than three years ago (Feb. 7, 2023), and no forum has previously adjudicated the validity or patentability of the challenged claims. There is no basis for any settled expectation that the challenged claims are valid or enforceable.

HFT Solutions has asserted the '381 patent against Citadel Securities in the Northern District of Illinois. This co-pending district court case is in its infancy, with no trial date or other deadlines set and no discovery completed. Indeed, Patent Owner has yet to propound *any* discovery in that litigation, and thus investment in this parallel proceeding by the court and the parties is negligible. The early stage of the district court litigation also suggests that a stay may be granted if IPR is instituted. Overlap between the issues in the parallel proceeding and the issues raised in this petition is at most partial—for example, Citadel Securities intends to assert in the district court that the claims of the '381 patent are invalid under § 112.

The primary references relied on in this IPR were not before the patent examiner during prosecution. The Altera reference in particular was located by Citadel Securities' engineers, who are persons of at least ordinary skill in the relevant field, through a Google search using the terms "FPGA PLL synchronous ethernet," which returned the Altera white paper on the first page of search results. Altera was not art of record during prosecution, and the only non-patent database searched by the examiner was the IBM Technical Disclosure Bulletin (IBM\_TDB), which does not contain Altera. The only non-patent literature in the prosecution history was identified by the applicant, and the prosecution history contains no rejections for anticipation or obviousness.

There are no economic, public health, or national security interests which favor denial. To the contrary, Citadel Securities is not controlled by any foreign entity, and economic interests favor institution. Patent owner HFT Solutions does not practice the challenged (or any) high-frequency trading patent. Rather, HFT seeks to stifle innovation in financial services by asserting patents that purport to claim known and regularly used hardware and techniques for high-frequency trading, which will disrupt well-established practices of Citadel Securities and other market participants in this space. Nor is Citadel Securities a serial petitioner—this is the first petition Citadel Securities has ever filed.

Finally, as demonstrated below, the merits of this petition are strong. The challenged claims are nothing more than verbose, obfuscated recitations of known techniques for clock synchronization using FPGAs and external PLLs. And this petition’s reliance on expert testimony is limited to a single expert declaration of approximately 125 pages.

## **V. SUMMARY OF THE PRIOR ART**

The claims of the ’381 patent take two well-known components (an FPGA and a PLL) and put them together in not only the exact the way they are designed to be combined, but as they have in fact been combined in prior art. By the time the ’381 patent was filed, numerous FPGAs were commercially available. Ex. 1001 at 9:32-37; *see also* Ex. 1002 at ¶¶ 34-40. FPGAs are useful “in applications that

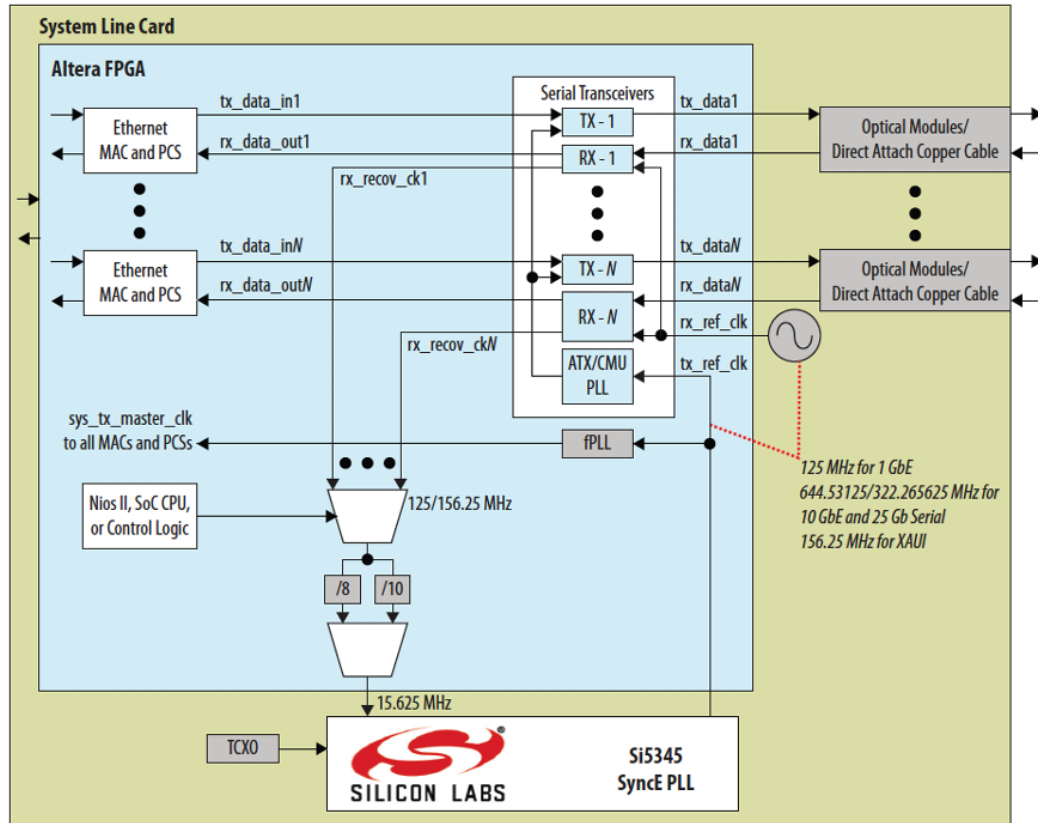
require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism,” including “in the financial industry in high frequency trading.” Ex. 1001 at 1:39-44. Likewise, numerous PLLs, a component used to synchronize clock signals, were also available at the time the patent was filed. Ex. 1002 at ¶¶ 47-54.

#### **A. Altera**

In November 2015, Altera Corporation published a white paper describing “a multiple-port 1G/10 Gbps Ethernet SyncE [Synchronous Ethernet] synchronization solution jointly developed by Altera and Silicon Labs, with a complete stable clock loop.” Ex. 1004 at 1. As the Altera white paper states, “[t]he solution consists of an Altera® SyncE reference design implementing up to ten 1G/10 Gbps Ethernet (1G/10GbE) ports in Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system. This solution can be used in wireless or wireline networking equipment to realize an accurate SyncE clock synchronization.” *Id.* at 2. More simply, the Altera solution consisted of an off-the-shelf FPGA combined with an off-the-shelf external PLL for high-performance clock synchronization for use with Ethernet networking. The Altera system—using a Stratix FPGA and Si5345 PLL—is shown in Figure 1. Altera also

describes test results using the Stratix FPGA and Si5345 system. *Id.* at 5-7; *see also* Ex. 1002 at ¶¶ 82-91.

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



Altera’s white paper is dated November 2015, and it was intended for dissemination to prospective customers and available for download from Altera’s website long before November 2018. *See* Ex. 1004 at 1 (advising “Altera customers . . . to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services”); Ex. 1009 at 4-5 (showing that the Altera White Paper was available online no later than October 18, 2016). Altera is therefore prior art under § 102(a)(1) (AIA) as a printed

publication available before the effective filing date of the '381 patent (November 5, 2018). *See Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1067 (Fed. Cir. 2024) (operating manuals were printed publications because they “were created for dissemination to the interested public to provide instructions about how to assemble, use, clean, and maintain Weber’s slicer, as well as guidance for addressing malfunctions that users might encounter”).

## **B. Stratix Handbook**

The Stratix FPGA used in the Altera white paper is an off-the-shelf product sold by Altera (now an Intel company) before the effective filing date of the '381 patent. Numerous printed publications describe the FPGA’s operation in detail. The Stratix Handbook—a lengthy reference manual published by Altera—is one such printed publication. Ex. 1005.

As relevant for the challenged claims, Volume 2 of the Stratix Handbook is intended to give “a complete understanding of Stratix<sup>®</sup> V transceivers,” which transmit and receive data and therefore make up a crucial component of an FPGA. *Id.* at 6. The Handbook begins by explaining the transceivers’ operation at a high level: “Stratix V transceivers are divided into two blocks: physical medium attachment (PMA) and physical coding sublayer (PCS). The PMA block connects the FPGA to the channel, generates the required clocks, and converts the data from parallel to serial or serial to parallel. The PCS block performs digital processing logic

between the PMA and the FPGA core.” *Id.* The Stratix Handbook has numerous accompanying block diagrams to further explain the operation of the receiver (RX) and transmitter (TX) portions of the transceivers. *See, e.g., id.* at 14 (showing RX PMA and TX PMA in more detail); *see also* Ex. 1002 at ¶¶ 92-108.

### PMA Architecture

The PMA receives and transmits off-chip high-speed serial data streams.

Figure 1-7: Receiver PMA Block Diagram

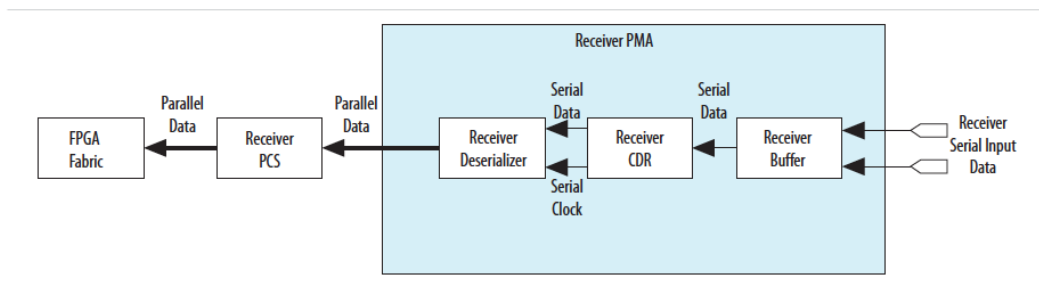
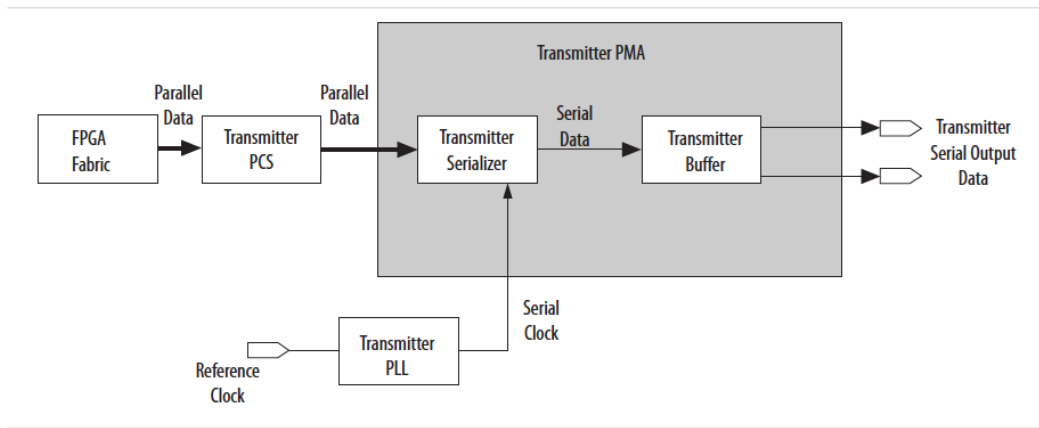


Figure 1-8: Transmitter PMA Block Diagram



The Stratix Handbook, dated January 23, 2015, was (and is) intended for dissemination to prospective customers and current users of the Stratix FPGA and was also available for download from Altera’s website long before November 2018. *See* Ex. 1005 at 6 (encouraging “Altera customers . . . to obtain the latest version of device specifications before relying on any published information” in the

Handbook); Ex. 1010 at 4-5 (showing that the Stratix Handbook was available online no later than January 9, 2017). The Stratix Handbook is prior art under § 102(a)(1) (AIA) as a printed publication available before the effective filing date of the '381 patent (November 5, 2018). *See Weber*, 92 F.4th at 1067 (operating manuals were printed publications).

The '381 patent concedes that the Stratix FPGA is prior art. Ex. 1001 at 9:32-35 (“Examples of currently available FPGAs include . . . the Stratix® V”). Although the examiner considered one page of the Stratix Device Handbook during prosecution, *id.* at 2, the Altera white paper that directs a skilled artisan to combine the Stratix FPGA with an external PLL was not art of record and therefore was not considered.

### **C. Si5345 Manual**

The Si5345 PLL used in the Altera white paper is an off-the-shelf product sold by Silicon Labs (now Skyworks) before the effective filing date of the '381 patent. Like the Stratix FPGA, numerous printed publications describe in detail the operation of Silicon Labs PLLs. The Si5345 Manual is a Family Reference Manual that describes three “Any-frequency, Any-output Jitter-Attenuator/Clock Multipliers” made by Silicon Labs—specifically, the Si5345, Si5344, and Si5342. Ex. 1006 at 1. “This Family Reference Manual is intended to provide system, PCB

design, signal integrity, and software engineers the necessary technical information to successfully use the Si5345/44/42 devices in end applications.” *Id.* at 9.

As the Si5345 Manual describes, “[t]he Si5345/44/42 jitter attenuating clock multipliers combine 4th generation DSPLL and MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance.” *Id.* Simply put, the PLLs are designed to clean and distribute clocks in systems that require extremely low levels of jitter (i.e., variations of the timing of a clock signal) and are capable of generating any combination of output frequency from any input frequency within specified ranges. *Id.*

The three PLLs significantly overlap in their function, structure, and capability, with the differences primarily being in the numbers of MultiSynths and available outputs. *See id.* at 9. Figure 1 provides a block diagram for all three PLLs.

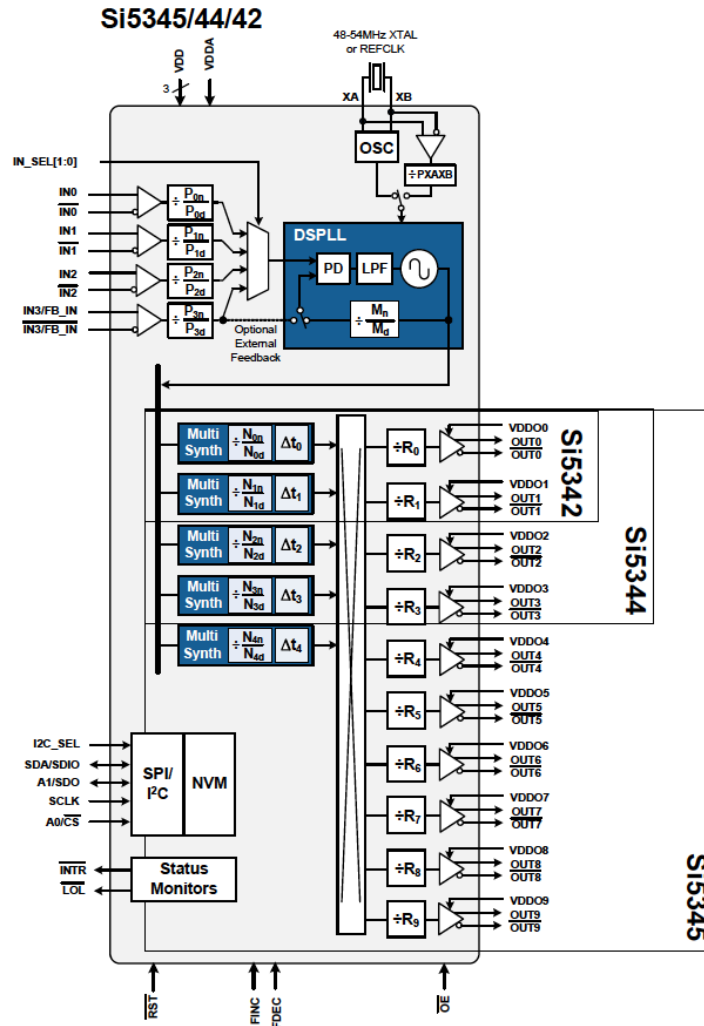
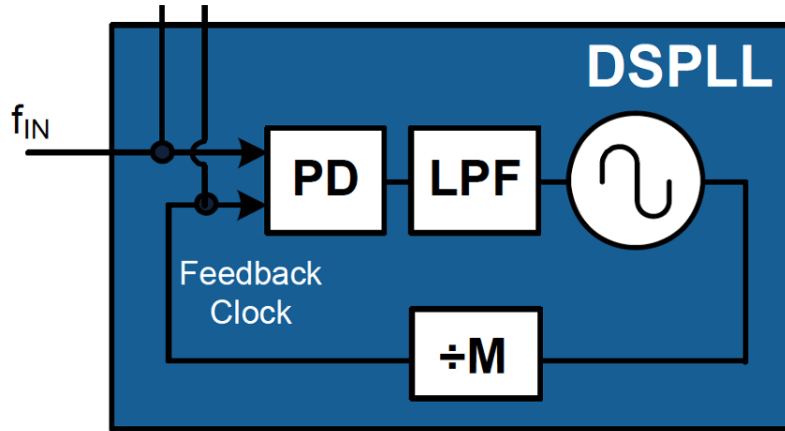


Figure 1. Block Diagram Si5345/44/42

Each PLL described in the Manual has a digital phase-locked loop (DSPLL, shown in blue box below) that includes a phase detector, a low pass filter, and voltage-controlled oscillator. *See, e.g., Ex. 1006 at 27.* The DSPLL uses those components in an iterative process to synchronize an input clock to a reference clock. *See id.* at 17 (describing “Acquisition Mode”); *see also Ex. 1002 at ¶¶ 109-112.*



Si5345/44/42 Figure 13 Excerpt

The Si5345 Manual—dated August 2015—was created and published by Silicon Labs for dissemination to prospective and current customers. *See* Ex. 1006 at 1 (“Rev. 1.0 8/15” and “Copyright © 2015”), 9 (“This Family Reference Manual is intended to provide . . . engineers the necessary technical information to successfully use the Si5345/44/42 devices in end applications.”), 183 (“Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation” and providing contact information). The Manual also directs readers to Silicon Labs’ website, where Silicon Labs made its data sheets and other information available for download. *Id.* at 183; Ex. 1011 at 4-5 (showing that Si5345/44/22 documentation was available online no later than November 22, 2015). Accordingly, the Si5345 Manual is prior art under § 102(a)(1) (AIA) as a printed publication available long before the effective filing date of the ’381 patent

(November 5, 2018). *See Weber*, 92 F.4th at 1067 (Fed. Cir. 2024) (operating manuals were printed publications).

**D. “A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT)” by John W. Lockwood**

As the ’381 patent acknowledges, by 2018, it was common knowledge that FPGAs were being “used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired.” Ex. 1001 at 1:42-44. Even as early as 2012, financial systems were implemented on FPGA-based systems. For example, John W. Lockwood’s 2012 paper describes the advantages of FPGA-based systems to reduce latency for high-frequency trading. Ex. 1007.

In his paper, Lockwood explained “why latency matters” in electronic trading, which was “growing rapidly” at the time of the 2012 publication. Ex. 1007 at 2. Lockwood further explained that high frequency “traders attempt to exploit fleeting inefficiencies in the market. . . . However, due to the increase in number of players in the HFT space which try to exploit these opportunities, the first few players to execute orders may be the only ones able to profit from a given opportunity.” *Id.* “The longer the time between a trader making a decision to trade and the order reaching the execution venue, the greater is the possibility and magnitude of slippage which translates into cost for traders.” *Id.* Lockwood also noted that some trading strategies “depend upon the ability to access market data and execute orders faster than other investors. Profiting from this activity requires traders to be able to react

in real time to market events using both low-latency and low-jitter market access.”

*Id.* Every “reduction in latency can improve arbitrage profitability.” *Id.*

Lockwood provided examples of how such systems could be implemented, including using an FPGA-based system to act “as the bridge between the host computer and the network,” which “allows user-designed custom processing logic to be integrated directly into the data path.” *Id.* at 3. Specifically, market data from an exchange enters the FPGA system, where it is processed in the FPGA to result in orders back to the market. The system is shown in Figure 2 of Lockwood:

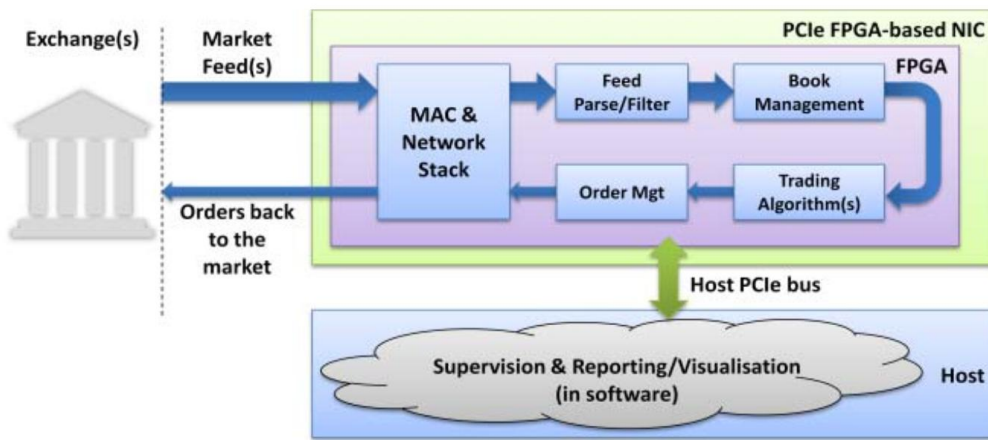


Figure 2 Typical Smart NIC in a supervised financial trading application

Lockwood further explained that “some financial processing systems are completely implemented on FPGA-based platforms without any host CPU,” which “yield[s] best possible latencies.” In this implementation, the data “no longer needs to make a round trip” through system’s interface for processing in the CPU, so “the

inherent latency and jitter introduced by the host’s operating system are entirely avoided.” Ex. 1007 at 3. Such as system is shown in the bottom portion of Figure 3.

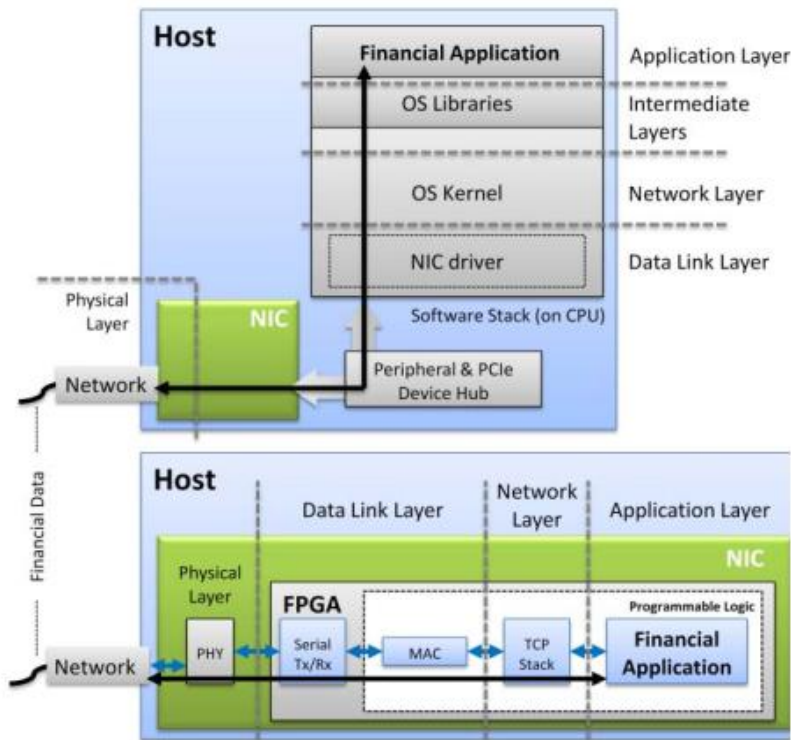


Figure 3 Software-based (top) and FPGA-based (bottom) trading platforms

Lockwood described numerous advantages to using FPGAs for high-frequency trading. For example, “[m]odern FPGAs can implement most aspects of any HFT trading application,” such that “[i]ncoming market data can typically be processed completely on the FPGA without needing to travel over and back to a host CPU.” *Id.* Additionally, “in the FPGA implementation, the incoming network data is fed directly into a custom-designed, highly-optimized and application-specific processing pipeline via hardware PHY [Physical] and MAC [Media Access Control]

blocks.” *Id.* at 4 (referring to the “Serial Tx/Rx” and “MAC” blocks in Figure 3). “Along with lower latency and minimal jitter, FPGAs can achieve significantly higher throughput using parallelism,” due to the FPGA’s ability to perform many operations simultaneously. *Id.* And “FPGAs offer the[se] performances benefits of custom hardware while retaining programmability” so that “[t]rading algorithms” implemented on the FPGAs “can be continually improved.” *Id.*; *see also* Ex. 1002 at ¶¶ 113-116.

Lockwood is prior art under § 102(a)(1) (AIA) as a printed publication available before the effective filing date of the ’381 patent. Lockwood was published in September 2012 and is available for download at <https://doi.org/10.1109/HOTI.2012.15>.

## **VI. THE ’381 PATENT**

### **A. Effective Filing Date**

The ’381 patent issued on February 7, 2023, from an application filed on April 18, 2022. The ’381 patent is a continuation of four previous applications. The ’381 patent also claims priority to two provisional applications, the earliest of which was filed on November 5, 2018. For the purposes of this IPR, Petitioner treats November 5, 2018 as the earliest effective filing date.

### **B. Specification**

The purported invention of the ’381 patent is a field programmable gate array with an external phase-locked loop. Ex. 1001 at 1. But both FPGAs and PLLs were

developed well before November 2018. The '381 patent acknowledges that it was known that “FPGAs[] may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism.” Ex. 1001 at 1:39-42. Indeed, the '381 patent concedes that, at the time of the invention, FPGAs were already being “used in the financial industry in high frequency trading,” *id.* at 1:42-44, and discloses that numerous FPGAs were commercially available, including “XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® [sic] Ultrascale, the Vitrex® [sic] Ultrascale Plus, the Stratix® V, the Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few,” *id.* at 9:32-37.

The '381 patent contends that it solves “a technical problem [] presented in FPGAs in that phase synchronization between the receiver side clock and the transmitter side clock will introduce unwanted latency that result in delay of processing.” Ex. 1001 at 1:53-56. According to the patent, “[t]he prior art sought to address this problem by including a clock domain crossing circuit in the FPGA.” *Id.* at 1:47-49. Rather than use a clock-domain crossing circuit, the '381 patent addresses that concern with “a field programmable gate array and an external phase controller providing phase matching between a receiver clock and a transmitter clock used in the field programmable gate array.” *Id.* at 2:6-10. But as detailed below, there

is nothing novel or nonobvious about using an external PLL to provide phase matching for an FPGA.

### **C. Challenged Claims**

The '381 patent contains twelve claims, eleven of which are challenged in this IPR.<sup>1</sup> Independent claim 1 claims a “method for processing a first serial data stream . . . to generate a second serial data stream” using an FPGA and an external PLL. Claims 2-14 are dependent claims.

The challenged claims of the '381 patent are unnecessarily long, but their length belies their simplicity. At a high level, the '381 patent claims methods for using a field programmable gate array (FPGA) that receives serial data, converts it to parallel data, syncs the internal clock to the received data, performs certain calculations, and then converts the stream back to serial before transmission of data off the FPGA.

The one independent method claim incorporates numerous subparts, which consist of several structural limitations (deserializer, computational circuitry, phase lock loop) and data stream and clock signal limitations.

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<sup>1</sup> Citadel does not challenge claim 5 here, as it is indefinite.

#### **D. Prosecution History**

The '381 patent underwent expedited examination through the Track One program. Ex. 1003 at 194. The only rejections during prosecution were based on double patenting in light of eight other patents and applications. *Id.* at 137-139, 165-169. The applicant overcame those rejections through terminal disclaimers. *Id.* at 128-129, 146-148. In the Notice of Allowance, the examiner's reasoning for allowance focused on the claim limitations that require a PLL external to the FPGA. *Id.* at 115-116.

On October 18, 2023, the patentee filed a request for certificate of correction. *Id.* at 2-3. That certificate was entered on November 14, 2023, correcting claim limitation 1(a). Ex. 1003 at 1.

#### **E. Level of Ordinary Skill**

At the time of the claimed invention, a POSA would have a bachelor's degree in electrical or computer engineering and 3-5 years of academic or industry experience working with clocking techniques for FPGAs with high-speed transceivers. Ex. 1002 at ¶ 32. This person could also be someone with a lower degree of education but with greater practical experience. It could also be someone with a higher degree of education and lower practical experience.

## F. HFT's Theory of Infringing the '381 Patent

Patent Owner's infringement theory in the district court bears directly on why the Petitioner's cited prior art discloses each limitation in the challenged claims. Ex. 1012.

First, Patent Owner accuses systems that include a Xilinx Ultrascale+ FPGA, which is an off-the-shelf FPGA sold by a third party. That is the same type of product as the Altera FPGA that Petitioner cites as the primary reference.

Second, Patent Owner accuses systems that include an external Si5346 Phase-Locked Loop (PLL). As discussed *infra*, a PLL synchronizes clock signals for use with an FPGA. The accused Si5346 PLL is an off-the-shelf PLL that is closely related to the Si5345 PLL used in this petition. In relevant respects, the Si5346 shares architecture and componentry with the Si5345 PLL, the prior-art reference Petitioner cites with respect to claim 1(g) and claim 8. *See, e.g.*, Ex. 1012 at 8 (citing UltraScale+), 17 (citing Si5346).

Petitioner recognizes that Patent Owner's infringement theories do not resolve the question of patentability or claim construction for an inter partes review. But the constructions implicit in the Patent Owner's infringement allegations ought to be considered when evaluating the elements of the prior art that disclose the recited limitations, and Petitioner adopts those implicit constructions here. *Cf. W. Digital Corp. v. Spex Techs., Inc.*, No. IPR2018-00084, 2018 WL 1990268, at \*5 (PTAB

Apr. 25, 2018) (“Petitioner’s statement that its Petition ‘is based on the claim constructions urged by Patent Owner’ in related District Court litigation . . . suffices to identify claim constructions Petitioner is adopting for purposes of the requested review in compliance with § 104(b)(3).”). Where appropriate, Petitioner indicates where the Patent Owner’s implied constructions relate to the disclosures in the prior art.

## **VII. CLAIM CONSTRUCTION**

Without conceding that the ’381 patent’s claims are supported under 35 U.S.C. § 112, for the purposes of this IPR, Petitioner interprets the claims “in accordance with the ordinary and customary meaning . . . as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b).

Where the challenged claims refer to a “deserializer,” Petitioner adopts the specification’s description that the deserializer may include a receiver PMA and receiver PCS. Ex. 1002 at ¶¶ 75-80; Ex. 1001 at Figs. 3A-E, 16:14-17:56.

## **VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE**

When the ’381 patent was filed, there was nothing new about combining an FPGA with an external PLL, and the methods claimed in the ’381 patent require nothing more than standard steps for processing data and clock signals using an

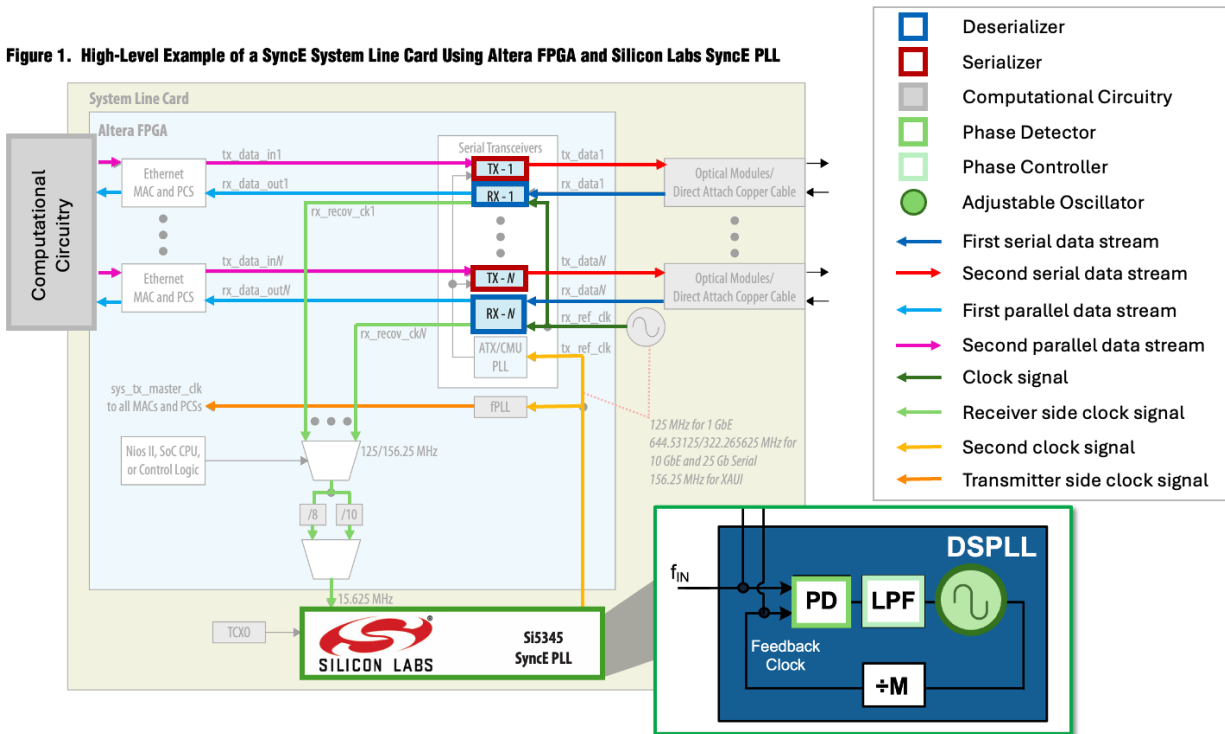
FPGA and external PLL. As described in detail below, the challenged claims are unpatentable.

**A. Ground 1A: Altera Anticipates Claims 1, 4, and 6-10**

Altera—a white paper published by a leading FPGA manufacturer—instructs using a Stratix FPGA in conjunction with an external Si5345 PLL for clock synchronization. Altera therefore anticipates claims 1, 4 and 6-10.

Figure 1 of Altera depicts nearly every limitation of the challenged claims.

Figure 1 is annotated below to indicate where key claim limitations are shown.



**1. A Skilled Artisan Would Recognize that the Features of the Stratix FPGA and Si5345 PLL Are Necessarily Present in Altera**

Altera is a white paper that describes the operation of “a high-performance SyncE solution based on . . . Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL).” Altera provides both a “SyncE reference design” and a test setup for “interoperability” between the Stratix FPGA and Si5345 PLL. Ex. 1004 at 3, 5. A POSA reading Altera would understand that the features of the Stratix FPGA and Si5345 PLL are necessarily present in the solution described in Altera. Ex. 1002 at ¶ 117. The white paper assumes that the reader can and will locate any information about the operation of the FPGA and PLL separately and so does not describe in depth every aspect of their operation. Ex. 1002 at ¶ 118.

In this situation, it is proper to turn to extrinsic evidence that describes the operation of each of the referenced components in detail to understand their inherent features.

“[R]ecourse to extrinsic evidence is proper to determine whether a feature, while not explicitly discussed, is necessarily present in a reference. The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the relevant art.” *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) (internal citations

omitted); *see also In re Haines*, No. 2024-2338, 2025 WL 1403578, at \*2 (Fed. Cir. May 15, 2025) (examiner properly used another publication “as evidence to explain why [the prior art’s] disclosure of a mass spectrometer implicitly discloses ‘obtaining mass spectral channel signals (m/z)’” (cleaned up)); *Sage Prods., LLC v. Stewart*, 133 F.4th 1376, 1385 (Fed. Cir. 2025) (“There was likewise nothing improper in the Board relying on evidence outside of the PAR to make findings as to what the skilled artisan would understand the PAR to be disclosing.”); *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) (“It is well established that such reliance on extrinsic evidence is proper in an inherency analysis.”).

Here, the Altera FPGA and Si5345 are explicitly referenced, and a POSA would be intimately familiar with the fact that if they wanted to learn more about either, they would easily be able to find and rely on extensive information about those devices available from Altera and Silicon Labs. Ex. 1002 at ¶ 118. In fact, the Altera white paper encourages customers “to obtain the latest version of device specifications before relying on any published information.” Ex. 1004 at 1. Altera and Silicon Labs made specifications and data sheets available for download from their respective websites, including the Stratix Handbook and Si5345 Manual used here. Ex. 1002 at ¶ 118; Ex. 1010; Ex. 1011. The ’381 patent even provides a URL for the Stratix Handbook. Ex. 1001 at 2.

Accordingly, the Stratix Handbook and Si5345 Manual demonstrate features that a skilled artisan would understand are necessarily present in the FPGA and PLL used in the Altera white paper, and it is proper to use them to explain why the Altera white paper is anticipatory.

## **2. Limitation-by-Limitation Analysis**

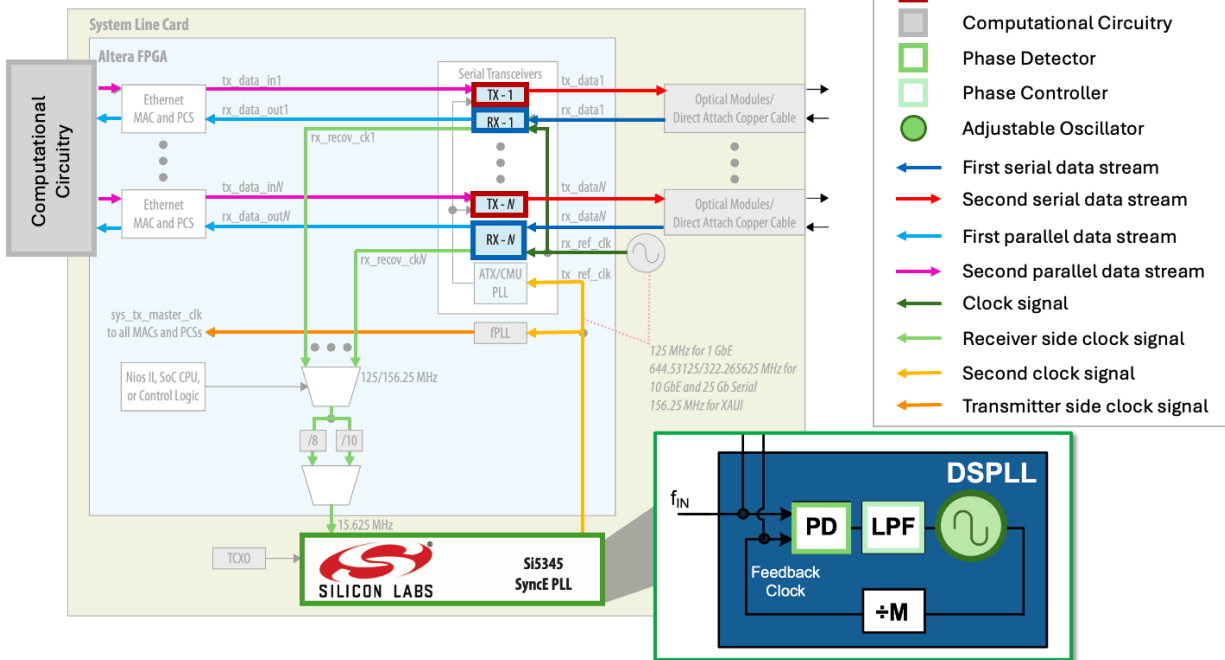
The analysis below specifies “where each element of the claim is found in” Altera. *See* 37 C.F.R. § 42.104(b)(4).

### **Claim 1 preamble**

To the extent the preamble is limiting, Altera discloses “[a] method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream.” Ex. 1002 at ¶¶ 120-122.

Altera is a system using “Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system.” Ex. 1004 at 2. In Altera, first serial data streams (rx\_data1-rx\_dataN) are received by the system and second serial data streams (tx\_data1-tx\_dataN) are transmitted from the system. The Altera system is designed for wireless or wireline networking, *id.*, indicating that the received data is processed for those networking applications. Ex. 1002 at ¶ 121. Altera Figure 1, shown below, is annotated throughout this petition.

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**

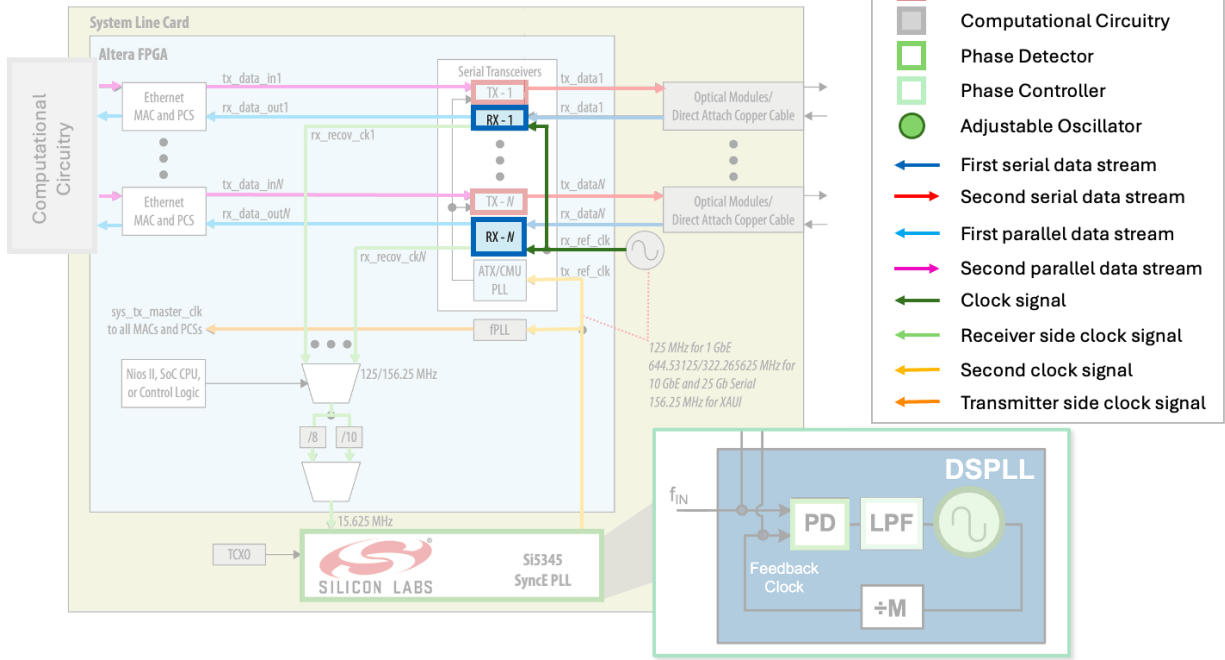


**Claim 1(a)**

Altera discloses “receiving, by a deserializer in a field programmable gate array, a clock signal.” Ex. 1002 at ¶¶ 123-126.

With respect to the clock signal, Altera discloses a receiver reference clock signal, “rx\_ref\_clk,” that is received by receiver blocks (RX-1 through RX-N) of the serial transceivers. Ex. 1004 at 2; Ex. 1002 at ¶ 124.

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



The deserializer in Claim 1(a) is represented by the receiver blocks (RX-1 through RX-N) and the receiver portion of the Ethernet MAC and PCS blocks shown in Altera. Ex. 1002 at ¶ 125. The '381 patent demonstrates that the claimed deserializer can include a receiver PMA and receiver PCS, as shown in Figure 3E below. *See, e.g.*, Ex. 1001 at 17:34-37 (“the deserializer 2104” may include a receiver PMA 3512 and receiver PCS 3508. The receiver PMA 3512 may include receiver buffer 3504, CDR 3516, and serial to parallel box 3118’.”), Fig. 3E. Like the '381 patent, each receiver of Altera includes a receiver PMA and a receiver PCS. Ex. 1005 at 14.

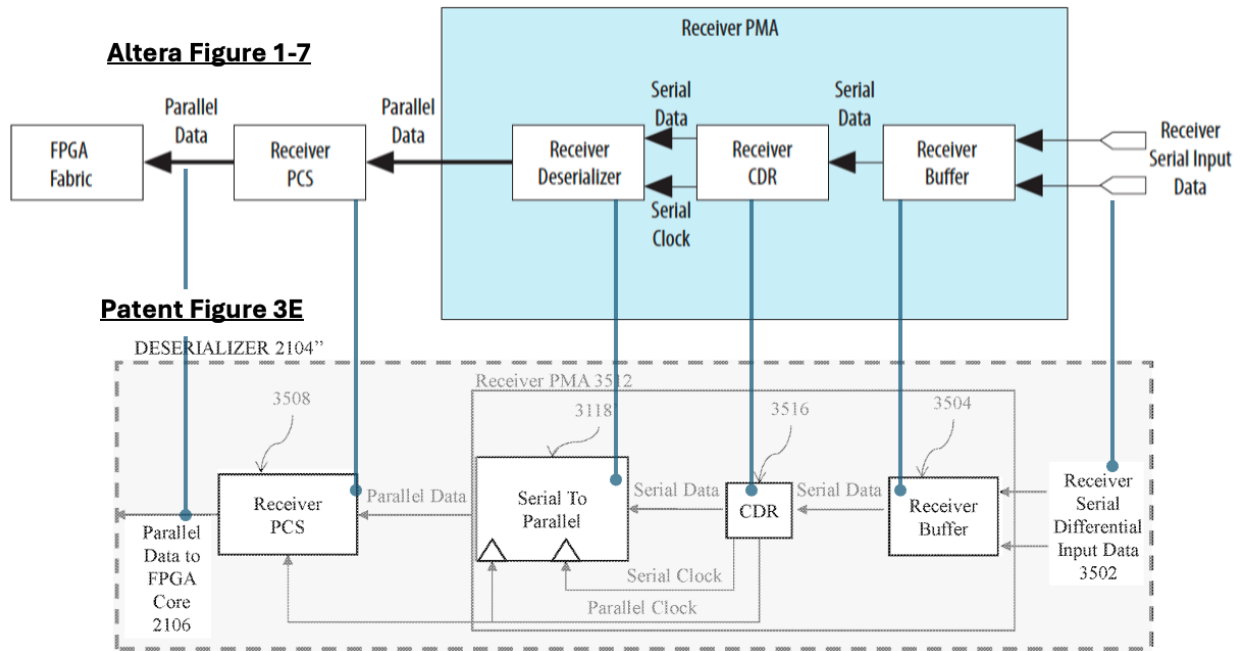
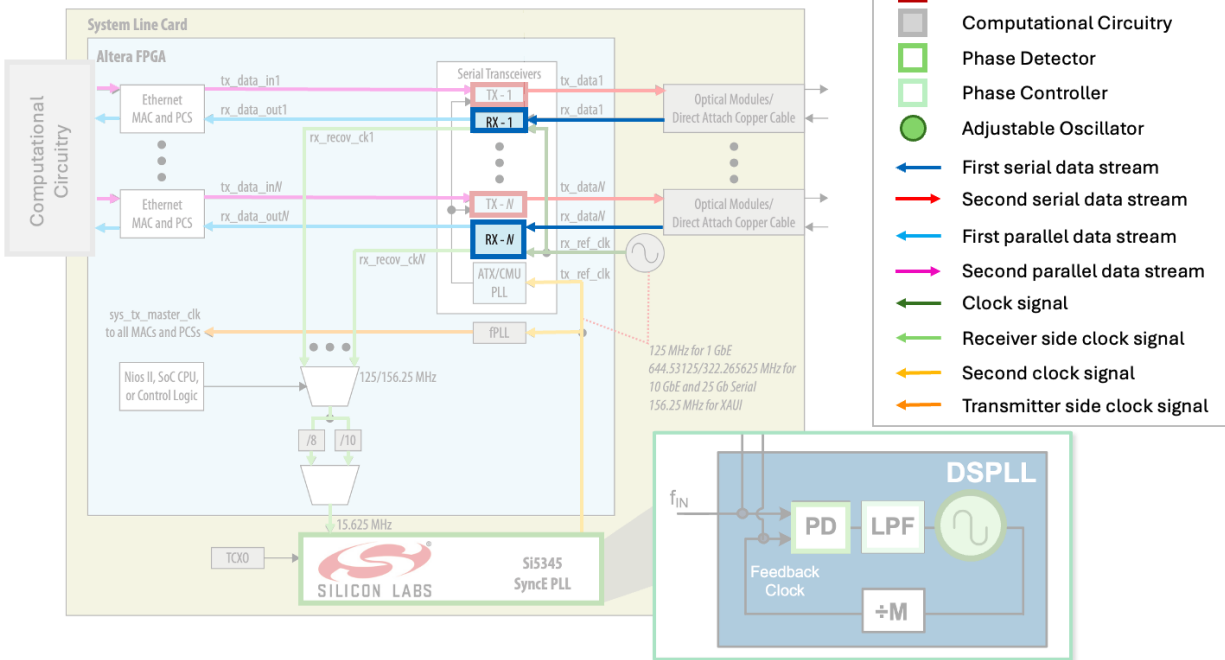


FIG. 3E

**Claim 1(b)**

Altera discloses “receiving, by the deserializer, the first serial data stream.” Ex. 1002 at ¶¶ 127-129. Altera discloses that the receivers (RX-1 through RX-N) of serial transceivers receive serial data (rx\_data1-rx\_dataN) from Optical Modules/Direct Attach Copper Cables. Ex. 1004 at 2. The “serial” nomenclature indicates that the serial transceiver receives serial data. Ex. 1002 at ¶ 128.

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



In addition, the Stratix Handbook depicts the receivers (the RX blocks shown in Altera) in more detail. Ex. 1002 at ¶ 129. The Stratix Handbook confirms that the receivers receive serial data. *Id.*; Ex. 1005 at 14 (“The PMA receives . . . off-chip high-speed serial data streams.”).

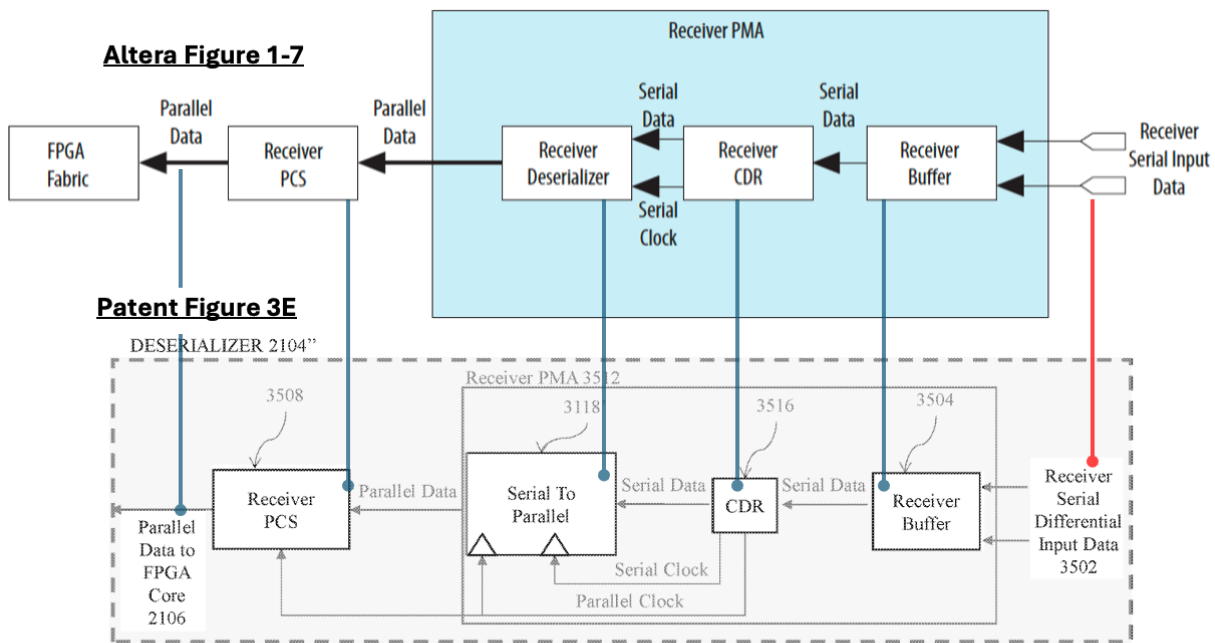
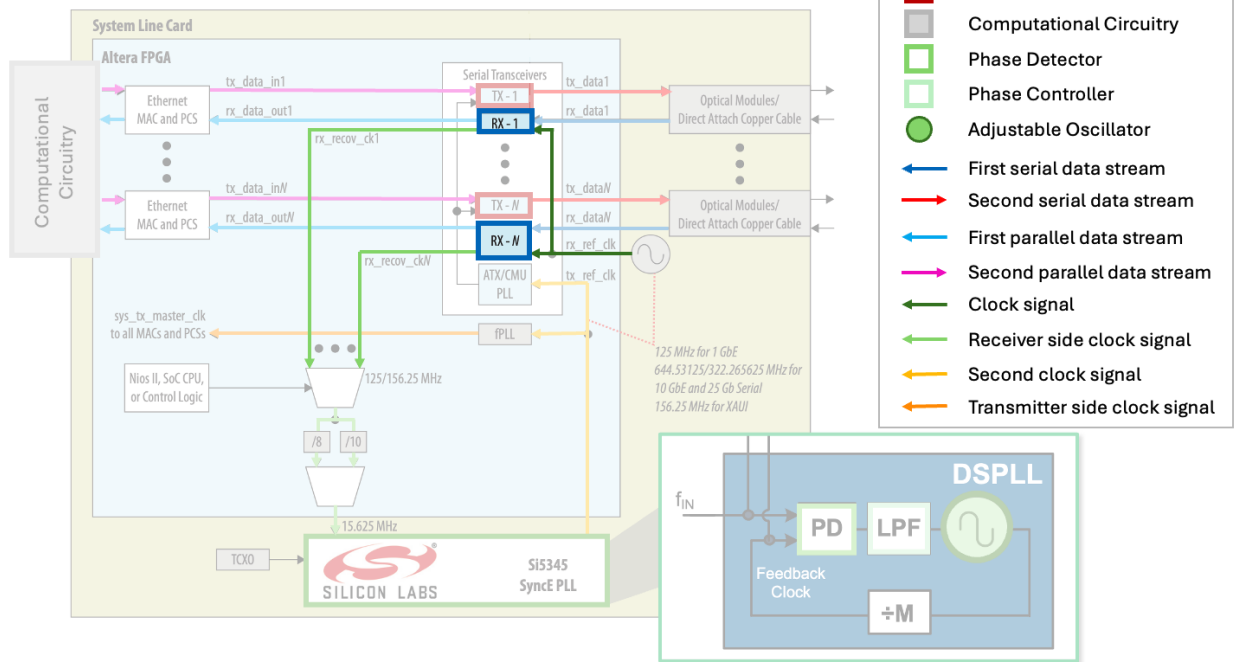


FIG. 3E

**Claim 1(c)**

Altera discloses “generating, by the deserializer, a receiver side clock signal.” Ex. 1002 at ¶¶ 130-133. In Altera, the “PHY IP cores recover the receiver (RX) clocks from their respective 1G/10 Gbps Ethernet ports.” Ex. 1004 at 3. The PHY IP core refers to the serial transceivers—specifically, the PHY IP core is the “physical coding layer (PCS) and physical medium attachment (PMA) (PHY) intellectual property (IP) instances.” *Id.* Accordingly, a POSA would understand that in Altera each receiver (e.g., receiver blocks (RX-1 through RX-N) located in the PMA) recovers the receiver (RX) serial clock and generates the corresponding receiver side clock associated with the parallel received data (the green line below). Ex. 1002 at ¶ 131.

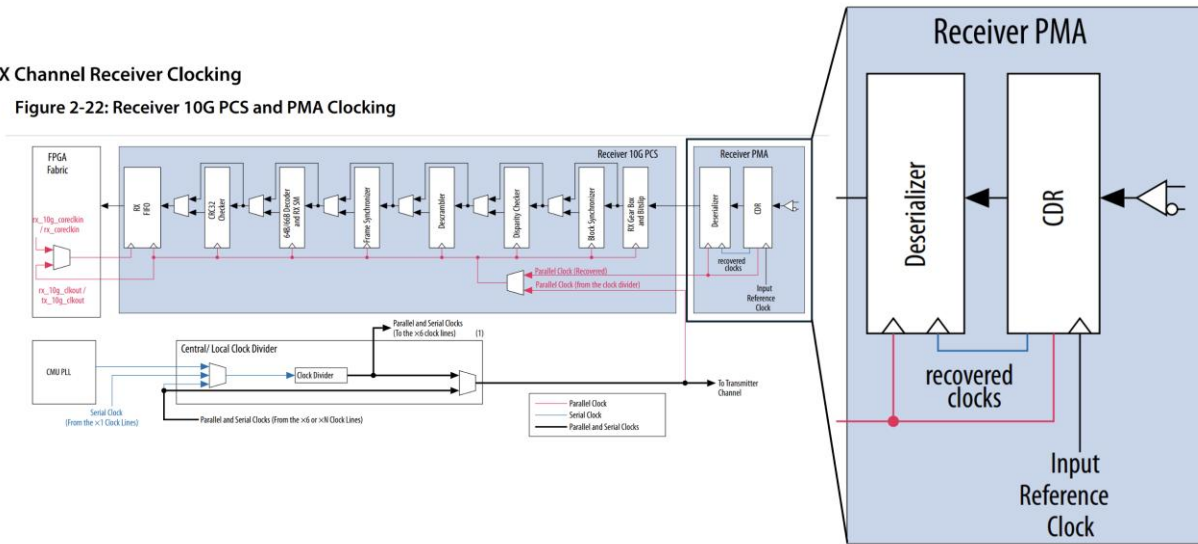
**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



The receiver PMA’s role in recovering the receiver serial clock and generating the corresponding receiver-side parallel clock is confirmed by the Stratix Handbook. *Id.* at ¶ 132; Ex. 1005 at 97 (Figures 2-22 and 2-23); *see also id.* at 6 (“The PMA block . . . generates the required clocks”), 33 (Figure 1-19). Those figures illustrate that the CDR—a clock data recovery circuit—within the Receiver PMA generates two recovered clocks, the parallel receiver side clock (shown in red) and the serial clock (shown in blue). Ex. 1002 at ¶ 132.

## GX Channel Receiver Clocking

Figure 2-22: Receiver 10G PCS and PMA Clocking



A CDR is a common circuit that can be used to generate a clock signal from a data stream. Ex. 1002 at ¶ 133. Like Altera, the '381 patent explains that the claimed deserializer can include a CDR for generating a clock signal. *See, e.g.*, Ex. 1001 at 8:16-18 (“FIG. 3C is an exemplary block diagram of a clock and data recovery (CDR) circuit suitable for use in the deserializer”), 10:56-58 (“The receiver clock domain is typically generated by a clock and data recovery (CDR) circuit from the incoming data stream.”), 16:18-22, 17:34-35 (“the deserializer 2104” may include a receiver PMA 3512 and receiver PCS 3508. The receiver PMA 3512 may include receiver buffer 3504, CDR 3516, and serial to parallel box 3118’.”).

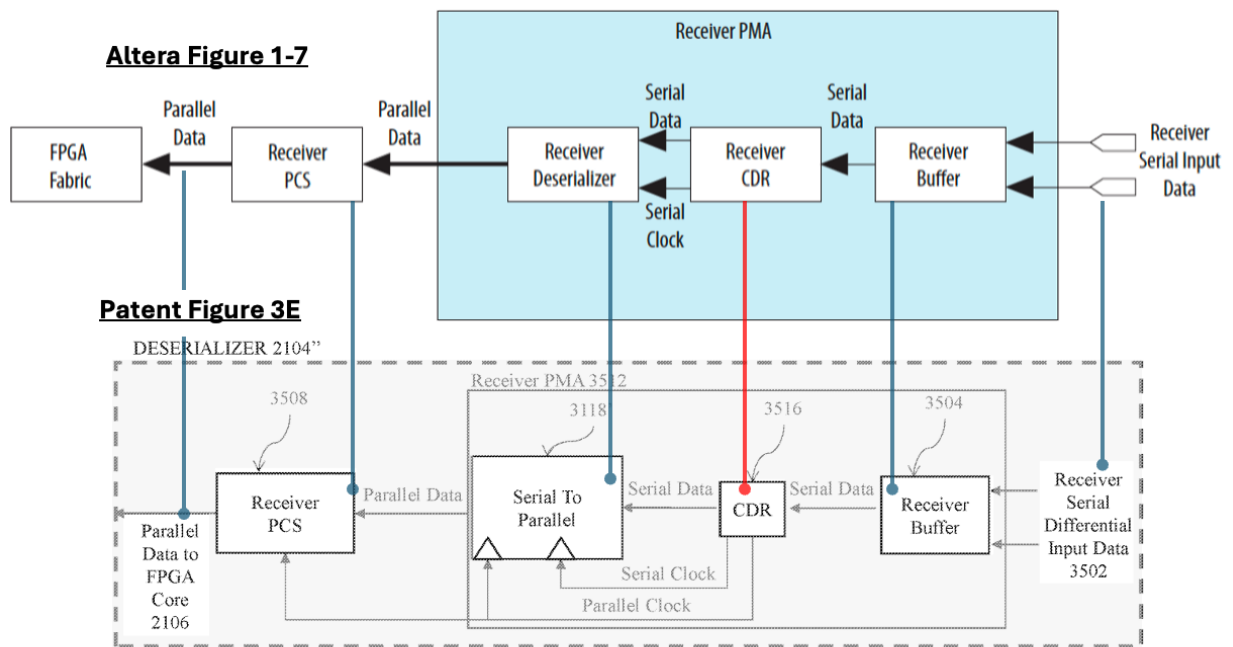
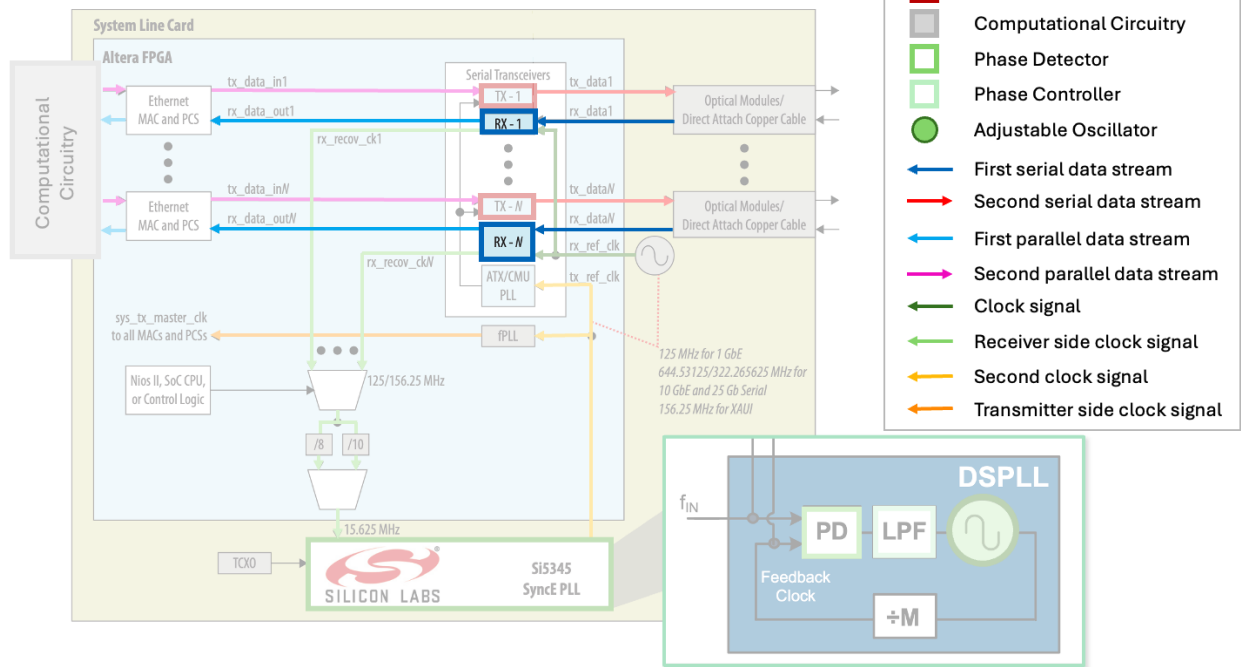


FIG. 3E

**Claim 1(d)**

Altera discloses “converting, by the deserializer, the first serial data stream into a first plurality of parallel data streams.” Ex. 1002 at ¶¶ 134-136. A skilled artisan would understand from Figure 1 of Altera that serial rx\_data is converted into parallel data, labeled rx\_data\_out, in the receiver (RX). Ex. 1002 at ¶ 135. Altera also discloses that there are multiple sets of these parallel data streams, as there are multiple receivers (a total of  $N$  of them), each of which converts a serial data stream to a parallel data stream. *Id.*

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



The Stratix Handbook confirms that the receiver converts serial data to parallel data. Ex. 1002 at ¶ 136. The Stratix Handbook explains that “[t]he PMA block connects the FPGA to the channel, generates the required clocks, and converts the data from parallel to serial or serial to parallel.” Ex. 1005 at 6. Figure 1-7 shows that the “Receiver Deserializer” of the Receiver PMA converts serial data to parallel data. *Id.* at 14; *see also id.* at 20.

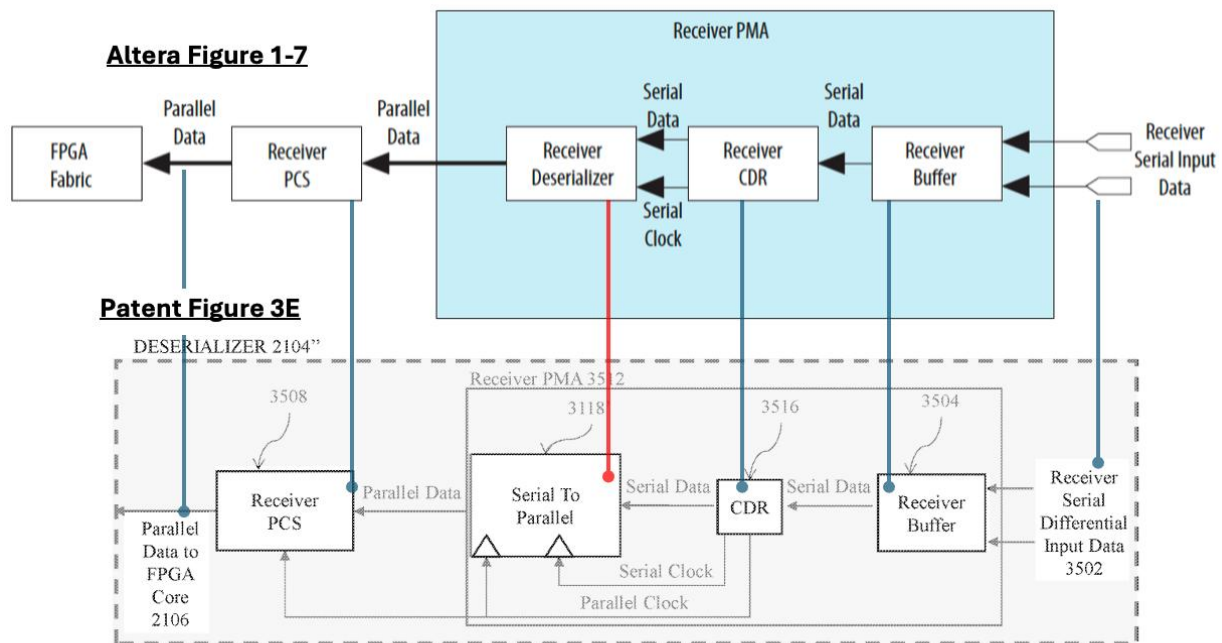
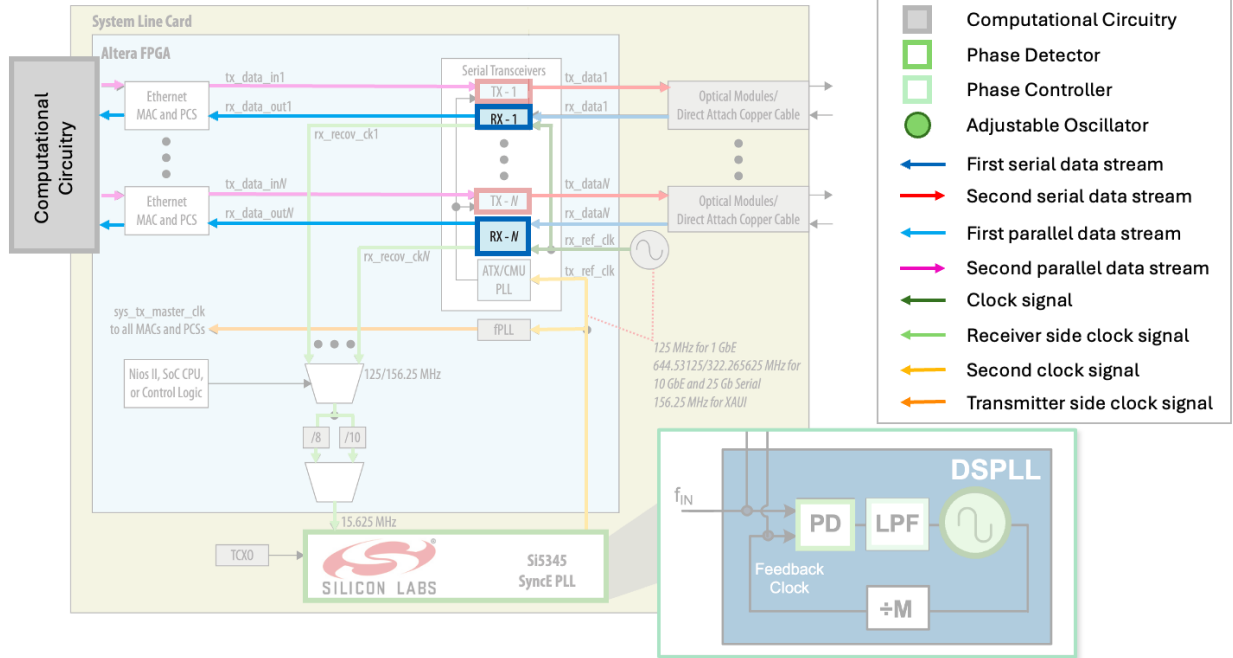


FIG. 3E

**Claim 1(e)**

Altera discloses “transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams.” Ex. 1002 at ¶¶ 137-139. As shown in Figure 1, a POSA would recognize that in Altera, the receivers transmit parallel data streams to computational circuitry within the FPGA. *Id.* at ¶ 138. Although the Altera white paper does not explicitly draw a representation of the computational circuitry, a POSA would understand that the computational circuitry is present in the Altera FPGA as shown in the grey box below (annotated in the diagram for sake of clarity). *Id.*

Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL



The Stratix Handbook confirms this. Ex. 1005 at 14. Figure 1-7 of the Handbook shows that parallel data is transmitted from the Receiver PCS of the receiver to the FPGA fabric. *Id.* A POSA would understand that FPGA fabric shown in Figure 1-7 refers to computational circuitry of the FPGA. Ex. 1002 at ¶ 139.

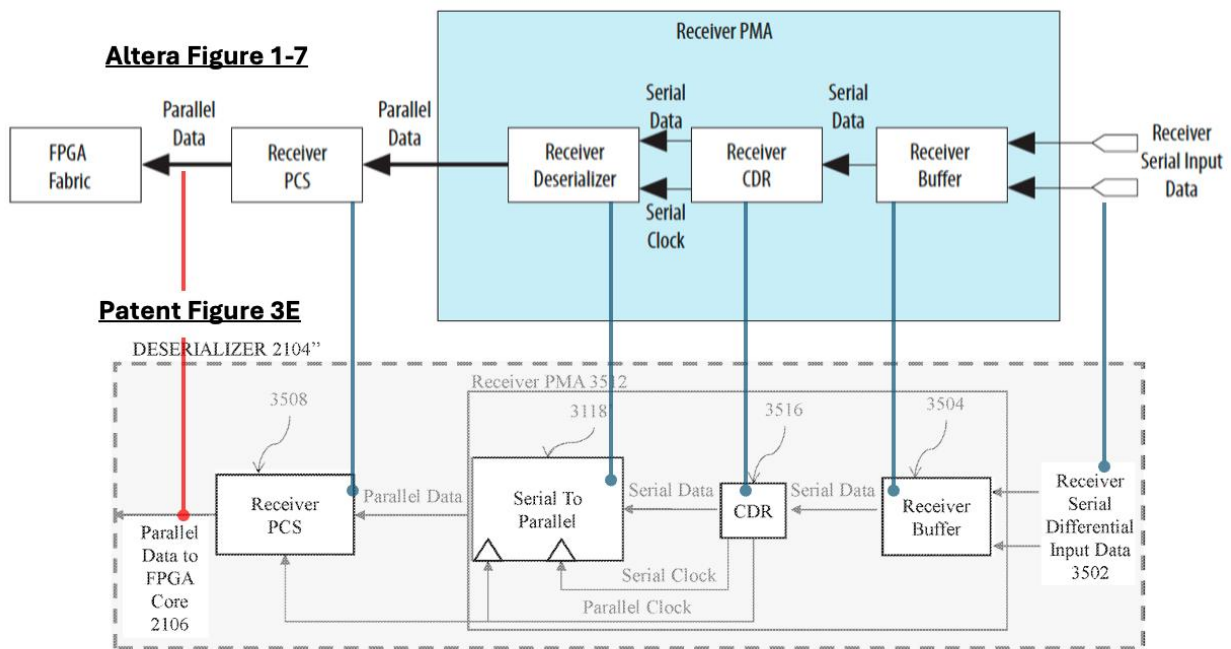
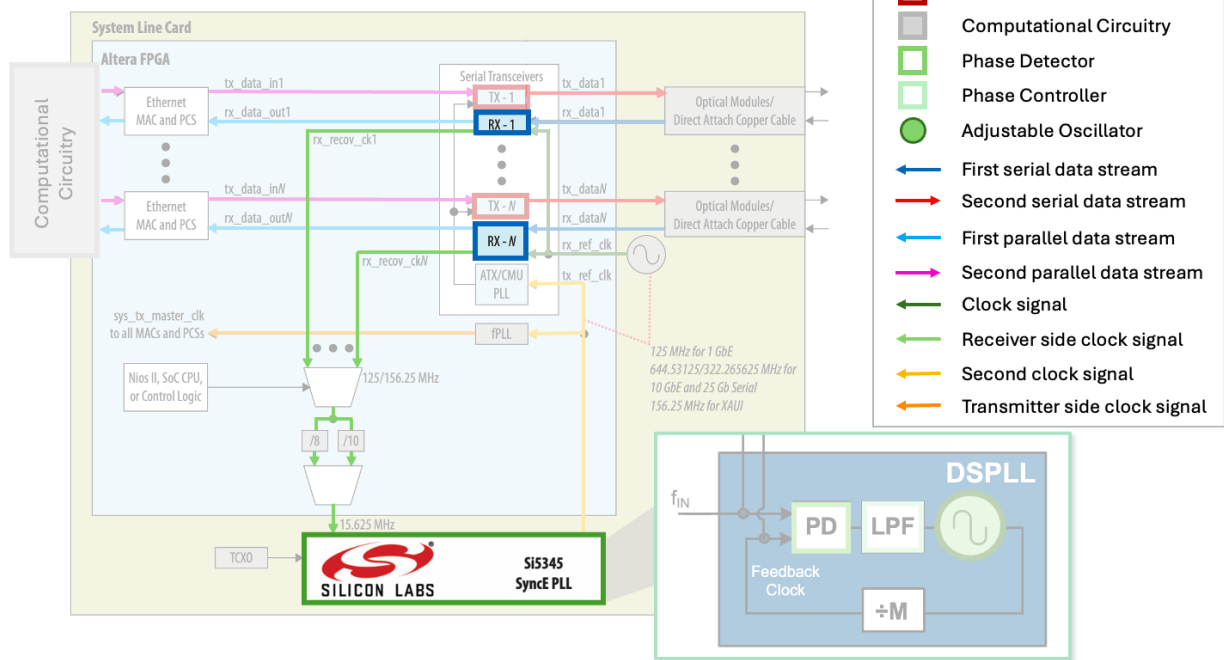


FIG. 3E

**Claim 1(f)**

Altera discloses “transmitting, from the deserializer to a phase lock loop of the field programmable gate array system that is not within the field programmable gate array, the receiver side clock signal.” Ex. 1002 at ¶¶ 140-142. Altera Figure 1 depicts the receiver-side clock signal (e.g., rx\_recov\_ck1) being transmitted from the receiver to the external Si5345 PLL (the light green lines below). *Id.* at ¶ 141. Altera also describes that step: “the RX clocks from multiple Ethernet ports are multiplexed in the FPGA fabric to the external jitter-attenuating PLL.” Ex. 1004 at 4.

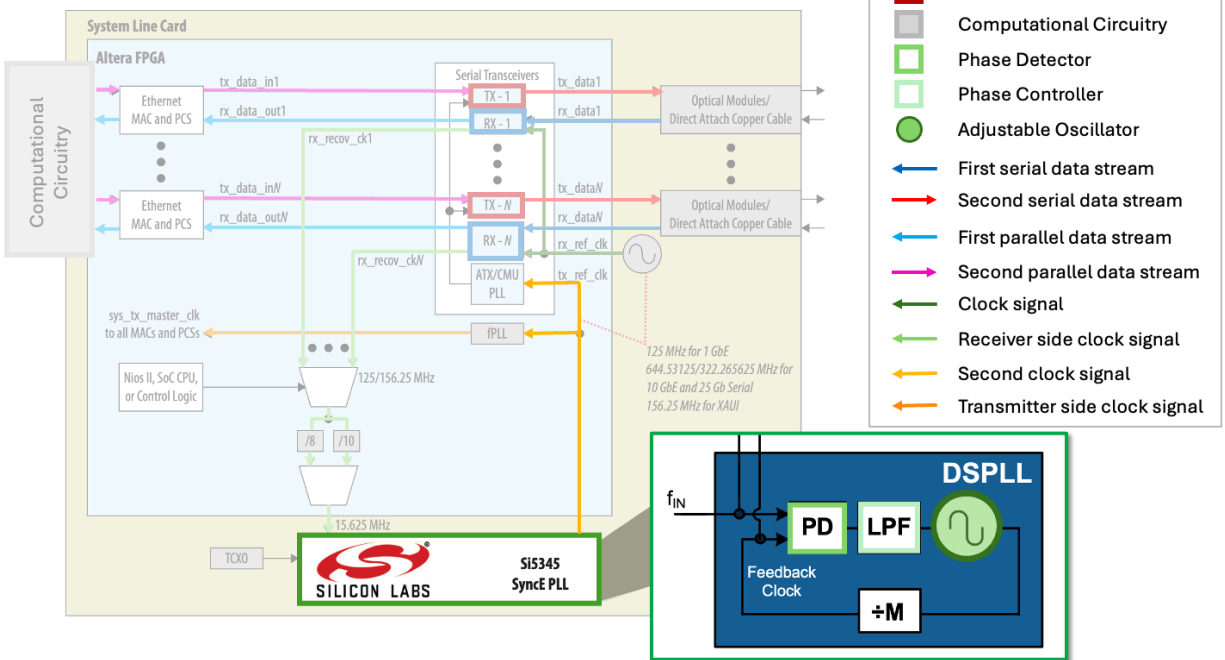
**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



**Claim 1(g)**

Altera discloses “generating, using the phase lock loop, a second clock signal.” Ex. 1002 at ¶¶ 143-144. Altera Figure 1 discloses that the external Si5345 PLL generates a second clock signal, tx\_ref\_clk. *Id.* at ¶ 144. Altera explains this step as: “[t]he Si5345 ITU-T G.8262 SyncE standard-compliant PLL from Silicon Labs then attenuates the selected clock signal’s wander and jitter to within the SyncE specification,” thereby generating a “stabilized clock.” Ex. 1004 at 3.

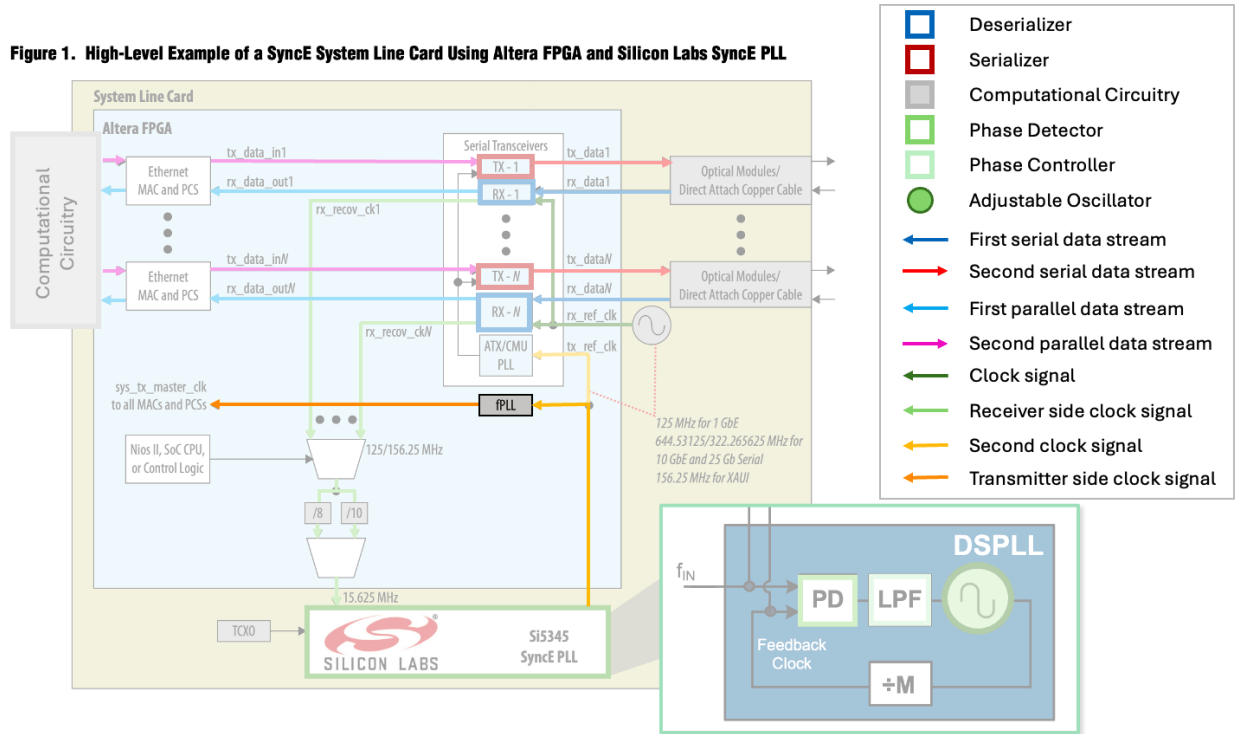
**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



**Claim 1(h)**

Altera discloses “generating, within the field programmable gate array, a transmitter side clock signal derived from the second clock signal.” Ex. 1002 at ¶¶ 145-146. Figure 1 shows that the tx\_ref\_clk clock is transmitted to the fPLL (fractional PLL) within the FPGA, which then generates a transmitter-side clock signal (sys\_tx\_master\_clk) derived from the tx\_ref\_clk (the second clock signal) generated by the external PLL. *Id.* at ¶ 146. Specifically, Altera explains that the “stabilized clock” generated by the Si5345 PLL (i.e., the “second clock signal”) “is used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” Ex. 1004 at 3;

see also *id.* at 4 (Si5345 PLL “suppl[ies] a clean reference clock for the serial transceivers’ TX PLLs synchronous to the RX recovered clock”).



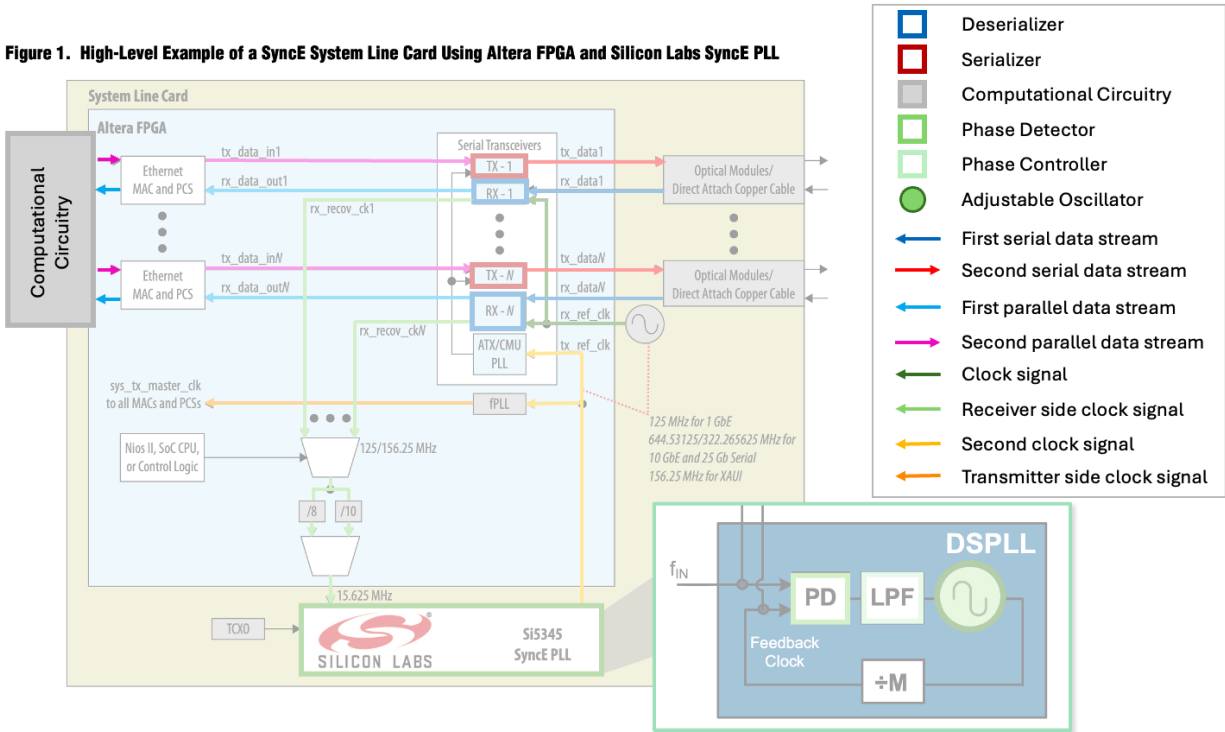
**Claim 1(i)**

Altera discloses “performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams.” Like all FPGAs, the Stratix FPGA used in Altera includes computational circuitry for performing operations on the first parallel data streams to generate the second parallel data streams. Ex. 1002 at ¶¶ 147-151; Ex. 1004 at 3 (discussing “FPGA core”).

The Stratix Handbook describes “the features of the logic array block (LAB) in the Stratix® V core fabric.” Ex. 1005 at 256. The logic array block “is composed

of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.”

*Id.* That logic array block is the computation circuitry within Altera. Ex. 1002 at ¶¶ 148-149.

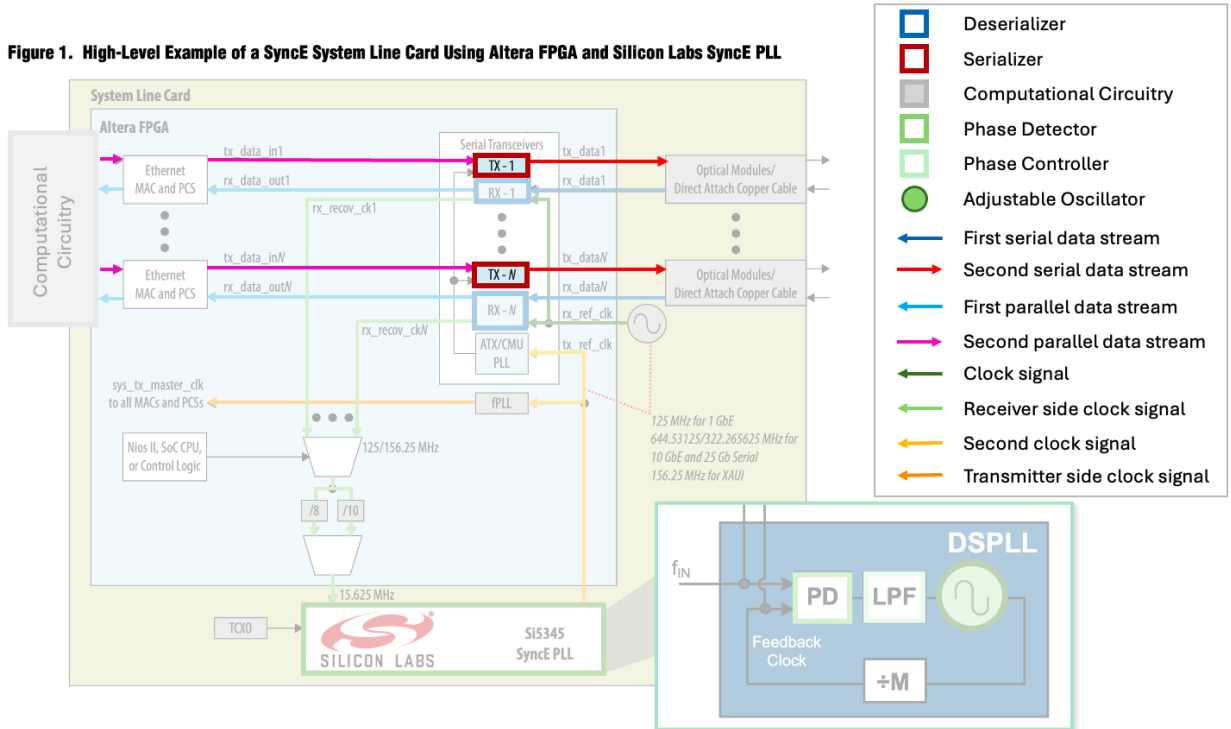


A skilled artisan would understand that any useful application of an FPGA that uses the transceivers (the RX and TX blocks) must also use the computational circuitry. Altera explains that the FPGA-based solution was used for “voice, data, and video” applications. Ex. 1004 at 1. Accordingly, a POSA would understand that, in order to use the FPGA-based solution of Altera, the parallel data streams received from the deserializer must go through the computational circuitry and undergo operations. Ex. 1002 at ¶¶ 150-151; *see also* Ex. 1013 at 2 (“In this system, the

programmable logic in the FPGA is loaded with a design that includes one or more Ethernet cores, along with any other application logic needed on the card.”).

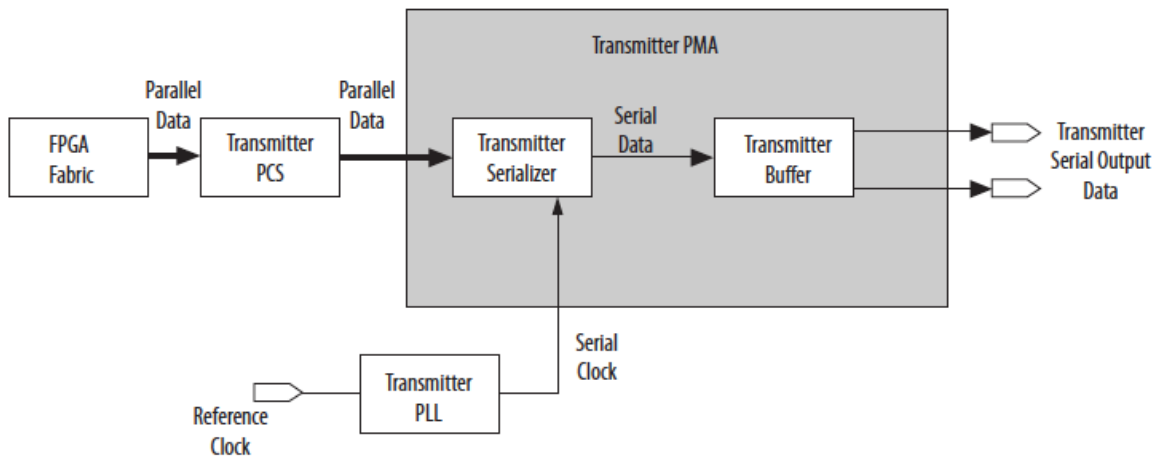
**Claim 1(j)**

Altera discloses “transmitting, from the field programmable gate array system, the second serial data stream, derived from the second plurality of parallel data streams.” Ex. 1002 at ¶¶ 152-154. As shown in Figure 1, the serialized data, tx\_data1 through tx\_dataN, is transmitted from the FPGA system to the optical modules/direct attach copper cable. *Id.* at ¶ 153. This data is derived from the second plurality of parallel data streams (tx\_data\_in1 through tx\_data\_inN), which are transmitted to the transmitter portion (TX-1 through TX-N) of the serial transceivers. *Id.* The transmitter converts the parallel data streams to serial data streams. *Id.*



The Stratix Handbook confirms that Altera discloses this limitation. Ex. 1002 at ¶ 154. Figure 1-8 depicts parallel data being transmitted from the FPGA fabric into a serializer in the Transmitter PMA. The serializer generates serial data streams that are then transmitted off the FPGA via a transmitter buffer connected to serial output data pins. Ex. 1005 at 14 (“The PMA . . . transmits off-chip high-speed serial data streams.”), 26 (“The serializer converts the incoming low-speed parallel data from the transceiver PCS or FPGA fabric to high-speed serial data and sends the data to the transmitter buffer.”).

**Figure 1-8: Transmitter PMA Block Diagram**



**Claim 1 wherein clause**

Altera discloses “wherein said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams.” Ex. 1002 at ¶¶ 155-159. A clock domain crossing operation within the computational logic is necessary when asynchronous clock domains exist within the computational logic.

*Id.* at ¶¶ 156-157. Altera explains that its SyncE solution supports “[g]eneration of all system clock frequencies from a single recovered clock frequency,” (e.g., rx\_recov\_clk) using the “PLL to maintain stability and accuracy.” Ex. 1004 at 3; *see also id.* at 2 (showing a “sys\_tx\_master\_clk”). “[A]ll system clock frequencies” refers to, among other things, the clocks depicted in Altera Figure 1, including the clocks used by the computational logic that processes the parallel data streams, all MACs, and all PCSs. Ex. 1002 at ¶ 158. In other words, there are no clock domains to cross because the processing of the parallel, deserialized data uses a single clock—one of the rx\_recov\_clk selected from the deserializers. *Id.* at ¶ 159.

#### **Claim 4**

Altera discloses “[t]he method of claim 1, wherein the set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.” Ex. 1002 at ¶¶ 160-162. Arithmetic, logical, pipeline, and memory access operations are the most basic functions implemented in an FPGA, and a POSA would understand that these are the main facilities provided by an FPGA. *Id.* at ¶ 162.

For example, the Stratix Handbook describes “the features of the logic array block (LAB) in the Stratix<sup>®</sup> V core fabric.” Ex. 1005 at 256. The logic array block “is composed of basic building blocks known as adaptive logic modules (ALMs)

that you can configure to implement logic functions, arithmetic functions, and register functions.” *Id.*

The Stratix Handbook also includes a chapter that explains how to utilize embedded memory blocks in the FPGA when a design needs low-latency data storage that sits close to the programmable logic. These operations are memory access operations. *Id.* at 271. That chapter also refers to optional pipelining, which breaks long data paths into multiple stages and takes advantage of an FPGA’s parallel-processing abilities. *Id.* at 290. Accordingly, Altera discloses that its operations are arithmetic, logical, pipeline, or memory access operations. Ex. 1002 at ¶ 162.

Altera further explains that the FPGA-based solution is used for “voice, data, and video” applications and includes up to 10 Ethernet ports. Ex. 1004 at 1-2. A POSA would understand that this network-connected FPGA would thus perform a variety of operations, including: computation of a checksum to verify the integrity of information during transmission (an arithmetic operation), extracting information from incoming data packets to look up or update statistics or metadata (a memory operation), and using combinatorial logic (AND, OR, NOT, XOR, etc.) to decide whether to process a packet further or drop it (a logical operation). A POSA would also understand that pipeline operations are ubiquitous in synchronous digital designs and used to allow concurrent processing, for example, when parsing parallel

data words (i.e., group of bits transferred together at the same time) of a received packet (from the deserializer), when a memory location is read, and when fields of a packet are modified ahead of its transmission (serialization). Ex. 1002 at ¶ 161.

### **Claim 6**

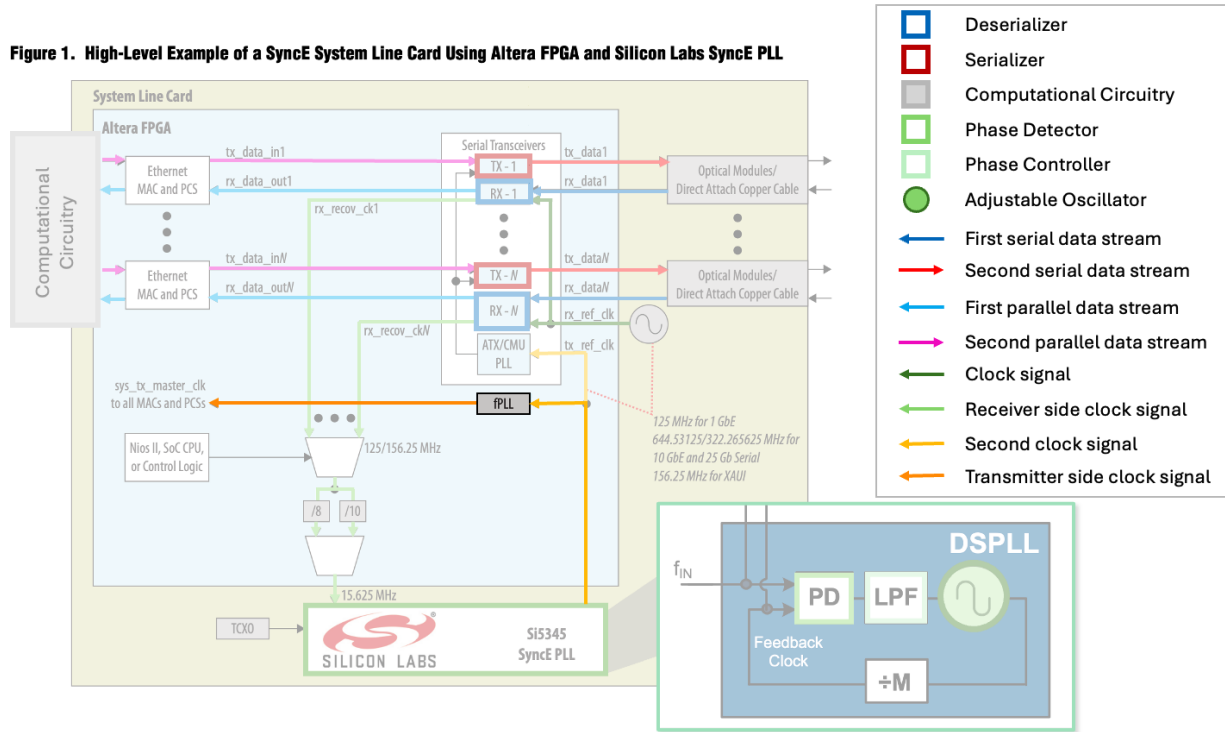
Altera discloses “[t]he method of claim 1, wherein at least a portion of the set of operations performed in step (h) are performed after step (g).” Ex. 1002 at ¶¶ 163-164.

Altera explains that a second clock signal is generated using the external PLL (step g) before the transmitter-side clock signal derived from the second clock signal is generated within the FPGA (step h). *Id.*; *see also above* at Claim 1(g), (h).

Altera explains that a “stabilized clock” is generated by the Si5345 PLL. Ex. 1004 at 3. That “stabilized clock” is then “used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” *Id.* at 3; *see also id.* at 4 (Si5345 PLL “suppl[ies] a clean reference clock for the serial transceivers’ TX PLLs synchronous to the RX recovered clock”).

Figure 1 shows this process. Ex. 1002 at ¶ 164. The tx\_ref\_clk clock (the “second clock signal”) generated by the external PLL is passed into the FPGA and is passed to the fPLL, which generates the transmitter side clock (sys\_tx\_master\_clk) that is provided to each the MAC and PCS for use with parallel data. Accordingly,

the transmitter side clock signal—which is derived from the second clock signal—must be generated after the second clock signal is generated by the external PLL. *Id.* Because Altera discloses that the totality of step (h) is performed after step (g), it is also true that at least a portion of step (h) is performed after step (g). *Id.*

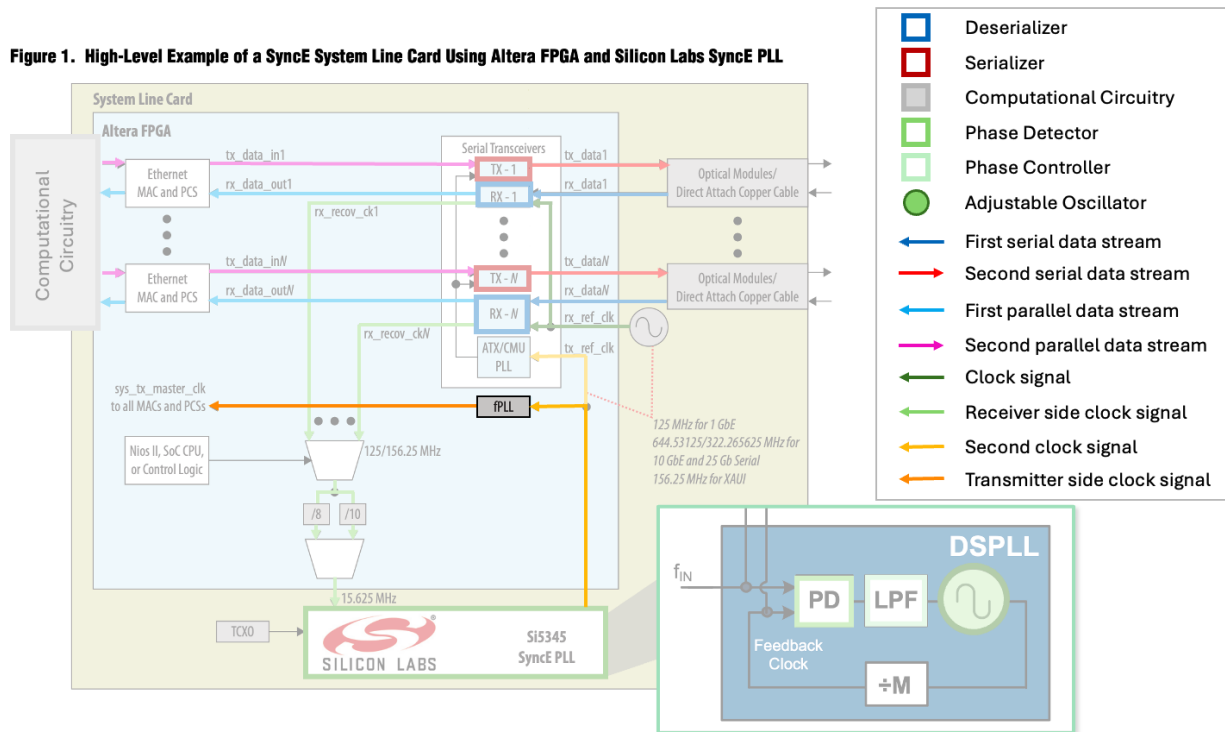


**Claim 7**

Altera discloses “[t]he method of claim 1, wherein all of the set of operations performed in step (h) are performed after step (g).” Ex. 1002 at ¶¶ 165-166. Altera explains that a second clock signal is generated using the PLL (step g) before the transmitter-side clock signal derived from the second clock signal is generated within the FPGA (step h). *Id.* Altera explains that a “stabilized clock” is generated by the Si5345 PLL. Ex. 1004 at 3. That “stabilized clock” is then “used to feed the

FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” Ex. 1004 at 3; *see also id.* at 4 (Si5345 PLL “suppl[ies] a clean reference clock for the serial transceivers’ TX PLLs synchronous to the RX recovered clock”).

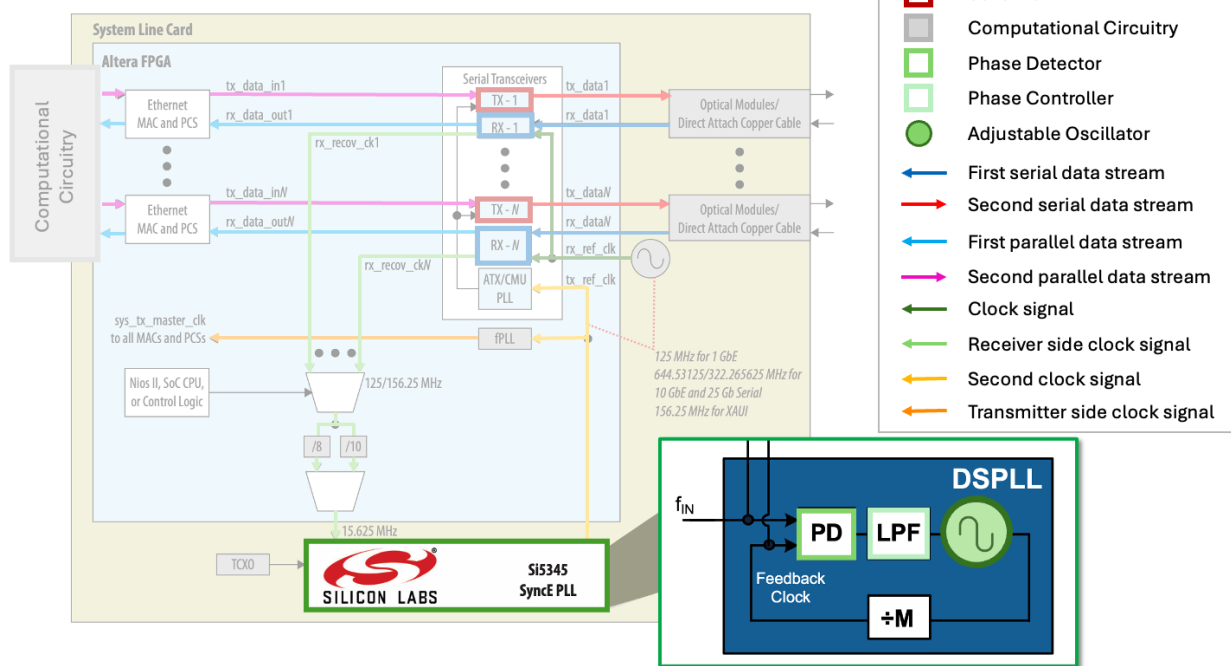
Figure 1 shows that the tx\_ref\_clk clock is transmitted to the ATX/CMU PLL within the serial transmitter (TX), which then generates a transmitter-side clock signal that is provided to each TX. Ex. 1002 at ¶ 166. Accordingly, all operations necessary to derive the transmitter side clock signal are performed after the second clock signal is generated by the external PLL. *Id.*



### Claim 8(i)

Altera discloses “[t]he method of claim 1, wherein step (g) further comprises (i) generating, by the phase lock loop, a feedback clock signal associated with the transmitter side clock signal by performing the following steps until a first output of a phase detector of the field programmable gate array system is below a first threshold level.” Ex. 1002 at ¶¶ 167-170. Step (g)—“generating, using the phase lock loop, a second clock signal”—occurs within the Si5345 PLL used in Altera. *Id.* The limitations of claim 8 describe a normal operation of a PLL. *Id.* at ¶ 168.

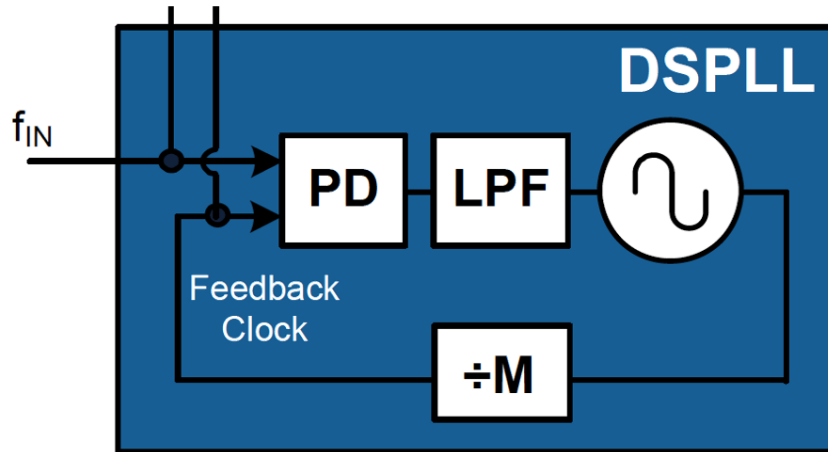
**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



With respect to the PLL’s generation of the feedback clock, in Si5345, “[i]f at least one valid clock is available for synchronization [e.g., the input clock], the DSPLL will automatically start the lock acquisition process. . . . During lock

acquisition the outputs will generate a clock [e.g., the feedback clock] that follows the VCO [voltage-controlled oscillator] frequency change as it pulls-in to [e.g., approaches] the input clock frequency.” Ex. 1006 at 17.

Figure 13 of Si5345 discloses that during lock acquisition, the PLL generates a “feedback clock” signal that is iteratively compared against the input clock signal. *Id.* at 27. The DSPLL continues in lock acquisition mode, following the steps set out in claim 8, until the output of the phase detector is below a first threshold level. “An example configuration where LOCK is indicated [is] when there is less than 0.2 ppm frequency difference at the inputs of the phase detector.” *Id.*; *see also* Ex. 1002 at ¶ 169.



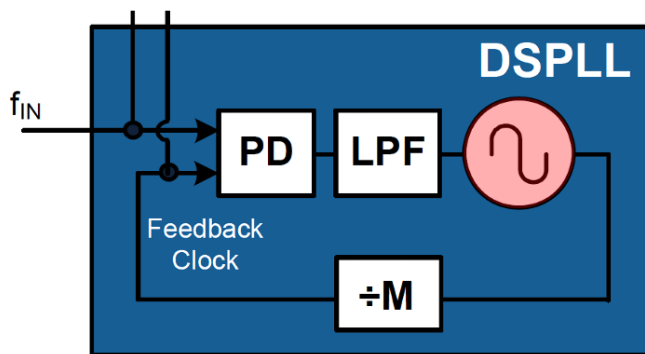
Si5345/44/42 Figure 13 Excerpt

Additionally, in Altera, the feedback clock is associated with the transmitter side clock signal—because it is connected to and drives the tx\_ref\_clk signal of the FPGA. Ex. 1002 at ¶ 170; Ex. 1004 at 2. Specifically, the feedback clock is used by

the external PLL in generating the second clock signal (tx\_ref\_clk), and the second clock signal is in turn used to derive the transmitter side clock signal (sys\_tx\_master\_clk). See Claim 1(g) and 1(h) above.

**Claim 8(i)(1)**

Altera discloses “generating, by an adjustable oscillator in the field programmable gate array system, the second clock signal.” Ex. 1002 at ¶¶ 171-172. The Si5345 SyncE PLL includes an adjustable oscillator, shown in red below, which generates a second clock signal. *Id.* at ¶ 172; Ex. 1006 at 10, 11, 27. When the PLL is in lock acquisition mode, as shown in Figure 13, the second clock signal is then transmitted to a divide-by-M, which generates the feedback clock signal. Ex. 1002 at ¶ 172; Ex. 1006 at 27. Ultimately, as shown in the line exiting the DSPLL in Figure 2, “the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock,” at which point the second clock signal will be output. Ex. 1006 at 17.



Si5345/44/42 Figure 13 Excerpt

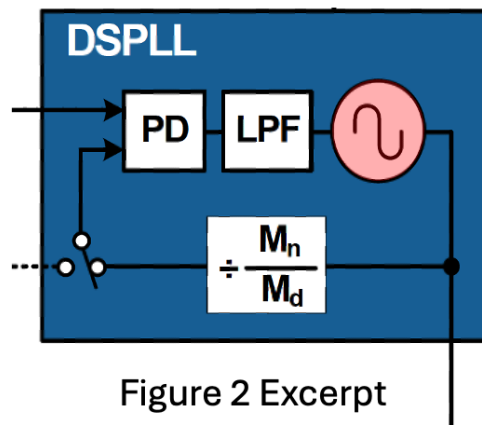
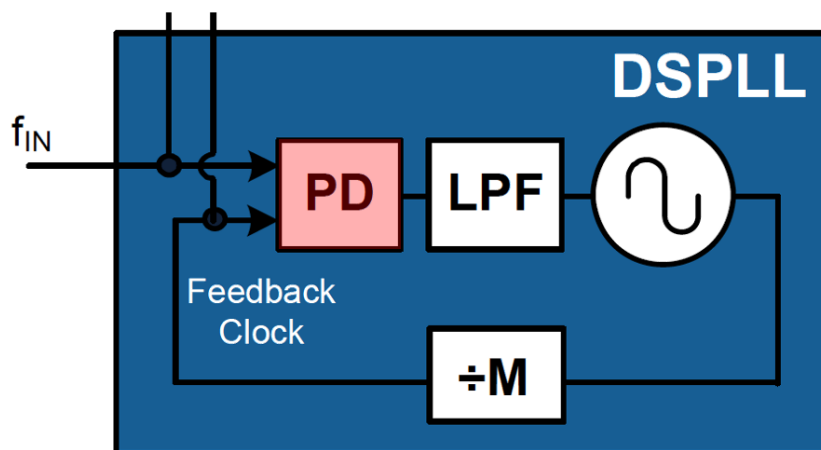


Figure 2 Excerpt

**Claim 8(i)(2)**

Altera discloses “generating, by the phase detector, the first output based on a comparison of the receiver side clock signal and the feedback clock signal obtained from the second clock signal.” Ex. 1002 at ¶ 173. The Si5345 includes a phase detector, abbreviated as “PD” and shown in red in Figure 13 below. *Id.*; Ex. 1006 at 10, 11, 27. The phase detector compares the input clock signal to the feedback clock signal. In Altera, the input clock signal is the receiver side clock signal, *see* Claim 1(f) above, and as discussed in Claim 8(i)(1), the feedback clock signal is obtained from the second clock signal passing through the (programmable) divider. Based on that comparison, the phase detector generates an output signal proportional to the phase difference between the two clock signals. Ex. 1002 at ¶ 173.

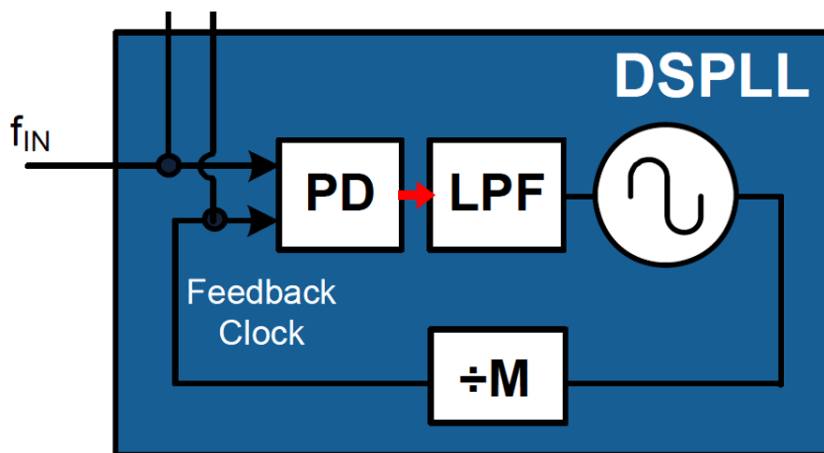


Si5345/44/42 Figure 13 Excerpt

**Claim 8(i)(3)**

Altera discloses “transmitting, from the phase detector to a phase controller of the field programmable gate array system, the first output.” Ex. 1002 at ¶¶ 174-176.

In Si5345, the phase detector (PD) transmits the first output signal to the low-pass filter (LPF), which controls the phase using by allowing only frequencies lower than a certain threshold to pass through the filter. Ex. 1006 at 10, 11, 27. The LPF is a phase controller because it controls the signal. Ex. 1002 at ¶¶ 175-176. In sum, the LPF receives the output of the phase detector, allows frequencies below a threshold to pass through the filter, and outputs phase control information. *Id.*

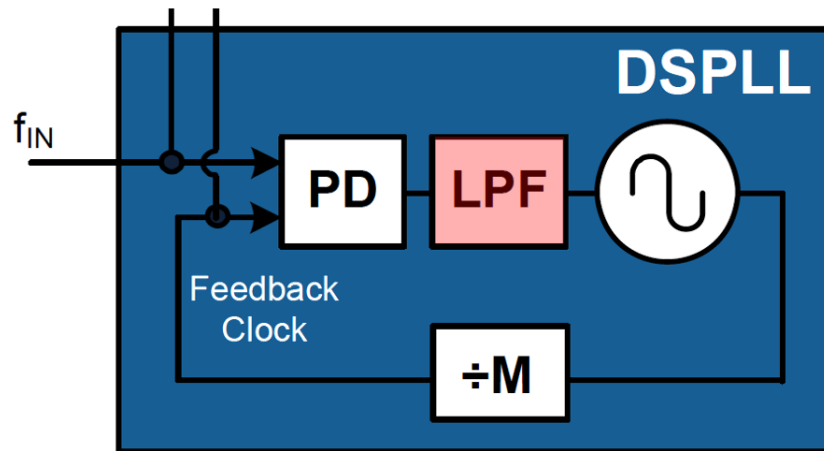


Si5345/44/42 Figure 13 Excerpt

**Claim 8(i)(4)**

Altera discloses “determining, by the phase controller, interim adjustment information based on the first output.” Ex. 1002 at ¶¶ 177-178. As explained above, the LPF is the phase controller. The LPF uses the first output from the phase detector

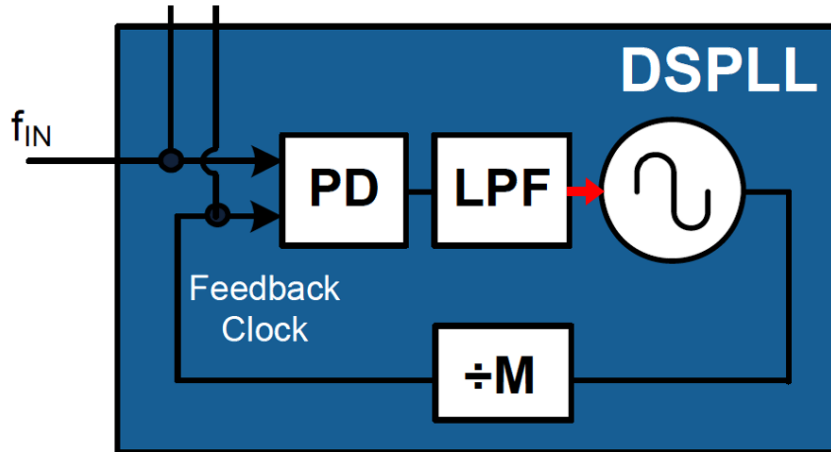
to determine how to adjust the phase of the clock signal by selectively passing only certain frequencies through toward the VCO. *Id.* The LPF operation results in interim adjustment information. *Id.*



Si5345/44/42 Figure 13 Excerpt

**Claim 8(i)(5)**

Altera discloses “transmitting, from the phase controller to the adjustable oscillator, the interim adjustment information.” Ex. 1002 at ¶¶ 179-180. In Si5345, the LPF transmits the interim adjustment information to the adjustable oscillator so the adjustable oscillator can adjust the clock signal. *Id.*; Ex. 1006 at 10, 11, 27.



Si5345/44/42 Figure 13 Excerpt

**Claim 8 wherein clauses**

Altera discloses “wherein, the adjustable oscillator adjusts the second clock signal based on the interim adjustment information.” Ex. 1002 at ¶ 181. As discussed for claim 8(i)(1), the adjustable oscillator adjusts the second clock signal. When the PLL is in lock acquisition mode, as shown in Figure 13, the second clock signal is then transmitted to an M divider, which generates the feedback clock signal. *Id.*; Ex. 1006 at 27. Ultimately, as shown in Figure 2 above, “the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock,” at which point the second clock signal will be output. Ex. 1006 at 17.

Altera also discloses “wherein steps (1) through (5) are repeated until the first output of the phase detector is below the first threshold level.” Ex. 1002 at ¶ 182. The DSPLL continues in lock acquisition mode, following the steps set out in claim 8, until the output of the phase detector is below a first threshold level, at which point

it enters the locked state. *Id.* “An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector.” Ex. 1006 at 27.

### **Claim 9**

Altera discloses “[t]he method of claim 1, wherein the first plurality of data streams has the same number of data streams as the second plurality of data streams.” A POSA would understand that there is a 1-to-1 correspondence of deserializers and serializers in Altera. Ex. 1002 at ¶¶ 183-184. Figure 1 shows that for every RX block there is also a TX block, totaling  $N$  number. Ex. 1004 at 2; *see also* Ex. 1005 at 7 (showing each transceiver channel has one receiver and one transmitter). And Altera explains that the “Altera® SyncE reference design implement[s] up to ten 1G/10 Gbps Ethernet (1G/10 GbE) ports,” indicating that in Altera there are up to 10 transceiver channels (e.g., 10 deserializers and 10 serializers). Ex. 1004 at 2; Ex. 1002 at ¶ 184.

### **Claim 10**

Altera discloses “[t]he method of claim 1, wherein the first plurality of data streams and the second plurality of data streams comprise one of the following: (i) eight (8) data streams; (ii) ten (10) data streams; (iii) sixteen (16) data streams; (iv) twenty (20) data streams; (v) thirty-two (32) data streams; (vi) forty (40) data streams; (vii) sixty-four (64) data streams; (viii) eighty (80) data streams; (ix) one

hundred twenty-eight (128) data streams; and (x) one hundred sixty (160) data streams.” *See* Claim 9 above. As above, Altera discloses at least a configuration with ten ports (i.e., ten deserializers and ten serializers), meaning there are 10 data streams. Ex. 1002 at ¶¶ 185-186.

**B. Ground 1B: Altera, the Stratix Handbook, and the Si5345 Manual Render Claims 1, 4, and 6-10 Obvious**

To the extent that a POSA would not have understood that the features of Stratix FPGA and Si5345 PLL are necessarily present in Altera, it would have been obvious to combine the Altera white paper, the Stratix Handbook, and the Si5345 Manual. A POSA would have been motivated to combine the Stratix Handbook and Si5345 Manual using Altera. Ex. 1002 at ¶ 187. Altera describes “a high-performance SyncE solution” that consists of “Altera’s Stratix® V FPGA interoperating with Silicon Labs’ Si5345 jitter-attenuating phase-locked loop (PLL) to provide a complete SyncE clock recovery, clock selection, and synchronization sub-system.” Ex. 1004 at 2. The Altera solution was developed by “Altera and Silicon Labs” and specifically used “the two companies’ products.” *Id.* at 2. And, as described above, a POSA would have been able to easily find and rely on the Stratix Handbook and Si5345 Manual, as they are among the specifications and data sheets that Altera and Silicon Labs made available for download from their respective websites. *See* § VIII.A.1 above.

Further, a POSA would have reasonably expected the combination of Stratix and Si5345 as set out in Altera to succeed, as Altera reports that its technique was successfully tested. Ex. 1002 at ¶ 188; Ex. 1004 at 6. For example, “Altera and Silicon Labs have validated that the jitter performance of Silicon Labs’ Si5345 PLL meets the requirement of Altera’s Stratix FPGA input reference clock and that the serial transceiver output jitter meets G.8262 requirements. The test includes Silicon Labs’ Si5345 PLL output jitter, phase noise tolerance at the PLL input, the clock synchronization loop’s phase noise filtering capability, and the ability of the loop to withstand short-term and long-term input interruptions and discontinuities.” *Id.* A POSA would have been confident in the success of the system since Altera “demonstrated a high-performance and flexible solution for frequency synchronization of telecom and data communication networks based on the Sync standard using the Ethernet infrastructure.” *Id.*; Ex. 1002 at ¶ 188.

Therefore, a POSA would have had reason to combine the Stratix FPGA with the Si5345 PLL in precisely the same way that Altera says they should be combined. *See Norian Corp. v. Stryker Corp.*, 363 F.3d 1321, 1328 (Fed. Cir. 2004) (affirming that a POSA would have been motivated to combine two references where one reference “expressly discussed the” other one). That combination of Altera, the Stratix Handbook, and the Si5345 Manual discloses all the limitations of claims 1,

4, and 6-10 for the same reasons as Altera anticipates those claims. Ex. 1002 at ¶ 189.

**C. Ground 2: Altera and Lockwood Render Claims 1-4 and 6-12 Obvious**

Altera (alone or in combination with the Stratix Handbook and Si5345 Manual) presents a solution to the latency inherent in clock-domain crossing that would have been obvious and attractive to a POSA for use in high-frequency trading applications, as Lockwood teaches. The combination of Altera and Lockwood renders claims 1 and 4 obvious, to the extent that they are not anticipated. Lockwood also would have motivated a skilled artisan to use Altera for trading, making claims 2 and 3 obvious. And Lockwood would have motivated a skilled artisan to make slight modifications to Altera to further reduce latency, making claims 11 and 12 obvious as well.

As a result, Altera and Lockwood would also make obvious claims 6-10, which depend from claim 1, for the same reasons. *See also* Ground 1A (explaining how the limitations of claims 6-10 are taught by Altera).

**1. A Skilled Artisan Would Have Been Motivated to Combine Altera and Lockwood**

It was common knowledge before the '381 patent that FPGA-based systems are useful for performing high-frequency trading operations, as even the patent acknowledges. Ex. 1001 at 1:42-44 (“FPGAs are used in the financial industry in

high frequency trading where the rapid processing of the FPGA is desired.”). Lockwood demonstrates how a skilled artisan would have put Altera to use for such trading. Ex. 1002 at ¶¶ 190-197.

Lockwood emphasized, back in 2012, “the race to minimize latency in high frequency trading.” Ex. 1007 at 7. In high-frequency trading, “[a] custom-designed datapath in an FPGA circuit offers the benefits of minimal, deterministic processing times down to clock cycles,” which are the smallest unit of time in which logic operations can occur. *Id.* at 8. In a regime like high-frequency trading in which even a few clock cycles can make a difference, a skilled artisan would have recognized that Altera offers a solution that eliminates the latency cost associated with clock-domain crossing circuits. *See id.* at 2 (“[T]he first few players to execute orders may be the only ones able to profit from a given opportunity” and “reduction in latency can improve arbitrage profitability”); Ex. 1014 at 1 (“HFT is all about speed and minimizing latency: the faster you can run trading strategies and algorithms for analyzing minute price changes and executing trade orders, the higher the probability to win over competition.”); Ex. 1015 at 2:13-14 (cited on the face of the ’381 patent and noting that speed of information delivery is a valuable dimension to the financial instrument trading and brokerage industry); Ex. 1002 at ¶ 192.

Additionally, Altera explains that the benefit of its SyncE synchronization solution is “high reliability,” resulting in “a high-performance and flexible solution

for frequency synchronization of telecom and data networks based on the SyncE standard using the Ethernet infrastructure.” Ex. 1004 at 2, 6. Lockwood explained that, even as of 2012, “Ethernet is currently more prevalent in the HFT ecosystem” and “will continue to dominate for the foreseeable future”—and the passage of time has demonstrated this to be true. Ex. 1007 at 2. Thus, long before 2018, as Lockwood demonstrated, a POSA would have been motivated to use Altera in high-frequency trading applications. Ex. 1002 at ¶ 193.

Lockwood provided several different examples in which a POSA would recognize that the Altera system could be utilized. Ex. 1002 at ¶ 194. For example, Lockwood described FPGA-based Smart Network Interface Controllers (NICs) as “another way to apply programmable logic” to the development of financial applications. “Smart NICs typically bring together high-speed network interfaces, a PCIe host interface, memory and an FPGA,” and in this arrangement, “some of the processing” is “offload[ed]” to the FPGA. *Id.* at 8. Specifically, “[t]he FPGA implements the NIC controller, acting as the bridge between the host computer and the network and allows user-designed custom processing logic to be integrated directly into the data path.” *Id.* at 3. This allowed a smart NIC to “function as a programmable trading platform.” *Id.* at 11. A POSA would recognize that Altera—which touts its usefulness in networking equipment, among other things—could be used as the FPGA in Lockwood Figure 2 and the computational circuitry of the

Altera FPGA would “function as a programmable trading platform.” *Id.*; see also Ex. 1004 at 2; Ex. 1002 at ¶ 194.

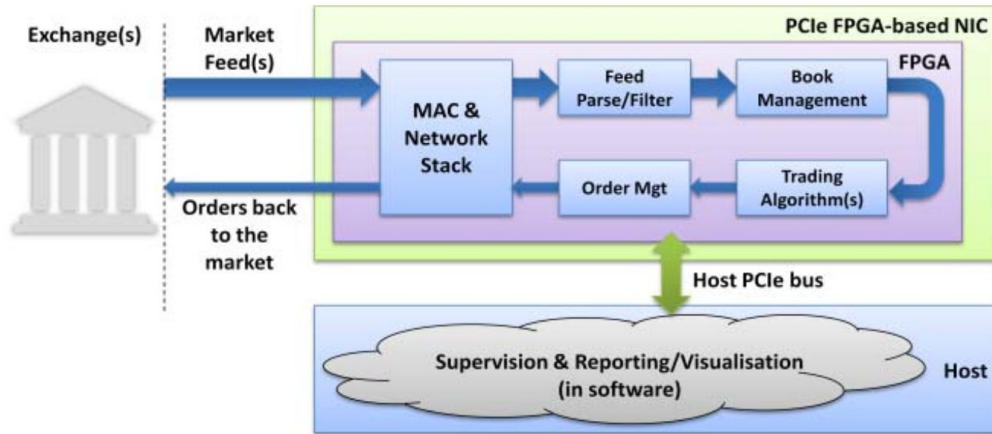
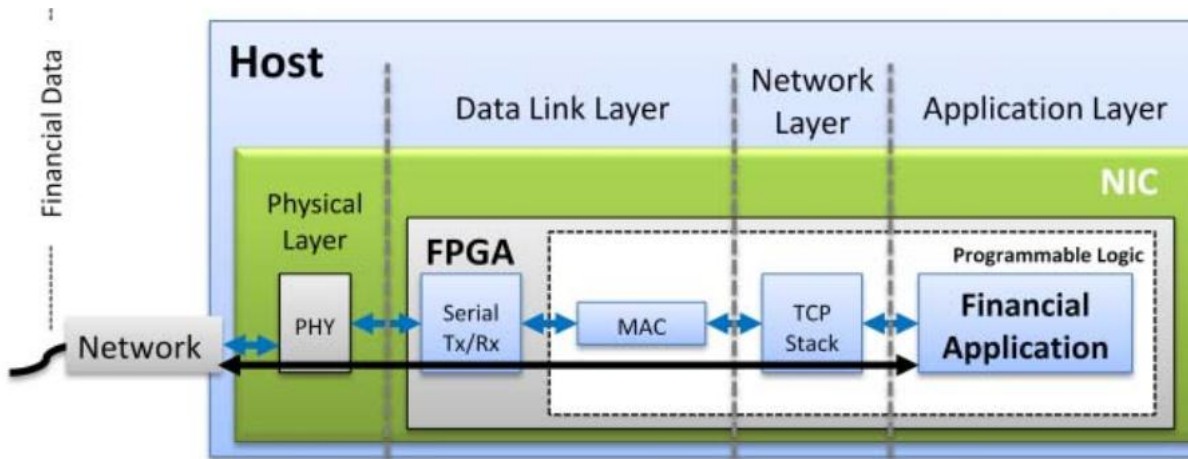


Figure 2 Typical Smart NIC in a supervised financial trading application

A skilled artisan would also recognize that Altera would be an attractive option to use for the FPGA shown in the FPGA-based trading platform displayed in Lockwood’s Figure 3, below. Ex. 1002 at ¶ 195. Altera’s solution largely relates to the data link layer shown in Figure 3 (e.g., the transceivers), and a skilled artisan would recognize that the “programmable logic” of the Altera FPGA could be used for financial applications, including high-frequency trading. *Id.*



A POSA seeking to implement the Altera FPGA for high-frequency trading would have a reasonable expectation of success. Ex. 1002 at ¶ 196. An FPGA is programmable, meaning the computational circuitry can be programmed for whatever function the user desires. Ex. 1005 at 256 (The “logic array block (LAB) in the Stratix<sup>®</sup> V core fabric . . . is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.”); Ex. 1016 at 39 (“an FPGA provides a blank slate of bitwise functional units that can be programmed to create any desired circuit or processor”). Therefore, a skilled artisan would recognize that the Altera FPGA’s programmable logic could be used to process financial data in high-frequency trading. Ex. 1002 at ¶ 196.

To the extent that a POSA would not have understood that the features of Stratix FPGA and Si5345 PLL are necessarily present in Altera, a POSA would have been motivated to combine Altera, the Stratix Handbook, and the Si5345 Manual for

the reasons discussed above, *see* Ground 1A above, and would have would have implemented this combination for the purposes and applications described in Lockwood for all the same reasons discussed in this section. Ex. 1002 at ¶ 197.

**2. Claim 1(e), 1(i), and/or 4: It Would Have Been Obvious to the Computational Circuitry Present in Altera**

To the extent that a POSA would not have understood that Altera describes using the computational circuitry of the Stratix FPGA—e.g., in claim limitations 1(e), 1(i), and/or 4—a POSA would have been motivated to use the Stratix computational circuitry with Altera. Ex. 1002 at ¶¶ 198-207.

**Claims 1(e) and 1(i)**

Altera and Lockwood teach “transmitting, from the deserializer to computational circuitry in the field programmable gate array, the first plurality of parallel data streams” and “performing, by the computational circuitry, a set of operations on at least a portion of the first plurality of parallel data streams to generate a second plurality of parallel data streams.” *Id.* at ¶¶ 199-205.

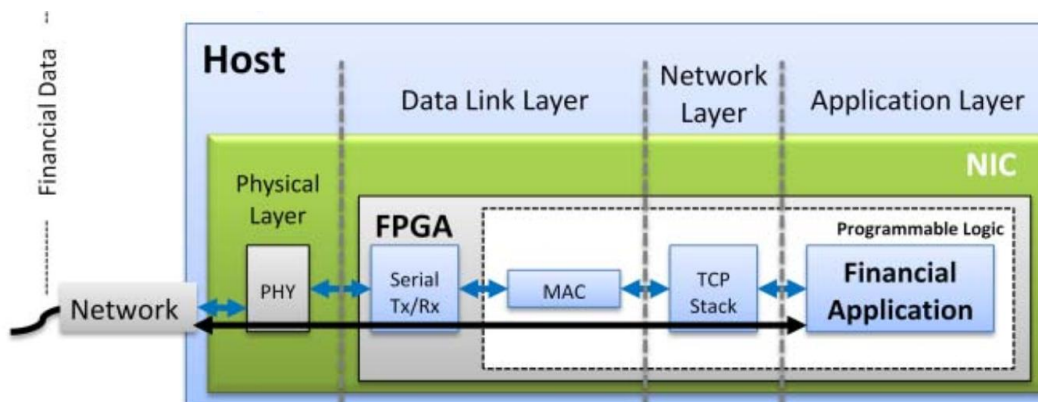
The Stratix FPGA contains a “logic array block (LAB) in the Stratix<sup>®</sup> V core fabric.” Ex. 1005 at 256. The logic array block “is composed of basic building blocks known as adaptive logic modules (ALMs) that you can configure to implement logic functions, arithmetic functions, and register functions.” *Id.* As explained above, that logic array block is the computation circuitry within Altera. Ex. 1002 at ¶ 200. It

would have been obvious and beneficial for a POSA to put this computational circuitry to use in the Altera solution. Ex. 1002 at ¶¶ 202-203.

One key benefit of an FPGA relative to other integrated circuits is that an FPGA is programmable, meaning that a customer can configure the FPGA to carry out any operations it needs, rather than the internal circuitry being fixed in manufacturing. *Id.* In the case of Altera, it would be obvious that a customer using the SyncE solution provided would use the programmable FPGA computational circuit to perform operations on the incoming data. *Id.* For example, another Altera SyncE white paper discloses that “[i]n this system, the programmable logic in the FPGA is loaded with a design that includes one or more Ethernet cores, along with any other application logic needed on the card.” Ex. 1013 at 2; *see also* Ex. 1016 at 39 (“an FPGA provides a blank slate of bitwise functional units that can be programmed to create any desired circuit or processor”).

Lockwood reinforces that conclusion. Ex. 1002 at ¶¶ 204-205. Lockwood Figure 3 depicted financial applications (e.g., trading algorithms) implemented in the programmable logic of the FPGA. Lockwood explained that “FPGAs offer the performance benefits of custom hardware while retaining programmability,” such that “[t]rading algorithms can be continually improved.” Ex. 1007 at 4; *see also id.* at 2 (“Flexibility is also vital to enable trading platforms to adapt to changing market conditions and trading strategies.”). Accordingly, it would have been obvious to

perform operations using the programmable computational circuitry of the Stratix FPGA in Altera. Ex. 1002 at ¶¶ 199-205.



#### Claim 4

Altera and Lockwood teach “[t]he method of claim 1, wherein the set of operations includes at least one of the following: (i) an arithmetic operation; (ii) a logical operation; (iii) a pipeline operation; and (iv) a memory access operation.” Ex. 1002 at ¶¶ 206-207.

The Stratix FPGA can be “configure[d] to implement logic functions, arithmetic functions, and register functions,” among others, all of which align with the operations described in claim 4. Ex. 1005 at 256. Further, a skilled artisan would understand that trading operations, like those described in Lockwood, will include at least logical or arithmetic operations. Ex. 1002 at ¶ 207; Ex. 1007 at 1 (“Traders employ a range of algorithms and heuristics to decide when and what to trade. These approaches combine current market data with historical data and outputs from computational models.”).

For example, Lockwood described a number of different operations performed within the computational circuitry of an FPGA including: an arithmetic operation (“net position = (total long positions) – (total short positions)”); a logical operation (“If it is a Buy order . . . , then . . . .”); a pipeline operation (“The breakup of 1μsec total delay is 400ns (PHY+MAC, high-speed serial receiver) + 200ns (parsing/ calculations) + 400ns (PHY+MAC, high-speed serial transmitter).”); and memory access operation (“[D]ata is stored in fast on-chip memory and QDR-II directly attached to the FPGA. This memory is accessed . . . when an order enters FPGA and the table lookups and computation are performed directly in logic.”). Ex. 1002 at ¶ 207; Ex. 1007 at 7.

### **3. Claims 2 and 3: It Would Have Been Obvious to Use Altera for Trading Applications**

Claims 2 and 3 require nothing more than using claim 1’s method for trading. The incoming serial data is “market data,” the outgoing serial data is “order entry data” or “trading data,” and (for claim 2 only) the operations performed by the computational logic “are associated with a trading algorithm.” Putting the Altera system to such use is obvious in light of Lockwood, including as described above. Ex. 1002 at ¶¶ 208-213.

#### **Claim 2**

Altera and Lockwood teach “[t]he method of claim 1, wherein the first serial data stream comprises market data, the second serial data stream comprises order

entry data, and the set of operations are associated with a trading algorithm.” *Id.* at ¶¶ 209-211. As described in Ground 1, Altera discloses first serial data received by the deserializer and second serial data transmitted from the FPGA system. *See* Claim 1(a) and 1(j) above.

A POSA would have been motivated by Lockwood to use Altera in trading applications. In a trading setting, a POSA would understand that the purpose of the FPGA system would be to supply market data such that an algorithm implemented in the FPGA can determine the orders to transmit to the marketplace. Ex. 1002 at ¶ 209; Ex. 1007 at 1 (“Traders receive multiple high-datarate UDP/IP market data streams over the network from trading venues.”), 2 (“HFT strategies therefore require low-latency market access both to receive market data as well as to transmit new orders.”). In that application, the first serial data would include market data—e.g., price and quantity-related data for orders and executions by market participants in a financial instrument, as reported by a trading venue, such as bid, asks, trades, and options auction notifications. Ex. 1002 at ¶ 209; Ex. 1001 at 22:66-23:3, 27:25-27. For example, Lockwood Figure 2 showed the first serial data as “market feed(s)” entering the FPGA. Ex. 1007 at 3; *see also id.* at Figure 3.

The second serial data would include order entry data—e.g., data related to entering orders to purchase or sell stocks, commodities, goods, and/or services. Ex. 1002 at ¶ 210; Ex. 1001 at 26:67-27:2. Lockwood Figure 2 showed the second

serial data as “[o]rders back to the market” exiting the FPGA system. Ex. 1007 at 3; *see also id.* at 1 (“The final step is to enter these orders into the exchange”), Fig. 3.

A POSA would understand that the set of operations used on the market data to generate the order entry data would be a trading algorithm—e.g., a set of rules implemented in the FPGA to determine which orders to send for execution in financial markets. Ex. 1002 at ¶ 211. Lockwood Figure 2 showed that “Trading Algorithm(s)” are implemented in the FPGA computational circuitry. Ex. 1007 at 3; *see also id.* at 1 (“Traders employ a range of algorithms and heuristics to decide when and what to trade. These approaches combine current market data with historical data and outputs from computational models.”), Fig. 3.

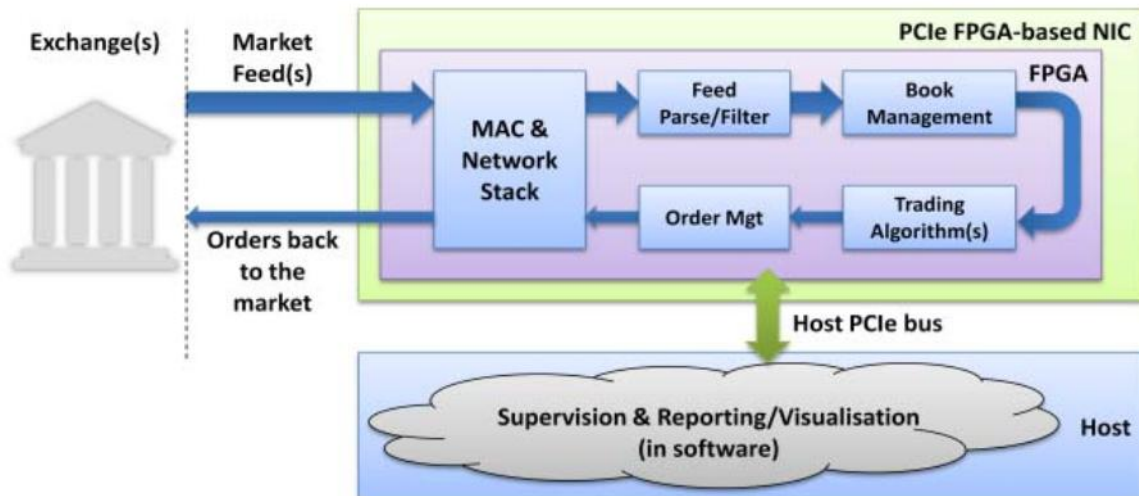


Figure 2 Typical Smart NIC in a supervised financial trading application

### **Claim 3**

Claim 3 is barely different from claim 2. Altera and Lockwood teach “[t]he method of claim 1, wherein the first serial data stream includes market data and the second serial data stream includes trading data.” Ex. 1002 at ¶¶ 212-213. For the reasons given for claim 2, in Altera and Lockwood “the first serial data stream includes market data.” *See* Claim 2 above.

Claim 3 requires “trading data” instead of Claim 2’s “order entry data.” The second serial data would include trading data—e.g., data related to trading (e.g., purchasing or selling) stocks, commodities, goods, and/or services. Ex. 1002 at ¶ 213; Ex. 1001 at 26:67-27:2. Lockwood Figure 2 showed the second serial data as “[o]rders back to the market” exiting the FPGA system. Ex. 1007 at 3; *see also id.* at 1 (“The final step is to enter these orders into the exchange”), Figure 3. A POSA would understand that orders sent back to the exchange are a type of trading data. Ex. 1002 at ¶ 213.

#### **4. Claim 11 and Claim 1 wherein clause: It Would Have Been Obvious to Modify Altera to Provide an External Feedback Clock into the Si5345 PLL**

Claim 11 requires that the frequency and phase of the transmitter side clock signal and receiver side clock signal are the same. It would have been obvious to a skilled artisan to match the phase and frequency of those clock signals, as it would reduce latency, and it would easily be implemented in Altera by utilizing the Si5345

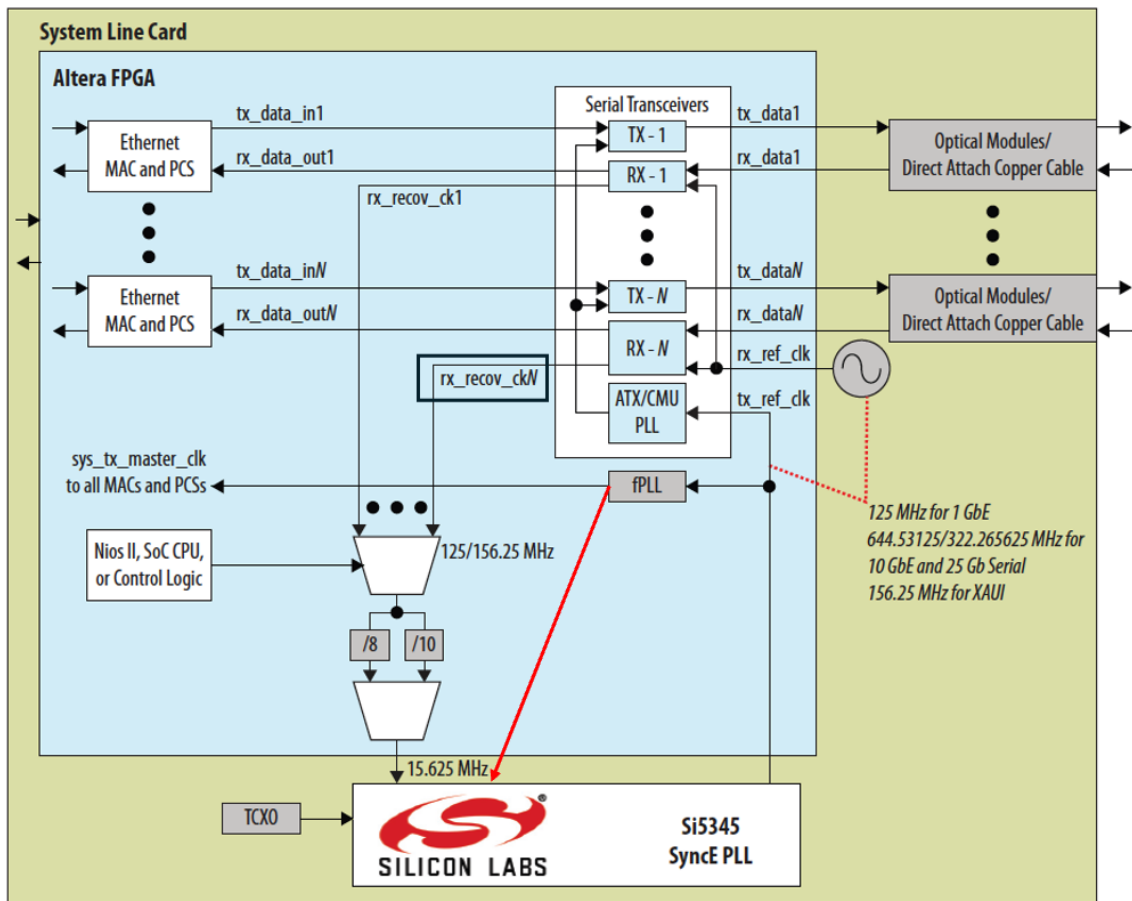
PLL's external feedback loop. That same modification would also ensure that no "clock domain crossing operations that delay processing of the first set of parallel data streams" are used in the computational circuit, to the extent that limitation is not anticipated by Altera. *See* Claim 1 where clause above.

### **Claim 11**

Based on Lockwood, a skilled artisan would have been motivated to modify Altera such that "the transmitter side clock signal and the receiver side clock signal have the same frequency and phase." Ex. 1002 at ¶¶ 214-220.

A POSA would have been motivated to phase align the receiver side and transmitter side clock signals by using the feedback input of the external PLL, as illustrated with the addition of the red line shown in Altera Figure 1 and described further below. *Id.* at ¶ 218.

**Figure 1. High-Level Example of a SyncE System Line Card Using Altera FPGA and Silicon Labs SyncE PLL**



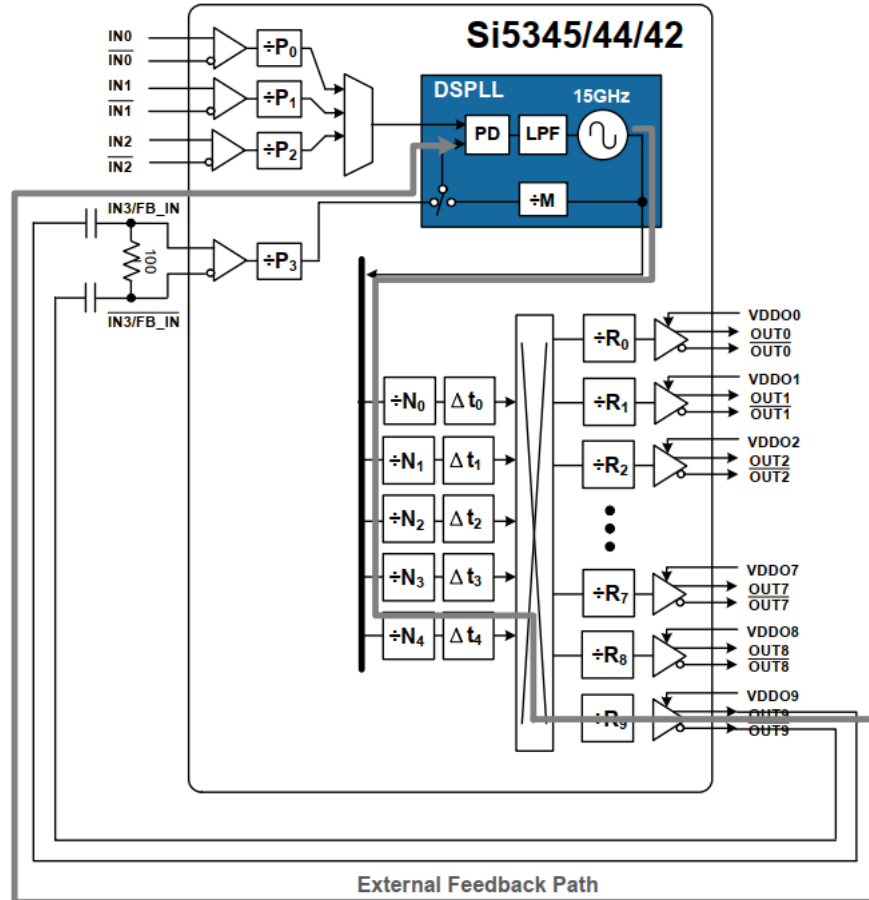
As Altera explains, SyncE solutions require accurate “clock synchronization,” which includes ensuring the frequency is the same (“ $\pm 4.6$  ppm frequency accuracy”) and phase noise is reduced (“Limited phase wander”). *Id.* at ¶ 215; Ex. 1004 at 2. The Altera solution is able to achieve both. *Id.* As explained with respect to claim 1, in Altera the receiver side clock signal (rx\_recov\_clk) is generated when the receiver side “PHY IP cores recover the receiver (RX) clocks from their respective 1G/10 Gbps Ethernet ports.” *Id.* at 3. The receiver side clock (rx\_recov\_clk) is then transmitted to the Si5345 PLL. *Id.* The purpose of the Si5345 PLL is to “generate

output clocks that are both frequency and phase locked to its selected input clock.” Ex. 1006 at 17. “This stabilized clock is used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” Ex. 1004 at 3.

Altera also shows a single clock from the fPLL (sys\_tx\_master\_clk) that is used for both MAC and PCS functions. A POSA would understand that the fPLL shown is configured such that the resulting transmitter side clock signal frequency matches the receiver side clock signal frequency. Ex. 1002 at ¶ 216. But the phases of the receiver-side clock signal (rx\_recov\_clk) and the transmitter side clock signal (sys\_tx\_master\_clk) will not necessarily be phase-aligned. However, a POSA would understand that aligning clock phases is a routine task that can be achieved a variety of ways. *Id.*

For example, a skilled artisan would understand that the external Si5345 PLL supports External Feedback Mode, also described as “Zero Delay Mode.” *Id.* at ¶ 217; Ex. 1006 at 44 (Figure 21). The “zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs.” *Id.* In “Zero Delay Mode,” rather than using the internal “feedback clock” discussed above with respect to claim 8 and shown in Figure 13 of the Si5345 Manual, the Si5345 PLL uses an external clock in the feedback loop. As a result

“[t]he phase difference between the output” and “the selected input [] will be nulled to zero.” *Id.* at 105.



**Figure 21. Si5345 Zero Delay Mode Set-up**

A POSA would have been motivated to phase align the receiver side and transmitter side clock signals for the purposes of reducing latency in the system. Ex. 1002 at ¶ 218. For example, a skilled artisan would understand that reducing latency can increase profitability. *See, e.g.,* Ex. 1007 at 2 (In 2012, “reduction in latency can improve arbitrage profitability”); Ex. 1014 at 1 (“HFT is all about speed and minimizing latency: the faster you can run trading strategies and algorithms for

analyzing minute price changes and executing trade orders, the higher the probability to win over competition.”); Ex. 1016 at 94-97. A POSA would employ the above feature of the external Si5345 PLL (i.e., the “Optional External Feedback” input) to compensate for signal delays that could otherwise cause the phases of these clock signals to diverge. This use of the feedback input of the external PLL is illustrated with the red line shown in Altera Figure 1 above.

A POSA would have a reasonable expectation that this minor modification to Altera would be successful. Ex. 1002 at ¶ 219. The modification utilizes capabilities already present in the Stratix FPGA and the Si5345 PLL and puts the Zero Delay Mode to precisely the use it is meant for. Si5345 Manual at 44 (“A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs.”).

### **Claim 1 wherein clause**

To the extent that Altera does not teach the limitation in claim 1’s wherein clause, a skilled artisan would understand that the modification described above with respect to claim 11 ensures that the method of claim 1 “does not use clock domain crossing operations that delay processing of the first set of parallel data streams.” A skilled artisan would have been motivated to make that change with a reasonable expectation of success for all the same reasons as apply to claim 11. Ex. 1002 at ¶¶ 221-223.

Specifically, a POSA would have been motivated by Lockwood to eliminate as much latency from the system as possible. *Id.* at ¶ 222. Implementing the red line in Altera to transmit the clock signal from the fPLL (sys\_tx\_master\_clk) to use as external feedback for the Si5345 PLL eliminates the need for any clock domain crossing operations in the path from receiving the first serial data to transmitting the second serial data. *Id.* Notably, this *exceeds* the requirements of the claim 1 wherein clause, which does not require eliminating all CDC operations but only those “that delay processing of the first set of parallel data streams.”

As discussed above with respect to claim 11, a POSA would have had a reasonable expectation in the success of this modification, which utilizes capabilities already present in the Stratix FPGA and Si5345 PLL and puts the Zero Delay Mode to precisely the use it is intended for. *Id.* at ¶ 223; Si5345 Manual at 44.

## **5. Claim 12**

Lockwood similarly would have motivated a skilled artisan to modify Altera such that “the transmitter side clock signal and the receiver side clock signal have the same frequency and different phases.” Ex. 1002 at ¶¶ 225-231.

As discussed with respect to claim 11, SyncE solutions require accurate “clock synchronization.” *Id.* at ¶ 226; Ex. 1004 at 2. As explained with respect to claim 1, in Altera the receiver side clock signal (rx\_recov\_clk) is generated when the receiver side “PHY IP cores recover the receiver (RX) clocks from their

respective 1G/10 Gbps Ethernet ports.” *Id.* at 3. The receiver side clock (rx\_recov\_clk) is then transmitted to the Si5345 PLL. *Id.* The purpose of the Si5345 PLL is to “generate output clocks that are both frequency and phase locked to its selected input clock.” Ex. 1006 at 17. “This stabilized clock is used to feed the FPGA’s serial transmitter (TX) PLL in sync with the master Ethernet port’s clock frequency to realize a complete synchronization loop.” Ex. 1004 at 3.

Altera also shows a single clock from the fPLL (sys\_tx\_master\_clk) that is used for both MAC and PCS functions. Ex. 1002 at ¶ 226. A POSA would understand that the fPLL shown is configured such that the resulting transmitter side clock signal frequency matches the receiver side clock signal frequency. *Id.* at ¶¶ 227-228. But the phases of the receiver-side clock signal (rx\_recov\_clk) and the transmitter side clock signal (sys\_tx\_master\_clk) will not necessarily have different phases. However, a POSA would understand that there are components in Altera that can be invoked to ensure that the phases of those clocks are different. *Id.*

For example, Altera includes an fPLL that generates the sys\_tx\_master\_clk. *Id.* at ¶ 229. That fPLL can be programmed to introduce a phase offset. Ex. 1005 at 358 (“The programmable phase shift feature allows the PLLs to generate output clocks with a fixed phase offset.”); *see also* Ex. 1017 at 1 (“Fractional PLLs use divide counters and different voltage-controlled oscillator (VCO) taps to perform frequency synthesis and phase shifts. For example, you can reconfigure the counter

settings and dynamically phase-shift the fractional PLL output clock in the PLLs of 28-nm devices . . . You can use these fractional PLL components to update the clock frequency, fractional PLL bandwidth, and phase shift in real time, without reconfiguring the entire FPGA.”). Through phase adjustment in the fPLL, the transmitter and receiver side clocks have the same frequency and different phase. Ex. 1002 at ¶¶ 229-230.

#### **6. Claims 6-10**

Altera and Lockwood would make obvious claims 6-10, which depend from claim 1, for the same reasons described above. *Id.* at ¶ 232; *see also* Ground 1A (explaining how the limitations of claims 6-10 are taught by Altera).

#### **IX. CONCLUSION**

Petitioner respectfully requests that inter partes review of the '381 patent be instituted and that the challenged claims be canceled as unpatentable.

Dated: November 25, 2025

Respectfully Submitted,

/Meg E. Fasulo/

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Lead Counsel for Petitioner

## CERTIFICATE OF WORD COUNT AND TYPE STYLE

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Petition, excluding the table of contents, table of authorities, certificate of word count, and certificate of service, totals 13,813 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(1).

This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft Word in 14-point Times New Roman.

Dated: December 3, 2025

Respectfully Submitted,

*/Meg E. Fasulo/*

Meg E. Fasulo (Reg. No. 75,820)  
Lead Counsel for Petitioner

## CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on December 3, 2025, a complete and entire copy of the PETITION FOR INTER PARTES REVIEW OF CLAIMS 1-4 AND 10-12 OF U.S. PATENT NO. 11,575,381 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.100 ET SEQ. including exhibits and testimony relied upon were served on Patent Owner via FedEx overnight at the correspondence address of record for the subject patent, as included below:

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