

IPR2026-00151
U.S. Patent No. 11,575,381

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CITADEL SECURITIES LLC,
Petitioner,

v.

HFT SOLUTIONS, LLC,
Patent Owner.

Case No. IPR2026-00151

U.S. Patent No. 11,575,381

NOTICE OF WITHDRAWAL OF INDEFINITENESS DEFENSES

LIST OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 11,575,381
1002	Expert Declaration of Kevin B. Stanton, Ph.D.
1003	File History of U.S. Patent No. 11,575,381
1004	Synchronous Ethernet Solutions with Altera FPGAs and Silicon Labs Jitter-Attenuating PLLs (“Altera”)
1005	Altera Stratix V Handbook (“Stratix Handbook”)
1006	Any-Frequency, Any-Output Jitter-Attenuators/Clock Multipliers Si5345, Si5344, Si5342 Family Reference Manual, August 2015 (“Si5345 Manual”)
1007	A Low-Latency Library in FPGA Hardware for High-Frequency Trading (HFT) by John W. Lockwood et al., 2012 IEEE 20th Annual Symposium on High-Performance Interconnects (September 2012), https://doi.org/10.1109/HOTI.2012.15 (“Lockwood”)
1008	Plaintiff HFT Solutions’ Response in Opposition to Defendant Citadel Securities’ Motion to Dismiss
1009	Declaration of Mina Ching regarding website of Altera White Papers
1010	Declaration of Mina Ching regarding website of Stratix V Device Handbook
1011	Declaration of Mina Ching regarding website of Si5345/44/33 Data Sheet
1012	Patent Owner’s Initial Infringement Contentions for the ’381 Patent
1013	Altera and IDT Synchronous Ethernet Solution for ITU-T G.8262
1014	“The Race to Zero Latency for High Frequency Trading” by Saul Sahoo

EXHIBIT NO.	DESCRIPTION
1015	U.S. Patent No. 10,169,814
1016	High-Frequency Trading, A Practical Guide to Algorithmic Strategies and Trading Systems by Irene Aldridge (2013)
1017	Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig Megafunctions, Application Note AN-661-3.0, Altera Corporation, November 2013
1018	Exploring Algorithmic Trading in Reconfigurable Hardware by Stephen Wray (2010)
1019	HDL Chip Design, A practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog by Douglas J. Smith, Doone Publications (1999)
1020	UltraScale Architecture Clocking Resources – User Guide, Xilinx, April 9, 2018
1021	Chip Hall of Fame: XC2064 FPGA, IEEE Spectrum, June 30, 2017
1022	List and comparison of FPGA companies by Jeff Johnson, FPGA Developer, July 15, 2011
1023	Understanding Clock Domain Crossing (CDC) Checks and Techniques by Saurabh Verna, <i>et al.</i> , EE Times, December 24, 2007
1024	Phaselock Techniques by Floyd Gardner, Third Edition (2005)
1025	Interactive Brokers’ Founder Changed Trading Forever. What He Sees Next by David Wignall, Barrons (October 2, 2025)
1026	Wall Street’s Quest to Process Data at the Speed of Light by Richard Martin, Rubinow (April 21, 2017)
1027	FPGA accelerated low-latency market data feed processing by Gareth W. Morris, <i>et al.</i> , 17 th IEEE Symposium on High Performance Interconnects (2009)
1028	The Once and Future Internet by Daniel Svensson, Design Lines (May 1, 2001)

EXHIBIT NO.	DESCRIPTION
1029	An Introduction to Synchronized Internet, Embedded (March 3, 2009)
1030	Design of Control Systems by A. Frank D’Souza, Prentice-Hall (1988)
1031	Clock Networks and PLLs in Stratix V Devices, Altera (May 6, 2013)
1032	<i>HFT Solutions, LLC v. Citadel Securities, LLC</i> , No. 24-cv-13213 (N.D. Ill.) (“ <i>HFT v. Citadel Securities</i> ”), D.I. 70 (Jan. 23, 2026)
1033	Northern District of Illinois Local Patent Rules
1034	<i>HFT v. Citadel Securities</i> , D.I. 34
1035	Plaintiff HFT Solutions, LLC’s Initial Disclosures (<i>HFT v. Citadel Securities</i>)
1036	Defendant Citadel Securities, LLC’s Initial Disclosures (<i>HFT v. Citadel Securities</i>)
1037	Matthew G. Sipe, <i>Patent Law 101: The View from the Bench</i> , 80 GEO. WASH. L. REV. 21 (April 2020)
1038	Docket Navigator Analytics (Motion Success by Year, National)
1039	Docket Navigator Analytics (Time to Trial, Northern District of Illinois)
1040	<i>HFT Solutions, LLC v. Jump Trading, LLC</i> , No. 24-cv-13214 (N.D. Ill.) (“ <i>HFT v. Jump Trading</i> ”), D.I. 30-1 (Apr. 21, 2025)
1041	<i>HFT v. Citadel Securities</i> , D.I. 46 (Aug. 29, 2025)
1042	<i>HFT v. Jump Trading</i> , D.I. 42 (Sept. 2, 2025)
1043	<i>HFT v. Citadel Securities</i> , D.I. 52 (Oct. 28, 2025)
1044	Letter from Kelson to Chang (Dec. 26, 2025)
1045	<i>HFT v. Citadel Securities</i> , D.I. 66 (Jan. 22, 2026)
1046	U.S. Patent No. 10,931,286

EXHIBIT NO.	DESCRIPTION
1047	M. Fasulo Email re Indefiniteness Claims

Petitioner Citadel Securities LLC hereby notifies the Director that, in the parallel district court proceedings between Petitioner and Patent Owner HFT Solutions, Citadel Securities has withdrawn its indefiniteness defenses regarding the '381 patent. *See* Ex. 1047. Citadel Securities will not argue in the parallel district court litigation that any asserted claim of the '381 patent is indefinite.

Patent Owner's argument regarding Rule 104(b)(3) is therefore moot. *See* Patent Owner's Preliminary Response, Paper 10, at 22-24. Citadel Securities respectfully submits that its now-withdrawn indefiniteness arguments do not provide a basis for denial of institution.

Dated: March 13, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies, that on this 13th day of March, 2026, the foregoing document is being served by electronic mail (e-mail) on counsel of record for Patent Owner as follows:

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