

**UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION**

HFT SOLUTIONS, LLC,)	
)	
Plaintiff,)	
)	Case No. 1:24-cv-13213
v.)	
)	Judge Sharon Johnson Coleman
CITADEL SECURITIES LLC,)	
)	
Defendant.)	
)	

MEMORANDUM OPINION AND ORDER

Plaintiff HFT Solutions, LLC (“HFT”) brought this action against Defendant Citadel Securities LLC (“Citadel”) alleging that Citadel infringed three of its patents. Citadel now moves to dismiss HFT’s Complaint [1] under Federal Rule of Procedure 12(b)(6) for failure to state a claim, maintaining that HFT’s asserted patent claims are patent-ineligible under 35 U.S.C. § 101. For the following reasons, the Court denies Citadel’s motion to dismiss HFT’s Complaint [30].

BACKGROUND

The following facts are presumed to be true for the purpose of resolving this motion. HFT is the owner of U.S. Patent Nos. 10,931,286 (the “286 Patent”), 11,128,305 (the “305 Patent”), and 11,575,381 (the “381 Patent” and, together with the ‘286 Patent and the ‘305 Patent, the “Patents”). (Dkt. 1) ¶¶ 2–4. According to the shared description in the Patents, the claims relate generally to “field programmable gate array” (“FPGA”) systems. FPGAs are microchips that facilitate rapid data processing within computer programs by distributing individual computations across “a single chip that has massive fine-grained parallelism,” (Dkt. 1-3) 1:40–42. In other words, the FPGA breaks up

complex computer program into several individual, simple computations, which it then carries out simultaneously on the same chip to improve data processing time.

HFT's Patents address a technological issue that causes "unwanted latency" (meaning unwanted delay in data processing) in FPGAs. *See id.* 1:53–56. When they receive an incoming (or "receiving side") clock signal, FPGAs are programmed to synchronize the outgoing "transmitting side" clock signal with the "phase" of the incoming signal. The "phase" refers to where the clock is within a time interval; for example, if the clock measures time in seconds, its phase refers to how far along the clock is from reaching the next second (half a second, three-fourths of a second, etc.). The prior art sought to synchronize the signals in the FPGA by including a "clock domain crossing" ("CDC") circuit. *Id.* 1:46–48. The extra circuitry "inherently add[s] a delay to the processing that takes place in the FPGA" due to the additional steps the CDC performs to match the phases. *Id.* 1:48–49. HFT's FPGA system is designed to minimize that delay by removing the CDC component and adding a "phase locked loop." *See* (Dkt. 1-1) 1:65–2:3. A phase locked loop is "an external phase controller providing phase matching between a receiver clock and a transmitter clock." (Dkt. 1-2) 2:4–5. In simpler terms, the phase locked loop adjusts the phase of the outgoing clock signal to match the phase of the incoming clock signal. This ensures that the FPGA's data processing remains continuously phase-synchronized between the two clocks, reducing the time spent aligning the signals.

Solving this problem is critical in the context of "high-frequency trading." High-frequency trading is a practice in the financial industry in which trades are carried out in a short timespan to seize on momentary favorable market prices and "provide a superior market return." (Dkt. 1) ¶ 6. Successful high-frequency trading strategies "fundamentally rely on being able to execute trades faster, sometimes microseconds or nanoseconds faster than competitors." *Id.* The trades include timestamps that are "accurate to the microsecond such that even small delays may present a large problem." (Dkt. 1-3) 1:50–52. Traders use FPGAs for their high processing speeds to execute these trades as quickly

as possible. When the FPGA experiences delay in processing, traders can miss out on favorable market prices where those prices shift faster than the trade can be completed. HFT's claimed systems are programmed to receive streams of incoming market data and transmit trading data, using the phase locked loop to minimize latency and align the timing of the clock signals in its data processing. *See* (Dkt. 1-1) 30:31–33.

Citadel engages in high-frequency trading and utilizes FPGA systems with phase locked loops for their rapid data processing. (Dkt. 1) ¶ 8; (Dkt. 1-4); (Dkt. 1-5); (Dkt. 1-6). HFT now brings this action against Citadel alleging that Citadel configured its FPGA systems in a manner that infringes HFT's Patents.

LEGAL STANDARD

To survive a Rule 12(b)(6) motion to dismiss for failure to state a claim, a complaint “must contain sufficient factual matter ... to ‘state a claim to relief that is plausible on its face.’” *Ashcroft v. Iqbal*, 556 U.S. 662, 678, 129 S.Ct. 1937, 173 L.Ed.2d 868 (2009) (quoting *Bell Atlantic Corp. v. Twombly*, 127 S. Ct. 1955, 1960 (2007)). A complaint is facially plausible when the plaintiff alleges “factual content that allows the court to draw the reasonable inference that the defendant is liable for the misconduct alleged.” *Id.* When considering a motion to dismiss a complaint, courts accept all well-pleaded factual allegations as true and draws all reasonable inferences in favor of the plaintiff. *Erickson v. Pardus*, 127 S. Ct. 2197, 2200 (2007) (per curiam).

DISCUSSION

HFT's Patents include two types of claims: method claims and system claims. Method claims seek to patent the sequence of steps in a process, while system claims seek to patent a tangible assembly of components. *See In re Kollar*, 286 F.3d 1326, 1332 (Fed. Cir. 2002) (distinguishing between “a claim to a product, device, or apparatus, all of which are tangible items, and a claim to a process, which consists of a series of acts or steps”). Regardless of the type of claim, the analysis of patent-

eligibility under § 101 is the same. Therefore, courts often analyze one claim as “representative” of a group of several types of claims, where “the claims at issue are ‘substantially similar and linked to the same’ ineligible concept.” *Mobile Acuity Ltd. v. Blippar Ltd.*, 110 F.4th 1280, 1290 (Fed. Cir. 2024) (internal citation omitted). It is important to determine whether it is appropriate to designate a representative claim before proceeding with the eligibility analysis, because the Court’s eligibility findings “extend to claims for which they are representative, and correspondingly do *not* extend to claims they do *not* represent.” *Id.* at 1291.

Citadel asserts that claim 1 of the ‘381 Patent, claim 1 of the ‘286 Patent, and claim 1 of the ‘305 Patent are representative of each of their respective Patents as a whole, because they “closely resemble [the remaining claims] and are based on the same abstract idea.” (Dkt. 30) at *14. HFT disputes this characterization. Citadel bears the initial burden to make a *prima facie* showing that the claims are “substantially similar and linked” to the same ineligible concept. *Mobile Acuity*, 110 F.4th at 1290. If it succeeds in that showing, the burden shifts to HFT to show why the eligibility of the supposedly representative claim “cannot fairly be treated as decisive of the eligibility of all claims in the group.” *Id.*

Claim 1 of the ‘381 Patent recites “[a] method for processing a first serial data stream, using a field programmable gate array system, to generate a second serial data stream” through receiving and transmitting clock signals. (Dkt. 1-3) 28:18–20. Claim 1 of the ‘286 Patent recites “[a] method for processing a first serial data stream comprising market data, using a field programmable gate array system, to generate a second serial data stream comprising order entry data.” (Dkt. 1-1) 28:9–12. Claim 1 of the ‘305 Patent recites a claim for the “field programmable gate array” system itself. (Dkt. 1-2) 30:8–10. The remaining claims of the Patents are dependent on each claim 1, the only independent claims in the Patents. A majority of the remaining claims in the ‘286 Patent claim some variation of “[t]he method of claim 1.” *See* (Dkt. 1-1) 29:1–30:50. The only claims that do not

reference claim 1 refer back to claim 11, another dependent claim directed to “[t]he method of claim 1, wherein the first amount of data streams is the same as the second amount of data streams.” *Id.* 29:44–46. The claims in the ‘381 and ‘305 Patents are similarly dependent on each respective claim 1. The dependence on each claim 1 supports Citadel’s contention that the claims resemble each other and are linked to the same concept.

Importantly, HFT puts forth no argument as to why claim 1 of each of the Patents cannot fairly represent the rest, except that “a cursory glance ... shows they do not resemble each other.” (Dkt. 35) at *15. HFT has no rebuttal Citadel’s *prima facie* showing of representativeness. Courts have found, for example, that patentees present “non-frivolous” arguments challenging representativeness where they articulate why a claim limitation not found in a representative claim has “distinctive significance” that would have a “material impact on the eligibility analysis.” *See Mobile Acuity*, 110 F.4th at 1290. But HFT does not explain how the patent-eligibility analysis of each claim 1 differs across the remaining claims, and its infringement allegations only refer to claim 1 of each Patent. *See* (Dkt. 1) ¶¶ 23 (Count 1), 10 (Count 2), 23 (Count 3).

Accordingly, the Court finds that Citadel has met its burden and will proceed in its analysis treating claim 1 of each Patent as representative of the Patents as a whole.

I. Patent Eligibility

“Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof” may obtain a patent for that subject matter. 35 U.S.C. § 101. Whether a subject matter is patent-eligible under § 101 is a “threshold test” before the patentee can enforce its patent rights. *Bilski v. Kappos*, 561 U.S. 593, 602, 130 S.Ct. 3218, 3225, 177 L.Ed.2d 792 (2010). The eligibility determination “turns on whether the claim elements or the claimed combinations are well-understood, routine, and conventional, which is a question of fact.” *Buffalo Patents, LLC v. Motorola Mobility LLC*, No. 22-cv-00621, 2023 WL 4594945,

at *5 (N.D. Ill. July 18, 2023) (Kocoras, J.). Accordingly, “only when there are no factual allegations that, taken as true, prevent resolving the eligibility question as a matter of law” is it appropriate for a court to determine patent eligibility at the Rule 12(b)(6) stage. *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121, 1125 (Fed. Cir. 2018). As every patent is presumed to be issued properly, *see* 35 U.S.C. § 282(a), Citadel must provide clear and convincing evidence that the covered subject matter is patent-ineligible. *Accenture Glob. Servs., GmbH v. Guidewire Software, Inc.*, 728 F.3d 1336, 1346 (Fed. Cir. 2013) (internal citation omitted).

The U.S. Supreme Court laid out a two-step framework for evaluating patent-eligibility in *Alice Corp. Pty. Ltd. v. CLAS Bank Int’l*, 573 U.S. 208, 134 S.Ct. 2347, 189 L.Ed.2d 296 (2014). First, a court must determine “whether the claims at issue are directed to a patent-ineligible concept.” *Id.* at 217. Patent-ineligible concepts include “laws of nature, physical phenomena, and *abstract ideas*.” *Diamond v. Chakerabarty*, 447 U.S. 303, 309, 100 S.Ct. 2204, 2207, 65 L.Ed.2d 144 (1980) (emphasis added). If the claims are directed to a patent-ineligible concept, the second step is for the court to “consider the elements of each claim both individually and as an ordered combination to determine whether the additional elements transform the nature of the claim into a patent-eligible application.” *Id.* The second step entails identifying an “‘inventive concept,’ or some element or combination of elements sufficient to ensure that the claim in practice amounts to ‘significantly more’ than a patent on an ineligible concept.” *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245, 1255 (Fed. Cir. 2014) (quoting *Alice*, 573 S.Ct. at 217).

II. Abstract Idea

Citadel argues that HFT’s claims are directed to the abstract idea of “synchronizing data processing with a clock” by “moving data through conventional computer processing components in synchronization with clock signals.” (Dkt. 30) at *6. HFT counters that Citadel’s characterizations of its asserted claims as “generic data-clock synchronization” and “mere data manipulation” are a “gross

oversimplification,” because HFT’s claims are directed to a “specific FPGA system architecture” rather than an abstract idea. (Dkt. 35) at *5, 8. The Court agrees.

At a high level, “all inventions ... embody, use, reflect, rest upon, or apply laws of nature, natural phenomena, or abstract ideas.” *Mayo Collaborative Servs. v. Prometheus Lab’s, Inc.*, 566 U.S. 66, 71, 132 S. Ct. 1289, 1293, 182 L. Ed. 2d 321 (2012). The Supreme Court so far has not articulated definitively when a claim constitutes nothing more than an “abstract idea.” *See Alice*, 573 U.S. at 221 (declining to “to delimit the precise contours of the ‘abstract ideas’ category”). Without a precise delineation between an invention and an “abstract idea,” courts performing the *Alice* step one analysis have found it “sufficient to compare claims at issue to those claims already found to be directed to an abstract idea in previous cases.” *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1334 (Fed. Cir. 2016). This Court will proceed with that approach and analyze HFT’s claims by examining analogous cases.

Claims related to computer technology are often found patent-eligible where they recite specific methods and systems for improving functionality or solving technological issues. In *Enfish, LLC v. Microsoft Corp.*, the Court of Appeals for the Federal Circuit affirmed the patent-eligibility of claims directed to a self-referential logical model for a computer database. 822 F.3d at 1330, 1336. The claimed invention enabled faster searching and more effective data storage by using one self-referential table of data, compared to the prior art “relational” systems which used multiple tables. There the claims were “not simply directed to *any* form of storing tabular data,” but were specifically directed at a distinct system that functioned differently and provided “a specific improvement to the way computers operate.” *Id.* At 1337–38. The court rejected defendant’s position that the claims were directed to the “concept of organizing data” into a table, as “describing the claims at such a high level of abstraction and untethered from the language of the claims all but ensures that the exceptions to § 101 swallow the rule.” *Id.*

In *Packet Intel. LLC v. NetScout Sys., Inc.*, claims directed to “a granular, nuanced, and useful classification of network traffic” were patent-eligible. 965 F.3d 1299, 1308 (Fed. Cir. 2020). The claims recited a method for monitoring and classifying streams of information known as “connection flows” across computer networks. *Id.* at 1303. The method used a “parser” system to extract and classify connection flows as belonging to their particular “conversational” flow. *Id.* at 1307. The method improved network traffic and solved a technical problem in the prior art, which “could not identify disjointed connection flows as belonging to the same conversational flow.” *Id.* at 1308. Rather than being directed at the abstract idea of “the collection, comparison, and classification of information,” the claims were directed at “specific technological features functioning together” that provided a specific technological solution, not an abstract result. *Id.* at 1310.

Uniloc USA, Inc. v. LG Elecs. USA, Inc. is particularly analogous to this case. The claimed invention in *Uniloc* improved the function of prior art communication systems by adding an additional data field to each transmitted message, allowing the systems to dispatch messages while simultaneously “polling” for secondary stations in the network that could receive them. 957 F.3d 1303, 1305 (Fed. Cir. 2020). This enhanced “the normal operation of the communication system itself” by “overcom[ing] a problem specifically arising in the realm of computer networks.” *Id.* at 1308. The claims were patent-eligible because they were directed to a specific “improvement to computer functionality, namely the reduction of latency experienced ... in communication systems,” not an abstract idea. Distinguishing from patent-ineligible claims, the Federal Circuit explained that the claims at issue did not “merely recite generalized steps to be performed on a computer using conventional computer activity,” but were directed to a certain modification to the composition of prior communication systems. *Id.*

Like the logical model in *Enfish*, the classification method in *Packet Intel.*, and the communication systems in *Uniloc*, the claims here are directed to a specific technological improvement.

HFT claims methods and systems for more efficiently synchronizing clock signals and solving the latency issue presented in the prior art—namely, by utilizing a phase-locked loop in conjunction with other components to expedite data processing in the FPGA. The system in claim 1 of the ‘305 Patent details the specific system architecture of the FPGA, including the configuration of data pins on its interface; a deserializer; a serializer with a phase control circuit; and circuitry connecting these components. *See* (Dkt. 1-2) 28:9–29:48. The methods in each claim 1 of the ‘286 and ‘381 Patents recite specific methods for processing and generating certain data streams in the FPGA system. *See* (Dkt. 1-1) 28:9–29:15; (Dkt. 1-3) 28:18–29:48. The claims plainly recite more than the abstract idea of “mere manipulation of data” and generic steps to perform “synchronizing data processing with a clock.” *See SRI Int’l, Inc. v. Cisco Sys., Inc.*, 930 F.3d 1295, 1303 (Fed. Cir. 2019) (affirming the patent-eligibility of a method claim for monitoring and analyzing network events where the claims recited not merely a well-known practice, but a “specific technique” to “solve a technological problem”).

The Court agrees that to characterize HFT’s claims as the “manipulation of data” is reductive. The distinctive systems and methods recited in HFT’s claims distinguish them from claims that add nothing more to the abstract manipulation of data. *See, e.g., SAP America, Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1163 (Fed. Cir. 2018) (claims were directed to the abstract idea of “performing statistical analysis” where the recited method consisted of nothing more than analyzing information using generic mathematical formulas and displaying the results). Citadel has not shown by clear and convincing evidence that HFT’s claims are directed to an “abstract idea.” Therefore, HFT’s claims are patent-eligible.

III. Inventive Concept

Even if this Court found that HFT’s asserted claims *are* directed to an abstract idea, under *Alice* step two, HFT’s claims are still patent-eligible if they recite an “inventive concept.” *See Alice*,

573 U.S. at 217; *see also* *Diamond v. Diehr*, 450 U.S. 175, 192, 177, 101 S.Ct. 1048, 67 L.Ed.2d 155 (1981)¹ (affirming patent-eligibility of a claim containing a well-known mathematical formula where the claim “implements or applies that formula in a structure or process which, when considered as a whole, is performing a function which the patent laws were designed to protect”). The Court finds that HFT’s claims would survive this step as well.

A claim directed at an abstract idea is patent-ineligible if it involves nothing more than “well-understood, routine, [and] conventional activities previously known to the industry.” *Alice*, 573 U.S. at 225. In the *Alice* step two analysis, courts consider the claim elements both individually and “as an ordered combination” to determine whether additional elements “transform the nature of the claim” into an “inventive concept.” *See id.* at 217. In the context of computer technology, the claims must “do more than simply instruct the practitioner to implement the abstract idea” on a generic computer. *Id.* at 225.

The asserted claims here involve multiple added components specifically aimed at improving clock synchronization in conventional FPGA systems. *See SRI Int’l*, 930 F.3d at 1304. HFT’s Patents explain that FPGAs conventionally include CDC circuits for phase synchronization, which “inherently add a delay to the processing that takes place in the FPGA.” *See* (Dkt. 1-1) 1:39–42. The claimed systems and methods serve to eliminate the CDC circuit and enhance the operation of the FPGA through adding a phase lock loop, among other specified components. Taking the facts asserted in the Patents as true, the solution described in the claims is not well-understood, routine, or conventional. *See Packet Intel.*, 965 F.3d at 1308 (affirming patent-eligibility where the “combination of elements in the claims” were not shown to have been “regarded as conventional, routine, or well-known by a skilled artisan at the time of the invention”).

¹ Though *Diehr* was decided before the Supreme Court’s decision in *Alice*, the *Alice* Court relied on *Diehr* in its reasoning that a computer-implemented process is patent-eligible where the claims “improve[] an existing technological process.” *Alice*, 573 U.S. at 223, 134 S. Ct. at 2358.

Citadel argues that the asserted claims must fail at *Alice* step two because HFT's Patents "add nothing" to an abstract idea "except generic and conventional components" (including FPGAs, phase lock loops, phase control circuits, and phase detectors) such that they constitute an "inventive concept." *See* (Dkt. 30) at *11–13. The fact that individual components named in HFT's claims are "known" does not render those claims patent-ineligible. Even if the claims incorporate well-known components, a claim may still recite an inventive concept "in the non-conventional and non-generic arrangement of known, conventional pieces." *BASCOM Glob. Internet Servs., Inc. v. AT&T Mobility LLC*, 827 F.3d 1341, 1350 (Fed. Cir. 2016). As explained, HFT's claims lay out a novel configuration of components aimed at improving the FPGA's data processing. Citadel has not argued that there is only one way of synchronizing a clock signal, and in fact the asserted claims here do not preempt *every* way of doing so. The Patents themselves describe another method: the prior art of using CDCs. Thus, even if HFT's claims were directed at the idea of synchronizing a clock signal, HFT recites an inventive concept to transform the claims into a patentable invention. *See BASCOM*, 827 F.3d at 1350. HFT's claims are directed at a discrete order of elements and are not merely a "drafting effort designed to monopolize [an abstract idea]," but serve to "improve[] an existing technological process." *Alice*, 573 U.S. at 220, 223.


At most, there is a factual dispute as to whether the asserted patents involve "well-understood, routine, conventional activit[ies]." That precludes granting Citadel's motion to dismiss. *See Mayo*, 566 U.S. at 73; *Buffalo Patents*, 2023 WL 5858921, at *4 (denying motion to dismiss where there was a factual dispute about whether the asserted patents involve an inventive concept).

CONCLUSION

For the foregoing reasons, the Court denies Citadel's motion to dismiss HFT's Complaint [30].

IT IS SO ORDERED.

Date: 12/1/2025

Entered: 

SHARON JOHNSON COLEMAN
United States District Judge