



Christina Belisario
Research Coordinator
Morrison Foerster
12531 High Bluff Drive
Suite 200
San Diego, CA 92130-2040
USA

21st November 2025

Dear Christina

According to our records, this item was receipted by The British Library on the 10th of April 2006 and would have been available for public use from that date.

A copy of the cover page with date stamp indicating the date of availability has been attached together with the copyright page, table of contents and article itself.

Please note that we can only provide the date that the British Library made this item available for public use; for the actual date of publication, please contact the publisher.

Yours sincerely

A handwritten signature in black ink, appearing to read "Ziaad Khan", with a long horizontal flourish extending to the right.

Ziaad Khan

British Library Research Service
Tel: +44 (0) 20 412 7903 research@bl.uk

THIN FILM TRANSISTOR
TECHNOLOGIES (TFTT VII)

03/04/06

7871889

BOSTON SPA

LS23 7BQ

PROCEEDINGS- ELECTROCHEMICAL SOCIETY PV



6695.400000

2004: Number 15

STM

Edited by
Y. Kuo

BRITISH LIBRARY
DOCUMENT SUPPLY CENTRE

10 APR 2006

CONFERENCE
INDEXED

PV 2004-15

THIN FILM TRANSISTOR TECHNOLOGIES (TFTT VII)

Proceedings of the International Symposium

Editor

Y. Kuo
Texas A&M University
College Station, Texas, USA



*Sponsoring Divisions:
Electronics and Dielectric Science & Technology*

Proceedings Volume 2004-15



THE ELECTROCHEMICAL SOCIETY, INC.
65 South Main St., Pennington, NJ 08534-2839, USA

Copyright 2005 by The Electrochemical Society, Inc.
All rights reserved.

This book has been registered with Copyright Clearance Center, Inc.
For further information, please contact the Copyright Clearance Center,
Salem, Massachusetts.

Published by:

The Electrochemical Society, Inc.
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

Library of Congress Catalogue Number: 2005920618

ISBN 1-56677-458-6

Printed in the United States of America

TABLE OF CONTENTS

PREFACE	iii
Poly-Si TFTs from Laser Crystallization Methods	
CW Laser Lateral Crystallization (CLC)* N. Sasaki	1
Novel Phase-Modulator for ELA-Based Lateral Growth of Si Y. Taniguchi, M. Jyumonji, H. Ogawa, M. Hiramatsu, and M. Matsumura	18
An Advanced Sample Structure for Excimer Laser Crystallization M. Hiramatsu, H. Ogawa, M. Jyumonji, T. Katou, N. Akita, and M. Matsumura	30
The Electrical Characteristics of the Poly-Si TFTs fabricated by 2-Dimensional Grain Growing ELA method I.-H. Song, H.-S. Shin, and M.-K. Han	38
A New Dual L-Gate Structure of Poly-Si TFT for Suppressing the Kink Effect in SLS/CW Laser Method S.-H. Jung, H.-S. Shin, and M.-K. Han	44
Poly-Si TFTs from Non Laser Crystallization Methods	
Reliability Study of MILC Poly-Si TFTs on Plastic Substrates Using PostFlex Transfer Process H. Li and S. Fonash	49
Reduction of the Leakage Current of Thin-Film Transistor on Metal-Induced Laterally Crystallized Polycrystalline Silicon Z. Meng, C. Wu, S. Xiong, X. Shi, H.S. Kwok, and M. Wong	57
TFTs Gate Dielectrics, Doping, Structures, etc.	
Low-Temperature Microwave Plasma Oxidation for Gate Dielectrics of Poly-Si TFTs using High-Density Surface Wave Plasma* K. Azuma	63
Fabrication and characterization of n- and p-channel poly-Si TFTs by sputtering deposition of ultra thin gate SiO ₂ films T. Serikawa, M. Miyashita, Y. Uraoka, and T. Fuyuki	74
Ion Shower Doping of Polysilicon Films on Plastic Substrates for Flexible TFT Arrays J. Kim, W.-S. Hong, S. Lee, D.-Y. Kim, J. S. Jung, J.-Y. Kwon, and T. Noguchi	80

* Invited Paper

A Simple CMOS Self-Aligned Double-Gate Poly-Si TFT Technology Z. Xiong, H. Liu, C. Zhu, and J. K. O. Sin	87
Influence of Channel Position on Characteristics of p-Channel c-Si TFT Inside a Location-Controlled Grain V. Rana, R. Ishihara, I. Andel, Y. Hiroshima, D. Abe, S. Inoue, T. Shimoda, J.W. Metselaar, and K. Beenakker	92
High Performance P-Channel Schottky Barrier Thin-Film Transistors with PtSi Source/Drain M.-H. Lee, T.-Y. Huang, K.-L. Yeh, and H.-C. Lin	99
Devices and Modeling	
Hot-Carrier Instability in N- and P-Channel Poly-Si Tofts* H. Tango, M. Suganuma, G. Usami and Y. Nogami	104
Switch-on Undershoot Current Observed in Thin Film Transistors F. Yan, P. Migliorato, and R. Ishihara	112
Modelling of Source Gated Transistors in Amorphous Silicon F. Balon and J. M. Shannon	119
An Investigation of the Electrically Active Defects in poly-Si Thin Film Transistors M. Exarchos, G. J. Papaioannou, D. N. Kouvatsos, and A. T. Voutsas	125
Simulation of Twin Boundary Effect on TFT Characteristics Y. Mo, F. Yan, P. Migliorato, and R. Ishihara	130
Circuits and Systems	
Thin Film Transistor Models for Circuit Simulation* B. Iñiguez, M. S. Shur, T. A. Fjeldly, and T. Ytterdal	136
TFT Mobility Requirement for AMOLED HDTVs* O.-K. Kwon	146
System Displays and TFT Device and Process Technologies* H. Abe	159
High Performance TFT Circuits for all-Integrated Systems on Stainless Steel Foils M. Troccoli, T. Afentakis, T. H. Chuang, Y. L. Chang, M. Hatalis, A. P. Voutsas, J. W. Hartzell, and V. Chouvardas	166

* Invited Paper

Materials and Substrates

Oxide Semiconductors for Flexible Electronics*	178
P. F. Carcia, R. S. McLean, I. Malajovich, and M. H. Reilly	
Thin-Film Transistors Based on Spin-Coated Chalcogenide Semiconductor Channels*	189
D. B. Mitzi, M. Copel, C. E. Murray, L. Kosbar, and A. Afzali	
Hydrogen-Induced Defects in Poly-Silicon Thin Films Observed by Raman Spectroscopy	200
K. Kitahara, Y. Ohashi, T. Yamada, and A. Moritani	
Analysis of Transfer Mechanism in Surface Free Technology by Laser Annealing / Ablation (SUFTLA)*	206
S. Inoue, M. Kasuga, S. Utsunomiya, and T. Shimoda	
High Mobility Top-Gate Micro-Crystalline Silicon TFTs Processed at Low Temperature (<200°C)	215
A. Saboundji, N. Coulon, C. Simon, T. Mohammed-Brahim, O. Bonnaud	
Polysilicon TFTs on Plastic	221
J. Y. Chen	
VHF PECVD Micro-crystalline Silicon Bottom Gate TFT With Thin Incubation Layer	232
J. Li, C. Wu, X. Zhang, Z. Meng, J. Liu, S. Zhao, Y. Zhao, S. Xiong, L. Zhang, and J. Jang	

Organic TFTs

Semiconducting Properties of Pentacene Thin Films Studied by Complex Impedance, Surface Mobility and Photo-induced Effects*	237
A. Toriumi, T. Yokoyama, T. Nishimura, T. Yamada, K. Kita, and K. Kyuno	
Bottom Contact Organic Thin-Film Transistors with Thiol-based SAM Treatment	249
M. Kawasaki, S. Imazeki, M. Ando, and M. Ohe	
Flexible QVGA Active Matrix Displays based on Organic Electronics*	257
F. J. Touwslager, H.E.A. Huitema, G. H. Gelinck, E. van Veenendaal, and P.J. G. van Lieshout	
Study of Organic Field-Effect Transistors from Poly-3-octylthiophene Solutions on Different Gate Dielectrics	263
M. Ploetner, S. Richter, P.-T. Nguyen, H. Heuer, A. Heinzig, T. Wegener, W. Plieth, and W.-J. Fischer	

* Invited Paper

New Applications and Film Preparation Methods

A Novel TFT-Driven Microchannel Electrophoresis Device for Proteins Separation and Identification Y. Kuo and H. H. Lee	270
Hydrogenated Amorphous Silicon Bipolar Junction Thin Film Transistors (a-Si:H B-TFTs) Y. Lei, Y. Kuo, and H. Nominanda	277
Highly pH Sensitive Suspended-Gate Silicon Thin Film Transistor (ISTFT) F. Bendriaa, F. Le Bihan, A.-C. Salaün, T. Mohammed-Brahim, and O. Bonnaud	284
High Dynamic Range Pixel Amplifier Architecture in Amorphous Silicon Technology for Diagnostic X-ray Imaging Applications G. Sanaie-Fard, R Sanaie-Fard, and K.S. Karim	289
New Pixel Circuit to Recover Threshold Voltage Shift in Amorphous Silicon TFT for Active Matrix OLEDs B.-H. You, H.-J. Lee, W.-J. Nam, H.-J. Lee and M.-K. Han	301
Low-Temperature Deposition of Poly-Si and SiGe Thin Films at 450°C and Fabrication of High Mobility TFTs Over 50 CM ² /VS* J.-i. Hanna, J. J. Zhang, J.-W. Lee, and K. Shimizu	308
AUTHOR INDEX	319
SUBJECT INDEX	323

HIGH PERFORMANCE TFT CIRCUITS FOR ALL-INTEGRATED SYSTEMS ON STAINLESS STEEL FOILS

M. Troccoli, T. Afentakis, T. K. Chuang, Y. L. Chang, M. Hatalis,
Display Research Laboratory, Lehigh University
16A Memorial Dr. East, Bethlehem, PA18015

Apostolos T. Voutsas, John W. Hartzell,
Sharp Laboratories of America, Camas, WA

Vasilios Chouvardas
Aristotle University of Thessaloniki, Dept. of Informatics, Greece

ABSTRACT

In an attempt to fabricate all inclusive systems we are presenting a study on several elements that would be used as building blocks for all-on-board integrated applications on stainless steel foils. These systems would include in the same substrate all or many of the components of a modern day electronic device such as PDA or cellular phone. We are reporting results on both digital and analog circuits on stainless steel foils. An extensive study on shift registers running at speeds greater than 1.0MHz is shown as well as oscillators operating at over 40 Mhz. Pixel circuits for driving organic light emitting diodes are presented as well as experimental OLED's on the same steel material substrate. The device technology of choice is that based on poly-silicon TFT technology as it has the potential of producing circuits with good performance and considerable cost savings over the established processes on quartz or glass substrates (amorphous Silicon a-Si:H or silicon on Insulator SOI).

1. INTRODUCTION

During the past decade, there has been an increased research and development effort towards the realization of highly integrated large area electronics, on flexible substrates. The main application targeted is displays and other matrix-based electronics, with focus on a systems-based approach. The appeal of flexible electronics lies in their capacity to realize novel circuits whose space / layout and mechanical restrictions do not permit the use of a rigid printed circuit board, and to utilize a roll-to-roll manufacturing process similar to a rolling photolithographic printing process, which can produce this type of circuits with a throughput 10-100 times higher than normal semiconductor processing. Displays are the preferred flexible electronic application because of the mechanical (robust, lightweight) and space saving advantages a conformal or foldable display has, and also because the specifications for pixel electronics such as thin film transistor (TFT) switches and current sources are relatively relaxed, compared to other high speed digital / analog electronics. However, a larger degree of system integration requires the incorporation of high performance digital and analog circuits for display driving and signal processing. A higher integration scale is highly desirable, because it is shown to increase system yield, since external connections - which are a substantial source of failure - are greatly reduced, and substantially decrease manufacturing costs.

The fabrication of highly integrated large area systems on flexible substrates with reasonable performance characteristics is - at this time - possible only with polysilicon. The high carrier mobility values that can be obtained with this approach, and the prospect of realizing highly efficient, low power CMOS circuitry are the two strongest assets of polysilicon TFT technology.

In order to realize monolithic flexible circuits, where all components are fabricated with the same process sequence on the substrate material, two distinct substrate materials can be used: (a) plastics and (b) thin metal foils. Other substrates, such as thin glass sheets, although flexible are still brittle and thus not suitable with the possible exception of use in specialized applications. The use of plastic substrates involves some serious issues, primarily spurring from the severely reduced thermal budget that can be tolerated. In this case, processing temperature should not be higher than about 200°C, and an ongoing effort is made to limit it in the 100°C - 150°C range. This is considerably lower than the approximate 400°C limit observed in low temperature polysilicon processing (LTPS) on glass substrates (such as Corning® 1737). An impact in device and circuit performance is usually observed from lowering temperatures in critical steps such as gate dielectric formation and contact anneal.

Good quality polysilicon TFTs have been fabricated on plastic substrates from the mid-1990s on [1]. This has been made possible in part by the continuous optimization of excimer laser crystallization equipment, which is the most suitable way of obtaining high mobility TFTs on plastics, where the thermal budget is severely constrained. Keeping processing temperatures at a maximum of 150°C, polysilicon TFTs with effective mobility values in the region of 60cm²/Vs have been fabricated on polyester substrates [2]. Higher quality devices (effective pmos mobility values around 170cm²/Vs and I_{ON}/I_{OFF} ratios of 10⁸) have been realized utilizing novel transfer processes from high temperature compatible, temporary substrates to permanent flexible ones [3,4].

Metal foils are largely immune to the problems affecting plastic substrates; stainless steel foils -for example- can tolerate temperatures above 1000°C, offering at the same time excellent resistance to corrosion and chemical attack and no water or oxygen absorption. During the late 1990s, excimer laser crystallization was used to produce high mobility (>100cm²/Vs) thin film transistors on steel foils for the first time [5]. Other crystallization approaches such as furnace annealing have also been utilized, but with significantly lower returns in device performance [6,7]. Progress has continued in the field, resulting in devices with mobility values higher than 200cm²/Vs and the fabrication of functional digital circuits for the first time on metal foils [8,9]. From the application viewpoint, thin metal foils have been recently utilized in the fabrication of active-matrix, a-Si TFT digital ink displays [10].

On this paper, we are presenting high-speed polycrystalline silicon thin film transistor digital circuits as well as all the elements needed for the fabrication of a display, representing some of the building blocks for such integrated systems. Both n-channel and p-channel excimer laser re-crystallized poly-silicon devices with effective mobility values in the region of 250cm²/Vs and 100cm²/Vs respectively, and ON vs. OFF current ratios at least seven orders of magnitude have been fabricated, and their characteristics are presented. Ring oscillators running at frequencies above 40MHz are described, along with static and dynamic shift registers, with maximum clock frequency exceeding 1.0MHz. The presented results indicate the potential of these circuits for possible row and column driving for displays or memory addressing. This paper outlines the fabrication and the performance of the above mentioned circuits first, followed by pixels circuits next, and finally the Organic Light Emitting Diodes (OLED's).

2. HIGH PERFORMANCE CIRCUITS

2.1 Circuit Fabrication

Type-304 Stainless steel foils, 100 μ m thick, were manually and chemically polished and cut to 100mm diameter wafer size substrates. The manual and chemical polishing step was developed and used in order to reduce the surface roughness of the untreated foils, which approached 1500 \AA . After polishing, an RMS value of surface roughness approaching 100 \AA was obtained.

After cleaning, the substrates were coated with an isolation layer of PECVD SiO₂, 750nm thick. The active amorphous Si film was PECVD deposited, crystallized with an Excimer Laser and patterned to form the TFT islands, 1000 \AA thick. The gate dielectric was PECVD silicon dioxide 1000 \AA thick, followed by a PECVD a-Si layer for the gate electrode. After these depositions, the gate electrode was n+ ion implanted and patterned, followed by the patterning of the gate dielectric and the drain / source region formation through p+ (BF₂) or n+ (P) ion implantation.

The drain and source TFT regions and poly-Si inter-connects were silicided using sputtered Ni and an in situ anneal at 400°C. A passivation oxide layer 3000 \AA thick was PECVD deposited and followed by the patterning of contact holes. In order to avoid aluminum hillocks that can lead to circuit failure, AlNi was selected as the most suitable metalization layer for this purpose. Aluminum and nickel were sputtered to a total thickness of 3000 \AA , then annealed in situ to form the alloy. After patterning the metal, the devices and circuits were measured.

2.2 Circuit Performance

Stand alone devices of various geometries were fabricated and tested, and their electrical characteristics are presented below. The minimum fabricated channel length was 2 μ m (minimum feature size). Figure 1 shows the I_{DS}/V_{GS} characteristics of two devices, taken at |V_{DS}| = 0.1V and 1.1V. Stand alone p- and n-type devices were measured, and their basic characteristics were recorded. Table 1 shows the average values of mobility, threshold voltage, inverse sub-threshold slope and off current for both types of gate oxide TFTs. For all devices, there is a difference between I_d(ON) and I_d(OFF) at least six orders of magnitude, which is one of the highest compared with previously published results.

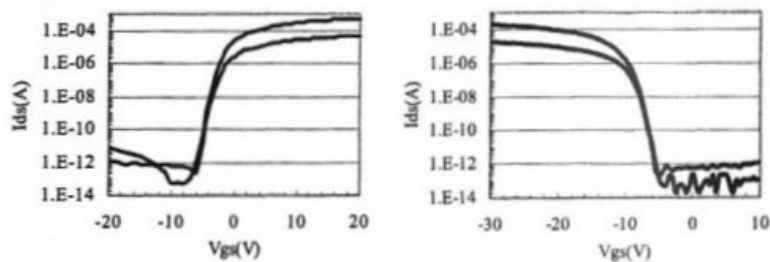


Fig. 1: Typical characteristics of PECVD oxide NMOS and PMOS devices at V_{ds}=0.1V and 1.1V (W/L=20/4)

Gate Oxide	Device (W/L=20/4)	Mobility (cm ² /Vs)	Vt (V)	SS (V/dec)	Ioff (A)
PECVD	NMOS	200	+1.4	1.4	1 pA
	PMOS	87	-9.8	2.4	0.1 pA

Table 1: Average values of PMOS and NMOS TFTs

A basic circuit for the evaluation of digital circuit performance is a ring oscillator (RO). The oscillators we have fabricated are composed of 19 CMOS inverter stages, and have buffered outputs. Both NMOS and PMOS devices have the same geometry 20 μ m/4 μ m. Figure 2 shows the RO frequency as a function of supply voltage. Powered with a supply voltage of 15V, its free running frequency was measured to be approximately 40.4MHz. This results in an average delay time of 1.302ns per inverter stage.

Architecture	f _{min} (kHz)	f _{max} (MHz)
Static	<10Hz	2.50
Dynamic	500Hz	1.50

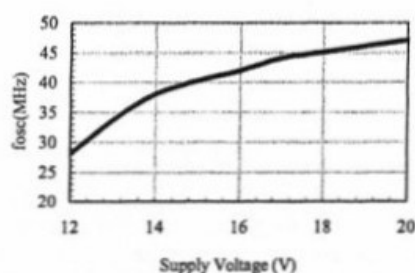


Table 2: Min. and max. speeds of SR's on steel vs. supply voltage

Fig. 2: Free-running frequency of RO

One of the most important memory and display driver circuits (for both active- and passive-matrix displays) is a shift register. Assuming the simplest driving scheme, the rows and the columns of the display matrix are activated one at a time, which is accomplished by the active shift register output (which can be high or a low signal) being shifted to the next bit, and eventually cycled to the register's input again.

Two types of shift registers have been designed and evaluated: a static, D-type latch-based design and a dynamic pass-gate gate design. Both are 10-bit, serial input, parallel output designs. Both are based on the clocked CMOS (C²MOS) logic architecture, which uses a non-overlapping pseudo two-phase clock signal for shift timing. The circuit schematics are shown in Figure 3; labels indicate the W/L ratios of the TFTs.

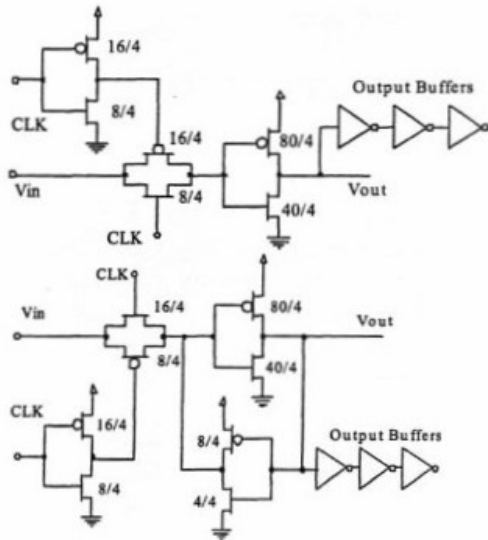


Fig. 3: One-half bit stage schematics of the fabricated dynamic (left) and static (right) shift registers.

The maximum clock frequency of a shift register (defined as the maximum frequency for bit error-free operation) depends on the register's propagation delay and, as such, is a function of device characteristics (effective mobility, threshold voltage), device geometry (primarily channel length) and operation conditions (supply voltage, clock signal levels) [11]. In order to design a register circuit for maximum performance, the effect of the parasitic capacitance to the conductive substrate should also be taken into account; we have shown that this parasitic capacitance is detrimental to circuit performance if the electrical isolation dielectric deposited on the substrate is not thick enough [12].

As a simple design rule, we consider a simple CMOS inverter, with device geometries W_p and W_n (PMOS and NMOS, respectively), channel length L and oxide capacitance C_{ox} . The propagation delay of the inverter can be approximated to a first degree as an RC product, where the capacitive term is the sum of the inverter's output capacitance, plus any load capacitance seen at the output. Assuming that an identical inverter is driven by the first one, we can express the capacitive term of the delay as follows:

$$C \approx \frac{1}{2}LC_{ox}(W_p + W_n) + \frac{3}{2}LC_{ox}(W_p + W_n) + C_p \quad (1)$$

where the first and the second terms of the sum represent the output capacitance of the first inverter and the input capacitance of the inverter it drives, respectively. C_p is the parasitic capacitance to the substrate, seen at the output of the first inverter. In order to figure out a suitable isolation dielectric thickness, we require that the parasitic term be negligible compared to the inherent capacitive terms, i.e.

$$C_p = \frac{\epsilon_0 \epsilon_d}{t_d} A \ll 6W_n LC_{ox} \Rightarrow \quad (2)$$

$$t_d \gg \frac{\epsilon_0 \epsilon_d}{6W_n LC_{ox}} A$$

where ϵ_d and t_d are the relative permittivity and the thickness of the isolation dielectric

layer, respectively, and A is the area of the conductive interconnects (metal / polysilicon) from the first to the second inverter. It is assumed that scaled inverters are used (i.e. $W_p = 2W_n$). It should be noted that C_p depends on the surface roughness, too, and it may deviate significantly from the parallel-plate capacitor formula of (2) for rough substrates. Table 2 shows the maximum and minimum operational frequency of the fabricated dynamic and static shift registers, measured at a supply voltage of 14V. Note that both of these designs could be successfully used for both column and row driver realizations in low to medium resolution active matrix array. The dc power consumption at the maximum frequency was approximately 52mW for the dynamic, and 70mW for the static design. Figure 4 shows the typical output waveforms of five consecutive shift register stages. The clock and input signals are also shown. The traces, from top to bottom, are: $V_{OUT(1)}$, $V_{OUT(2)}$, $V_{OUT(3)}$, $V_{OUT(4)}$, $V_{OUT(5)}$, CLK, V_{INPUT} . Figure 5 shows two completed shift registers, a dynamic and a static one. Note that most part of the circuit area is occupied by the output buffer structures.

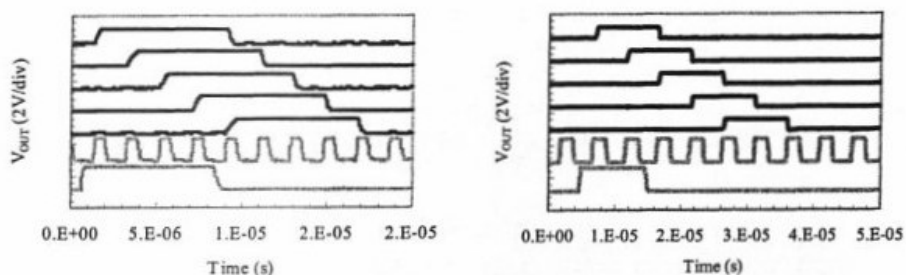


Fig. 4: Output waveforms of dynamic (top) and static (bottom) shift registers, at 500 and 200kHz, respectively.



Fig. 5: Dynamic (left) and static (right) 10-stage shift registers on stainless steel foil.

3. OLED DISPLAY CIRCUITS

3.1 Pixel architectures

Two different circuit architectures have been implemented. The first one is the standard 2-TFT design [13]. In this circuit, M1 behaves as a voltage controlled current source, and M2 is the control switch. This means that there are three lines going into each pixel (V_{data} , V_{add} and V_{dd}). This circuit works as follows: an analog voltage is programmed

in the data line during addressing time (when M2 is turned ON by the address line.) This voltage activates M1 allowing a controlled current to flow through it. When the addressing period is over, M2 is turned OFF and C stores the data voltage. This allows M1 to keep supplying the correct current during the non-addressing time. This pixel architecture was implemented with two topologies: an all PMOS design, and a CMOS design with the driving transistor being NMOS and the switch being PMOS.

This circuit does not compensate for TFT device parameter variations such as mobility or threshold voltage. Several pixel designs have been proposed to compensate for such variations. One approach that has attracted a great deal of interest in the last few years is the current addressing technique [14]. When directly addressing with a current, turn-ON voltages and mobility variations do not affect the LED current. This is done by programming the current source with a reference current instead of a voltage, so the current provided by that source is not a function of the voltage on the transistor's gate (instead, the voltage on the gate is a function of the current.)

The 4 TFT current copy circuit is perhaps a good compromise between performance and complexity. This circuit works as follows: during addressing time, a reference current is sunk through I_{data} . Since M1 is diode connected, a corresponding voltage is established on its gate to allow that current to flow. When M2 and M3 are turned OFF and M4 is turned ON, C holds the programmed voltage on the gate of M1 allowing that current to now flow through the diode. (Figure 6 shows all three pixel circuits)

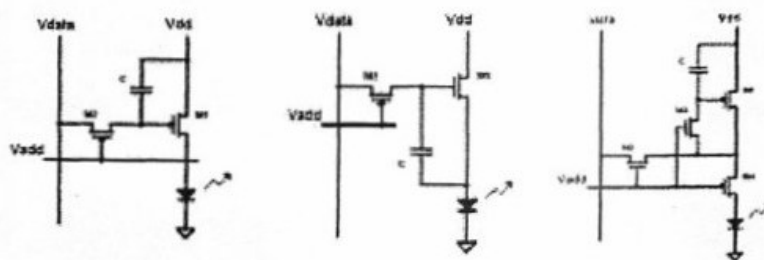


Fig. 6: 2 TFT pixel PMOS (left) CMOS (center), 4 TFT pixel (right).

Both architectures were implemented with two different layouts. The more traditional layout requires a power supply line. However, when using metal foil substrates the high conductivity of stainless steel can be used to bring in power to each pixel creating a less resistive power distribution. The main motive for developing this approach was to increase the light emitting area of the display, since the common power supply line can be omitted. An extra contact layer is required to create contacts between the pixels and the substrate. These contacts are formed after the patterning the first metal contact holes during the fabrication of electric circuits. A second PECVD passivation oxide follows, and then vias that make contact between the AlNi layer and the Indium Tin Oxide film that follows are patterned and opened. After the patterning of the ITO film, the organic electroluminescent material is deposited, followed by the OLED cathode deposition and final display encapsulation.



Fig. 1: The AM-OLED pixel structure on steel and cross section (vertical dimensions not to scale)

3.2 Pixel Performance

The overall functionality of both pixel designs and both layout implementations were proven at different load impedances 10K, 50K and 100K to account for possible variations in OLED performances. Also the 2-TFT pixel was demonstrated with three pitch sizes: 250 x 250 μm and 110 x 105 μm for the PMOS implementation, and 125 x 125 μm for the CMOS implementation.

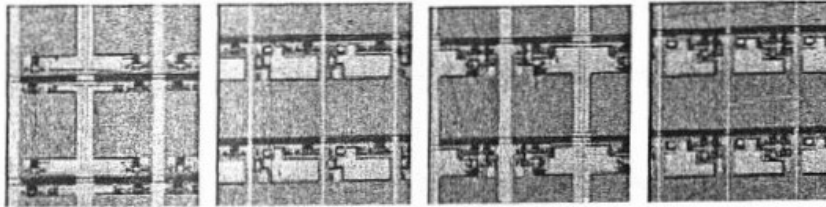


Fig. 7: 2 TFT pixels (left) and 4 TFT pixels (right); all 250 μm pitch

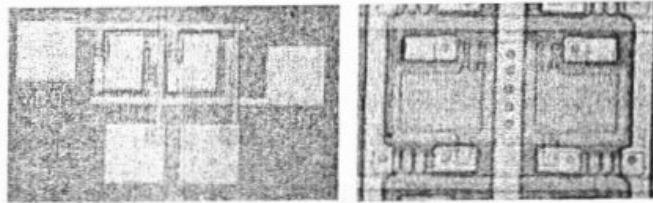


Fig. 8: 2 TFT pixels 125 μm x 125 μm (left) and 2 TFT pixels 110 μm x 105 μm (right)

Figure 9 shows the average current measured through different pixels over a range of data values and its normalized variation as a function of data voltage, in the 2 TFT pixels. This normalized variation curve was extrapolated to obtain percentage variation of threshold voltage and mobility of the measured devices. We can obtain the theoretical variation by solving the difference equations for mobility (3) and threshold voltage (4) at different gate bias. (First level approximation done with TFT's working on saturation.)

$$(3) \quad \partial I = \partial \mu \cdot k \cdot (V_{gs} - V_t)^2$$

$$(4) \quad \partial I = \partial V_t \cdot 2 \cdot k \cdot \mu \cdot (V_{gs} - V_t)$$

If we normalize for the absolute value of current and notice that $\partial \mu = \bar{\mu} \cdot \xi_\mu$ and $\partial V_t = \bar{V}_t \cdot \xi_{V_t}$ (where $\bar{\mu}$, ξ_μ and \bar{V}_t , ξ_{V_t} are the average and the percentage mobility and threshold voltage variations respectively), we obtain:

$$(5) \quad \frac{\partial I}{I} = \xi_{\mu} \quad \text{for mobility changes of } \xi_{\mu} \text{ percent, and}$$

$$(6) \quad \frac{\partial I}{I} = 2 \cdot \frac{\bar{V}_t \cdot \xi_{V_t}}{V_{GS} - \bar{V}_t} \quad \text{for threshold voltage changes of } \xi_{V_t} \text{ percent.}$$

The extrapolated numbers from figure 9 were 4% for mobility and 9% for threshold voltage which approximate the actual variations seen when obtaining Table 1. Figure 10 shows the output current versus the programming current in the 4 TFT pixels. The nonlinearity at low current levels can be explained by assuming non-saturation behavior of the driving TFT's. Furthermore, the line impedance that the driving TFT sees when programming is different from the OLED's impedance. As a consequence, the finite output impedance for these devices also explains the loss of linearity between programming current and operating current. [14]

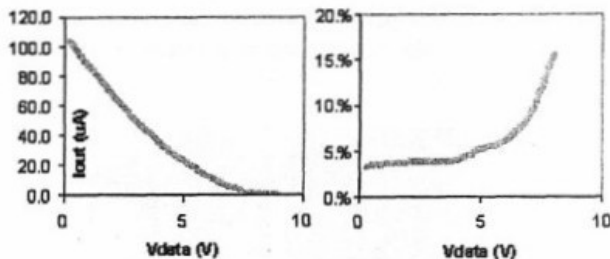


Fig. 9: Typical output current versus input data for 2 TFT pixels and normalized deviations

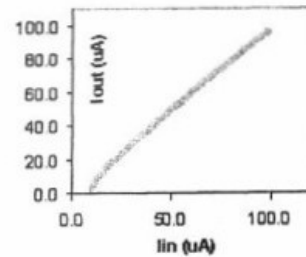


Fig. 10: Output current vs. programming current in 4 TFT pixels

4. DISPLAY OLED

4.1 OLED Fabrication

Liquid Crystal Displays have now been in the market for a number of years; however recent enhancements on Organic Light Emitting Devices (OLED's) offer a new alternative to the Flat Panel Display industry. OLED's offer improved luminous efficiency, high brightness, and excellent viewing angle. In addition, OLED displays have thinner profiles, weigh less, and consume less power than LCD's. Due to their emissive nature, OLED displays do not require a backlight which makes this technology a lower cost and more suitable alternative to flexible display applications.

Their structure consist of a series of thin films that usually include electron and hole injection layers, electron and hole transport layers, and an emissive layer. (In general, polymer OLED's only require a hole transport layer and an emissive layer.) The anode (metal that makes contact with the hole injection layer) is usually made of a high work function metal such as transparent Indium-Tin Oxide (ITO) while the cathode is made by a low work function metal. When the holes and electrons recombine in the emissive layer light is produced.

The PLED's presented in this paper are formed with an anode layer of Al/Ni/ITO (1000A/500A/500A.) PEDOT and PPV are spun on top of the anode sequentially, after etching the insulating layer, SiO₂. By following each spin-casting of the polymers, a

drying process has to be performed in order to evaporate the solvent. The drying process can be done either on a hot plate or in a vacuum oven. In the current process, solvent drying is done on the hot plate. The thickness of PEDOT and MEH-PPV adopted are 800Å and 600Å respectively. Thicker films relate to a higher threshold voltage, however, a thicker PEDOT film has more capability of compensating the anode surface resulting in improved yield. A thinner PPV film facilitates the electron and hole recombination, but the thinner film cannot withstand high electric fields. For a top-emitting OLED device, the semi-transparent or transparent cathode is required. Usually, this cathode consists of two different metals. One is the low work function metal (Al, Ca, Ba, Cs, Ag, Li, Mg.....etc.), which is in contact with the light-emitting layer and enhances the electron injection, PPV. Mostly, this metal film is very thin, such as 50Å; the other metal plays a role of carrying the current, and ITO or IZO is almost the one and only choice. Ideally, both of these two metals have to be evaporated, rather than being sputtered, in order to reduce the ion bombardment upon the surface of PPV.

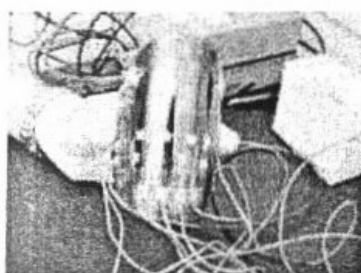


Fig. 11: Flexible passive matrix OLED

4.2 OLED Performance

When using an Al/Ni anode, it essentially becomes AlNiO₂ because of the O₂ plasma treatment before the spin-casting of polymers [15]. Some documentation has proved that NiO₂ has the work function of 5.0eV as high as ITO does [16]. This reproducible result has also been found on our device, which was PLEDs on flexible steel. The NiO₂ surface is capable of forming the well-performed holes-injecting interface with PEDOT. One more advantage is that Al/NiO₂ surface can reflect more light than Al/Ni/ITO, presuming that Ni catalyzes the formation of Tin Oxide (SnO₂). That results in the darkness on the surface of Al/Ni/ITO. In our system, Al was sputtered as the low work function metal first, using a low RF power of 50W. Another sample with e-beam evaporated Al was prepared on the thin steel substrate, and it showed a better performance than with sputtered Al (Figure 12). ITO was sputtered in both cases and the thickness was around 900Å. Characteristics of electroluminescence and photoluminescence were measured (Fig. 13 and 14) as well as the spectrum of the flexible PLED taken at different voltages. The measurements at 10 V and 11 V were taken twice. In between, there was some degradation of the PLED due to high current during the elapsed time. The degradation of the PLED was measured with two scans taken a half hour apart (Fig. 15). In the interim, the PLED was fed a 9 V signal. The % Change is slightly more for off-peak wavelengths than for the peak wavelength.

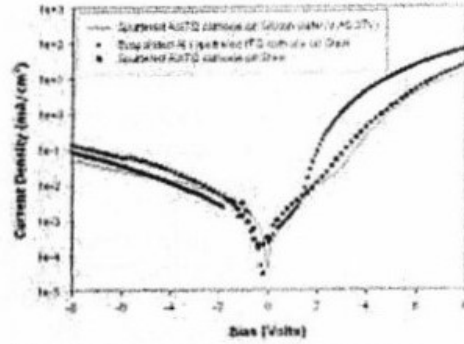


Fig. 12: I-V Curve for OLED

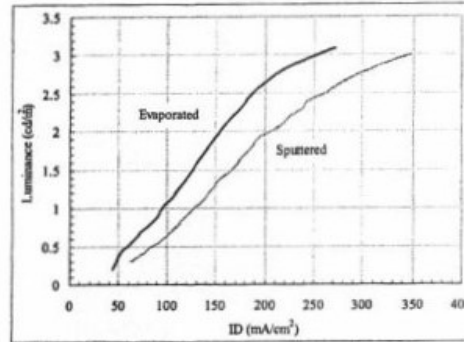


Fig. 13: Luminance of OLED

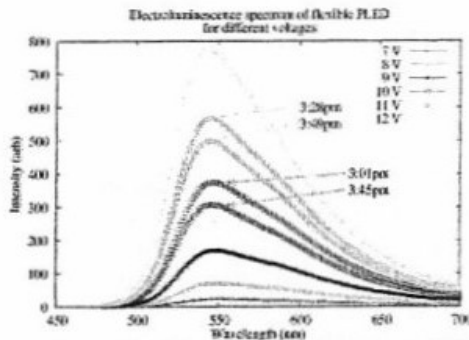


Fig. 14: Electroluminescence of PLED

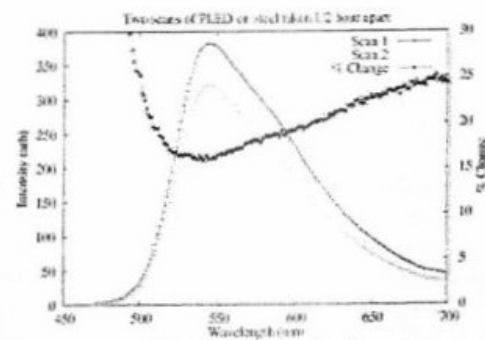


Fig. 15: Electroluminescence degradation

5. CONCLUSION

This paper discussed fabrication issues and measurement results of excimer laser annealed polysilicon TFT devices, circuits and display elements on flexible, type-304 stainless steel foil substrates. We have demonstrated this is possible with a high temperature, CMOS compatible poly-Si TFT fabrication process. This process has resulted in devices adequate not only for active matrix displays implementations, but for integrated display driver circuits too, further enhancing the cost savings realizable with

this approach. The functionality of several pixels has been proven and stand alone PLED structures have been demonstrated on stainless steel substrates.

These results justify the fabrication of high performance digital circuits for display driver and other medium to high-speed applications on flexible metal foils, and underscore the substantial practical advantages of this type of substrate for high volume, low cost highly integrated flexible electronics.

REFERENCES

- [1] P.M. Smith, P.G. Carey, T.W. Sigmon, "Excimer Laser Crystallization and Doping of Silicon Films on Plastic Substrates", *Applied Physics Letters*, Vol. 70, pp. 342-344, 1997.
- [2] S.D. Theiss, P.G. Carey, P.M. Smith, P. Wickboldt, T. Sigmon, Y. Tung, T. King, "Polysilicon Thin Film Transistors Fabricated at 100oC on a Flexible Plastic Substrate", *Technical Digest - International Electron Devices Meeting*, pp.257-260, 1998.
- [3] S. Utsunomiya, S. Inoue, T. Shimoda, "Low-Temperature Poly-Si TFT Transferred onto Plastic Substrates by Using Surface Free Technology by Laser Ablation / Annealing", *Journal of the Society for Information Display*, Vol. 10, pp. 69-73, 2002.
- [4] Y. Lee, H. Li, S. Fonash, "High-Performance Poly-Si TFT on Plastic Substrates Using a Nano-Structured Separation Layer Approach", *IEEE Electron Device Letters*, Vol. 24, No. 1, pp. 19-21, 2003.
- [5] T. Serikawa, F. Omata, "High-Mobility Poly-Si TFTs Fabricated on Flexible Stainless Steel Substrates", *IEEE Electron Device Letters*, Vol. 20, pp. 574-576, 1999.
- [6] M. Wu, K. Pangal, J.C. Sturm, S. Wagner, "High Electron Mobility Polycrystalline Silicon Thin-Film Transistors on Steel Foil Substrates", *Applied Physics Letters*, Vol. 75, No. 15, pp. 2244-2246, 1999.
- [7] R. Howell, M. Stewart, S. Karnik, S. Saha, M. Hatalis, "Poly-Si Thin-Film Transistors on Steel Substrates", *IEEE Electron Device Letters*, Vol. 21, pp. 70-72, 2000.
- [8] M. Stewart, T. Afentakis, G. Sarcona, M. Hatalis, "Low-Temperature Flat Panel Display Driver Circuits in RTP Crystallized Polysilicon", *SID Digest*, Vol. 31, p. 462, 1999.
- [9] T. Afentakis, M. Hatalis, T. Voutsas, J. Hartzell, "High Performance Polysilicon Circuits on Thin Metal Foils", *Proceedings of the SPIE*, Vol. 5004, pp. 122-126, 2003.
- [10] Y. Chen, J. Au, P. Kazlas, A. Ritenour, H. Gates, J. Goodman, "Ultra-thin, high-resolution, Flexible Electronic Ink Displays Addressed by a-Si Active-Matrix TFT Backplanes on Stainless Steel Foil", *Technical Digest - International Electron Devices Meeting*, pp. 389-392, 2002.
- [11] T. Afentakis, M. Hatalis, "Modeling and Performance of Polysilicon TFT Circuits on Stainless Steel Foil Substrates" *SPIE Proceedings*, Vol. 4295, pp. 95-101, 2001.
- [12] T. Afentakis, M. Stewart, R. Howell, M. Hatalis, "Polysilicon TFT Display Driver Circuits on Stainless Steel Foil Substrates" *SID Digest*, Vol. 33, pp. 538-541, 2000.
- [13] M. Hatalis et al., *SPIE Proceedings* Vol. 3057, p.277
- [14] I. Hunter et. al., 40th Society for Information Display Meeting. OLED addressing, V I Seminar M-6
- [15] M. G. Mason, L. S. Hung, and C. W. Tang, *J. Appl. Phys.* 86, 1688 (1999).
- [16] Chan-Jae Lee, Dae-Gyu Moon, and Jung-In Han, *SID 03 DIGEST*, 533 (2003).