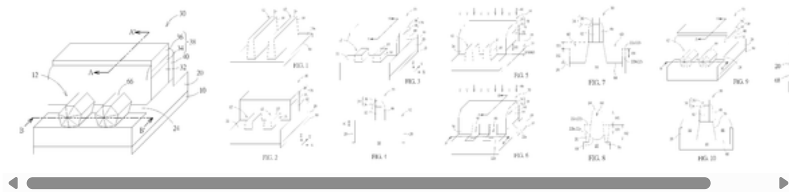
Patents 9,318,609

Semiconductor device with epitaxial structure

Abstract

A semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface, and the isolation structure at two sides of the gate structure has a second top surface. The first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in direct contact with the fin structure.

Images (7)



Classifications

H01L29/7851

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Worldwide applications

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2015-02-12	Application filed by United Microelectronics Corp
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Claims (10)

Hide Dependent

What is claimed is:

1. A semiconductor device, comprising:

a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure, wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and

an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

2. The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

3. The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

4. The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

5. The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

6. The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

7. The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

8. The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

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9. The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

10. The semiconductor device according to claim 1, further comprising:

another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and

a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

Description

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 13/913,511, filed on Jun. 9, 2013, the disclosure of which is hereby incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of semiconductor devices, and more particularly to a semiconductor device with an epitaxial structure.

2. Description of the Prior Art

As semiconductor devices switching speeds continue to increase and operating voltage levels continue to decrease, the performances of metal-oxide-semiconductor filed effect transistors (MOSFETs) and other types of transistors, such as bipolar junction transistors, need to be correspondingly improved. Currently, along with the development of the MOSFETs, one of the main goals in the industry is to increase the carrier mobility so as to further increase the operation speed of the MOSFETs.

In order to improve the device performances, crystal strain technology has been developed. Crystal strain technology is becoming more and more attractive as a means for getting better performances in the field of MOS transistor fabrication. Putting a strain on a semiconductor crystal alters the speed at which charges move through that crystal. Strains make the MOS transistors work better by enabling charge carriers, such as electrons or holes, to pass through the silicon lattice of the channel more easily. Currently, attempts have been made to use a strained silicon layer as a part of MOS transistors in which an epitaxial silicon germanium (SiGe) structure or an epitaxial silicon carbide (SiC) structure is formed. In this type of MOS transistor, a biaxial tensile strain is induced in the epitaxy silicon layer due to the difference in lattice constants between SiGe or SiC and Si. As a result, the band structure is altered, and the carrier mobility is increased.

However, due to the continuous shrinkage in the size of the semiconductor devices, the aspect ratio of the epitaxial layer also gets higher, which often incur unwanted defects, such as void defects in the epitaxial layer. These defects inside the epitaxial layer reduce the stress required to be imposed onto the corresponding channel region. As a result, how to prevent the formation of the defects inside the epitaxial layer is an important issue.

SUMMARY OF THE INVENTION

To this end, on object of the present invention is to provide a semiconductor device with an epitaxial layer so that stress imposed on the channel region can be increased.

According to a preferred embodiment of the invention, a semiconductor device is provided. The semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is indirect contact with the fin structure.

One feature of the present invention is to provide a semiconductor device with an epitaxial layer and a fabrication method thereof. Since the process for etching the isolation structure is optionally carried out prior to and/or after the formation of the recess, the height of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process. Furthermore, since the epitaxial structure is not sealed during the epitaxial growth process, the void defects may be also avoided as a result.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention, wherein:

FIG. 1 is a schematic perspective diagram showing the semiconductor device at the beginning of the fabrication process;

FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a gate structure;

FIG. 3 is a schematic perspective diagram showing the semiconductor device after the formation of a spacer;

FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3;

FIG. 5 is a schematic perspective diagram showing the semiconductor device after etching the isolation structure;

FIG. 6 is a schematic perspective diagram showing the semiconductor device after etching fin structures;

FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6;

FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6;

FIG. 9 is a schematic perspective diagram showing the semiconductor device after the formation of an epitaxial layer;

FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9; and

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FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9.

DETAILED DESCRIPTION

In the following description, numerous specific details are given to provide a thorough understanding of the invention. It will, however, be apparent to one skilled in the art that the invention may be practiced without these specific details. Furthermore, some well-known system configurations and process steps are not disclosed in detail, as these should be well-known to those skilled in the art.

Likewise, the drawings showing embodiments of the apparatus are not to scale and some dimensions are exaggerated for clarity of presentation. Also, where multiple embodiments are disclosed and described as having some features in common, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention. Please refer to FIG. 1. FIG. 1 is a schematic perspective view showing the semiconductor device of at the beginning of the fabrication process. As shown in FIG. 1, a substrate **10** is provided. The substrate **10** may be a semiconductor substrate such as a silicon substrate, a silicon containing substrate, a III-V semiconductor-on-silicon (such as GaAs-on-silicon) substrate, or a graphene-on-silicon substrate. Preferably, the substrate **10** is not a silicon-on-insulator (SOI) substrate. Still referring to FIG. 1, a plurality of fin structures **12** is disposed on the substrate **10**. More precisely, the method for fabricating the fin structures **12** may include the following processes, but not limited thereto. First, a bulk substrate (not shown) is provided and a hard mask layer (not shown) is formed thereon. The hard mask layer is then patterned to define the location for forming fin structures **12** in the bulk substrate. Afterwards, an etching process is performed to form fin structures **12** in the bulk substrate. After the above processes, the fabrication method for the fin structures **12** is complete. In this case, the fin structures **12** may be regarded as protruding from the surface **10** *a* of the substrate and the compositions of the fin structures **12** and the substrate **10** may be the same, such as epitaxial silicon. In another case, when the substrate is chosen from a III-V semiconductor-on-silicon substrate rather than the above-mentioned bulk substrate, the main compositions of the fin structures may differ from that of the underlying substrate.

In this embodiment, the hard mask layer (not shown) is optionally removed in a later process after the formation of the fin structures **12**, so that a tri-gate MOSFET can be formed in the following processes. There are three contact faces between each fin structure **12** and the following formed dielectric layer serving as a carrier channel region. Compared with planar MOSFETs, the tri-gate MOSFETs have wider channel width within the same channel length. When a driving voltage is applied, the tri-gate MOSFET may produce an on-current twice higher than conventional planar MOSFETs. In another embodiment, the hard mask layer (not shown) is reserved to form a fin field effect transistor (Fin FET), which is another kind of multi-gate MOSFET. Since the hard mask layer is reserved in the fin field effect transistor, there are only two contact surfaces between each fin structure **12** and the following formed dielectric layer.

Please refer to FIG. 2. FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure. An isolation structure **10** is formed on the substrate **10** between each fin structure **12** so as to electrically isolate subsequently-formed transistors from one another. The isolation structure **20** may have the configuration shown in FIG. 2. At this stage, a lower portion of each fin structure **12** is embedded in the isolation structure **20** and each fin structure **12** exposed out of the isolation structure **20** may have a first height H**1**. The isolation structure **10**, for example, may be a shallow trench isolation (STI) structure, which may be formed through a STI fabrication process. Since the fabrication process for the STI structure is well-known to those skilled in the art, the detailed description of this is therefore omitted, and is not limited thereto.

Still referring to FIG. 2, in a following step, a gate dielectric layer (not shown), a sacrificial electrode layer (not shown) and a cap layer (not shown) are sequentially formed to cover the substrate **10** and the fin structures **12**. Then, the gate dielectric layer, the sacrificial electrode layer and the cap layer are patterned to form a stack structure. The stack structure may be regarded as a gate structure **30** including the gate dielectric layer (not shown), the sacrificial electrode layer **32** and the cap layer **38**. The gate structure **30** crosses over two fin structures **12** and covers the isolation structure **20** between them. Specifically, the gate structure **30** may cover a top surface **14** and two side surfaces **16** of portions of each fin structure **12**, and may cover a top surface **22** of portions of the isolation structure **20**. Additionally, the gate structure **30** is preferably aligned with a first direction X, while the fin structures **12** are preferably aligned with a second direction Y and protruding from the substrate **10** along a third direction X. In this embodiment, the first direction X, the second direction Y, and the third direction Z are mutually orthogonal to one another, but not limited thereto.

For the sake of clarity, only one gate structure **30** is depicted in FIG. 2 to FIG. 11. The number of which, however, may be increased depending on the requirements for different products. For example, more than one mutually parallel gate structure may be disposed on the substrate so that one fin structure may be concurrently covered by more than one gate structure. Besides, the same one gate structure is preferably used as a gate for transistors with the same conductivity type, like gates for PMOS transistors or gates for NMOS transistors.

In this embodiment, a gate-last for high-k last process is used so that the gate structure **30** may be regarded as a dummy gate structure. In other words, the gate dielectric layer will be replaced with a gate dielectric layer having a high dielectric constant in later processes and the sacrificial electrode layer **32** will be replaced with a conductive metal layer. Therefore, the material of the gate dielectric layer may be just a sacrificial material suitable for being removed in later processes. The sacrificial electrode layer **32** may be made of polysilicon, but it is not limited thereto. The cap layer **36** may be a single-layered or a multi-layered structure composed of a nitride layer or an oxide layer used to serve as a patterned hard mask. In this embodiment, the cap layer **36** is a double-layered structure composed of a bottom layer **34** and a top layer **34**. The bottom layer **34** may be a nitride layer and the top layer **34** may be an oxide layer, but not limited thereto.

In the above paragraphs, a gate-last for high-k first process is used. However, the present embodiment may also adopt a gate-last for high-k last process. In this case, the gate dielectric layer is a gate dielectric layer having a high dielectric constant, which may be the group selected from hafnium oxide (HfO_2), hafnium silicate ($HfSiO_4$), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate ($SrTiO_3$), zirconium silicate ($ZrSiO_4$), hafnium zirconate ($HfZrO_4$), strontium bismuth tantalate ($SrBi_2Ta_2O_9$, SBT), lead zirconate titanate ($PbZr_xTi_{1-x}O_3$, PZT) and barium strontium titanate ($BaxSr_{1-x}TiO_3$, BST), but it is not limited thereto. Additionally, a barrier layer (not shown) may be formed on the gate dielectric layer to serve as an etching stop layer to protect the gate dielectric layer during the removal of the sacrificial electrode layer **32** and to prevent above disposed metals from diffusing downwards to the gate dielectric layer and from polluting the gate dielectric layer. The barrier layer (not shown) may be a single layer structure or a multilayer structure composed of tantalum nitride (TaN) or titanium nitride (TiN) etc.

Please refer to FIG. 3 and FIG. 4, wherein FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3. After the formation of the gate structure, a spacer **40** is formed on the sidewalls of the gate structure **30** to define the position of an epitaxial structure. In this embodiment, the spacers **40** are respectively formed on each side of the gate structure **30** and cover portions of the top surface **22** of the isolation structure **20**. More precisely, the method for forming the spacers **40** may include the following steps. A material layer is deposited on the gate structure **30** and the substrate **10**, and then an etching process is performed to form the spacers **40**. The spacers **40** may be a single-layered structure, such as a silicon nitride layer or a silicon oxynitride layer, or a double-layered structure, such as a silicon oxide/silicon nitride layer, but not limited thereto. In this embodiment, the spacers **40** represent spacers for defining and forming an epitaxial structure, so that other spacers may be formed before/after the spacers **40** are formed to form a lightly doped source/drain region (as shown) or a source/drain region (as shown). For simplifying and clarifying the present invention, FIG. 3 to FIG. 11 only depict the spacers **40** for forming the epitaxial structure.

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Please refer to FIG. 5. FIG. 5 is a schematic perspective view showing the semiconductor device after etching the isolation structure. After the formation of the spacers **40**, the isolation structure **20** exposed from the gate structure **30** and the spacers **40** may be further etched by a suitable etching process. In this way, a top surface **22** of portions of the isolation structure **20** may be etched down to a predetermined depth (also called a first depth D**1**) and a structure shown in FIG. 5 is obtained. More precisely, a first etching process **42**, such as a wet etching or a dry etching process, may be carried out to selectively remove the isolation structure **20** rather than the gate structure **30** and the fin structures **12**. Through this process, not only portions of the sidewalls of the isolation structure **20** that are disposed under gate structure **30** and the spacers **40** may be exposed, but also portions of the fin structures **12** originally embedded in and in direct contact with the isolation structure **20** are exposed. At this time, the isolation structure **20** under the gate structure **30** and the spacers **40** may have a relatively high first top surface **22** *a*, while the isolation structure **20** exposed from the gate structure **30** may have a relatively low second top surface **22** *b*. There is a height difference H**2** between the first top surface **22** *a* and the second top surface **22** *b*. For example, the height difference H**2** may range from 100 Angstroms' to 250 Angstroms, preferably 150 Angstroms, but not limited thereto.

Please refer to FIG. 6 to FIG. 8. FIG. 6 is a schematic perspective view showing the semiconductor device after etching fin structures. FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6. FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6. As shown in FIG. 6 to FIG. 8, a second etching process **46** is carried out to etch the fin structures **12** under the gate structure **30** and the spacers **40**. After the etching process, a recess **60** may be formed in each fin structure **12** at at least one side of the gate structure **30**. Furthermore, according to this embodiment, the ends of the fin structures **12** at two sides of the gate structure **30** may respectively have a recess **60**, and a bottom surface **68** of the recess **60** is preferably shallower than a bottom surface **26** of the isolation structure **20**. More precisely, as shown in FIG. 7 and FIG. 8, there is a difference between the bottom surfaces **62** of the recesses **60** and the top surface **14** of the original fin structure **12**, which height is equal to the first height H**1** plus the second depth D**2** . During the second etching process **46**, the top surface **22** of the isolation structure **20** at both sides of the gate structure **30** is also recessed down to a predetermined depth. This diminished value is equal to a first depth D**1**. Preferably, the second depth D**2** is greater (also called deeper) than the first depth D**1**.

Furthermore, the above etching process may include at least a dry etching step and/or at least a wet etching step. For example, the substrate **10** may be etched down to a predetermined depth through a dry etching step and then may be laterally etched to form a desired profile of the recess **60** through a wet etching step, but is not limited thereto. In this embodiment, the recess **60** has an upwardly-curved cross-sectional profile, but is not limited thereto, as the cross-sectional profile of the recess depends upon the specific requirements. Additionally, a wet cleaning process (not shown) may be performed optionally to clean the surface of the recess **60** after the etching. The wet cleaning process may include a dilute hydrofluoric acid (DHF) containing process, but it is not limited thereto.

It should be noted that, the timing for etching the isolation structure **20** exposed from the gate structure **30** and the spacers **40** and the timing for etching the fin structures **12** may be reversed. More precisely, according to the present embodiment, the fin structures **12** exposed from the gate structure **30** and the spacers **40** may be etched first and the isolation structure **20** not covered by the gate structure **30** and the spacers **40** are etched thereafter. In other words, one feature of the present invention is that, through etching the isolation structure **20**, the height difference between the bottom surface **68** of each recess **60** and the top surfaces **22** of the isolation structure **20** at both sides of the gate structure **30** can be reduced. Therefore, the removal of the isolation structure **20** and the formation of the recess **60** may be carried out in either sequence and both can meet the needs of the present invention.

Please refer to FIG. 9 to FIG. 11. FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer. FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9. FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9. As shown in FIG. 9 to FIG. 11, an epitaxial growth process, such as a molecular beam epitaxy (MBE) process, a co-flow epitaxial growth process, a cyclic selective epitaxial growth process or the likes, maybe carried out in order to grow an epitaxial structure **60** in each corresponding recess **60**. More precisely, each epitaxial structure **66** may completely cover the bottom surface **68** and sidewalls **70** of the corresponding recess **60**. Furthermore, the composition of the epitaxial structure **66** may be correspondingly modified according to the conductivity types of the semiconductor devices. In this way, a certain stress may be imposed on the channel regions adjacent to the top surface **14** and the two sides of the fin structure **12**. For example, in a P-type semiconductor device, the epitaxial structure **66** may be doped or un-doped silicon germanium layer so as to apply a compressive stress to the channel regions. Besides, the epitaxial structure **66** may include a multilayer or a surrounded structure with a different germanium concentration gradually varying from the inside to the outside or/and from bottom to top. For example, the epitaxial layer **66** may include epitaxial Si, at least a layer of epitaxial SiGe with a relatively low concentration of Ge, at least a layer of epitaxial SiGe with a relatively high concentration of Ge, an epitaxial Si layer and so forth, which are disposed sequentially from bottom to up. In another case, in an N-type semiconductor device, the composition of the epitaxial structure **66** may include silicon phosphorous (SiP), silicon carbide (SiC), phosphorus-doped silicon carbide or the likes, so as to provide a tensile stress to the channel regions.

Furthermore, regardless of the composition of the epitaxial structure **66**, since the height difference between the bottom surface **68** of each recess **60** and the top surface **22** *b* of the isolation structure **20** at two sides of the gate structure **30** has been reduced in the above processes, the epitaxial structure **66** may not be sealed during the following epitaxial growth process and the void defects maybe avoided as a result. In other words, one feature of the present invention is that, through etching the isolation structure **20** at two sides of the gate structure **30**, the epitaxial structure **66** may be formed with a desired height (also called depth) and without any void defects. Accordingly, the epitaxial structure may apply the required stress to the channel regions thereby increasing the carrier mobility of the semiconductor device.

After the formation of the above epitaxial structures, the following semiconductor processes maybe optionally carried out. For example, a high-k last replacement metal gate (RMG) process may be carried out so that the gate structure composed of polysilicon inside may be replaced with a metal gate structure. The RMG process may include the following processes: (1) depositing an interlayer dielectric to surround the gate structure; (2) removing the gate structure to leave a trench; (3) forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench; and (4) forming a conductive layer to fill up the trench. Afterwards, a contact formation process may be carried out to form a contact electrically connecting the epitaxial structure. Since the RMG process and the contact formation process are well-known to those skilled in the art, the detailed description of these is therefore omitted for the sake of clarity.

In the following paragraph, a modified embodiment of the above embodiment is disclosed and the description below is mainly focused on differences among each embodiment. In addition, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

Please refer to FIG. 3 and FIG. 5. According to this modified embodiment, after the formation of the spacers, the first etching process is also carried out to expose not only portions of the sidewalls of the isolation structure **20** disposed under the gate structure **30** and the spacers **40**, but also to expose portions of the fin structures **12** originally embedded in and in direct contact with the isolation structure **20**. Afterwards, with a slight difference from the process described in the above embodiment, the second etching process is not carried out in this modified embodiment so that no recess is formed in the fin structures. Finally, similarly to the structure shown in FIG. 9, the epitaxial growth process is carried out to form the epitaxial structure **66** on the surface of the fin structure. The following processes are all similar to those described in the previous embodiment, the detailed description of which is therefore omitted for the sake of clarity. In this modified embodiment, since portions of the isolation structure **20** are removed, the epitaxial structure **66** may effectively apply stress to the corresponding channel regions.

It should be noted that, for the sake of clarity, only the non-planar FETs are described in the above paragraphs. However, planar FETs may also be formed without departing from the scope and spirit of the present invention. More precisely, in this case, the gate structure may be formed to cover a planar active region and portions of the isolation structures. Then, the active region and the isolation structure at two sides of the gate structure are etched sequentially. Finally, an epitaxial growth process is carried out. Similarly, through etching the isolation structure at two sides of the gate structure, the epitaxial structure may be formed with a desired height (also called depth) without void defects. Accordingly, the epitaxial structure may apply the required stress to the channel regions thereby increasing the carrier mobility of the semiconductor device.

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To summarize, the present invention provides a semiconductor device. By performing the process for etching the isolation structure and associated with an optional recess, the difference in height between the bottom surface of the recess and the top surface of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial structure may not be sealed during the following epitaxial growth process and the void defects may be avoided. Accordingly, the epitaxial structure may apply a required stress to the channel regions and increase the carrier mobility of the semiconductor device.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

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US20100144121A1	2008-12-05	2010-06-10	Cheng-Hung Chang	Germanium FinFETs Having Dielectric Punch-Through Stoppers

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US20100167506A1	2008-12-31	2010-07-01	Taiwan Semiconductor Manufacturing Co., Ltd.	Inductive plasma doping
US20120193713A1	2011-01-31	2012-08-02	Pranita Kulkarni	FinFET device having reduce capacitance, access resistance, and contact resistance
US8765533B2	2012-12-04	2014-07-01	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin-like field effect transistor (FinFET) channel profile engineering method and associated device
Family To Family Citations				

* Cited by examiner, † Cited by third party

Cited By (16)

Publication number	Priority date	Publication date	Assignee	Title
Family To Family Citations				
US9559189B2 *	2012-04-16	2017-01-31	United Microelectronics Corp.	Non-planar FET
US9054189B1 *	2014-01-06	2015-06-09	Samsung Electronics Co., Ltd.	Semiconductor device and method for fabricating the same
KR102168963B1 *	2014-01-21	2020-10-22	삼성전자주식회사	Semiconductor device and method for fabricating the same
US9236397B2 *	2014-02-04	2016-01-12	Globalfoundries Inc.	FinFET device containing a composite spacer structure
US20150255353A1 *	2014-03-05	2015-09-10	Globalfoundries Inc.	Forming source/drain regions with single reticle and resulting device
US10263108B2	2014-08-22	2019-04-16	Taiwan Semiconductor Manufacturing Company, Ltd.	Metal-insensitive epitaxy formation
DE102015100860A1	2014-08-22	2016-02-25	Taiwan Semiconductor Manufacturing Company, Ltd.	Metal-insensitive epitaxy formation
US9653605B2	2014-10-17	2017-05-16	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin field effect transistor (FinFET) device and method for forming the same
US9679978B2 *	2015-09-24	2017-06-13	Samsung Electronics Co., Ltd.	Semiconductor device and method for fabricating the same
KR102413371B1	2015-11-25	2022-06-28	삼성전자주식회사	Semiconductor device
US9570567B1	2015-12-30	2017-02-14	Taiwan Semiconductor Manufacturing Co., Ltd.	Source and drain process for FinFET
CN107275399B *	2016-04-06	2022-06-28	联华电子股份有限公司	Semiconductor element and manufacturing method thereof
CN107958935B *	2016-10-18	2020-11-27	中芯国际集成电路制造(上海)有限公司	Fin-type field effect transistor and method of forming the same
US9812363B1 *	2016-11-29	2017-11-07	Taiwan Semiconductor Manufacturing Company, Ltd.	FinFET device and method of forming same
CN110957220B *	2018-09-27	2023-04-25	中芯国际集成电路制造(上海)有限公司	Semiconductor structure and forming method thereof
CN119653769B *	2024-11-29	2025-12-16	北京大学	Semiconductor structure fabrication methods, semiconductor structures, devices and equipment

* Cited by examiner, † Cited by third party, ‡ Family to family citation

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Publication	Publication Date	Title
US9318609B2	2016-04-19	Semiconductor device with epitaxial structure
US9337193B2	2016-05-10	Semiconductor device with epitaxial structures
US10014227B2	2018-07-03	Semiconductor device having strained fin structure and method of making the same
US8796695B2	2014-08-05	Multi-gate field-effect transistor and process thereof
US8575708B2	2013-11-05	Structure of field effect transistor with fin structure
US8853013B2	2014-10-07	Method for fabricating field effect transistor with fin structure
US9397184B2	2016-07-19	Semiconductor device having metal gate and manufacturing method thereof

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US9093477B1	2015-07-28	Implantation processing step for a recess in finFET
US9583394B2	2017-02-28	Manufacturing method of semiconductor structure
US20160020323A1	2016-01-21	Semiconductor device and method of fabricating the same
US9685541B2	2017-06-20	Method for forming semiconductor structure
US9780169B2	2017-10-03	Semiconductor structure having epitaxial layers
CN102956453B	2017-02-22	Semiconductor device and manufacturing method thereof
US20160190011A1	2016-06-30	Epitaxial structure and process thereof for forming fin-shaped field effect transistor
US9450094B1	2016-09-20	Semiconductor process and fin-shaped field effect transistor
CN104241360B	2019-07-23	Semiconductor device and method for fabricating the same
US20220246761A1	2022-08-04	Semiconductor device and method for fabricating the same
TW201448120A	2014-12-16	Semiconductor device and fabrication method thereof
US8709910B2	2014-04-29	Semiconductor process
TWI543370B	2016-07-21	Mos transistor process

Priority And Related Applications

Parent Applications (1)

Application	Priority date	Filing date	Relation	Title
US13/913,511	2013-06-09	2013-06-09	Division	Semiconductor device and fabrication method thereof

Priority Applications (1)

Application	Priority date	Filing date	Title
US14/620,209	2013-06-09	2015-02-12	Semiconductor device with epitaxial structure

Applications Claiming Priority (2)

Application	Filing date	Title
US13/913,511	2013-06-09	Semiconductor device and fabrication method thereof
US14/620,209	2015-02-12	Semiconductor device with epitaxial structure

Legal Events

Date	Code	Title	Description
2015-02-12	AS	Assignment	**Owner name**: UNITED MICROELECTRONICS CORP., TAIWAN **Free format text**: ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNORS:HUNG, YU-HSIANG;FU, SSU-I;CHANG, CHUNG-FU;AND OTHERS;SIGNING DATES FROM 20130502 TO 20130603;REEL/FRAME:034954/0176
2016-03-30	STCF	Information on status: patent grant	**Free format text**: PATENTED CASE
2019-09-05	MAFP	Maintenance fee payment	**Free format text**: PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1551); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY **Year of fee payment**: 4
2023-08-06	MAFP	Maintenance fee payment	**Free format text**: PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1552); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY **Year of fee payment**: 8
2023-10-20	AS	Assignment	**Owner name**: MARLIN SEMICONDUCTOR LIMITED, IRELAND **Free format text**: ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:UNITED MICROELECTRONICS CORPORATION;REEL/FRAME:065294/0055

Effective date: 20231013

Concepts

machine-extracted

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Name	Sections	Count	Query match
semiconductor	title,claims,abstract,description	44	0.000
isolation	claims,abstract,description	54	0.000
substrate	claims,abstract,description	29	0.000
spacer group	claims,description	22	0.000
silicon	claims,description	14	0.000
silicon	claims,description	13	0.000
Silicon	claims,description	9	0.000
Silicon-germanium	claims,description	7	0.000
metal	claims,description	5	0.000
metal	claims,description	5	0.000
silicon carbide	claims,description	5	0.000
[Si].[Ge]	claims,description	3	0.000
silicon carbide	claims,description	3	0.000

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