A Folded-channel MOSFET for Deep-sub-tenth Micron Era

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Deep-sub-tenth micron MOSFETs with gate length down to 20 nm are reported. To improve the short channel effect immunities, a novel "Folded Channel Transistor" structure is proposed. The quasi-planar nature of this new variant of the vertical double-gate SOI MOSFETs [1],[2] simplified the fabrication process. The special features of the structure (Fig. 1) are: (1) a transistor is formed in a vertical ultra-thin Si fin and is controlled by a double-gate, which suppresses short channel effects; (2) the two gates are self-aligned and are aligned to the S/D; (3) S/D is raised to reduce the parasitic resistance; (4) new low-temperature gate or ultra-thin gate dielectric materials can be used because they are deposited after the S/D; and (5) the structure is quasi-planar because the Si fins are relatively short.

Figure 2 shows the process flow and the SEM pictures at two fabrication steps. Using SOI wafers as the starting material, Si_3N_4 and SiO_2 layer were deposited on the 50-nm SOI layer. Using 100 keV EB lithography and ashing technique, ~20 nm wide Si fins were patterned and etched. Then, 100-nm P-doped a-Si and 300-nm SiO_2 were deposited and the result is shown in the top SEM picture. The a-Si becomes polycrystalline later and provides a good contact at the side surface of the Si fin. After delineating the a-Si S/D pattern, SiO_2 spacers were formed on the side-walls of the S/D. Through sufficient over-etching, SiO_2 was removed from the sides of the relatively low Si fins. The top-view SEM picture shows a 15-nm thin Si fin visible in the 50-nm spacer gap, which determines the gate length. After growing 2.5-nm gate oxide on the side surfaces of the Si fin, B-in-situ-doped SiGe (60% Ge) was deposited as the gate. During the gate oxidation, P was diffused from the raised S/D into the Si fin region to form S/D extension. We did not use metal electrodes in this experiment so that additional S/D extension diffusion can be optimized. This explains the large parasitic resistance of over 3000 ohm/device. The W of the devices is twice the height of the Si fins or approximately 100 nm.

Typical I-V characteristics of 30-nm gate length are shown in Fig. 3. In spite of low channel impurity concentration (10^{16} cm^{-3}), the leakage current caused by DIBL was well suppressed. The Vt roll-off characteristics of a 20-nm Si width devices are shown in Fig. 4. Vt is defined as the gate voltage when Ids=10^{-10} A. Good roll-off characteristics are observed for folded channel structure. Figure 5 shows the subthreshold swing dependence on the Si width. Since the thin body of the double-gate device prevents the punch-through, the folded channel devices show small swings. In Fig. 6, the transconductance (Gm) are plotted with the Si width as a parameter. Interestingly, Gm peaks at 30-nm of Si width. This is because that the thin body increases the parasitic resistance but also can increase the mobility and reduce the charge centroid, resulting in an optimum in the Si width. Finally, to achieve high current drivability and demonstrate discretely variable W, multiple fin devices are fabricated as shown in Fig. 7.

In conclusion, a folded channel structure is demonstrated in deep-sub-tenth micron region suitable for terabit-scale integration.

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[1] D. Hisamoto et al., IEEE Trans. Electron Devices, vol. 38, pp. 1419-1424, 1991.
[2] B. Majkusiak et al., IEEE Trans. Electron Devices, vol. 45, pp. 1127-1134, 1998.

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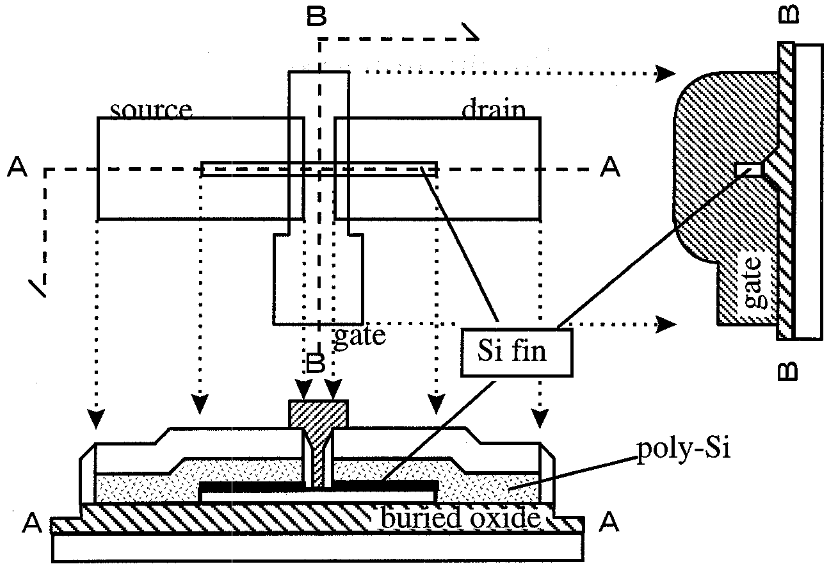

Fig. 1 Folded channel MOSFET layout design and device structure. The bottom is A-A cross section, and the right is B-B cross section

SiO_2/Si_3N_4

Si

(1) After depositing Si_3N_4 and SiO_2 stacked layer, Si fin was formed.

(2) Phosphorus-doped-poly Si and SiO_2 stacked layer deposited.

(3) Source and drain were etched while Si fin was covered by the mask layer.

(4) Spacer SiO_2 layer was etched down into buried oxide layer.

(5) After depositing B-doped SiGe, gate pattern was delineated

50 nm

Cross sectional SEM picture of 15-nm Si vertical fin. The height is 50 nm.

source

buried oxide step

Si fin

drain

Top view of channel region after spacer etching. The spacer gap between source and drain is 50 nm.

Fig. 2 Folded channel MOSFET process flow

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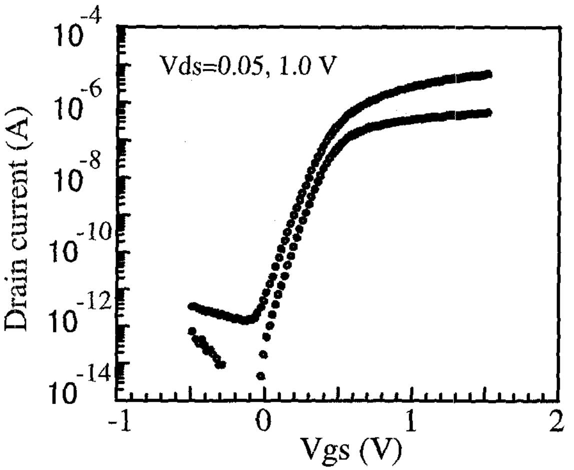

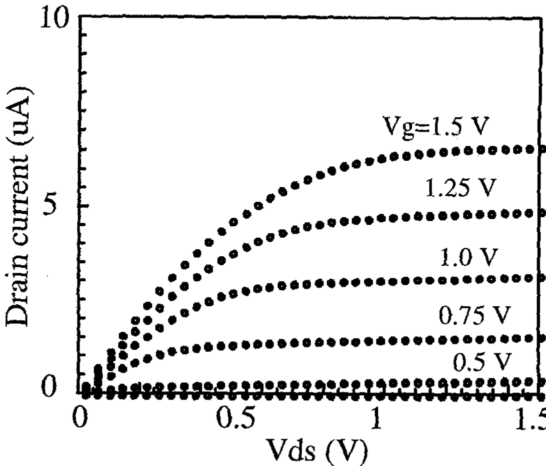

Fig. 3 Folded channel MOSFET I-V characteristics for 30-nm gate length and 20-nm Si width.

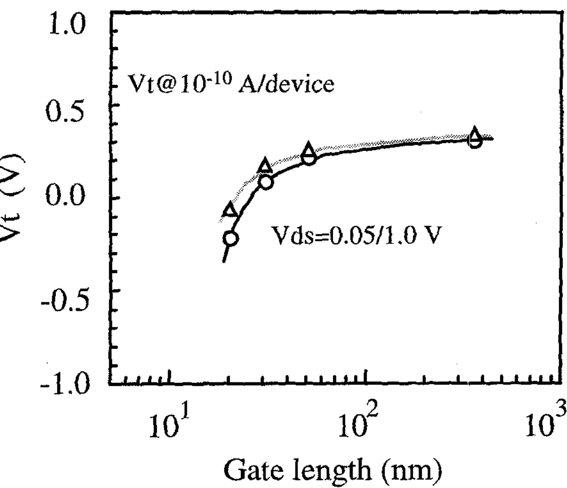

Fig. 4 Threshold voltage dependence on gate length for 20-nm Si width.

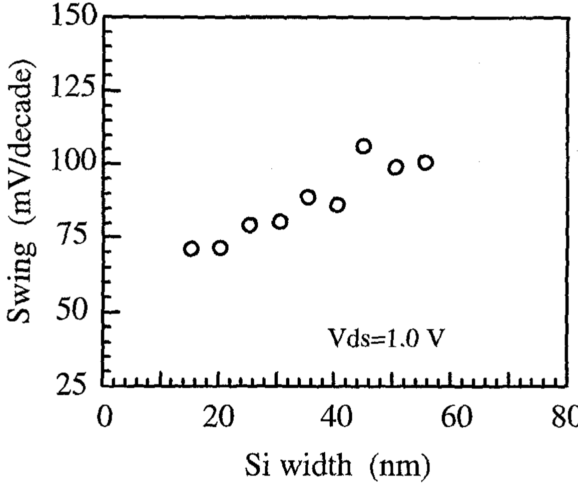

Fig. 5 Subthreshold swing vs. Si width. Gate length is 30 nm.

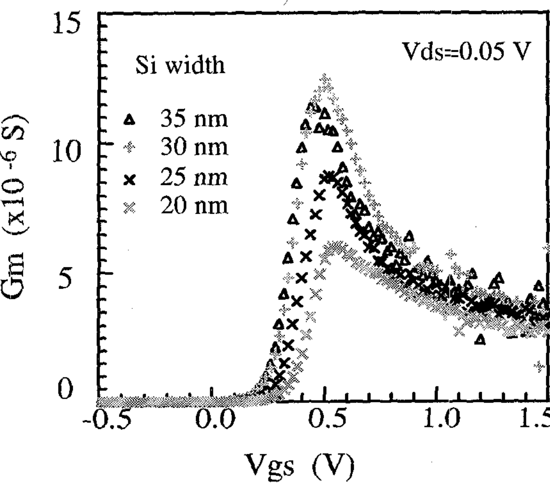

Fig. 6 Transconductance characteristics for various Si width.

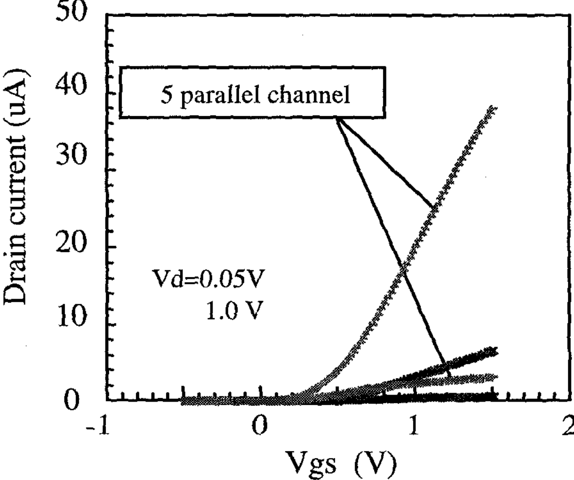

Fig. 7 Current drivability comparison between single channel and 5-parallel channel device

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