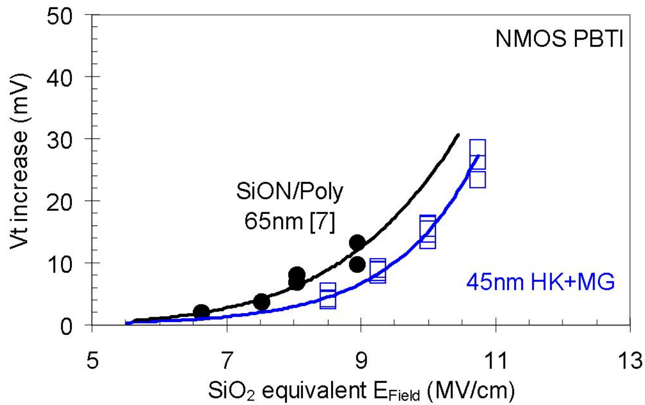

Fig. 15 NMOS PBTI V_T shift vs. electric field

concerns have been overcome. Oxide breakdown (Fig. 13) is improved relative to 65nm SiON transistors, supporting 30% higher E-field. PMOS NBTI (Fig. 14) is improved compared to 65nm SiON transistors at the same E-field and is matched at 50% higher E-field. NMOS PBTI (Fig. 15) is better than 65nm and supports 15% higher E-field; the net BT shift for NMOS and PMOS is matched to 65nm at 30% higher field. Note that while NMOS transistors are considered stable for SiON/Poly, they actually show PBTI at very high E-fields.

INTERCONNECTS

Nine layers of copper interconnect are employed along with low-k CDO dielectrics (Fig. 16). Lower layer metal pitches are matched to the contacted gate pitch, while upper layer metal pitches increase progressively to optimize density and performance. Compared to 65nm [7] interconnect capacitance is reduced by aggressive scaling of the SiCN etch stop layer, and by extending the use of CDO to more layers, including Metal-1. The Metal-9 layer is very thick and is used for improved on-die power distribution. Packaging is 100% Pb-free with Cu bumps and SnAgCu solder. Interconnects are optimized to reliably withstand the added stress of Pb-free packaging on CDO films.

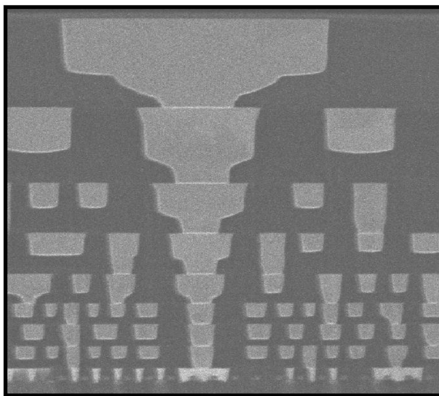

Fig.16 Cross-section of 8 of the 9 Cu interconnect layers

SRAM AND PRODUCTS

The 45nm yield learning vehicle was a 153Mbit SRAM featuring a 0.346μm^2 SRAM cell and over a billion transistors. The first fully functional 45nm 153Mb SRAM was reported in Jan 2006; yields are now at mature levels. The SRAM has demonstrated 3.8 Ghz operating frequency at 1.1V power supply and stable low voltage operation (Fig. 17). High yield has also been demonstrated on microprocessors for server, desktop, mobile & handheld applications (Fig. 18).

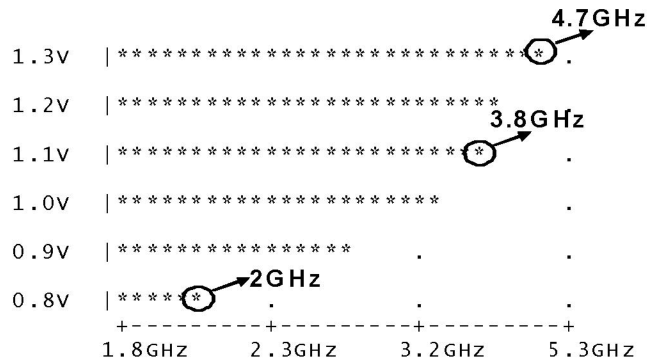

Fig. 17 Voltage-Frequency shmoo for 153Mb SRAM

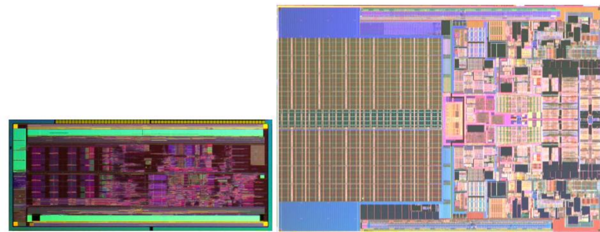

Fig. 18 Die photos of single core & dual core microprocessors

CONCLUSIONS

For the first time, high-k + metal gate transistors have been integrated into a manufacturable 45nm process. Combined with third generation strained silicon these transistors provide record drive current at low leakage and at tight contacted gate pitch. Ring oscillators demonstrate 23% gate delay reduction compared to 65nm [8] at the same I_{OFF} and 10% lower V_{DD}.

Low-k CDO is employed for low interconnect RC delay and is integrated with 100% Pb-free packaging. Aggressive pitch scaling and trench contact based local routing achieve good layout density, while low cost is maintained using novel 193nm dry patterning techniques for critical layers. The technology maintains historical scaling trends for performance and density. Mature yield has been demonstrated and the technology is now in high volume manufacturing.

REFERENCES

1. V. Misra, G. Lucovsky,and G. Parsons, "Issues in High-k Gate Stack Interfaces," *MRS Bull.*, vol. 27, no. 3, pp. 212-216, 2001.
2. C. Hobbs *et al.*, "Fermi Level Pinning at the Poly-Si/Metal Oxide Interface," in *Symp. VLSI Tech. Dig.*, pp. 9-10, 2003.
3. G. Ribes *et al.*, "Review on High-k Dielectrics Reliability," *IEEE Trans. on Device and Materials Rel.*, vol. 5, no. 1, pp. 5-19, 2005.
4. R. Kotlyar et al., "Inversion Mobility and Gate Leakage in High-k/Metal Gate MOSFETs," *IEDM Tech. Dig.*, p. 391, 2004.
5. R. Chau *et al.*, "High-k/Metal-Gate Stack and its MOSFET Characteristics," *IEEE Electron Device Lett.*,vol.25,no.6, p.408, 2004
6. K. Mistry *et al.*, "Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology," *Symp. VLSI Tech. Dig.*, pp. 50-51, 2004.
7. P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD, and 0.57μm^2 SRAM Cell" *IEDM Tech. Dig.*, pp. 657-660, 2004.
8. S. Tyagi *et al.*, "An advanced low power, high performance, strained channel 65nm technology," *IEDM Tech. Dig.*, pp. 1070-1072, 2005.
9. H. Takeuchi *et al.*, "Impact of Oxygen Vacancies on High-k Gate Stack Engineering" *IEDM Tech. Dig.*, pp. 829-832, 2004.

TSMC Exhibit 1019