High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress Liners Using Gate-Last Damascene Process on (100) Substrates

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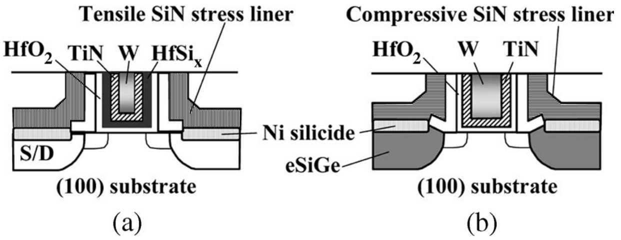
***Abstract*—Newly proposed mobility-booster technologies are demonstrated for metal/high-k gate-stack n- and pMOSFETs. The process combination of top-cut SiN dual stress liners and damascene gates remarkably enhances local channel stress particularly for shorter gate lengths in comparison with a conventional gate-first process. Dummy gate removal in the damascene gate process induces high channel stress, because of the elimination of reaction force from the dummy gate. PFETs with top-cut compressive stress liners and embedded SiGe source/drains are performed by using atomic layer deposition TiN/HfO$_2$ gate stacks with $T_{\rm inv} = 1.4$ nm on (100) substrates. On the other hand, nFETs with top-cut tensile stress liners are obtained by using HfSi$_x$/HfO$_2$ gate stacks with $T_{\rm inv} = 1.4$ nm. High-performance n- and pFETs are achieved with $I_{\rm on} = 1300$ and 1000 μA/μm at $I_{\rm off} = 100$ nA/μm, $V_{\rm dd} = 1.0$ V, and a gate length of 40 nm, respectively.**

***Index Terms*—HfO$_2$, HfSi$_x$, Channel stress, damascene gate, electron mobility, embedded SiGe (eSiGe), gate last, high-k, hole mobility, metal gate, replacement gate, stress simulation, TiN, top-cut stress liner.**

I. INTRODUCTION

METAL/HIGH-k gate stacks have been recently investigated for $T_{\rm inv}$ scaling, the reduction of gate leakage currents, and the suppression of $V_{\rm th}$ variations. The gate-last damascene process having dual band-edge work function metals is one of the candidates to achieve high-performance MOSFETs [1]–[4]. The damascene gate process has an advantage in the work function stability of metal electrodes to accomplish low $V_{\rm th}$ MOSFETs, because of the low-temperature process. Moreover, we have reported that the damascene gate process considerably enhances channel stress from embedded SiGe (eSiGe) source/drains, due to dummy gate removal [5]. The SiN stress liner is another important technology to enhance MOSFETs performance [6], [7]. The stress liners that are applied for the damascene gate devices are cut to remove the dummy gates, as shown in Fig. 1. It has been reported that discontinuous stress liners maintain high mobility for fully silicided gate MOSFETs [8]. However, the effects have been unclear for the damascene gate devices using the stressors yet.



(a) (b)

Fig. 1. Schematic diagrams of metal/high-k gate stack MOSFETs with top-cut stress liners using damascene gate process. (a) nFET. (b) pFET. Stress liners are cut on the top of gate electrodes.

In this paper, we present drivability effects on metal/high-k MOSFETs using the SiN stress liners with the damascene gate process and eSiGe. After device fabrication, channel stresses from both the top-cut dual stress liners and eSiGe will be discussed by using stress and mobility simulations in the damascene gate process. Then n- and pFETs with the stress enhancement technologies using dual work function metal/high-k gates are going to be demonstrated. After that, the advantages in the damascene gate technologies are going to be described by using benchmarks.

II. EXPERIMENTS

Cross-sectional structures of n- and pFETs are schematically shown in Fig. 1. The devices consist of metal/high-k gate stacks, top-cut SiN stress liners, and eSiGe, for only pFETs, on (100) substrates. A flow of device fabrication is shown in Fig. 2. MOSFETs are fabricated on the basis of the gate-last damascene process. After poly-Si dummy gate formation, Si recess was carried out and selective epitaxial films of eSiGe were formed by using dummy gates and spacers for only pFETs. SiN stress liners with 1.6-GPa tensile stress (t-SL) and 2.0-GPa compressive stress (c-SL) were deposited for n- and pFETs, respectively, after Ni silicidation. The stress liners were cut only on the top of dummy gates by using CMP to expose dummy gate tops after premetal dielectric (PMD) deposition. To improve mobility in the thinner $T_{\rm inv}$ region, ozone water treatment was used prior to HfO$_2$ atomic layer deposition (ALD) after dummy gate removal [9]. After postdeposition anneal at 500 °C, HfSi$_x$ was deposited by utilizing physical vapor deposition for

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- ● (100) Substrate
- ● Dummy Gate and Dummy Spacer Formations
- ○ Si Recess (60nm) and SiGe S/D Epi (only pFETs)
- ● Dummy Spacer Removal
- ● Extension/Halo I/I's
- ● Main Spacer and S/D I/I
- ● Silicidation
- ● Stress Liners Deposition
- ● (1.6GPa tensile / 2.0GPa compressive SiN films)
- ● PMD Deposition and CMP
- ● Dummy Gate Removal
- ● Pre-treatment (Ozone Water)
- ● HfO_2 Deposition and PDA (500°C)
- ○ $HfSi_x$ Depositon (only nFETs)
- ● TiN Deposition

Fig. 2. Fabrication flow using gate-last damascene process for metal/high-k gate MOSFETs with SiN stress liners and eSiGe on (100) substrates.

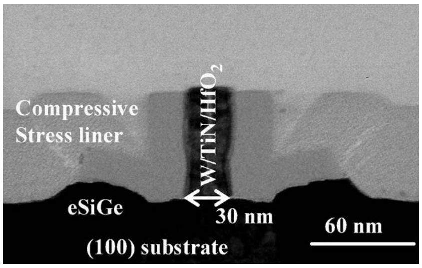

Fig. 3. Cross-sectional TEM image of pFET with W/TiN/HfO_2 gate stacks, c-SL, and eSiGe on (100) substrate. MOSFETs with 30-nm gate length were fabricated.

only nFETs. Following that, TiN was formed by using ALD for n- and pFETs. Fig. 3 shows a cross-sectional transmission-electron-microscope (TEM) image of a fabricated pFET. We successfully integrated top-cut stress liners into damascene gate devices with eSiGe and 30-nm gate length. For reference, metal/high-k and poly-Si/SiO_2 gate MOSFETs without top-cut stress liners were also fabricated.

III. STRESS AND MOBILITY SIMULATIONS

To investigate stress distributions around a channel, we simulated lateral (S_{xx}) and vertical (S_{zz}) stress distributions at four critical steps in the fabrication process: (a) after c-SL deposition; (b) after PMD CMP; (c) after dummy gate removal; and (d) after metal gate formation. Simulated S_{xx} and S_{zz} distributions around the channel of pFETs are shown in Figs. 4 and 5, where a gate length is 40 nm, and eSiGe and c-SL thicknesses are 80 and 60 nm, respectively. Fig. 6 shows average channel stress between the gate center and edge at a depth of 1 nm from the Si surface for simulated S_{xx} and S_{zz}, and relative hole mobility, corresponding to the four process steps in Figs. 4 and 5. The relative hole mobility was calculated by using simulated average values of the S_{xx} and S_{zz}, and piezoresistance coefficients [10]

$$\frac{\mu_{h_{\mathrm{xx}}}}{\mu_{h_0}} = 1 - 0.718 S_{\mathrm{xx}} + 0.663 S_{\mathrm{yy}} + 0.011 S_{\mathrm{zz}} \qquad (1)$$

where $\mu_{h_{\mathrm{xx}}}$, μ_{h_0}, and S_{yy} are hole mobility in lateral, hole mobility without stress, and channel stress along the y-axis (Fig. 4), respectively. Equation (1) indicates that the hole mobility is enhanced by increases in compressive and tensile stress for the S_{xx} and S_{zz}, respectively, and also that the coefficient of the S_{xx} is approximately 70 times larger than that of the S_{zz}. As shown in Fig. 6, compressive S_{xx} after the PMD CMP slightly decreases in comparison with that after the c-SL deposition. However, after the dummy gate removal, compressive S_{xx} dramatically increases because of the elimination of reaction force from the dummy gate. On the other hand, tensile S_{zz} after the metal gate formation decreases, as compared to that after the c-SL deposition. Despite the decrease in the tensile S_{zz}, the hole mobility after the metal gate formation is greater than that after the c-SL deposition due to the large compressive S_{xx}, as shown in Fig. 6 and its large coefficient in (1).

Similarly, calculated average channel stress and relative electron mobility for nFETs are shown in Fig. 7, where a gate length and t-SL thickness are 40 and 25 nm, respectively. The relative electron mobility is expressed as

$$\frac{\mu_{e_{\mathrm{xx}}}}{\mu_{e_0}} = 1 + 0.316 S_{\mathrm{xx}} + 0.176 S_{\mathrm{yy}} - 0.534 S_{\mathrm{zz}} \qquad (2)$$

where $\mu_{e_{\mathrm{xx}}}$ and μ_{e_0} are electron mobility in lateral and without stress, respectively. Equation (2) indicates that the electron mobility is enhanced by increases in tensile and compressive stress for the S_{xx} and S_{zz}, respectively. After the metal gate formation, tensile S_{xx} and S_{zz} increase, as compared to those after the t-SL deposition. Because of the relatively large coefficient of the S_{zz} in (2), an increase in the electron mobility are small in comparison with that in the hole mobility. However, due to the comparatively large increase in the tensile S_{xx}, the electron mobility after the metal gate formation is slightly higher than that after the t-SL deposition. Therefore, it is considered that both the hole and electron mobilities of damascene gate MOSFETs are enhanced by applying each top-cut stress liner.

IV. RESULTS AND DISCUSSION

A. Characteristics of pFETs

The dependence of peak transconductances $(g_{m,\mathrm{peak}})$ on gate length for no-eSiGe pFETs with and without the c-SL is shown in Fig. 8. V_{th} roll-off characteristics of the devices are almost the same. Higher $g_{m,\mathrm{peak}}$ indicates hole mobility enhancement because of the top-cut c-SL in the damascene gate process. Fig. 9 shows I_{on} dependence on $1/T_{\mathrm{inv}}$ for poly-Si/SiO_2 and TiN/HfO_2 gate stacks without eSiGe. The I_{on} is extracted at $I_{\mathrm{off}} = 100$ nA/μm and $V_{\mathrm{gs}} = V_{\mathrm{ds}} = -1.0$ V. A 60-nm c-SL achieves 46% I_{on} enhancement. Fig. 10 shows the relationship between normalized $I_{\mathrm{on}}(I_{\mathrm{off}} = 100$ nA/μm, $V_{\mathrm{ds}} = V_{\mathrm{gs}} = -1.0$ V$)$ and c-SL thicknesses with and without eSiGe. The I_{on} increases with an increase in the c-SL thickness. The combination of a 40-nm c-SL and 80-nm eSiGe achieves more than 200% I_{on} enhancement in comparison with neither c-SL nor eSiGe. Therefore, it is confirmed that the drivability of eSiGe-S/D pFETs is further enhanced by the top-cut c-SL.

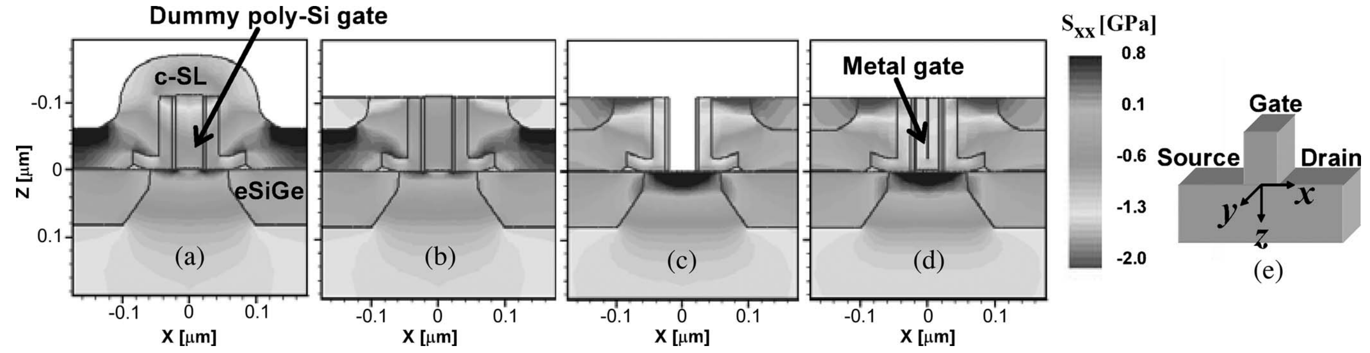

Fig. 4. Simulated lateral channel stress (S_{xx}) distributions for pFETs. (a) After c-SL deposition. (b) After PMD CMP. (c) After dummy gate removal. (d) After metal gate formation. (e) Axial directions in stress simulation. A gate length is 40 nm, and eSiGe and c-SL thicknesses are 80 and 60 nm, respectively.

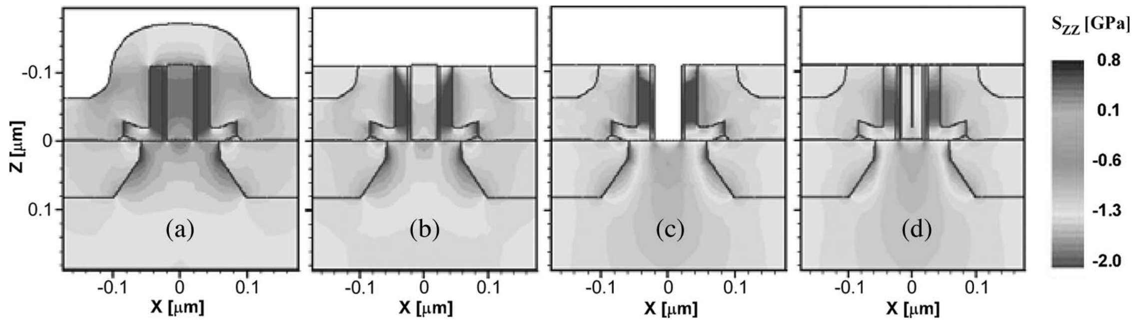

Fig. 5. Simulated vertical channel stress (S_{zz}) distributions for pFETs. Symbols of (a) to (d) correspond to the process steps, as shown in Fig. 4.

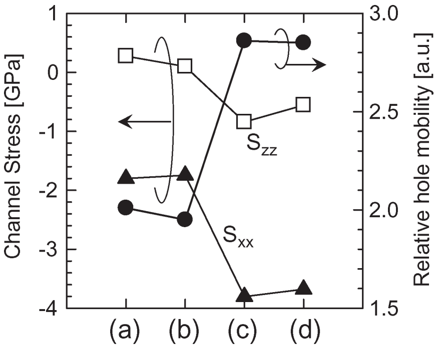

Fig. 6. Simulated S_{xx} and S_{zz} and relative hole mobility for pFETs, calculated by using piezocoefficients. Symbols of (a) to (d) correspond to the process steps, as shown in Figs. 4 and 5.

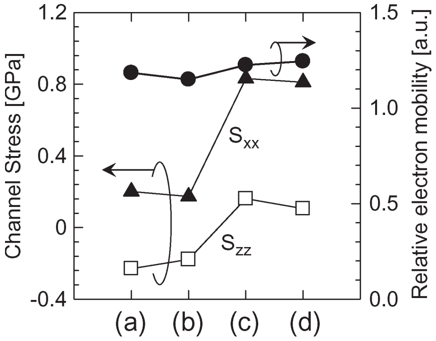

Fig. 7. Simulated S_{xx} and S_{zz} and relative electron mobility for nFETs at four critical steps in the fabrication process. (a) After t-SL deposition. (b) After PMD CMP. (c) After dummy gate removal. (d) After metal gate formation. A gate length and t-SL thickness are 40 and 25 nm, respectively.

The dependence of I_d gain on gate length, due to the top-cut c-SL, is shown in Fig. 11, where the I_d gain means a fraction of I_d with and without the top-cut c-SL at a gate overdrive ($V_{\mathrm{gs}} - V_{\mathrm{th}}$) of -0.7 V. The I_d gain increases continuously with a decrease in the gate length for both linear and saturation regions. On the other hand, conventional gate-first pFETs have been reported that the I_d gain is saturated due to an increase in the surface doping concentration [6], [7]. This is possibly because of the process combination of the top-cut c-SL, eSiGe, and damascene gate. It seems that high channel stress is induced even for damascene gate pFETs with shorter gate lengths. Fig. 12 shows I_{on}–I_{off} characteristics at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = -1.0$ V, where c-SL and eSiGe thicknesses are 40 and 80 nm, respectively. I_{on} enhancement rates at $I_{\mathrm{off}} = 100$ nA$/\mu$m are 28% for no eSiGe and 35% for eSiGe devices. Excellent drivability enhancement is achieved by using the top-cut c-SL and eSiGe for the damascene gate pFETs as supported by stress and mobility simulations.

B. Characteristics of nFETs

The dependence of $g_{m,\mathrm{peak}}$ on gate length is shown in Fig. 13, where a t-SL thickness is 25 nm. Fig. 14 shows the I_{on}–$1/T_{\mathrm{inv}}$ relationship for poly-Si/SiO$_2$ and HfSi$_x$/HfO$_2$ gate stack devices, where the I_{on} is extracted at $I_{\mathrm{off}} = 100$ nA$/\mu$m and $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.0$ V. Higher $g_{m,\mathrm{peak}}$ and 10% I_{on} enhancement are achieved by using the 25-nm top-cut t-SL. These results indicate that channel stress enhanced by the process combination of the top-cut t-SL and damascene gate improves the electron mobility. Fig. 15 shows I_d gain dependence on gate length, due to the top-cut t-SL, for linear and saturation currents, where gate overdrive is constant. I_d gains still increase

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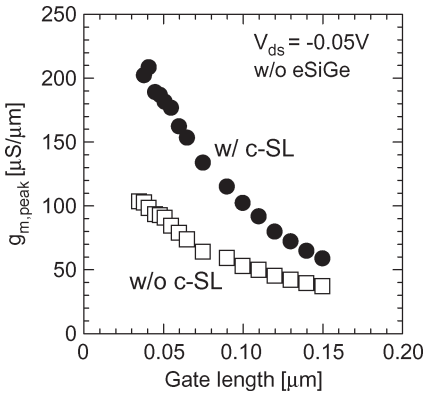

Fig. 8. Peak transconductance ($g_{m,\mathrm{peak}}$) dependence on gate length for no-eSiGe pFETs with and without 60-nm c-SL.

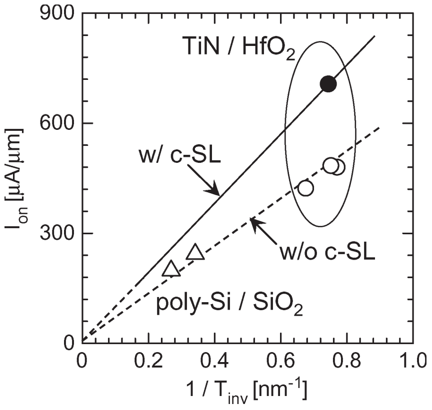

Fig. 9. I_{on} dependence on $1/T_{\mathrm{inv}}$ for poly-Si/SiO$_2$ and TiN/HfO$_2$ gate stack pFETs without eSiGe. A c-SL thickness is 60 nm, and the I_{on} is extracted at $I_{\mathrm{off}} = 100$ nA/μm, $V_{\mathrm{gs}} = V_{\mathrm{ds}} = -1.0$ V. By using the top-cut c-SL, 46% I_{on} enhancement is achieved.

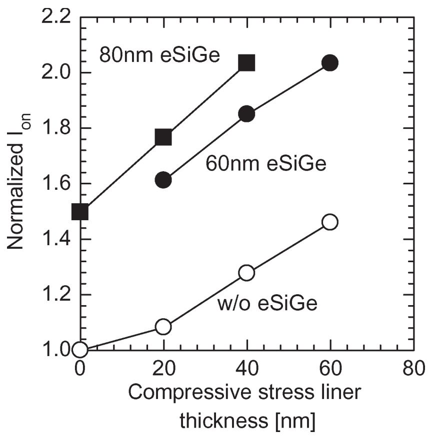

Fig. 10. Normalized I_{on} dependence on c-SL thickness with and without eSiGe for pFETs, where I_{on} is extracted at $I_{\mathrm{off}} = 100$ nA/μm, $V_{\mathrm{ds}} = V_{\mathrm{gs}} = -1.0$ V. More than 200% I_{on} enhancement is achieved by the device with a 40-nm c-SL and 80-nm eSiGe in comparison with the no-stressor device.

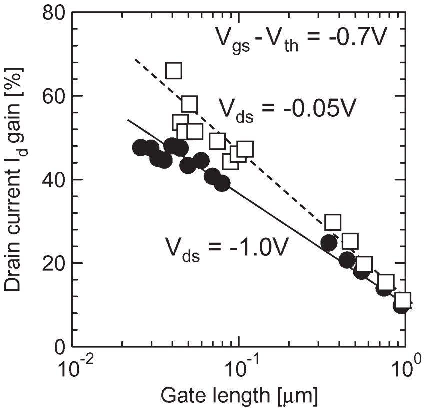

Fig. 11. I_d gain dependence, due to top-cut c-SL, on gate length for pFETs, where V_{gs} overdrive is constant. C-SL and eSiGe thicknesses are 40 and 80 nm, respectively. The I_d gains are plotted for both linear ($V_{\mathrm{ds}} = -0.05$ V) and saturation ($\mathrm{V_{ds}} = -1.0$ V) regions.

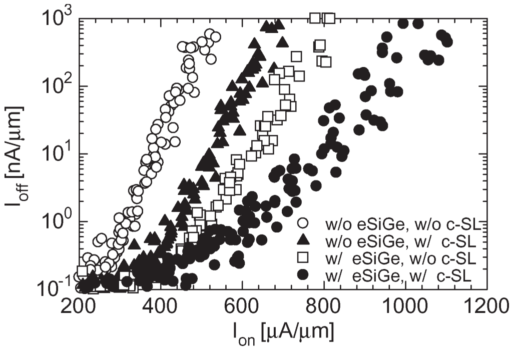

Fig. 12. I_{on}–I_{off} characteristics of pFETs with and without 40-nm c-SL and 80-nm eSiGe, at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = -1.0$ V. I_{on} enhancement rates at $I_{\mathrm{off}} =$ 100 nA/μm are 28% for no eSiGe and 35% for eSiGe devices.

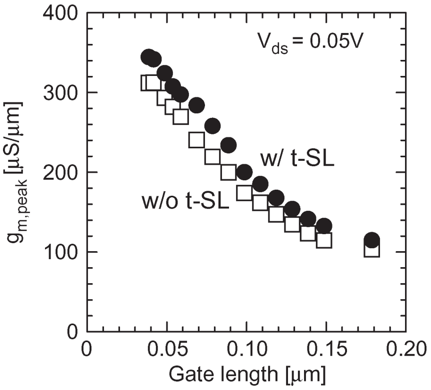

Fig. 13. Dependence of $g_{m,\mathrm{peak}}$ on gate length for nFETs with and without 25-nm t-SL. V_{th} roll-off characteristics of the devices are almost the same.

even for shorter gate lengths. High channel stress in shorter gate lengths is probably caused by the process combination of the top-cut t-SL and damascene gate as well as pFETs. I_{on}–I_{off} characteristics are shown in Fig. 16. An I_{on} gain at $I_{\mathrm{off}} = 100$ nA/μm and $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.0$ V is approximately 10%. As supported by stress and mobility simulations, high drive currents for nFETs are also achieved by using the top-cut t-SL in the damascene gate process.

V. BENCHMARKS OF CMOS DEVICES

In this section, the performances achieved by this paper are summarized and the benchmark data are shown to compare with recently published data for high-performance MOSFETs. Figs. 17 and 18 show I_d–V_{gs} and I_d–V_{ds} characteristics of 40-nm gate length MOSFETs with top-cut stress liners. High

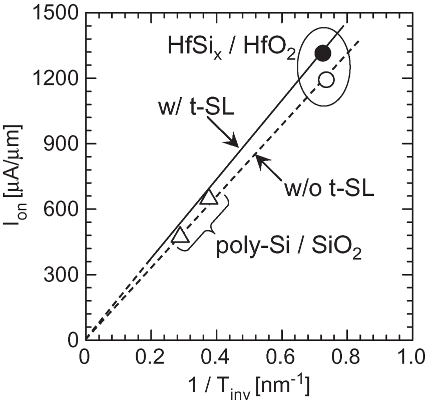

Fig. 14. $I_{\rm on}$–$1/T_{\rm inv}$ relationship between poly-Si/SiO$_2$ and HfSi$_x$/HfO$_2$ gate stacks, where t-SL thickness is 25 nm. The $I_{\rm on}$ is extracted at $I_{\rm off} = 100$ nA/μm, $V_{\rm ds} = V_{\rm gs} = 1.0$ V.

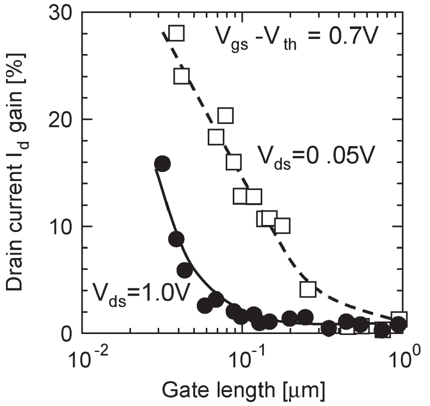

Fig. 15. Dependence of I_d gain, due to top-cut t-SL, on gate length for nFETs at $V_{\rm gs} - V_{\rm th} = 0.7$ V, where t-SL thickness is 25 nm. The I_d gains are plotted for both linear ($V_{\rm ds} = 0.05$ V) and saturation ($V_{\rm ds} = 1.0$ V) currents.

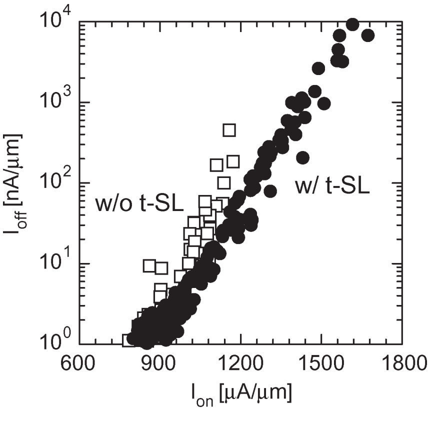

Fig. 16. $I_{\rm on}$–$I_{\rm off}$ characteristics of nFETs at $V_{\rm ds} = V_{\rm gs} = 1.0$ V. A t-SL thickness is 25 nm. An $I_{\rm on}$ gain at $I_{\rm off} = 100$ nA/μm is approximately 10%.

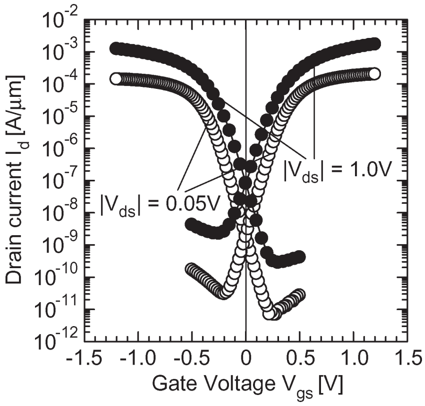

Fig. 17. I_d–$V_{\rm gs}$ characteristics of n- and pFETs at $V_{\rm ds} = 0.05$ and 1.0 V, where gate length is 40 nm. Stress liner thicknesses are 25 and 40 nm for n- and pFETs, respectively. A 80-nm eSiGe is applied for pFETs.

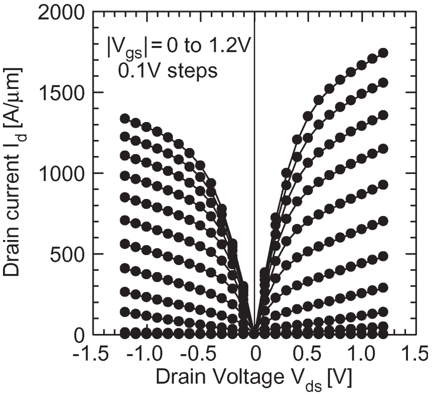

Fig. 18. I_d–$V_{\rm ds}$ characteristics of each device, as shown in Fig. 17.

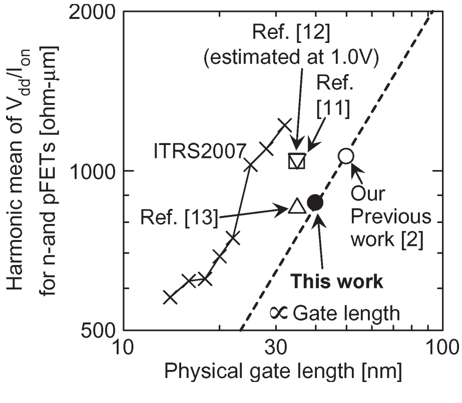

Fig. 19. Comparison of harmonic mean of $V_{\rm dd}/I_{\rm on}$ for n- and pFETs on physical gate length for this paper, our previous work, published data and ITRS2007, where $I_{\rm on}$ ratio of n- to pFET for ITRS2007 applies 1.3 : 1.

drive currents of 1300 and 1000 μA/μm at $V_{\rm dd} = 1.0$ V and $I_{\rm off} = 100$ nA/μm are remarkably obtained for n- and pFETs even on (100) substrates, respectively. The device performances compared with the published data are summarized in Table I [11]–[13]. Higher performances among the published data are achieved by our technologies. Fig. 19 shows the comparison of harmonic mean of $V_{\rm dd}/I_{\rm on}$ for n- and pFETs on physical gate length for this paper, our previous work [2], published papers (Table I) and International Technology Roadmap for Semiconductor (ITRS) 2007 [14]. It is observed that the harmonic mean of $V_{\rm dd}/I_{\rm on}$ is proportional to gate length for this and our previous works by the application of channel strain technologies along with the demand of ITRS. Furthermore, it suggests that the technologies reported in this paper would accomplish further performance enhancement in proportion to gate length by scaling.

TABLE I
PERFORMANCE COMPARISON BETWEEN THIS PAPER AND PUBLISHED DATA OF HIGH-PERFORMANCE MOSFETs

		This work	Our previous work [2]	Ref. [11]	Ref. [12]	Ref. [13]
V_{dd} [V]		1.0	1.0	1.0	1.2	1.0
Gate length [nm]		40	50	35	35	35
T_{inv} [nm]		1.4	1.6	1.2 (phy.)	1.2 (phy.)	1.0 (EOT)
nFET	I_{on} [μA/μm]	1300	1050	1210	1750	1360
	I_{off} [nA/μm]	100	100	100	100	100
pFET	I_{on} [μA/μm]	1000	830	710	1060	1070
	I_{off} [nA/μm]	100	100	100	100	100
Substrate		(100)	(110)	(100)	(100)	-

VI. CONCLUSION

The effects of top-cut stress liners for damascene gate MOSFETs were investigated by stress simulation and demonstration. These were found that the process combination of top-cut dual stress liners and damascene gates induces high channel stress and also that the I_d gain increases continuously with the decrease in the gate length for both n- and pFETs, as compared to conventional gate-first MOSFETs. These results indicated that high channel stress was induced particularly for shorter gate lengths. Therefore, high drive current n- and pFETs were successfully achieved by using top-cut stress liners with dual metal/high-k gates and eSiGe for damascene gate devices. In order to understand the mechanism of these effects on the gate length, it is needed to analyze exactly the channel strain for the damascene gate devices with short gate lengths. These technologies are strong candidates for high-performance devices in the coming generation.

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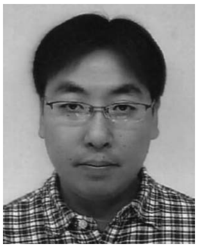

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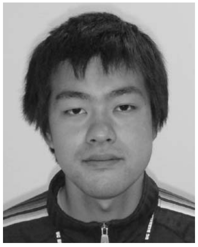

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