UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,

Patent Owner.

Case No. IPR2026-00130

U.S. Patent No. 9,318,609 B2

DECLARATION OF JOSEPH MCALEXANDER

I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

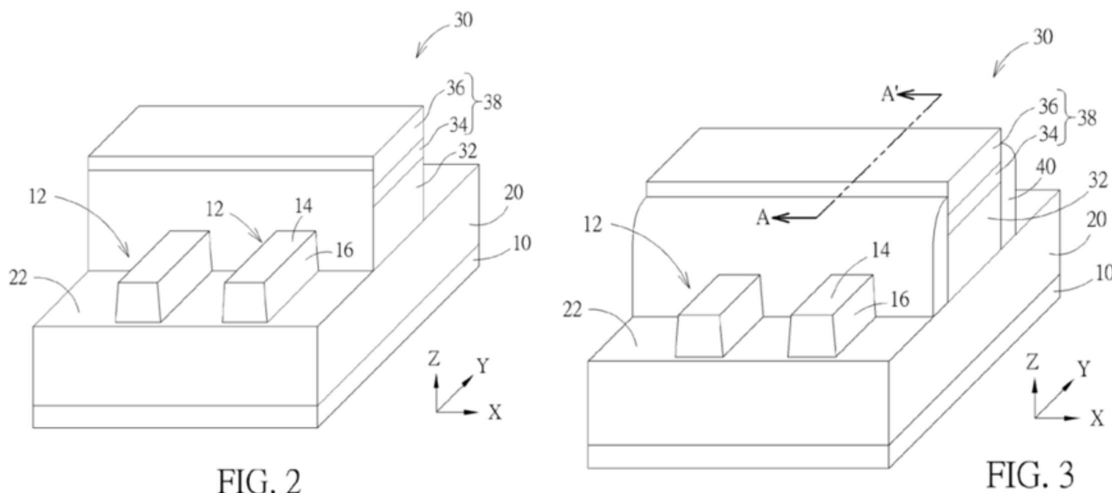
- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. OVERVIEW

4. Neither of the Petition's primary references (Xu for Grounds 1A and 1B, Ching for Grounds 2A-C) discloses or renders obvious an """isolation structure . . . ***surrounding*** the fin structure," as required by all challenged claims. An important feature of the '609 patent's claimed semiconductor device is that the

isolation structure surrounds the fin structure on all four sides, thereby completely isolating the fin structure. That the isolation structure surrounds the fin structures is confirmed by the ’609 patent’s specification, which explains that “a lower portion of each fin structure is ***embedded*** in the isolation structure 20,” indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:52-53 (emphasis added). This is further confirmed by the ’609 patent’s figures, which consistently illustrate the isolation structure 20 covering all four sides of the fin structures 12:



EX1001 at Figs. 2 and 3; *see also id.* at Fig. 5.

5. In contrast, in Xu, “isolation features 130” do not surround the fin structures on all four sides of the fins 120, but rather only cover two sides of the fins 120:

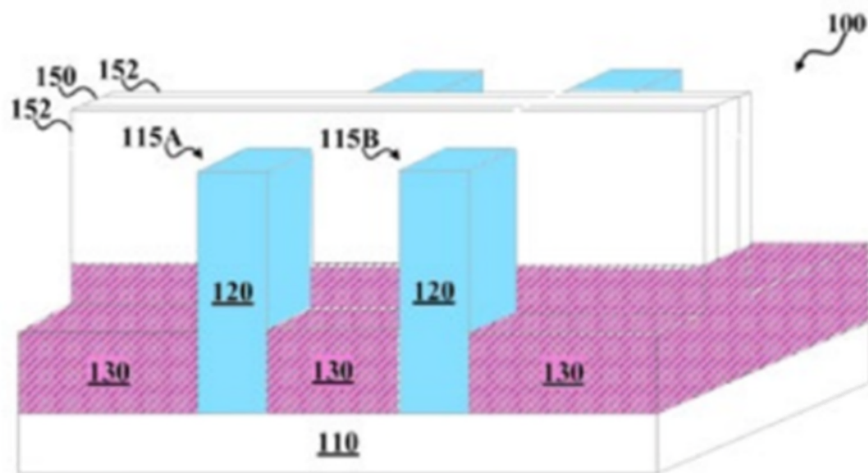


FIG. 3

Pet., 16 (showing annotated EX1004-Xu, Fig. 3).

6. Although Xu states that "[i]solation features 130 . . . surround the fin structures 115A and 115B" (EX1004-Xu at 3:54-56), a POSITA would have understood that Xu's usage of the term "surround" is inconsistent with that term as required by the claimed semiconductor device. Moreover, even if Xu's isolation features 30 are interpreted as "surrounding" fins 120, Xu's isolation features nevertheless do not surround Xu's "fin structure" because, unlike the '609 patent's claimed semiconductor device, Xu's device merges its fins together into a single, merged "fin structure." Xu explains that a "fin template 135 is formed by merging together the fins 120 of the FinFET device 100." EX1004-Xu at 5:2-4. A "semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135."

Id. at 5:8-10. Xu's Figure 4 illustrates the merging together of fins 120 to form fin template 135:

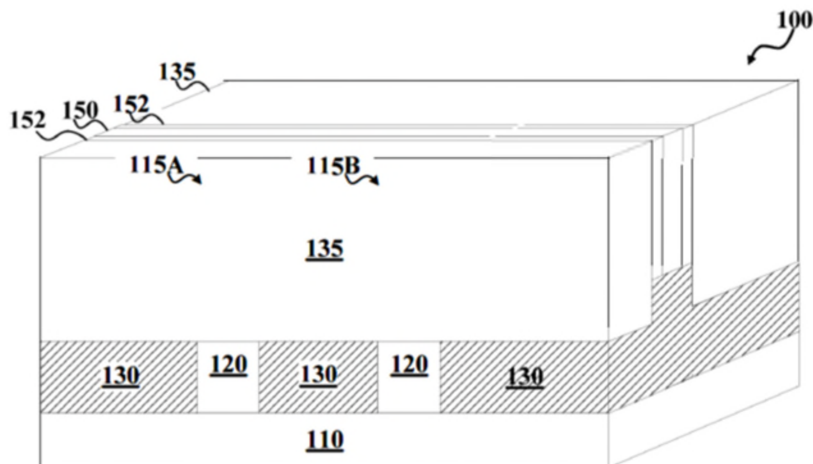


FIG. 4

Id. at Fig. 4. 58.

7. As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its fin structure because it does not enclose any side of the merged fin structure, *e.g.*, the part made up of fin template 135.

8. Similarly, in Ching, the alleged isolation structure (STI regions 22) does not surround the alleged fin structure (semiconductor strip 21) on all four sides, but rather only cover two sides of semiconductor strip 21:

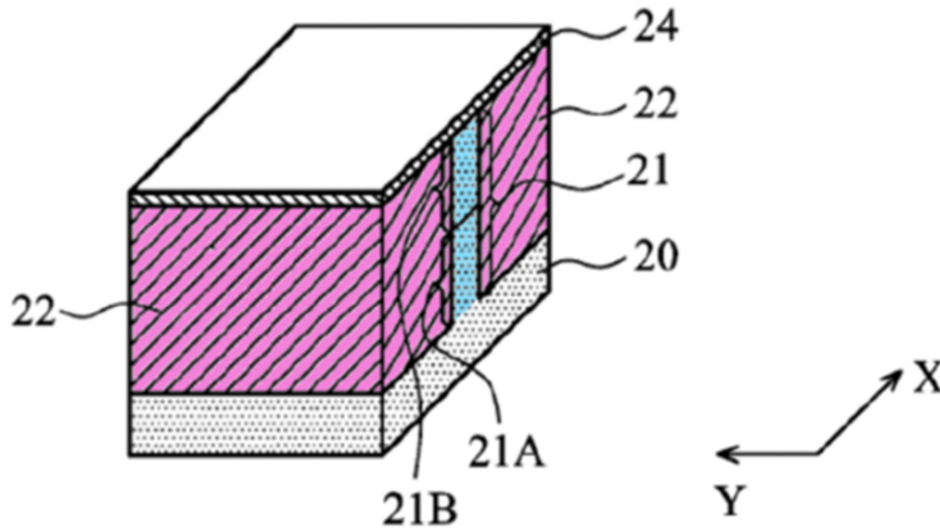


Fig. 1

Pet. at 57 (showing annotated EX1005-Ching, Fig. 1).

9. The Petition argues that "[t]o the extent the claim language requires the isolation structure to *fully* circle the fin structures . . . [a] POSITA would have further understood that, in Ching, the shallow trench isolation regions ('STI regions 22') isolate 'semiconductor strips 21' from one another *and* isolate the transistors that will ultimately be formed from 'semiconductor strips 21' from one another." Pet. at 59. But this argument is conclusory and contradicted by Ching's own disclosure, which states that "semiconductor strip 21 is formed ***between, and contacting, neighboring*** STI regions 22." EX1005-Ching at 2:5-6 (emphasis added). That Ching's semiconductor strips are formed between neighboring STI regions demonstrates that the STI regions do not surround the semiconductor strips, because

the STI regions would need to merge in order to enclose the semiconductor strips on all four sides.

III. MATERIALS CONSIDERED

10. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

IV. UNDERSTANDING OF THE LAW

11. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

12. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

a. a method claim, which covers a process/activity, or

b. an apparatus claim, which covers a physical machine, etc.

13. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

14. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

15. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

16. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

17. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other

principles may be relied on in evaluating whether a claimed invention would have been obvious.

18. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a "nexus") between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

19. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

20. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components

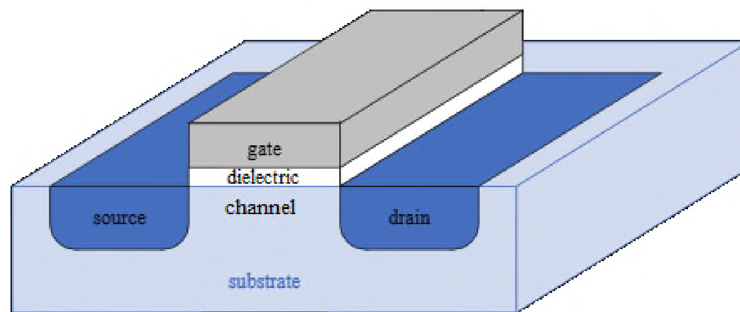
of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

A. Basic Transistor Components

21. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3.

22. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex. 2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34.

23. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See*, *e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



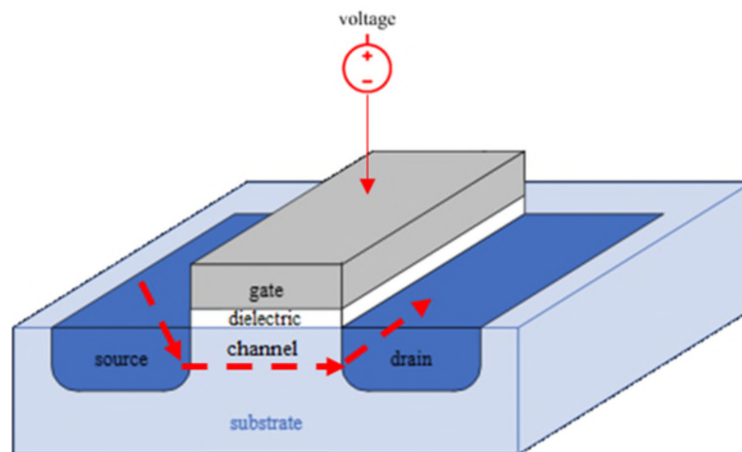
See, *e.g.*, Ex. 2002 at 510-511.

24. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511.

25. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511. When a voltage is applied to the gate, the dielectric

prevents the "flow of charge" (current) between the gate and the channel, but the applied voltage results in the creation of a "field effect" in the channel. Ex. 2002 at 510-511. This "field effect" either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511.

26. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



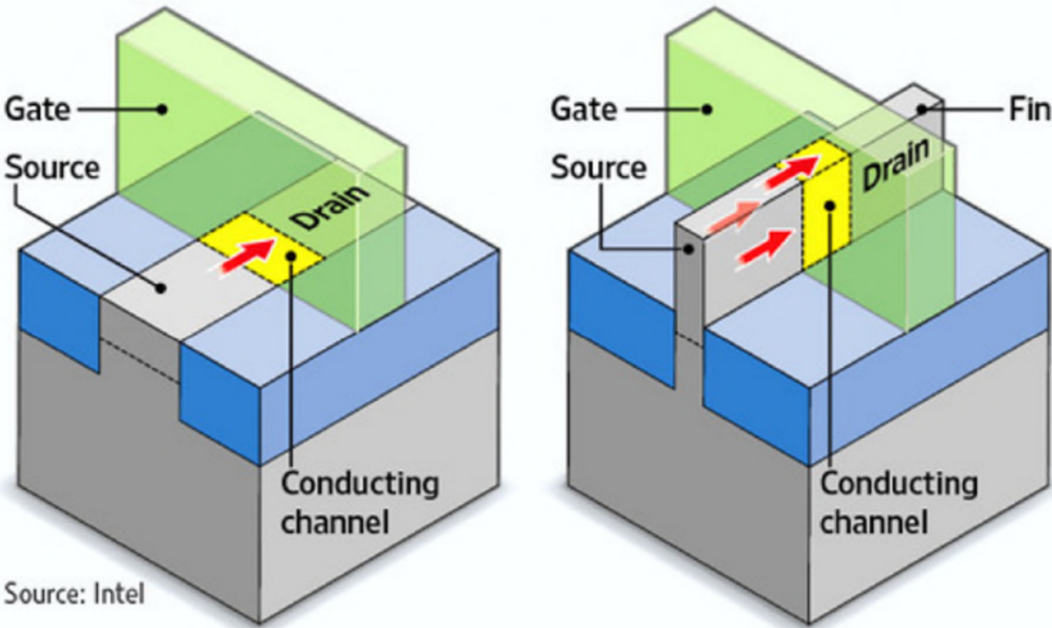
B. Planar vs. Three-Dimensional Transistors

27. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased

computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a "FinFET."

28. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a "planar" FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

29. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



30. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor ("FinFET"), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

31. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

32. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

33. In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13.

34. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called "wafers." Ex. 2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

35. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14.

36. In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15.

2. The Wafer Fabrication Stage

37. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. Ex. 2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* Ex. 2002 at 29-31, 71. For purposes of

understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

38. **Layering** is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72.

39. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72.

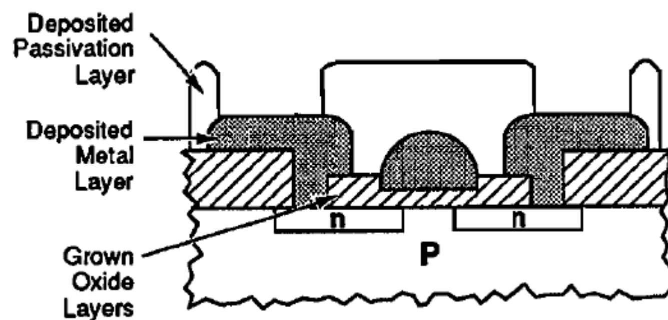


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

40. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73. This creates a pattern on the wafer surface. Ex. 2002 at 72-73.

41. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

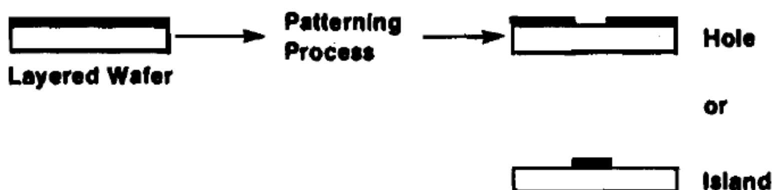


Figure 4.7 Patterning.

42. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

> These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

Ex. 2002 at 73.

VI. THE CHALLENGED ’609 PATENT

43. The ’609 patent “provide[s] a semiconductor device with an epitaxial layer so that stress imposed on the channel region can be increased.” EX1001 at 1:54-56. According to a preferred embodiment of the invention:

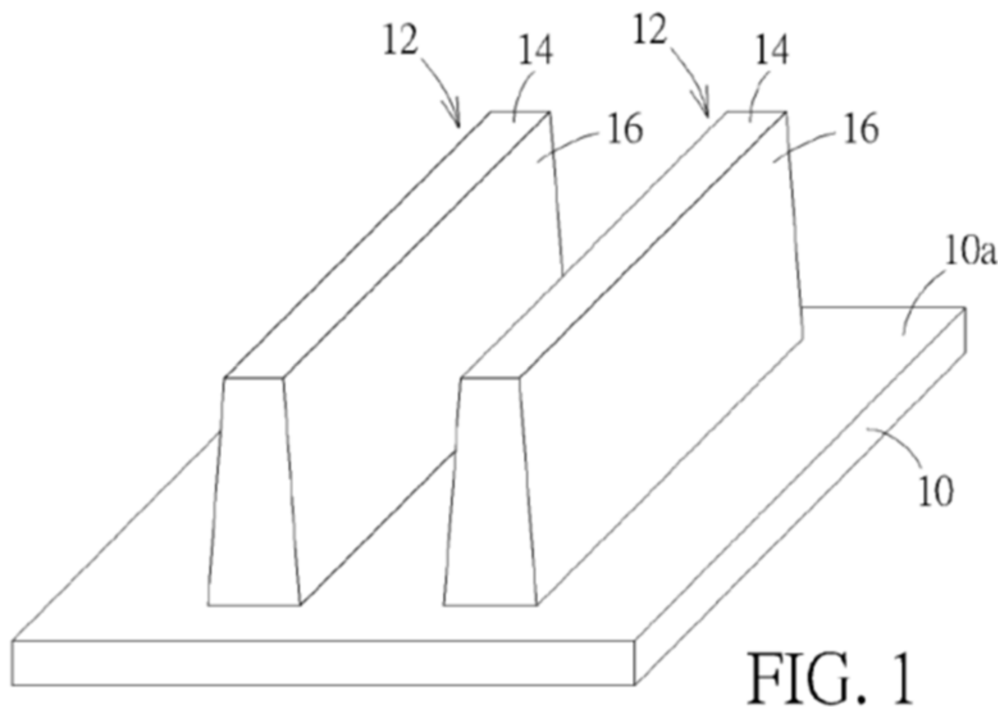
> The semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in [] direct contact with the fin structure.

Id. at 1:57-2:3.

44. The invention of the ’609 patent provided benefits over prior-art semiconductor devices. For example, “[s]ince the process for etching the isolation structure is optionally carried out prior to and/or after the formation of the recess, the height of the isolation structure at two sides of the gate structure may be reduced.

In this way, the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process." *Id*. at 2:6-12. "Furthermore, since the epitaxial structure is not sealed during the epitaxial grown process, the void defects may be also avoided as a result." *Id*. at 2:12-15.

45. Figures 1 to 11 of the '609 patent illustrate "a fabrication method of a semiconductor device according to a preferred embodiment of the present invention." *Id*. at 2:24-26. "FIG. 1 is a schematic perspective view showing the semiconductor device of at the beginning of the fabrication process." *Id*. at 3:4-6.



Id. at Fig. 1.

Marlin Semiconductor Ltd., Exhibit No. 2001
Case No. IPR2026-00130
Page 20 of 35

46. At the beginning of the fabrication process, the device includes a substrate 10 and fin structures 12 protruding from the substrate. Notably, as shown, the fin structures 12 do not extend to the edge of the substrate 10.

47. Next, "FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure." EX1001 at 3:46-47.

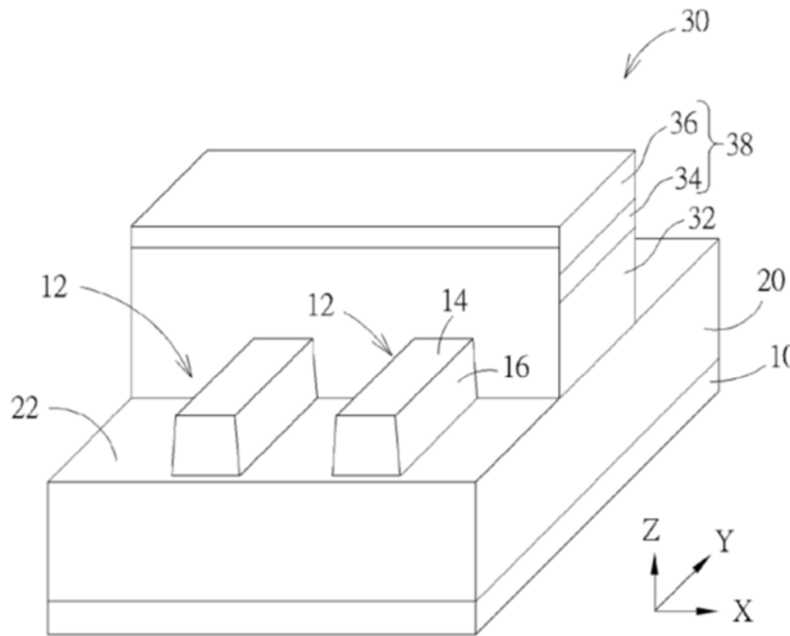


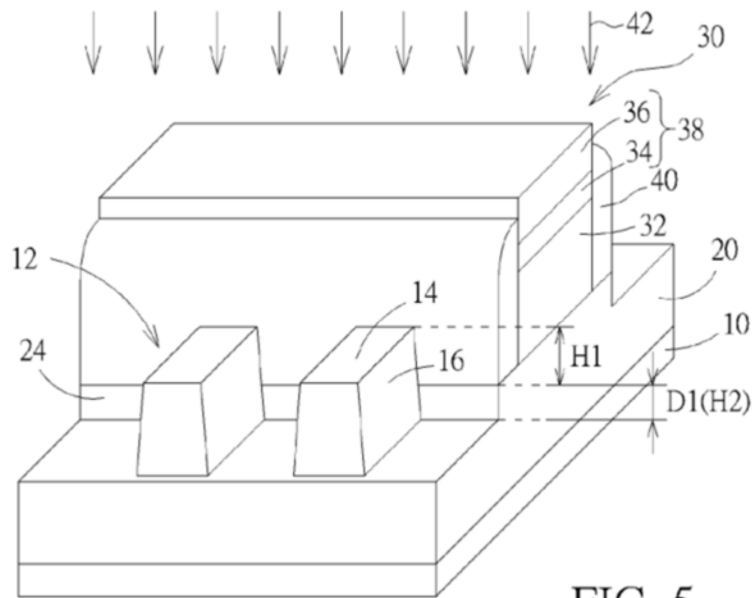
FIG. 2

Id. at Fig. 2.

48. As shown, "[a]t this stage, a lower portion of each fin structure 12 is ***embedded*** in the isolation structure 20." *Id*. at 3:52-53 (emphasis added). That is, as clearly shown in Fig. 2, the isolation structure fully surrounds each side of the lower portion of each fin structure. Forming the isolation structure to fully surround

the fin structures in this manner is important in order to fully isolate each fin structure, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference. Figure 2 also illustrates the formation of a gate structure 30 which "may cover a top surface 14 and two side surfaces 16 of portions of each fin structure 12, and may cover a top surface 22 of portions of the isolation structure 20." EX1001 at 4:4-7.

49. "FIG. 5 is a schematic perspective view showing the semiconductor device after etching the isolation structure" as represented by the "D1" etched depth. *Id*. at 5:17-19, 24.

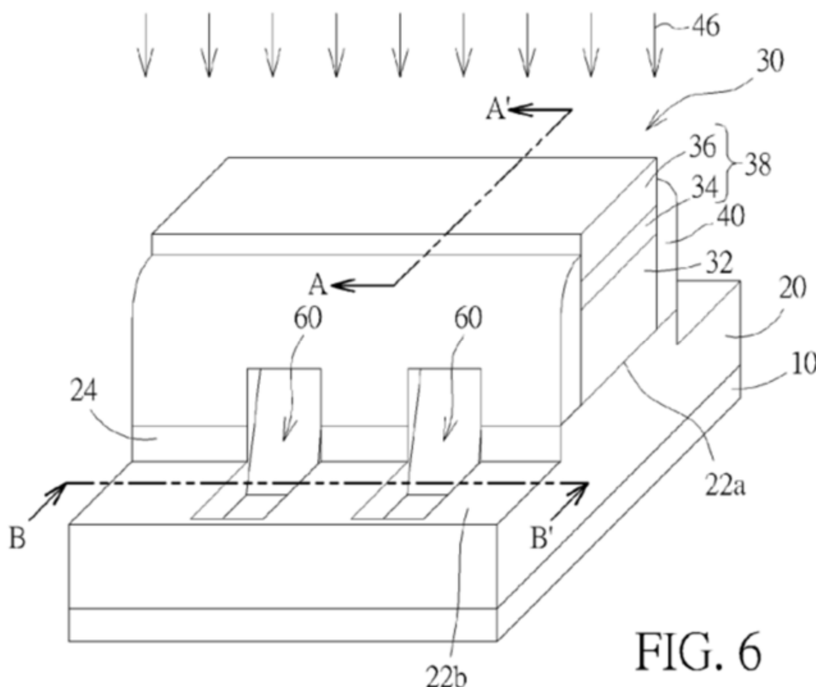


Id. at Fig. 5.

50. "After the formation of the spacers 40, the isolation structure 20 exposed from the gate structure 30 and the spacers 40 may be further etched by a

suitable etching process. In this way, a top surface 22 of portions of the isolation structure 20 may be etched down to a predetermined depth." *Id*. at 5:19-24. "At this time, the isolation structure 20 under the gate structure 30 and the spacers 40 may have a relatively high first top surface 22a, while the isolation structure 20 exposed from the gate structure 30 may have a relatively low second top surface 22b." *Id*. at 5:33-37. This first top structure 22a and second top structure 22b is shown in Fig. 6, depicted below.

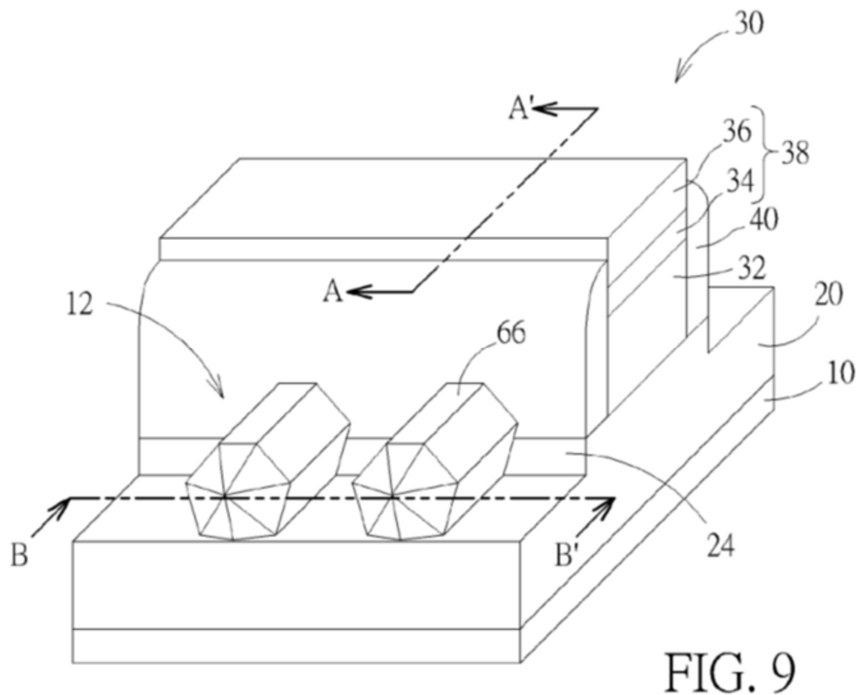
51. "FIG. 6 is a schematic perspective view showing the semiconductor device after etching fin structures." *Id*. at 5:42-44.



Id. at Fig. 6.

52. “As shown in FIG. 6 . . . a second etching process 46 is carried out to etch the fin structures 12 under the gate structure 30 and the spacers 40. After the etching process, a recess 60 may be formed in each fin structure at at least one side of the gate structure 30.” *Id*. at 5:47-51. Because the isolation structure 20 fully surrounds the fin structures on all four sides, when the fin structures are etched down to form recesses 60, the isolation structure 20 fully surrounds the recesses 60, as can be seen in Fig. 6 above.

53. Finally, “FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer.” EX1001 at 6:29-31. Figure 9 illustrates an embodiment of the claimed semiconductor device:



Id. at Fig. 9.

54. "As shown in FIG. 9 . . . an epitaxial growth process . . . maybe carried out in order to grow an epitaxial structure [66] in each corresponding recess 60." *Id*. at 6:34-39. "[E]ach epitaxial structure 66 may completely cover the bottom surface 68 and sidewalls 70 of the corresponding recess 60." *Id*. at 6:39-41; *see also* Fig. 10. Because the isolation structure 20 surrounds the recesses 60 on all four sides, when the epitaxial structures 66 are formed in the recesses 60, the isolation structure 20 also fully surrounds the epitaxial structures 66 formed in the recesses 60, as can be seen in Fig. 9 above. This beneficially ensures that the epitaxial structures are structurally separate and isolated, preventing unwanted contact and electrical interaction and thereby ensuring that each fin structure operates independently without interference. Further, the epitaxial structures may be formed to avoid the occurrence of "void defects. EX1001 at 7:3-7 ("[T]hrough etching the isolation structure 20 at two sides of the gate structure 30, the epitaxial structure 66 may be formed with a desired height (also called depth) and without any void defects."). Thus, the '609 patent's isolation structure provides an improvement over prior-art semiconductor devices by mitigating defects associated with the growth of epitaxial structures.

55. The above-described innovative aspects of the invention are embodied in all challenged claims via independent claim 1, which recites:

1. A semiconductor device, comprising:

[1.a] a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

[1.b] ***an isolation structure, disposed on the surface of the substrate and surrounding the fin structure***;

[1.c(i)] a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure,

[1.c(ii)] ***wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface***; and

[1.d] an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

EX1001, claim 1 (annotated to identify claim elements).

VII. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

A. Xu Fails To Disclose Or Render Obvious "An Isolation Structure, Disposed On The Surface Of The Substrate And Surrounding The Fin Structure"

1. Xu's Alleged Isolation Structure Does Not Surround A Fin

56. The Petition alleges that Xu's "isolation features 130" (the alleged isolation structure) surround the "fins 120." Pet., 16. However, as shown in the

Marlin Semiconductor Ltd., Exhibit No. 2001
Case No. IPR2026-00130
Page 26 of 35

figure below (annotated in the Petition), Xu's "isolation features 130" do not surround the fin structures on all four sides of the fins 120, but rather only cover two sides of the fins 120:

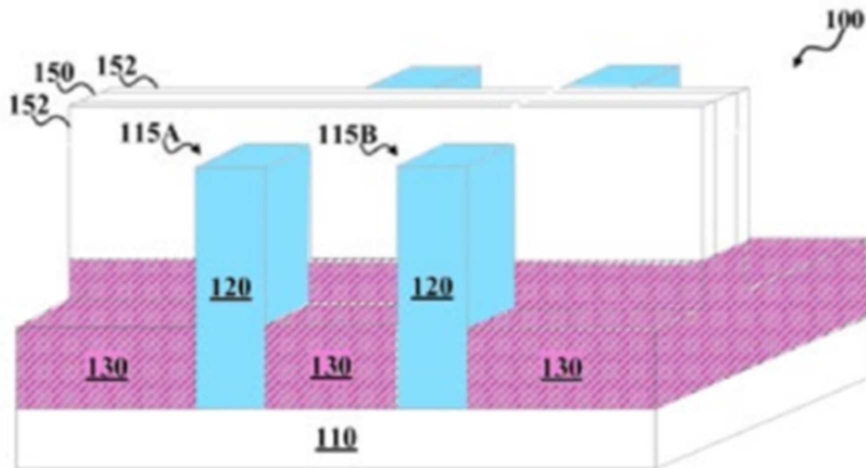


FIG. 3

Pet., 16 (showing annotated EX1004-Xu, Fig. 3).

57. This is in contrast with the challenged claims, which require the "isolation structure . . . ***surrounding*** the fin structure." As explained above, an important feature of the '609 patent's claimed semiconductor device is that the isolation structure surrounds the fin structure on all four sides, thereby completely isolating a fin structure and its corresponding epitaxial structure from other fin/epitaxial structures. That the isolation structure surrounds the fin structures is confirmed by the '609 patent's specification, which explains that "a lower portion of each fin structure is ***embedded*** in the isolation structure 20," indicating that the isolation structure covers all four sides of each fin structure. EX1001 at 3:52-53

(emphasis added). This is further confirmed by the '609 patent's figures, which consistently illustrate the isolation structure 20 covering all four sides of the fin structures 12, not merely two of the sides as in Xu:

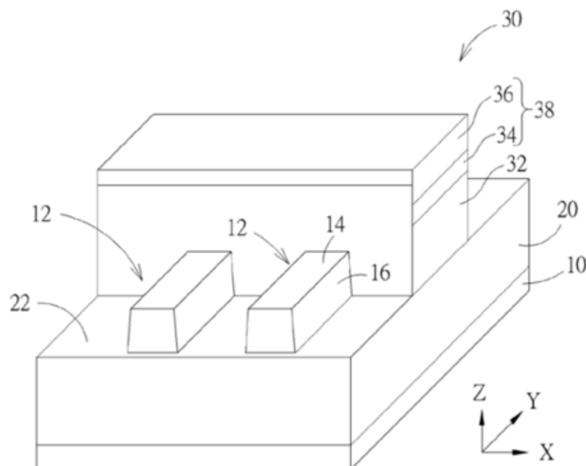


FIG. 2

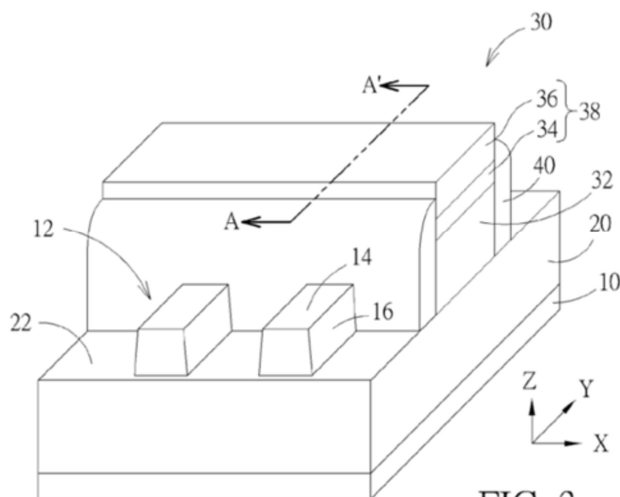


FIG. 3

EX1001 at Figs. 2 and 3; *see also id*. at Fig. 5.

58. Moreover, the figures also illustrate that the isolation structure 20 surrounds all four sides of the etched down fin structures (recesses 60) and the epitaxial structures 66 formed over the etched down fin structures:

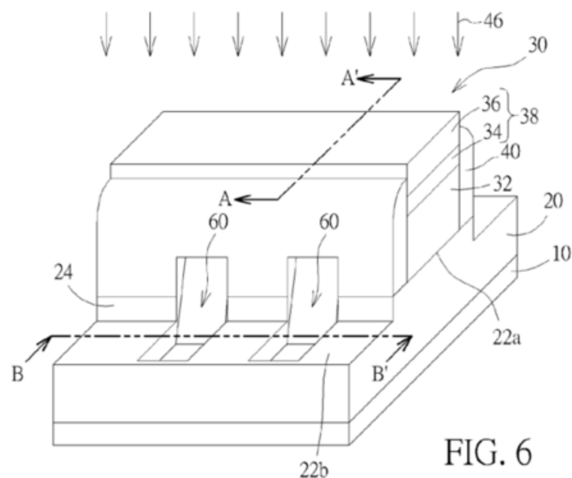


FIG. 6

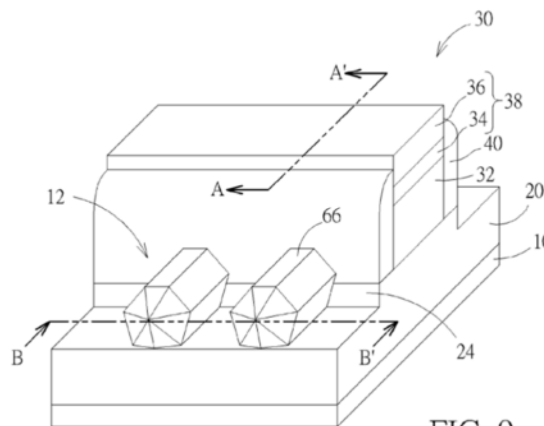


FIG. 9

EX1001 at Figs. 6 and 9.

59. Thus, a POSITA would have understood that, in the claimed semiconductor device, the isolation structure surrounds each fin structure on all four sides. *See* EX2004 ("surround" means "to enclose on all sides").

60. In contrast, Xu's "isolation features 130" do not surround the fin structures as required by the challenged claims. *Id*. Although Xu states that "[i]solation features 130 . . . surround the fin structures 115A and 115B" (EX1004-Xu at 3:54-56), a POSITA would have understood that Xu's usage of the term "surround" is inconsistent with that term as required by the claimed semiconductor device. That passage in Xu describes Xu's Figure 2, which shows that isolation features 130 do not, in fact, surround the fin structures but rather only cover two sides of each fin:

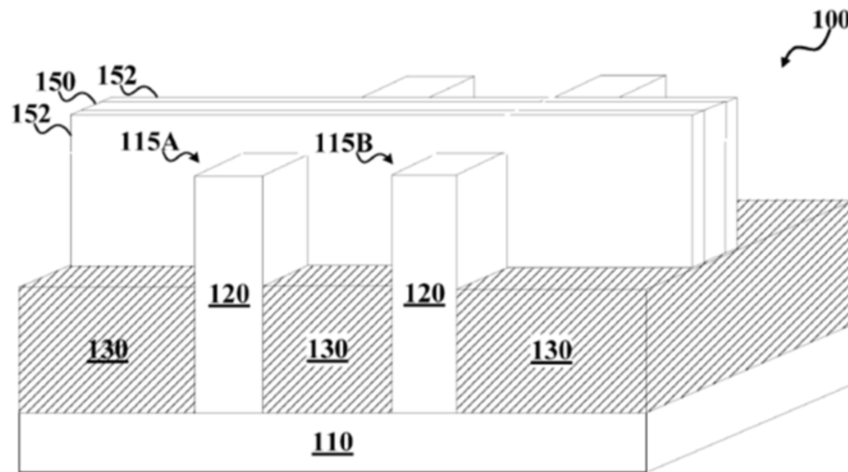


FIG. 2

EX1004-Xu at Fig. 2.

61. In contrast to the '609 patent's figures, which all illustrate the isolation structure surrounding the fin structures, all of Xu's figures consistently illustrate "isolation features 130" as covering only two sides of the fins 120. EX1004-Xu at Figs. 2-6, 8A-C, 9A-C, 10A, 11A, 13A, 14A, 15A, 16A.

2. Xu's Alleged Isolation Structure Does Not Surround Xu's Merged Fin Structure

62. Moreover, Xu fails to disclose or render obvious this limitation for an additional reason. Even if Xu's isolation features 30 are interpreted as "surrounding" fins 120, Xu's isolation features nevertheless do not surround Xu's "fin structure" because, unlike the '609 patent's claimed semiconductor device, Xu's device merges its fins together into a single, merged "fin structure." For example, Xu explains that a "fin template 135 is formed by merging together the fins 120 of

the FinFET device 100." EX1004-Xu at 5:2-4. A "semiconductor material is epitaxially grown by an epi process until the fins 120 of the fin structures 115A and 115B are merged together to form the fin template 135." *Id.* at 5:8-10. Xu's Figure 4 illustrates the merging together of fins 120 to form fin template 135:

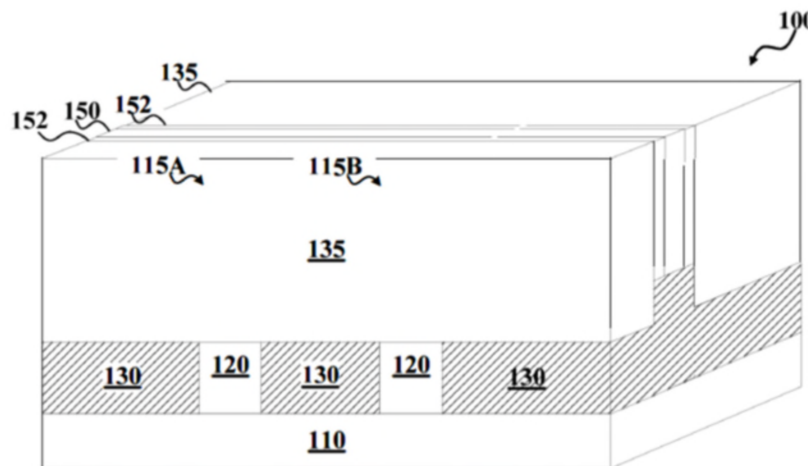


FIG. 4

Id. at Fig. 4.

63. Xu explains that "[t]hough the fins 120 and fin template 135 are depicted separately, it is understood that 'fin template' can refer to the newly grown epi semiconductor material alone (depicted as fin template) or the newly grown epi semi-conductor material combined with the initial fins (depicted as fins 120). *Id.* at 5:28-33. Thus, a POSITA would have understood that Xu's device's "fin structure" includes both fins 120 and fin template 135, which merges adjacent fin structures 115A and 115B, thus teaching away from the express claimed "surrounding" requirement of the '609 patent.

64. As shown in Figure 4 above, Xu's fin template 135 is disposed on top of isolation features 130. As such, Xu's "isolation features 130" do not surround its fin structure because it does not enclose ***any*** side of the merged fin structure, *e.g.*, the part made up of fin template 135.

65. Accordingly, Xu does not disclose "an isolation structure . . . surrounding the fin structure, as required by all challenged claims." The Petition also alleges that Xu renders obvious this limitation but does not provide any explanation or analysis on this point. Pet. at 16-17.

B. Ching Fails To Disclose Or Render Obvious "An Isolation Structure, Disposed On The Surface Of The Substrate And Surrounding The Fin Structure"

66. The Petition alleges that "Ching discloses 'STI regions 22' (magenta) disposed on the surface of substrate 20 (green) and surrounding the 'semiconductor strip 21' (blue) as shown in Figure 1." Pet. at 56.

Marlin Semiconductor Ltd., Exhibit No. 2001
Case No. IPR2026-00130
Page 32 of 35

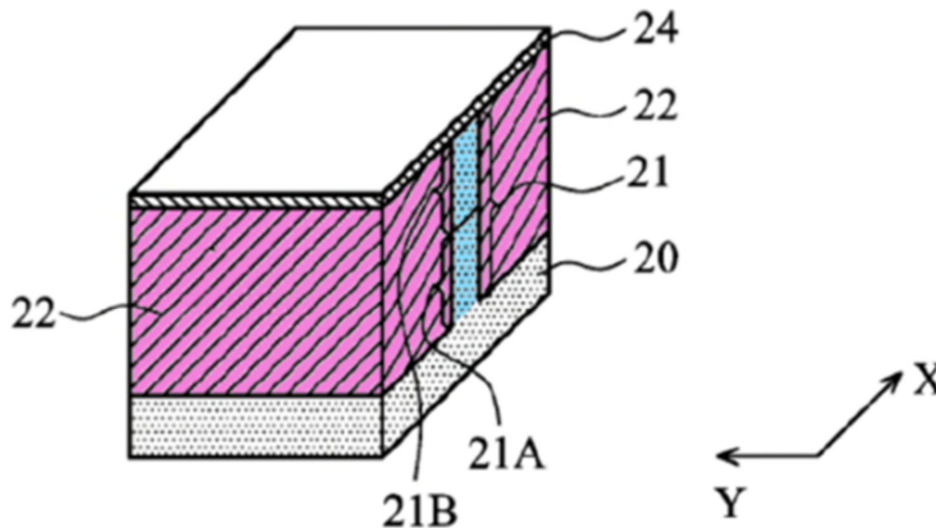


Fig. 1

Pet. at 57 (showing annotated EX1005-Ching, Fig. 1).

67. However, as shown in Figure 1 above, Ching's STI regions 22 do not surround the alleged fin structure (semiconductor strip 21) on all four sides, but rather only cover two sides of semiconductor strip 21.

68. As explained above with respect to Xu, a POSITA would have understood that, in the '609 patent's claimed semiconductor device, the isolation structure surrounds each fin structure on all four sides. *See* EX2004. In contrast, in Ching, STI regions 22 only cover two sides of the alleged fin structure. This is apparent from Ching's description of the STI regions, which explains that "semiconductor strip 21 may be formed by etching a portion of the original substrate

20 ***between*** STI regions 22, and epitaxially growing semiconductor strip 21 between STI regions 22." EX1005-Ching at 2:23-27 (emphasis added). That is, as illustrated in Ching's Fig. 1, "STI regions 22" are two distinct regions that do not merge, and semiconductor strip 21 is etched between the two regions, such that STI regions 22 only cover two sides of the semiconductor strip 21. *Id*. This is different from the '609 patent's device, in which "a lower portion of each fin structure 12 is ***embedded*** in the isolation structure 20." EX1001 at 3:52-53 (emphasis added). Thus, Ching does not disclose "an isolation structure, disposed on the surface of the substrate and surrounding the fin structure," as required by the challenged claims.

69. The Petition argues that "[t]o the extent the claim language requires the isolation structure to *fully* circle the fin structures . . . Ching discloses and renders this obvious as well." Pet. at 59. The Petition argues that "[a] POSITA would have further understood that, in Ching, the shallow trench isolation regions ('STI regions 22') isolate 'semiconductor strips 21' from one another *and* isolate the transistors that will ultimately be formed from 'semiconductor strips 21' from one another." *Id*. But this argument is circular and conclusory. A POSITA would have understood that Ching's STI regions would only "isolate the transistors that will ultimately be formed from semiconductor strips 21 from one another"—as the Petition argues—if they surround the semiconductor strips (on all four sides). The Petition's argument thus merely states the conclusion that a POSITA would have understood that STI

regions surround the semiconductor strips. But this conclusion is wholly unsupported by Ching's disclosure. Indeed, Ching actually ***contradicts*** the Petition's argument, stating that "semiconductor strip 21 is formed ***between, and contacting, neighboring*** STI regions 22." EX1005-Ching at 2:5-6 (emphasis added). As explained above, that Ching's semiconductor strips are formed between neighboring STI regions demonstrates that the STI regions do not surround the semiconductor strips, because the STI regions would need to merge in order to enclose the semiconductor strips on all four sides. Tellingly, the Petition does not cite to any part of Ching in making its obviousness argument, instead citing only its expert's declaration. Pet. at 59 (citing EX1003 at ¶165). But the expert provides no analysis to support the Petition's conclusion, instead simply stating the same conclusory argument as the Petition. EX1003 at ¶165. I understand that such conclusory expert testimony is inadequate to support an obviousness determination.

70. Accordingly, Ching does not disclose or render obvious "an isolation structure . . . surrounding the fin structure, as required by all challenged claims."

Dated: February 26, 2026

Joseph C. McAlexander III