UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	02/14/2017	9570567	T1516.10285US01	7120

97149 7590 01/25/2017

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Che-Cheng Chang, New Taipei City, TAIWAN;
TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD., Hsinchu, TAIWAN;
Chih-Han Lin, Hsinchu City, TAIWAN;
Horng-Huei Tseng, Hsinchu City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

97149 7590 10/03/2016

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	12/30/2015	Che-Cheng Chang	T1516.10285US01	7120

TITLE OF INVENTION: SOURCE AND DRAIN PROCESS FOR FINFET

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/03/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, TRUNG Q	2819	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 Maschoff Brennan
   2 ________
   3 ________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD. ,

(B) RESIDENCE: (CITY and STATE OR COUNTRY): HSINCHU, TAIWAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☑ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-5394 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /R. Burns Israelsen Reg. No. 42685/ Date December 30, 2016

Typed or printed name R. Burns Israelsen Registration No. 42685

Electronic Patent Application Fee Transmittal

Application Number:	14984514
Filing Date:	30-Dec-2015
Title of Invention:	SOURCE AND DRAIN PROCESS FOR FINFET
First Named Inventor/Applicant Name:	Che-Cheng Chang
Filer:	Robert Burns Israelsen/Trisha Rhone
Attorney Docket Number:	T1516.10285US01

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
	Total in USD ($)			**960**

Electronic Acknowledgement Receipt

EFS ID:	27929519
Application Number:	14984514
International Application Number:	
Confirmation Number:	7120
Title of Invention:	SOURCE AND DRAIN PROCESS FOR FINFET
First Named Inventor/Applicant Name:	Che-Cheng Chang
Customer Number:	97149
Filer:	Robert Burns Israelsen/Trisha Rhone
Filer Authorized By:	Robert Burns Israelsen
Attorney Docket Number:	T1516.10285US01
Receipt Date:	30-DEC-2016
Filing Date:	30-DEC-2015
Time Stamp:	21:22:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	010317INTEFSW21240600
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	T1516-10285US01_Examiners_Statement_of_Allowance.pdf	225777 89e7ed7a2ba7d6bf6d3aabfac5b732e540ef830e	no	1
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	T1516-10285US01_Issue_Fee_Transmittal.pdf	159858 7ee3c3f373366eef87bc8c40f08ec3d7b15d2245	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30340 f6aa7aee0a99abd6b107871f7f5d9d951dd1caa6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	415975		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :	TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.	
Application No.:	14/984,514	Art Unit 2819
Filed:	December 30, 2015	
Conf. No.:	7120	
For:	SOURCE AND DRAIN PROCESS FOR FINFET	
Examiner:	DANG, TRUNG Q	
Customer No.:	97149	
Attorney Docket No.:	T1516.10285US01	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant acknowledges Examiner's statements of Reasons for Allowance of the above-referenced patent application and agrees that the claimed subject matter is patentable. However, Applicant takes no position regarding the Reasons for Allowance presented by the Examiner other than the positions Applicant may have previously taken during prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed to Applicant as an indication of the basis for Applicant's belief that the claims are patentable. Furthermore, Applicant respectfully asserts that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record and Applicant does not waive its rights to such arguments by not further addressing such reasons herein.

Dated this 30th day of December, 2016.

Respectfully submitted,

/R. Burns Israelsen, Reg. No. 42685/

Registration No. 42685
Attorney for Applicant
Customer No. 97149
Telephone No. (435) 252-1360

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

97149 7590 10/03/2016

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

EXAMINER	
DANG, TRUNG Q	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/03/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	12/30/2015	Che-Cheng Chang	T1516.10285US01	7120

TITLE OF INVENTION: SOURCE AND DRAIN PROCESS FOR FINFET

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/03/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

97149 7590 10/03/2016

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	12/30/2015	Che-Cheng Chang	T1516.10285US01	7120

TITLE OF INVENTION: SOURCE AND DRAIN PROCESS FOR FINFET

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	01/03/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, TRUNG Q	2819	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
   (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
   (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1 ______________________
   2 ______________________
   3 ______________________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies ______________

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number __________ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature ______________________ Date ______________________

Typed or printed name ______________________ Registration No. ______________________

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	12/30/2015	Che-Cheng Chang	T1516.10285US01	7120

97149 7590 10/03/2016

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/03/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/984,514	Applicant(s) CHANG ET AL.	
	Examiner TRUNG Q. DANG	Art Unit 2819	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 9/9/16*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on______.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. ______ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/TRUNG Q DANG/
Primary Examiner, Art Unit 2819

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

Claims 1-15 are allowed over prior art of record for the same reason indicated in previous Office action.

For amended claim 16, closest pertinent prior art is a reference to Cappellani et al. (US 2011/0147842). However, the reference fails to teach or suggest the claimed features regarding a dielectric layer which is disposed on the fin structure and covers a top surface and two opposite side surfaces of the fin structure, wherein the dielectric layer comprises two first portions protruding from the side surfaces of the fin structure such that two first recesses are formed in the dielectric layer, each of the first recesses is surrounded by the dielectric laver and the substrate, and the first recesses are opposite to each other. Specifically, Fig. 3A of the reference does not show the dielectric layer 318 covers a top surface of the fin structure 216, and Fig. 4A does not show the recess is surrounded by the dielectric layer 318 and the substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRUNG Q. DANG whose telephone number is (571)272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ALLEN PARKER can be reached on 571-270-5841. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TRUNG Q DANG/
Primary Examiner, Art Unit 2819

9/19/16

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	57700	(H01L29/785 H01L29/7841 H01L29/66795 H01L29/7851 H01L29/0688 H01L29/0649 H01L29/0847 H01L29/7848 H01L29/66636 H01L29/165 H01L29/66545).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:31
L2	23772	fin$1fet$1 or fin$1mosfet$1 or fin$1mos or fin adj3 (mosfet or fet or field adj2 effect)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:32
L3	44221	gate near10 replac$7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:32
L4	18651	recess$4 with fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:32
L5	15305916	source or drain or s$1d or source$1drain or drain$1source or d$1s	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:33
L6	52677	(epi or epitax$5) with 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:35
L7	942	2 and 3 and 4 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:36
L8	864	7 and (1 or 257/401.ccls. or 438/283.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:36
L9	31427	(dummy or sacrif$5) near5 gate	US-PGPUB; USPAT;	OR	ON	2016/09/19 13:37

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L10	8350	9 with (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:37
L11	400	8 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:37
L12	400	11 and (@ad<="20151230" or @rlad<="20151230")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:38
L13	700	recess with surround$4 with substrate with (insulat$4 or dielectric)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:40
L14	3	12 and 13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:40
L15	6	13 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:42
L16	47928	che.in. near2 chang.in. or chih.in. near2 lin.in. or horng.in. near2 tseng.in. or taiwan.as. near2 semiconductor.as. near2 manufacturing.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:42
L17	270	16 and 4 and 6 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:43
L18	141	17 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/19 13:43
S1	21751	fin$1fet$1 or fin$1mosfet$1 or fin$1mos or fin adj3 (mosfet or fet	US-PGPUB; USPAT;	OR	ON	2016/06/12 20:43

		or field adj2 effect)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB				
S2	42904	gate near10 replac$7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:44	
S3	17854	recess$4 with fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:44	
S4	14911784	source or drain or s$1d or source$1drain or drain$1source or d$1s	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:45	
S5	50795	(epi or epitax$5) with S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:47	
S6	783	S1 and S2 and S3 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:47	
S7	781	S6 and (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:48	
S8	781	S7 and (@ad<="20151230" or @rlad<="20151230")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:48	
S9	29912	(dummy or sacrif$5) near5 gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:57	
S10	7776	S9 with (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:57	
S11	345	S8 and S10	US-PGPUB; USPAT;	OR	ON	2016/06/12 20:57	

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S12	53135	(H01L29/785 H01L29/7841 H01L29/66795 H01L29/7851 H01L29/0688 H01L29/0649 H01L29/0847 H01L29/7848 H01L29/66636 H01L29/165 H01L29/66545).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:29
S13	3140	S12 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S14	1059	S2 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S15	781	S14 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S16	779	S15 and (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S17	779	S16 and (@ad<="20151230" or @rlad<="20151230")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S18	464	S17 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S19	11048	etch$4 with fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:32
S20	415	S18 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:32
S21	295	S20 and S9	US-PGPUB; USPAT;	OR	ON	2016/06/12 22:32

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S22	46022	che.in. near2 chang.in. or chih.in. near2 lin.in. or horng.in. near2 tseng.in. or taiwan.as. near2 semiconductor.as. near2 manufacturing.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:33
S23	514	S22 and S1 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34
S24	308	S23 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34
S25	219	S24 and (S3 or S19)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L19	3098	recess$4.clm. with fin.clm.	US-PGPUB; USPAT	OR	ON	2016/09/19 14:19
L20	4058	fin$1fet$1.clm. or fin$1mosfet$1.clm. or fin$1mos.clm. or fin.clm. adj3 (mosfet or fet or field adj2 effect).clm.	US-PGPUB; USPAT	OR	ON	2016/09/19 14:20
L21	148	recess.clm. with surround$4.clm. with substrate.clm. with (insulat$4 or dielectric).clm.	US-PGPUB; USPAT	OR	ON	2016/09/19 14:21
L22	2	19 and 20 and 21	US-PGPUB; USPAT	OR	ON	2016/09/19 14:21

9/19/2016 2:23:40 PM
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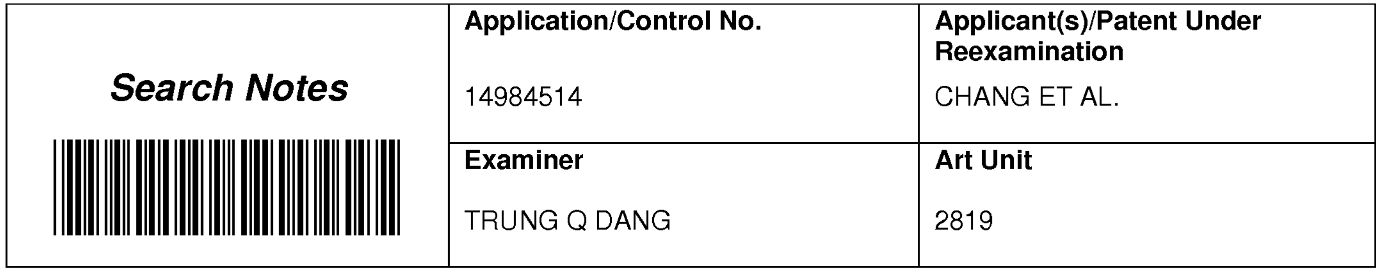


Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984514	CHANG ET AL.
	Examiner	**Art Unit**
	TRUNG Q DANG	2819

CPC- SEARCHED

Symbol	Date	Examiner
H01L29/785, 29/7841, 29/66795, 29/7851, 29/0688, 29/0649, 29/0847, 29/7848, 29/165, 29/66545	9/19/16	TD

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

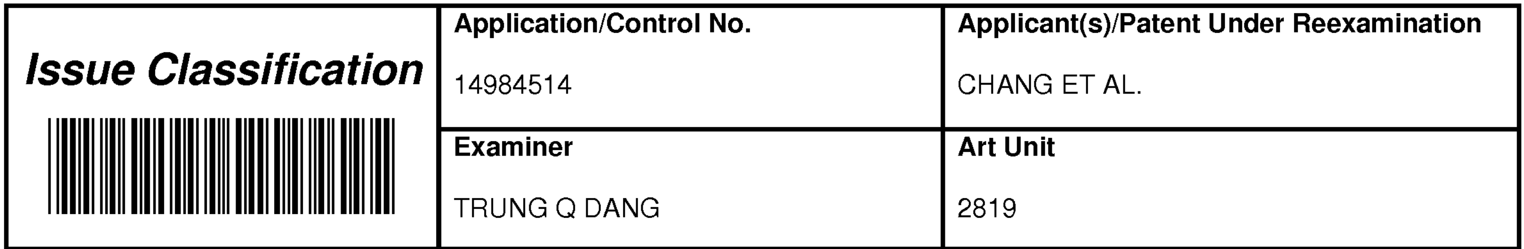
Class	Subclass	Date	Examiner
257	401	9/19/16	TD
438	283	9/19/16	TD

SEARCH NOTES

Search Notes	Date	Examiner
EAST update: search cpc, us-clas/subcls with text limited, text, inventor and assignee	9/19/16	TD

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
US-PGPUB, USPAT, UPAD	claim search	9/19/16	TD



Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984514	CHANG ET AL.
	Examiner	**Art Unit**
	TRUNG Q DANG	2819

CPC					
Symbol				**Type**	**Version**
H01L	29	/	41791	F	2013-01-01
H01L	29	/	785	I	2013-01-01
H01L	29	/	66545	I	2013-01-01
H01L	29	/	6656	I	2013-01-01
H01L	29	/	66795	I	2013-01-01
H01L	21	/	30604	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
		/					
		/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/TRUNG Q DANG/ Primary Examiner.Art Unit 2819 (Primary Examiner)	9/19/16 (Date)	O.G. Print Claim(s) 16	O.G. Print Figure 2E, 3G

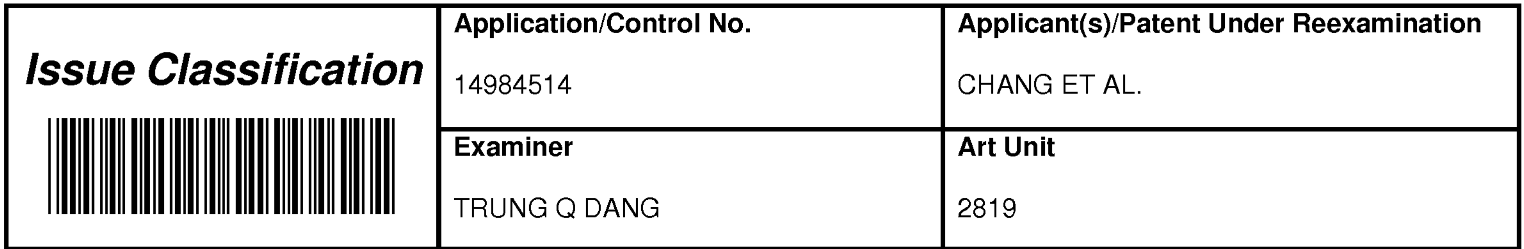
Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984514	CHANG ET AL.
	Examiner	Art Unit
	TRUNG Q DANG	2819

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION					
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED
257	401	H	0	1	L	27 / 088 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
438	283				

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 20	
/TRUNG Q DANG/ Primary Examiner.Art Unit 2819 (Primary Examiner)	9/19/16 (Date)	O.G. Print Claim(s) 16	O.G. Print Figure 2E, 3G



Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984514	CHANG ET AL.
	Examiner	**Art Unit**
	TRUNG Q DANG	2819

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4		20												
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	6														
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	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/TRUNG Q DANG/ Primary Examiner.Art Unit 2819 (Primary Examiner)	9/19/16 (Date)	O.G. Print Claim(s) 16	O.G. Print Figure 2E, 3G

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BIB DATA SHEET

CONFIRMATION NO. 7120

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/984,514	12/30/2015 **RULE**	257	2819	T1516.10285US01

APPLICANTS
TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD., Hsinchu, TAIWAN;

INVENTORS
Che-Cheng Chang, New Taipei City, TAIWAN;
Chih-Han Lin, Hsinchu City, TAIWAN;
Horng-Huei Tseng, Hsinchu City, TAIWAN;

** **CONTINUING DATA** *************************

** **FOREIGN APPLICATIONS** *************************

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
01/13/2016

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /TRUNG Q DANG/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	10	20	3

ADDRESS

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098
UNITED STATES

TITLE

SOURCE AND DRAIN PROCESS FOR FINFET

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1600	No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other ________________ ❑ Credit

BIB (Rev. 05/07).

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/984,514	Filing Date 12/30/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/09/2016	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
SHARON HARRIS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: TRUNG Q DANG
Group Art Unit: 2819
Confirmation No.: 7120
Att. Doc. No.: T1516.10285US01

In re PATENT APPLICATION of

Applicant: CHANG ET AL.	)	
	)	
Appl. No.: 14/984,514	)	
	)	AMENDMENT
Filed: 12/30/2015	)	
	)	
For: SOURCE AND DRAIN PROCESS FOR FINFET	)	
	)	
	)	

AMENDMENT

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

The Office Action dated June 20, 2016, has been carefully considered. In response thereto, Applicants hereby submit the following amendments and remarks.

Amendments to the claims begin on page 2 of this paper.

Remarks begin on page 10 of this paper.

AMENDMENTS TO THE CLAIMS:

The following list of claims will replace all prior versions and listings of claims in the application.

LISTINGS OF CLAIMS:

1. (Original) A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the

fin structure to remove the third portions and a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers; and

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses.

2. (Original) The method of claim 1, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

3. (Original) The method of claim 1, wherein the operation of forming the spacers forms the spacers from silicon nitride.

4. (Original) The method of claim 1, wherein an operation of

forming the dummy gate forms the dummy gate from polysilicon.

5. (Original) The method of claim 1, the method further comprising performing a wet clean operation on the first recesses and the second recesses after the second etching operation is completed.

6. (Original) The method of claim 1, the method further comprising performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate after the second etching operation is completed.

7. (Original) The method of claim 6, wherein the epitaxy operation forms the source and the drain each of which comprises a silicon germanium (SiGe) layer.

8. (Original) The method of claim 6, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

9. (Original) A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the fin structure to remove the third portions of the dielectric layer, a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions of the dielectric layer and the portions of the second portions of the dielectric

layer, thereby forming two first recesses respectively in the spacers;

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses;

performing a wet clean operation on the first recesses and the second recesses; and

performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate.

10. (Original) The method of claim 9, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

11. (Original) The method of claim 9, wherein the operation of forming the spacers forms the spacers from silicon nitride.

12. (Original) The method of claim 9, wherein an operation of forming the dummy gate forms the dummy gate from polysilicon.

13. (Original) The method of claim 9, wherein the epitaxy operation is performed to form the source and the drain each of which comprises a silicon germanium (SiGe) layer.

14. (Original) The method of claim 9, wherein an operation of forming the fin structure is performed by recessing the substrate.

15. (Original) The method of claim 9, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

16. (Currently amended) A FinFET comprising:

a substrate;

a fin structure on the substrate;

a dielectric layer which is disposed on the fin structure and covers <u>a top surface and </u>two opposite side surfaces of the fin structure, wherein

the dielectric layer comprises two first portions protruding from the side surfaces of the fin structure such that two first recesses are formed in the dielectric layer, each of the first recesses is surrounded by the dielectric layer and the substrate, and the first recesses are opposite to each other;

a metal gate on a second portion of the dielectric layer, wherein the second portion is sandwiched between the first portions of the dielectric layer;

two spacers on the first portions of the dielectric layer respectively, wherein the spacers respectively protrude from the first portions of the dielectric layer such that two second recesses are formed in the spacers;

a source which is disposed in one of the first recesses and one of the second recesses on the substrate; and

a drain which is disposed in the other one of the first recesses and the other one of the second recesses on the substrate.

17. (Original) The FinFET of claim 16, wherein the fin structure is formed from silicon, and the dielectric layer is formed from silicon oxide.

18. (Original) The FinFET of claim 16, wherein the spacers are

formed from silicon nitride.

19. (Original) The FinFET of claim 16, wherein the source and the drain are formed from silicon germanium.

20. (Original) The FinFET of claim 16, wherein each of the source and the drain comprises an epitaxy layer.

REMARKS

The Examiner is thanked for carefully reviewing the present application. Applicant has thoroughly reviewed the Office Action including the Examiner's remarks and the references cited therein. The above amendment and following remarks are believed to be fully responsive to the Office Action and render all claims at issue patentably distinguishable over the cited references.

Favorable reconsideration is requested in view of the above amendments and the following remarks.

Claim 16 is amended to overcome the 102 rejection. Therefore, claims 1-20 are now pending in the application. Support for the above amendments is found in at least paragraphs [0015] and [0023], and FIG. 1A, FIG. 1B, and FIG. 2B. These amendments contain no new matter.

Claim Rejections - 35 USC §102

1. Claims 16-20 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Cappellani et al. (US 2011/0147842, hereinafter referred to as "Cappellani"). These rejections are respectfully traversed. As will be fully explained below, it is respectfully submitted that Cappellani does not anticipate the claims as amended, and the Applicant respectfully requests that the section 102(a)(1) rejections be withdrawn.

Amended claim 16 now recites "a dielectric layer which is

disposed on the fin structure and **covers a top surface and two opposite side surfaces** of the fin structure", and "each of the first recesses is **surrounded by the dielectric layer and the substrate.** "

The Examiner equates the fin spacers 318 of the multi-gate device disclosed by Cappellani to the dielectric layer of the FinFET recited in the amended claim 16. Office Action, page 2.

However, in the multi-gate device disclosed by Cappellani (see FIG. 3A through FIG. 4B), the fin spacers 318 do not cover a top surface of the doped fin region 208, but rather the fin spacers 318 only cover side surfaces of the doped fin region 208. In addition, the multi-gate device of Cappellani includes no recess which is surrounded by the fin spacers 318 and the semiconductor substrate 202. Thus, Cappellani at least fails to teach or suggest the features of "a dielectric layer which is disposed on the fin structure and **covers a top surface** and two opposite side surfaces of the fin structure", and "each of the first recesses is **surrounded by the dielectric layer and the substrate,**" as recited in amended claim 16.

According to the aforementioned description, the multi-gate device disclosed by Cappellani is different from the FinFET recited in amended claim 16, and Cappellani fails to teach **each and every** limitation of amended claim 16 of the present application.

Accordingly, Applicant respectfully submits that Cappellani fails to teach or anticipate all of the features of amended claim 16, and amended claim 16 is allowable.

Claims 17-20 depend from and add further features to amended claim 16. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding further features. Accordingly, Applicant respectfully requests that the section 102 rejections be withdrawn.

Allowed Subject Matter

The Office Action acknowledges that claims 1-15 are directed to allowable subject matter. Applicants thank Examiner for the careful review and allowance of those claims. Applicants agree with Examiner that claims 1-15 are patentable, but respectfully disagree with Examiner's statement of reasons for allowance as set forth in the Office Action. Applicants submit that it is the claim as a whole, rather than any particular element, that makes each of the claims allowable. No single element should be construed as the reason for allowance of a claim because it is each of the elements of a claim that makes it allowable. Therefore, Applicants do not concede that the reasons for allowable subject matter given by Examiner are the only reasons that make, or would make, the claims allowable and do not make any admission or concession concerning Examiner's statement in the Office Action.

CONCLUSION

In light of the above remarks, all rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited. If there are any remaining issues to be resolved, Applicant requests that Examiner contacts the undersigned attorney for a telephone interview.

September 9, 2016
Date

Respectfully submitted,

/Brian Parke/

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Registration No. 59,226
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Maschoff Brennan

TSMC Exhibit 1064
Page 38 of 110

Electronic Acknowledgement Receipt

EFS ID:	26877024
Application Number:	14984514
International Application Number:	
Confirmation Number:	7120
Title of Invention:	SOURCE AND DRAIN PROCESS FOR FINFET
First Named Inventor/Applicant Name:	Che-Cheng Chang
Customer Number:	97149
Filer:	Brian Gary Parke/Brian Gonzalez
Filer Authorized By:	Brian Gary Parke
Attorney Docket Number:	T1516.10285US01
Receipt Date:	09-SEP-2016
Filing Date:	30-DEC-2015
Time Stamp:	12:22:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-09-09_OA-Response_T1516-10285US01.pdf	253071 bdc504dcaeb63935e8f998e943e7b0cd4f0d3e0b	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	13
Warnings:			
Information:			
	Total Files Size (in bytes):	253071	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/984,514	12/30/2015	Che-Cheng Chang	T1516.10285US01	7120

97149 7590 06/20/2016
Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
06/20/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@mabr.com
info@mabr.com

Office Action Summary	Application No. 14/984,514	Applicant(s) CHANG ET AL.	
	Examiner TRUNG Q. DANG	Art Unit 2819	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-15* is/are allowed.

7)☒ Claim(s) *16-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 16-20 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Cappellani et al. (US 2011/0147842).

Regarding claim 16, with reference to the reproduced Figs. 4A and 4B, the prior art teaches the claimed invention in that it discloses a FinFET comprising:

a substrate 202;

a fin structure on the substrate;

a dielectric layer 318 which is disposed on the fin structure and covers two opposite side surfaces of the fin structure, wherein the dielectric layer comprises two first portions protruding from the side surfaces of the fin structure such that two first recesses are formed in the dielectric layer, and the first recesses are opposite to each other;

a metal gate 213 on a second portion of the dielectric layer 318, wherein the second portion is sandwiched between the first portions of the dielectric layer;

two spacers 319 on the first portions of the dielectric layer 318 respectively, wherein the spacers 319 respectively protrude from the first portions of the dielectric 318 layer such that two second recesses 421 (Fig. 4B) are formed in the spacers 319;

a source 618 which is disposed in one of the first recesses and one of the second recesses on the substrate; and

a drain 618 which is disposed in the other one of the first recesses and the other one of the second recesses on the substrate (Fig.6A).

For claims 17 and 18, see ¶0032.

For claims 19 and 20, see ¶0045.

Allowable Subject Matter

3. Claims 1-15 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 1 and 9 are allowable over prior art of record because the prior art does not teach or suggest the following steps, taken with other limitations of the claims as a whole, including: performing a first etching operation on the dielectric layer and the fin structure to remove the third portions and a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers; and performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in

the dielectric layer, wherein the second recesses respectively communicate with the first recesses.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRUNG Q. DANG whose telephone number is (571)272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

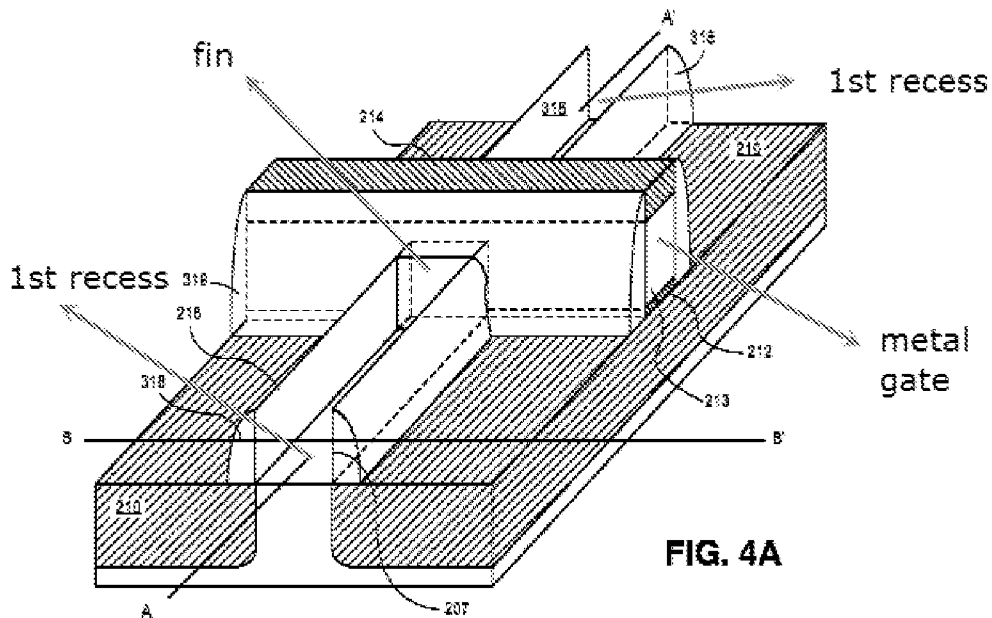
If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, ALLEN PARKER can be reached on 571-270-5841. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TRUNG Q DANG/
Primary Examiner, Art Unit 2819

6/13/16



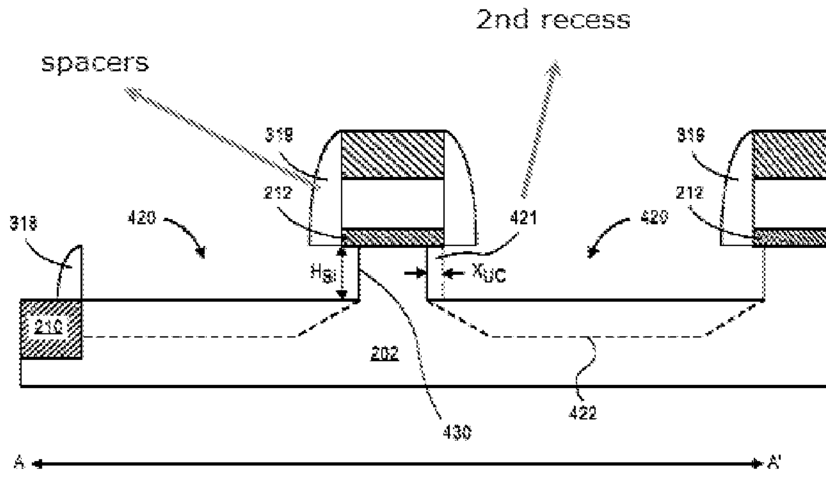


FIG. 4B

Notice of References Cited	Application/Control No. 14/984,514	Applicant(s)/Patent Under Reexamination CHANG ET AL.	
	Examiner TRUNG Q. DANG	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2015/0255571 A1	09-2015	Xu; Jeffrey Junhao	H01L29/6681	257/288
*	B	US-2014/0361373 A1	12-2014	Hung; Yu-Hsiang	H01L29/7848	257/365
*	C	US-2014/0299934 A1	10-2014	KIM; Seok-Hoon	H01L29/7848	257/347
*	D	US-2014/0227847 A1	08-2014	YOON; IL-YOUNG	H01L29/66545	438/283
*	E	US-2011/0147842 A1	06-2011	Cappellani; Annalisa	H01L21/26506	257/365
*	F	US-2011/0147828 A1	06-2011	Murthy; Anand S.	H01L21/02057	257/327
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 7120

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/984,514	12/30/2015 RULE	257	2819	T1516.10285US01

APPLICANTS
TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD., Hsinchu, TAIWAN;

INVENTORS
Che-Cheng Chang, New Taipei City, TAIWAN;
Chih-Han Lin, Hsinchu City, TAIWAN;
Horng-Huei Tseng, Hsinchu City, TAIWAN;

** **CONTINUING DATA** *************************

** **FOREIGN APPLICATIONS** *************************

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** **
01/13/2016

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /TRUNG Q DANG/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	10	20	3

ADDRESS

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098
UNITED STATES

TITLE

SOURCE AND DRAIN PROCESS FOR FINFET

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1600	No.____________ to charge/credit DEPOSIT ACCOUNT No.____________ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other ________________ ❑ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	21751	fin$1fet$1 or fin$1mosfet$1 or fin$1mos or fin adj3 (mosfet or fet or field adj2 effect)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:43
S2	42904	gate near10 replac$7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:44
S3	17854	recess$4 with fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:44
S4	14911784	source or drain or s$1d or source$1drain or drain$1source or d$1s	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:45
S5	50795	(epi or epitax$5) with S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:47
S6	783	S1 and S2 and S3 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:47
S7	781	S6 and (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:48
S8	781	S7 and (@ad<="20151230" or @rlad<="20151230")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:48
S9	29912	(dummy or sacrif$5) near5 gate	US-PGPUB; USPAT;	OR	ON	2016/06/12 20:57

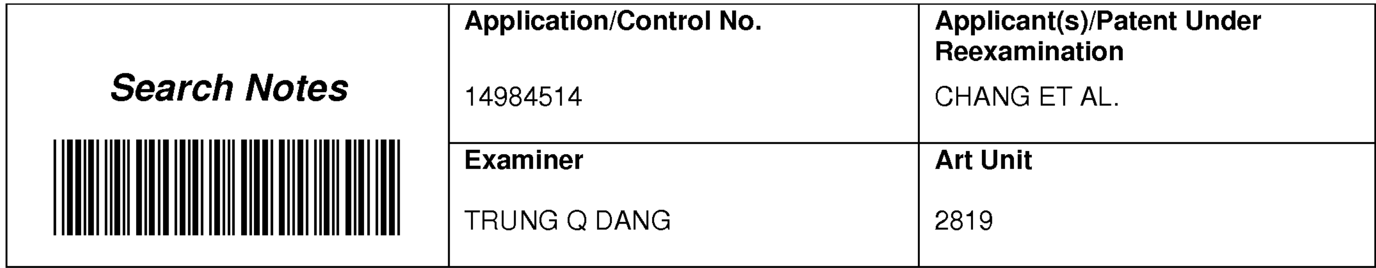
			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S10	7776	S9 with (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:57
S11	345	S8 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 20:57
S12	53135	(H01L29/785 H01L29/7841 H01L29/66795 H01L29/7851 H01L29/0688 H01L29/0649 H01L29/0847 H01L29/7848 H01L29/66636 H01L29/165 H01L29/66545).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:29
S13	3140	S12 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S14	1059	S2 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S15	781	S14 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:30
S16	779	S15 and (spacer or side$1wall$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S17	779	S16 and (@ad<="20151230" or @rlad<="20151230")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S18	464	S17 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:31
S19	11048	etch$4 with fin	US-PGPUB; USPAT;	OR	ON	2016/06/12 22:32

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S20	415	S18 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:32
S21	295	S20 and S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 22:32
S22	46022	che.in. near2 chang.in. or chih.in. near2 lin.in. or horng.in. near2 tseng.in. or taiwan.as. near2 semiconductor.as. near2 manufacturing.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:33
S23	514	S22 and S1 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34
S24	308	S23 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34
S25	219	S24 and (S3 or S19)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 23:34

EAST Search History (Interference)

<This search history is empty>

6/13/2016 8:25:02 AM
C:\Users\tdang1\Documents\EAST\Workspaces\14984514.wsp



Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14984514	CHANG ET AL.
	Examiner	**Art Unit**
	TRUNG Q DANG	2819

CPC- SEARCHED

Symbol	Date	Examiner
H01L29/785, 29/7841, 29/66795, 29/7851, 29/0688, 29/0649, 29/0847, 29/7848, 29/165, 29/66545	6/12/16	TD

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
EAST: search cpc, text, inventor and assignee	6/12/16	TD

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/984,514

APPLICATION AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1600

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/984,514	12/30/2015	2812	1600	T1516.10285US01	20	3

CONFIRMATION NO. 7120

FILING RECEIPT

97149
Maschoff Brennan
1389 Center Drive, Suite 300
Park City, UT 84098

Date Mailed: 01/14/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Che-Cheng Chang, New Taipei City, TAIWAN;
Chih-Han Lin, Hsinchu City, TAIWAN;
Horng-Huei Tseng, Hsinchu City, TAIWAN;

Applicant(s)

TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD., Hsinchu, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 97149

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/13/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/984,514**

Projected Publication Date: 07/06/2017

Non-Publication Request: No

Early Publication Request: No
Title

SOURCE AND DRAIN PROCESS FOR FINFET

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number			
Filing Date			
First Named Inventor	Che-Cheng CHANG		
Title	SOURCE AND DRAIN PROCESS FOR FINFET		
Art Unit			
Examiner Name			
Attorney Docket Number	T1516.10285US01		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/R. Burns Israelsen/	**Date**	December 30, 2015
Name	R. Burns Israelsen	**Telephone**	(435) 252-1360
Registration Number	42685		

MASCHOFF BRENNAN, PLLC
1389 Center Drive, SUITE 300
PARK CITY, UTAH 84098, USA

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 97149

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name	Maschoff Brennan Intellectual Property and Complex Litigation				
Address	1389 CENTER DRIVE, SUITE 300				
City	PARK CITY	State	UT	Zip	84098
Country	USA				
Telephone	435-252-1360	Email	docket@mgiip.com		

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

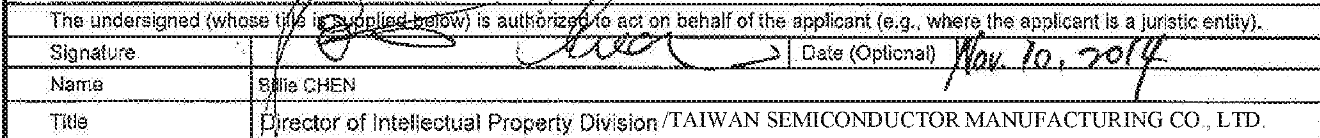
TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)



SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	Nov. 10, 2014
Name	Billie CHEN		
Title	Director of Intellectual Property Division /TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Che-Cheng		CHANG	

Residence Information (Select One) ○ US Residency ● Non US Residency ○ Active US Military Service

City	New Taipei City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	NO.8, LI-HSIN RD.6		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	Hsinchu	State/Province	
Postal Code	300	Country i	TW

Inventor 2 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chih-Han		LIN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Hsinchu City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	NO.8, LI-HSIN RD.6		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	Hsinchu	State/Province	
Postal Code	300	Country i	TW

Inventor 3 — Remove

Legal Name

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Horng-Huei		TSENG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Hsinchu City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	NO.8, LI-HSIN RD.6		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	Hsinchu	**State/Province**	
Postal Code	300	**Country** i	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	97149
Email Address	docket@mabr.com — Add Email — Remove Email

Application Information:

Title of the Invention	SOURCE AND DRAIN PROCESS FOR FINFET		
Attorney Docket Number	T1516.10285US01	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	97149		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Remove

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	
If the Applicant is an Organization check here.	☒
Organization Name	TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.

Mailing Address Information For Applicant:

Address 1	NO.8, LI-HSIN RD.6		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	HSINCHU	**State/Province**	
Country	TW	Postal Code	300
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/R. Burns Israelsen/		Date (YYYY-MM-DD)	2015-12-30
First Name	R. Burns	Last Name	Israelsen	Registration Number	42685

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	T1516.10285US01
	Application Number	
Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SOURCE AND DRAIN PROCESS FOR FINFET
First Named Inventor/Applicant Name:	Che-Cheng CHANG
Filer:	Robert Burns Israelsen/Vanessa Mangum
Attorney Docket Number:	T1516.10285US01

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
	Total in USD ($)			**1600**

Electronic Acknowledgement Receipt

EFS ID:	24477770
Application Number:	14984514
International Application Number:	
Confirmation Number:	7120
Title of Invention:	SOURCE AND DRAIN PROCESS FOR FINFET
First Named Inventor/Applicant Name:	Che-Cheng CHANG
Customer Number:	97149
Filer:	Robert Burns Israelsen/Vanessa Mangum
Filer Authorized By:	Robert Burns Israelsen
Attorney Docket Number:	T1516.10285US01
Receipt Date:	30-DEC-2015
Filing Date:	
Time Stamp:	15:58:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1600
RAM confirmation Number	2746
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	T1516-10285US01_Declaration.pdf	290055 4b14d3c2d8339235d2295b717790497aedbd9825	no	6
Warnings:					
Information:					
2	Drawings-only black and white line drawings	T1516-10285US01_Drawings.pdf	287609 06292d64036e90e3e719adee96ad4a29f521f44c	no	10
Warnings:					
Information:					
3		T1516-10285US01_Specification.pdf	359617 50660029cd97f80f5208ad05c437208a551a5878	yes	21

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	16
Claims	17	20
Abstract	21	21

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
Warnings:					
Information:					
4	Power of Attorney	T1516-10285US01_POA_.pdf	758167 eff32901a71dba5fb67a5e8f1940a2606f6db4e2	no	2
Warnings:					
Information:					
5	Application Data Sheet	T1516-10285US01_ADS.pdf	1822944 c1b077df0c837f9195eb5845093f613d8271abf5	no	9
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	35211 1b21f1e59470d6868684a599949e5e938163e1fc	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	3553603

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PTO/AIA/01 (06-12)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ■ The attached application, or
- ☐ United States application or PCT international application number ________________

  filed on ________________________.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Che-Cheng CHANG Date (Optional) : 2015/12/24

Signature: Che-Cheng Chang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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ochangzb 2015/12/24 11:05:33

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET

As the below named inventor, I hereby declare that:

This declaration is directed to:

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- [ ] United States application or PCT international application number ____________

filed on ____________.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Chih-Han LIN   Date (Optional): 2015/12/24

Signature: Chih-Han Lin

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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ochangzb 2015/12/24 11:05:33

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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NP-17724-US/P20150972US00

PTO/AIA/01 (06-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SOURCE AND DRAIN PROCESS FOR FINFET

As the below named inventor, I hereby declare that:

This declaration is directed to:

■ The attached application, or

☐ United States application or PCT international application number ____________

filed on ____________.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Horng-Huei TSENG Date (Optional) : ____________

Signature: Horng-Huei Tseng

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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cchangzb 2015/12/24 11:05:49

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

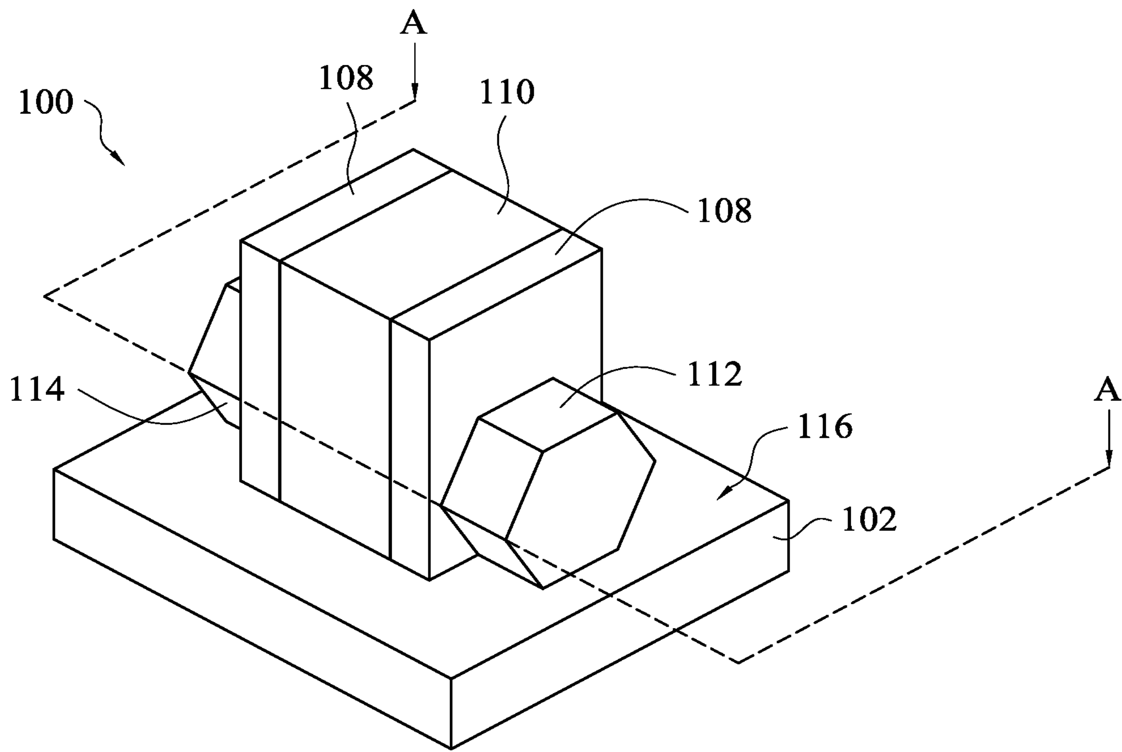

FIG. 1A

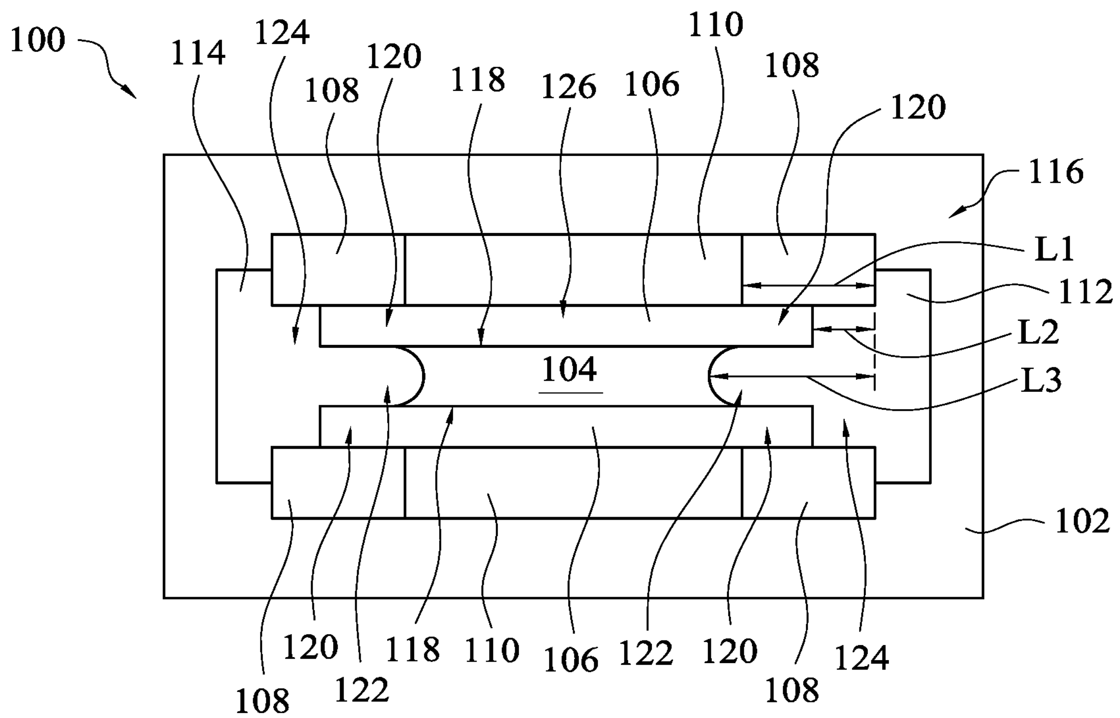

FIG. 1B

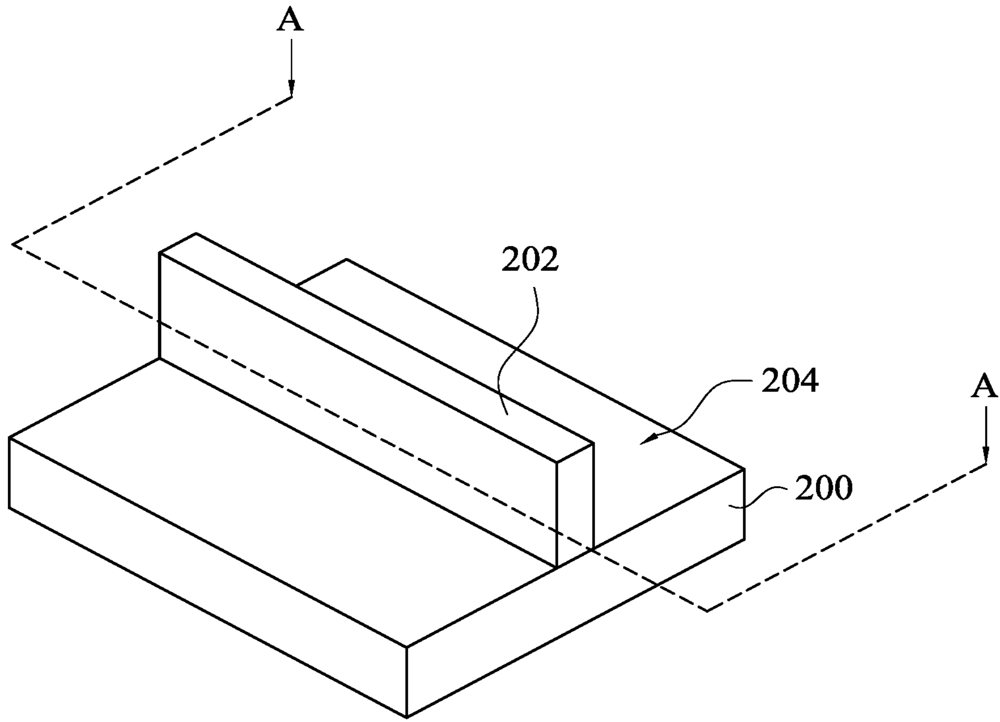

FIG. 2A

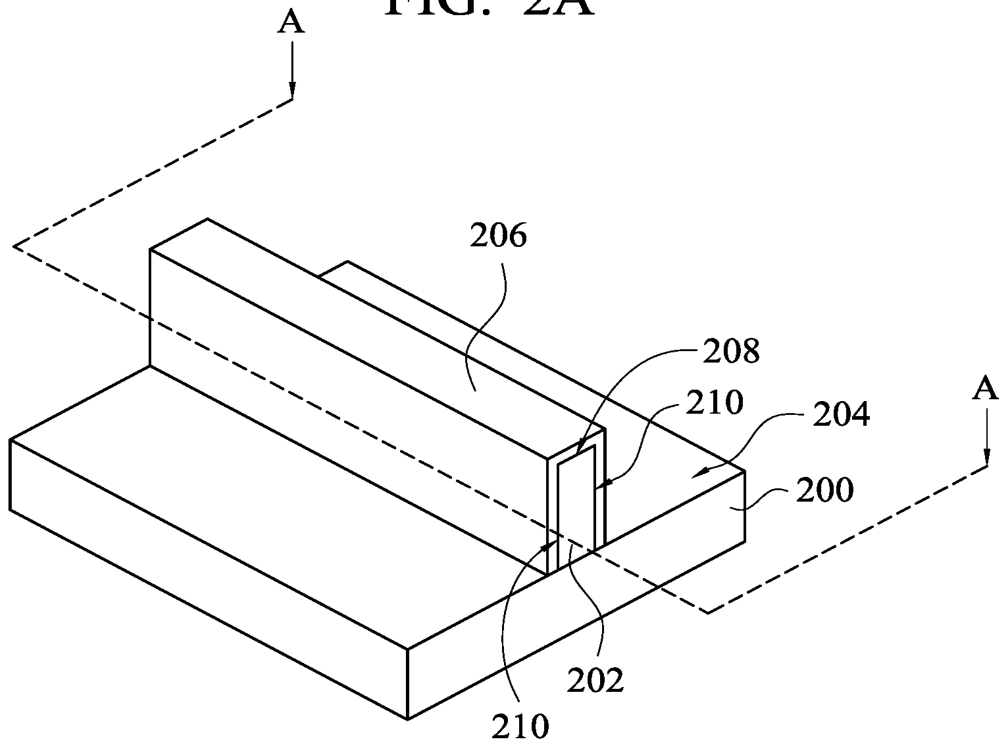

FIG. 2B

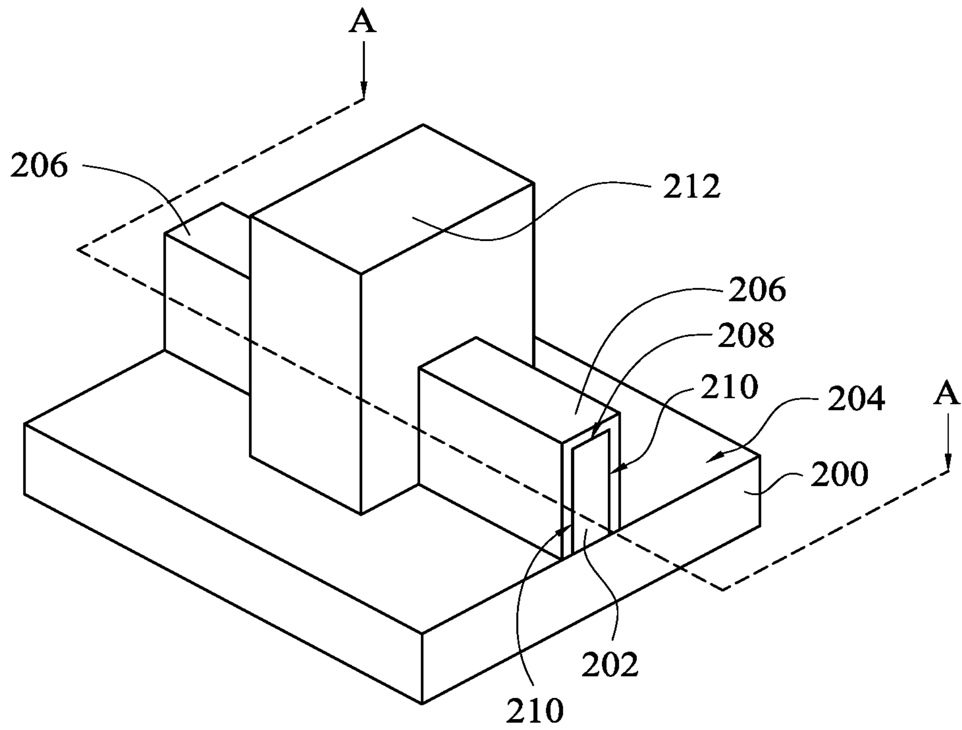

FIG. 2C

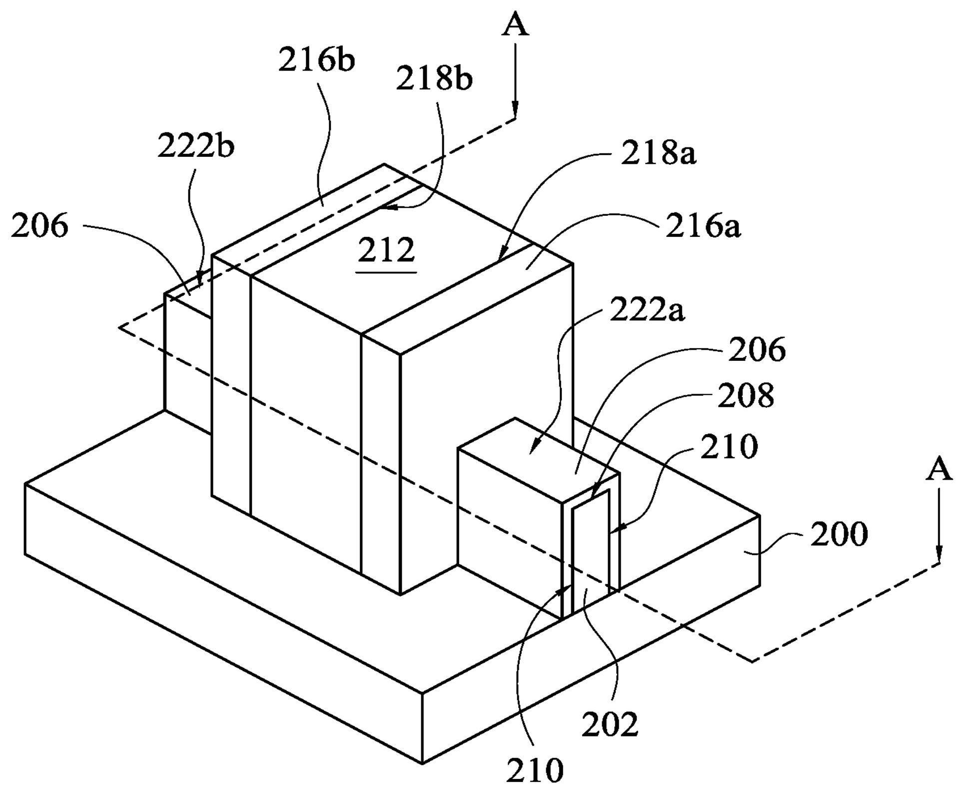

FIG. 2D

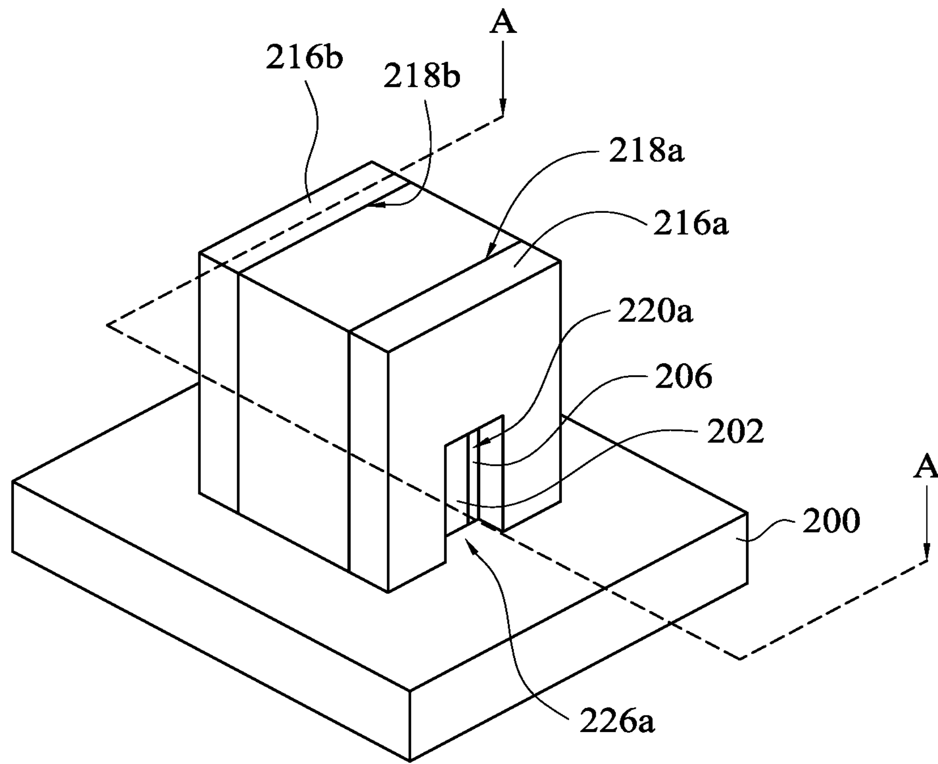

FIG. 2E

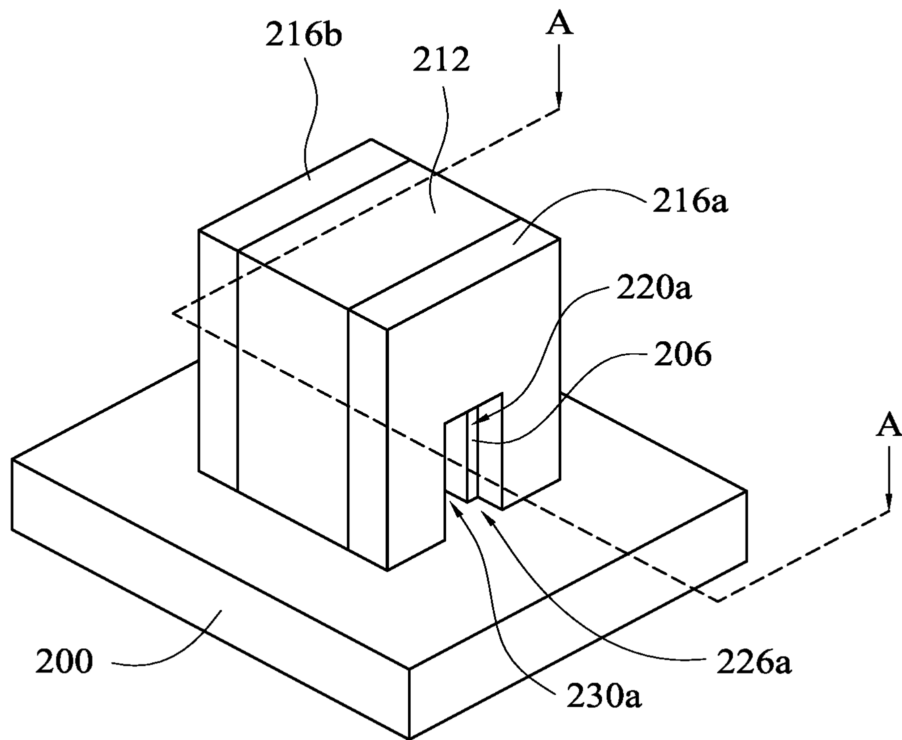

FIG. 2F

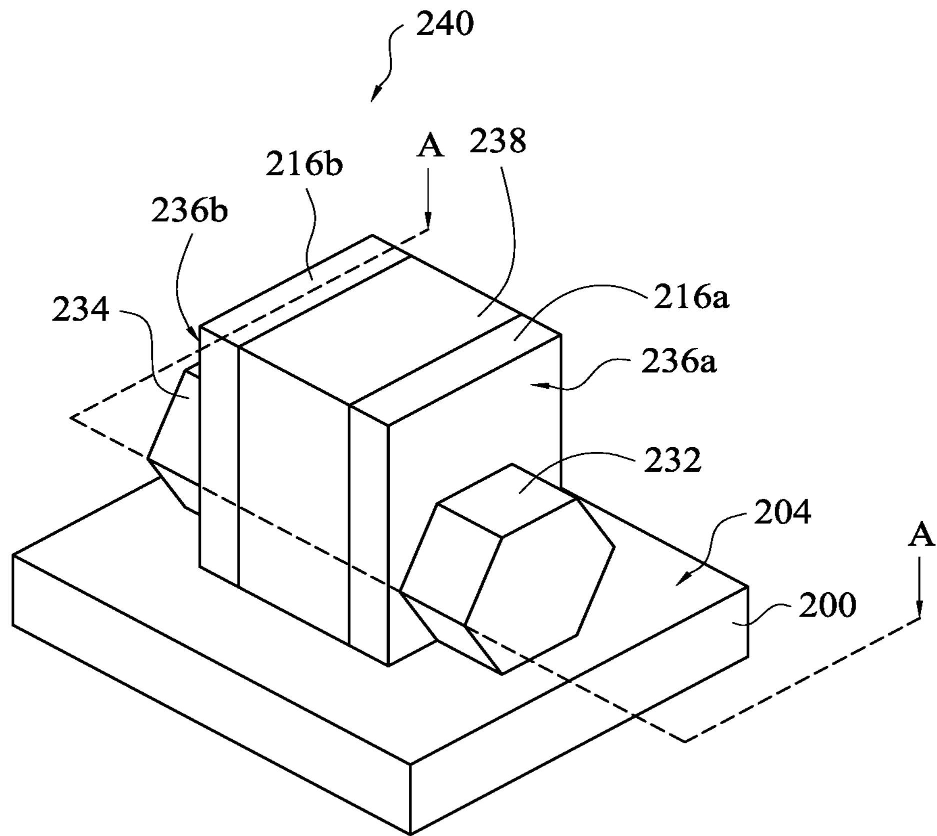

FIG. 2G

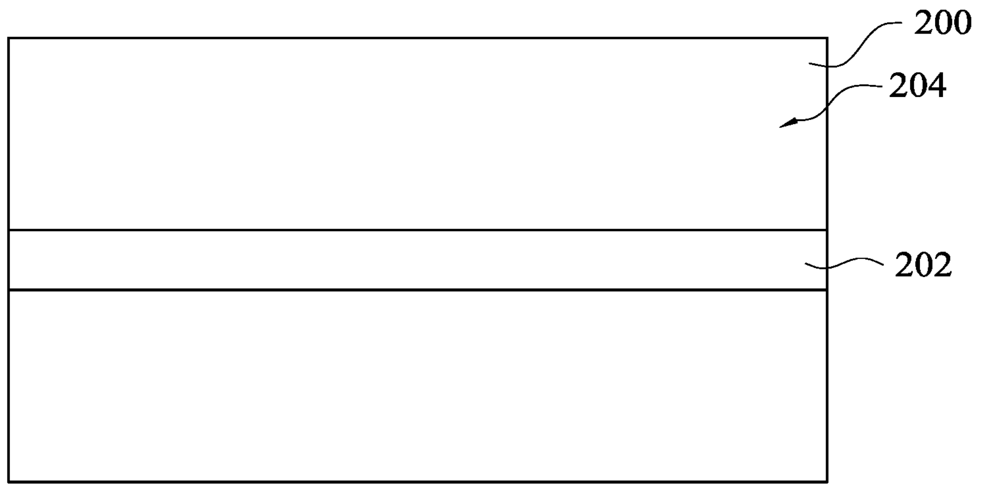

FIG. 3A

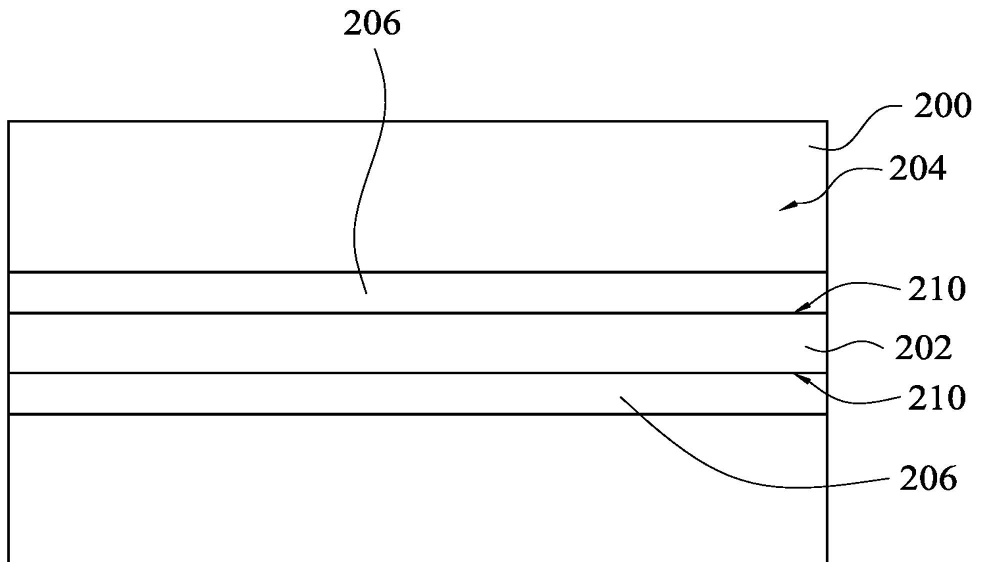

FIG. 3B

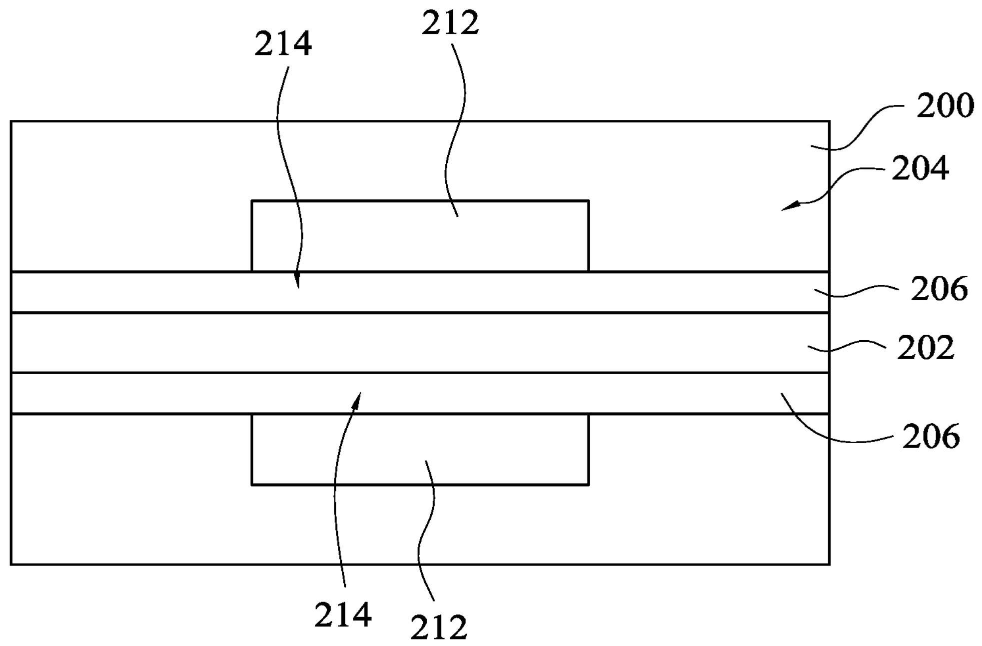

FIG. 3C

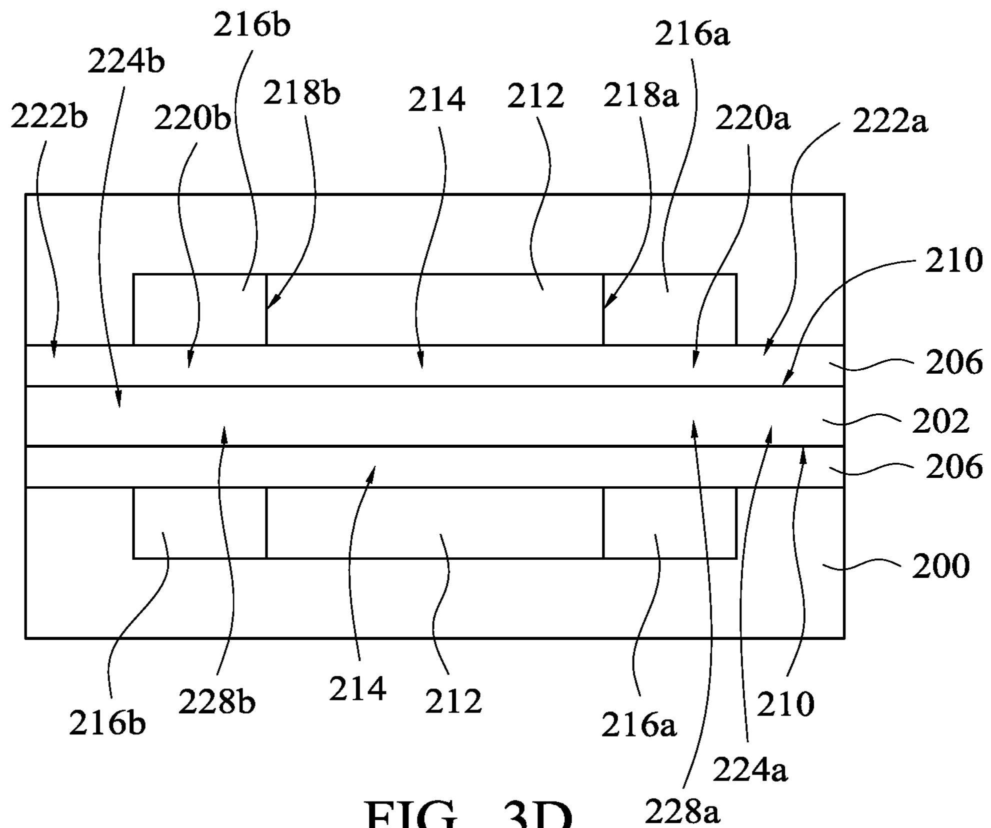

FIG. 3D

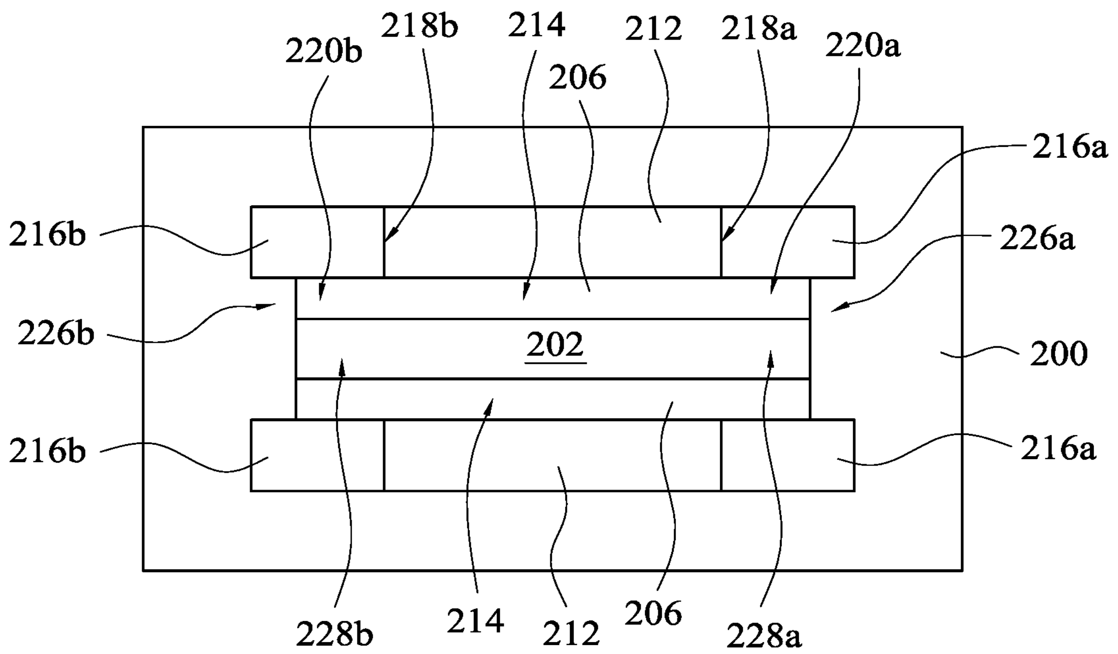

FIG. 3E

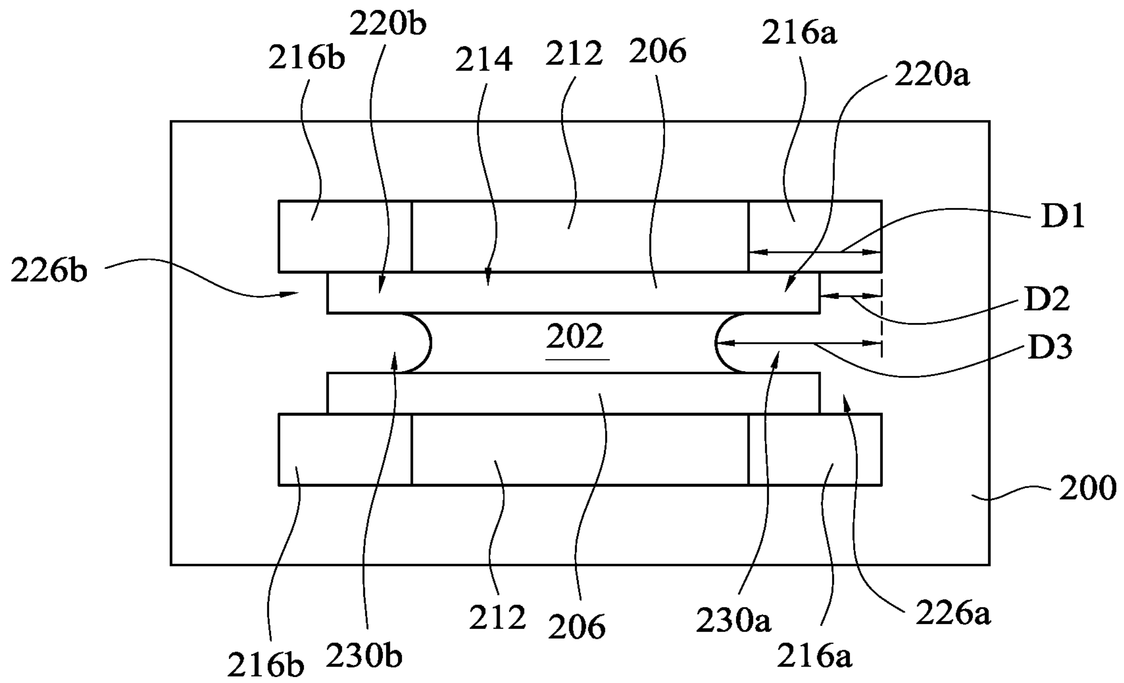

FIG. 3F

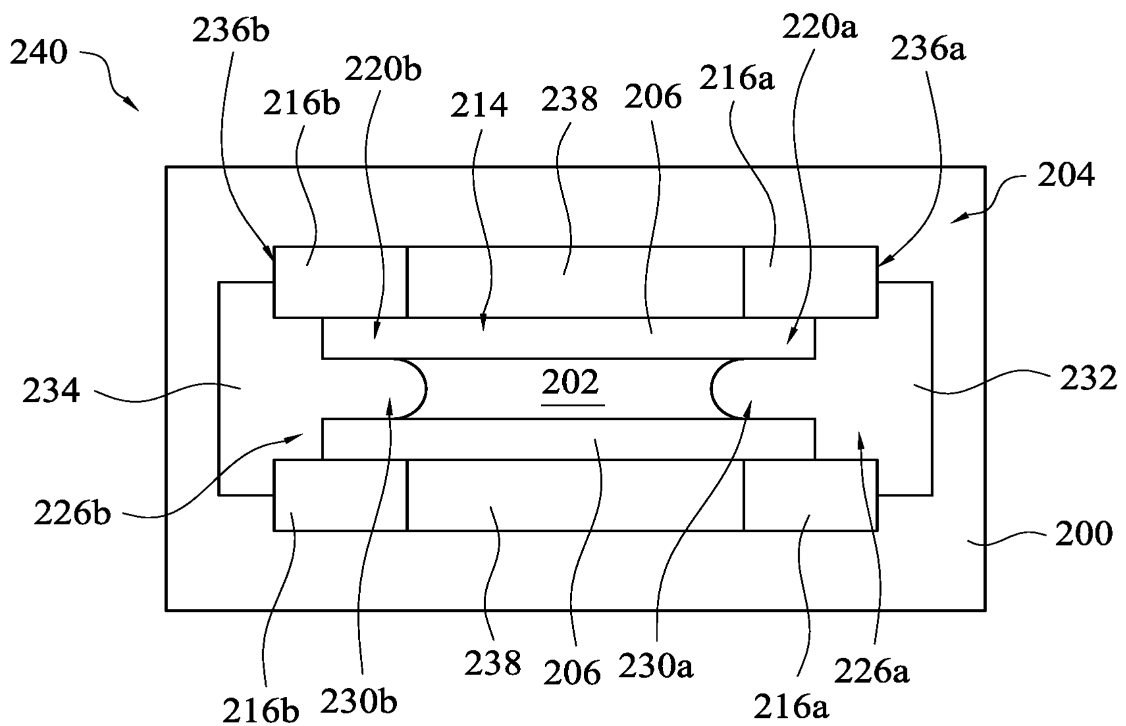

FIG. 3G

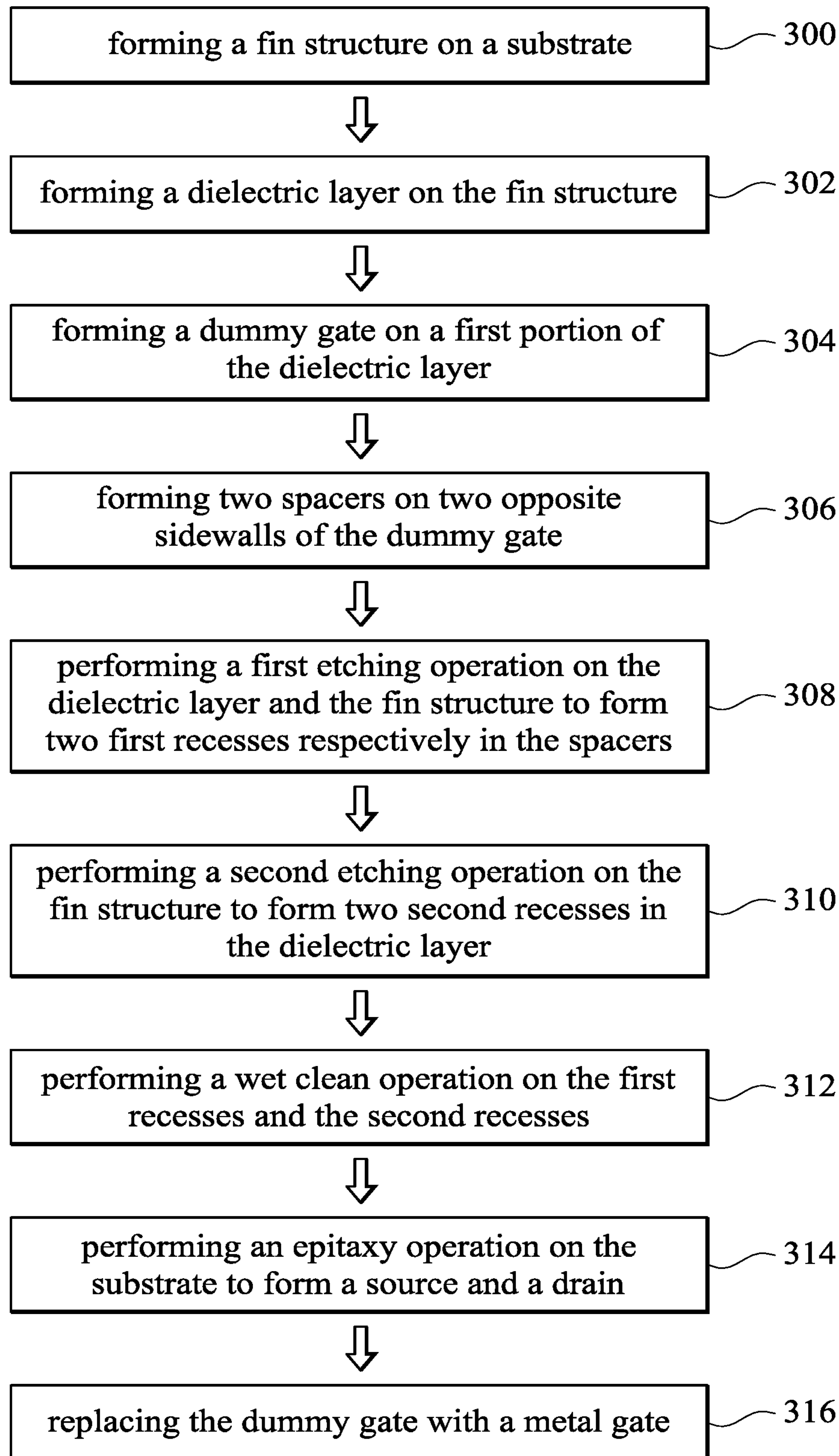

FIG. 4

SOURCE AND DRAIN PROCESS FOR FINFET

BACKGROUND

[0001] The semiconductor integrated circuit (IC) industry has experienced rapid growth. In the course of the IC evolution, functional density (defined as the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. A scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. But, such scaling down has increased the complexity of processing and manufacturing ICs. For these advances to be realized, similar developments in IC manufacturing are needed.

[0002] For example, as the semiconductor IC industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design have resulted in the development of three-dimensional (3D) devices such a fin-like field effect transistors (FinFETs). However, conventional FinFET devices and methods of fabricating the FinFET devices have not been entirely satisfactory in every aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. 1A is schematic three-dimensional diagram of a FinFET in accordance with various embodiments.

[0005] FIG. 1B is schematic top view of the FinFET taken along line A-A of FIG. 1A.

TSMC Exhibit 1064
Page 90 of 110

[0006] FIG. 2A through FIG. 2G are three-dimensional diagrams of intermediate stages showing a method for manufacturing a FinFET in accordance with various embodiments.

[0007] FIG. 3A through FIG. 3G are schematic top views of the FinFET taken along line A-A of FIG. 2A through 2G respectively.

[0008] FIG. 4 is a flow chart of a method for manufacturing a FinFET in accordance with various embodiments.

DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact.

[0010] Terms used herein are only used to describe the specific embodiments, which are not used to limit the claims appended herewith. For example, unless limited otherwise, the term "one" or "the" of the single form may also represent the plural form. The terms such as "first" and "second" are used for describing various devices, areas and layers, etc., though such terms are only used for distinguishing one device, one area or one layer from another device, another area or another layer. Therefore, the first area can also be referred to as the second area without departing from the spirit of the claimed subject matter, and the others are deduced by analogy. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. As

used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0011] In a typical FinFET replacement polysilicon gate (RPG) technology with a high-k metal gate last (HKMG) process, an operation of removing of a portion of a fin structure and a portion of a dielectric layer covering the fin structure needs a high over-etching amount of the fin structure and the dielectric layer, thereby enlarging a process window for each of sequential deposition process of a high-k dielectric layer and a metal gate, thus enhancing a performance of the FinFET. However, the high over-etching amount of the dielectric layer shortens a portion of the dielectric layer that is used for blocking a dummy gate which covers a portion of the dielectric layer and the underlying fin structure, such that an extrusion path is decreased to result in footing of the dummy gate, and thus causing a metal gate extrusion issue.

[0012] Embodiments of the present disclosure are directed to providing a FinFET and a method for manufacturing the FinFET, in which a first etching operation is performed on a fin structure and a dielectric layer covering the fin structure to recess the fin structure and the dielectric layer, so as to form two first recesses respectively in two spacers which cover the dielectric layer and the fin structure, and then a second etching operation is performed on the fin structure to further recess the fin structure to form two second recesses in the dielectric layer, in which the seconds respectively communicate with the first recesses. Thus, portions of the dielectric layer used for blocking a dummy gate are lengthened, the dummy gate covering the dielectric layer and the fin structure and being sandwiched between the spacers, such that each extrusion path is increased, thereby enhancing the yield of the FinFET.

[0013] Referring to FIG. 1A and FIG. 1B, FIG. 1A is schematic three-dimensional diagram of a FinFET in accordance with various embodiments, and FIG. 1B is schematic top view of the FinFET taken along line A-A of FIG. 1A. In some embodiments, a FinFET 100 includes a substrate 102, a fin structure 104, a dielectric layer 106, a metal gate 110, two spacers 108, a source 112 and a drain 114. The fin

structure 104, the dielectric layer 106, the metal gate 110, the spacers 108, the source 112 and the drain 114 are disposed on the substrate 102.

[0014] The fin structure 104 is disposed on the substrate 102. In some exemplary examples, the fin structure 104 is formed by recessing the substrate 102, and thus the fin structure 104 protrudes from a recessed surface 116 of the substrate 102, and the fin structure 104 and the substrate 102 are formed from the same material. The substrate 102 and the fin structure 104 may be composed of a single-crystalline semiconductor material or a compound semiconductor material. For example, silicon, germanium or glass may be used as a material of the substrate 102 and the fin structure 104. In some exemplary examples, the substrate 102 and the fin structure 104 are composed of silicon.

[0015] Referring to FIG. 1B again, the dielectric layer 106 is disposed on the fin structure 104 and covers two opposite side surfaces 118 of the fin structure 104. The dielectric layer 106 includes two first portions 120, in which the first portions 120 disposed at two opposite ends of the dielectric layer 106. A cross-section of each of the first portions 120 is in an inverted U-shape. Each of the first portions 120 of the dielectric layer 106 protrudes from the side surfaces 118 of the fin structure 104 to form a first recess 122 in the dielectric layer 106. Thus, the first recesses 122 are opposite to each other. In some examples, the fin structure 104 and the dielectric layer 106 are formed from different materials, such that the dielectric layer 106 has an etching selectivity with respect to the fin structure 104 during an operation of etching the fin structure 104. For example, the fin structure 104 may be formed from silicon, and the dielectric layer 106 may be formed from silicon oxide.

[0016] Referring to FIG. 1A and FIG. 1B, the metal gate 110 is disposed on a second portion 126 of the dielectric layer 106. In the dielectric layer 106, the second portion 126 is adjacent to the first portions 120, in which the first portions 120 are located at two opposite ends of the second portion 126, such that the second portion 126 is sandwiched between the first portions 120. A cross-section of the metal gate 110 is in an inverted U-shape.

[0017] As shown in FIG. 1A and FIG. 1B, the spacers 108 are respectively disposed on the first portions 120 of the dielectric layer 106. A cross-section of each of the spacers 108 is in an inverted U-shape. The spacers 108 respectively protrude from the first portions 120 of the dielectric layer 106 which are covered by the spacer 108, so as to form two second recesses 124 in the spacers 108. The second recesses 124 correspondingly communicate with the first recesses 122. In some examples, the spacers 108 and the fin structure 104 are formed from different materials, such that the spacers 108 have an etching selectivity with respect to the fin structure 104 during an operation of etching the fin structure 104. In some exemplary examples, the spacers 108, the dielectric layer 106 and the fin structure 104 are formed from different materials. For example, the spacers 108 may be formed from silicon nitride, while the fin structure 104 may be formed from silicon, and the dielectric layer 106 may be formed from silicon oxide.

[0018] As shown in FIG. 1B, the fin structure 104 is further recessed to form the first recesses 122, such that a length L1 of each spacer 108 is greater than a length L2 of each second recess 124, and a length L3 of a combination of the first recess 122 and the corresponding second recess 124 is greater than the length L1 of each spacer 108. In some exemplary examples, the length L1, the length L2 and the length L3 are within a range from 0.5Å to 100Å.

[0019] As shown in FIG. 1A and FIG. 1B, the source 112 is disposed in one of the first recess 122 and the corresponding second recess 124 on the substrate 102, and protrudes from the second recess 124. In addition, the drain 114 is disposed in the other one of the first recess 122 and the corresponding second recess 124 on the substrate 102, and protrudes from the second recess 124. In some examples, the source 112 and the drain 114 may extend through the recessed surface 116 into the substrate 102. For example, each of the source 112 and the drain 114 may include an epitaxy layer. In some exemplary examples, the source 112 and the drain 114 are formed from silicon germanium (SiGe).

[0020] Referring to FIG. 1B again, the first recesses 122 are respectively formed in the first portions 120 of the dielectric layer 106, such that extrusion paths of the metal gate 110 are increased with the existence of the first portions 120 of the dielectric layer 106, and thus the metal gate 110 can be effectively blocked by the first portions 120 of the dielectric layer 106, thereby enhancing the yield of the FinFET 100.

[0021] Referring to FIG. 2A through FIG. 2G and FIG. 3A through FIG. 3G, FIG. 2A through FIG. 2G are three-dimensional diagrams of intermediate stages showing a method for manufacturing a FinFET in accordance with various embodiments, and FIG. 3A through FIG. 3G are schematic top views of the FinFET taken along line A-A of FIG. 2A through 2G respectively. As shown in FIG. 2A and FIG. 3A, a substrate 200 is provided. In some examples, the substrate 200 may be optionally recessed to form a fin structure 202 on a surface 204 of the substrate 200 by using, for example, a photolithography process and an etching process.

[0022] In the operation of recessing the substrate 200, a portion of the substrate 200 is removed. In such examples, the fin structure 202 is composed of a portion of the substrate 200, such that the fin structure 202 is formed from a material the same as that of the substrate 200. The substrate 200 and the fin structure 202 may be composed of a single-crystalline semiconductor material or a compound semiconductor material. In some examples, silicon, germanium or glass may be used as a material of the substrate 200 and the fin structure 202. In some exemplary examples, the substrate 200 and the fin structure 202 are formed from silicon.

[0023] As shown in FIG. 2B and FIG. 3B, a dielectric layer 206 is formed on a top surface 208 and two opposite side surfaces 210 of the fin structure 202. In the fin structure 202, the side surfaces 210 are connected to two opposite edges of the top surface 208. For example, the side surfaces 210 may extend along an extending direction of the fin structure. Thus, a cross-section of each of the dielectric layer 206 is in an inverted U-shape. For example, the dielectric layer 206 may be formed by using a deposition process or a thermal oxidation process. The deposition process may be a chemical vapor deposition (CVD) process or a plasma-enhanced chemical vapor

TSMC Exhibit 1064
Page 95 of 110

deposition (PECVD) process. In some examples, the fin structure 202 and the dielectric layer 206 are formed from different materials, such that the dielectric layer 206 has an etching selectivity with respect to the fin structure 202 during an operation of etching the fin structure 202. For example, the fin structure 202 may be formed from silicon, and the dielectric layer 206 may be formed from silicon oxide.

[0024] As shown in FIG. 2C and FIG. 3C, a dummy gate 212 is formed on a first portion 214 of the dielectric layer 206. In some exemplary examples, the dummy gate 212 extends from one of the side surfaces 210 to the other one of the side surfaces 210 through the top surface 208 of the fin structure 202, such that a cross-section of the dummy gate 212 is in an inverted U-shape. In some examples, the dummy gate 212 is formed by using a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process, for example. In some exemplary examples, the dummy gate 212 is formed from polysilicon.

[0025] As shown in FIG. 2D and FIG. 3D, two spacers 216a and 216b are respectively formed on two opposite sidewalls 218a and 218b of the dummy gate 212. In some examples, an operation of forming the spacers 216a and 216b includes forming the spacers 216a and 216b on two second portions 220a and 220b of the dielectric layer 206 respectively, and exposing two third portions 222a and 222b of the dielectric layer 206. In the dielectric layer 206, the second portion 220a is located between the first portion 214 and the third portion 222a, and the second portion 220b is located between the first portion 214 and the third portion 222b. For example, the second portions 220a and 220b are closely adjacent to opposite sides of the first portion 214 respectively, and the third portions 222a and 222b are closely adjacent to the second portions 220a and 220b respectively.

[0026] As shown in FIG. 2D, each of the spacers 216a and 216b extends from one of the side surfaces 210 to the other one of the side surfaces 210 through the top surface 208 of the fin structure 202, such that a cross-section of each of the spacers 216a and 216b is in an inverted U-shape. For example, the spacers 216a and 216b are formed by

using a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a physical vapor deposition (PVD) process, for example. The etching process may be an etching back process. In some examples, the spacers 216a and 216b and the fin structure 202 are formed from different materials, such that the spacers 216a and 216b have an etching selectivity with respect to the fin structure 202 during an operation of etching the fin structure 202. In some exemplary examples, the spacers 216a and 216b, the dielectric layer 206 and the fin structure 202 are formed from different materials. For example, the spacers 216a and 216b may be formed from silicon nitride, while the fin structure 202 may be formed from silicon, and the dielectric layer 206 may be formed from silicon oxide.

[0027] Referring to FIG. 3D, a first etching operation is performed on the dielectric layer 206 and the fin structure 202 to remove the third portions 222a and 222b and a portion of each of the second portions 220a and 220b of the dielectric layer 206, and two first portions 224a and 224b of the fin structure 202 underlying the third portions 222a and 222b and the portions of the second portions220a and 220b of the dielectric layer 206. As shown in FIG. 2E and FIG. 3E, after the first etching operation is completed, the spacers 216a and 216b respectively protrude from the first portions 220a and 220b of the dielectric layer 206, so as to form two first recesses 226a and 226b in the spacers 216a and 216b respectively. In some examples, the first etching operation is a high bias etching operation. The first etching operation may be performed by using a dry etching technique.

[0028] Referring to FIG. 3D and FIG. 3E simultaneously, a second etching operation is performed on the fin structure 202 to remove two second portions 228a and 228b of the fin structure 202 which are respectively adjacent to the first portions 224a and 224b of the fin structure 202. As shown in FIG. 2F and FIG. 3F, after the second etching operation is completed, the remaining second portions 220a and 220b of the dielectric layer 206 protrude from two opposite ends of the fin structure 202 to respectively form second recesses 230a and 230b in the dielectric layer 206. The second recesses 230a and 230b correspondingly communicate with the first recesses 226a and 226b. In some examples, the second etching operation is a high selectivity etching operation, and the

dielectric layer 206 has an etching selectivity with respect to the fin structure 202 during the second etching operation. Thus, a cross-section of each of the second portions 220a and 220b of the dielectric layer may be in an inverted U-shape after the second etching operation is completed. The second etching operation may be performed by using a dry etching technique.

[0029] Referring to FIG. 3F again, with a two-step etching process, the fin structure 202 is further recessed to form the second recesses 230a and 230b during the second etching operation, such that a length D1 of each of the spacers 216a and 216b is greater than a length D2 of each of the first recesses 226a and 226b, and a length D3 of a combination of the first recess 226a and the second recess 230a or a combination of the first recess 226b and the second recess 230b is greater than the length D1 of each of the spacers 216a and 216b. In some exemplary examples, the length D1, the length D2 and the length D3 are within a range from 0.5Å to 100Å.

[0030] By using a two-step etching process, the second recesses 230a and 230b are respectively formed in the second portions 220a and 220b of the dielectric layer 206, such that extrusion paths of the dummy gate 212 are increased with the existence of the second portions 220a and 220b of the dielectric layer 206, and thus the dummy gate 212 can be effectively blocked by the second portions 220a and 220b of the dielectric layer 206.

[0031] In some examples, after the second etching operation is completed, a wet clean operation may be optionally performed on the first recesses 226a and 226b and the second recesses 230a and 230b to remove particles, products and/or contaminants from the first recesses 226a and 226b and the second recesses 230a and 230b. During the wet clean operation, the dummy gate 212 can be effectively protected by the second portions 220a and 220b of the dielectric layer 206, thereby preventing the dummy gate 212 from extruding.

[0032] As shown in FIG. 2G and FIG. 3G, a source 232 may be formed in the first recess 226a and the second recess 230a on the substrate 200, and a drain 234 may be formed in the first recess 226b and the second recess 230b on the substrate 200. For

example, the source 232 may be formed to fill the first recess 226a and the second recess 230a and protrude from the spacer 216a, such that the source 232 may cover a portion of an outer surface 236a of the spacer 216a and a portion of the surface 204 of the substrate 200. The drain 234 may be formed to fill the first recess 226b and the second recess 230b and protrude from the spacer 216b, such that the drain 234 may cover a portion of an outer surface 236b of the spacer 216b and a portion of the surface 204 of the substrate 200. In some examples, an operation of forming the source 232 and the drain 234 is performed by using an epitaxy process. In some exemplary examples, each of the source 232 and the drain 234 is formed to include a silicon germanium (SiGe) layer.

[0033] Referring to FIG. 2F and FIG. 2G simultaneously, after the source 232 and the drain 234 are completed, the dummy 212 are replaced with a metal gate 238 to complete a FinFET 240. In some examples, an operation of replacing the dummy gate 212 includes removing the dummy gate 212 to form a recess between the spacers 216a and 216b and expose the first portion 214 of the dielectric layer 206, and forming the metal gate 238 fill the recess and cover the first portion 214 of the dielectric layer 206. For example, an operation of removing the dummy gate 212 may be performed using a dry etching technique or a wet etching technique. An operation of forming the metal gate 238 may be performed by using a deposition process and a patterning process, in which the deposition process may be a chemical vapor deposition process or a physical vapor deposition process, and the patterning process may include a chemical mechanical polishing process.

[0034] Referring to FIG. 4 with FIG. 2A through FIG. 2G and FIG. 3A through FIG. 3G, FIG. 4 is a flow chart of a method for manufacturing a FinFET in accordance with various embodiments. The method begins at operation 300, where a substrate 200 is provided. In some examples, the substrate 200 may be optionally recessed to form a fin structure 202 on a surface 204 of the substrate 200 by using, for example, a photolithography process and an etching process. In the operation of recessing the substrate 200, a portion of the substrate 200 is removed. In such examples, the fin structure 202 is composed of a portion of the substrate 200, such that the fin structure

202 is formed from a material the same as that of the substrate 200. In some examples, silicon, germanium or glass may be used as a material of the substrate 200 and the fin structure 202.

[0035] At operation 302, as shown in FIG. 2B and FIG. 3B, a dielectric layer 206 is formed on a top surface 208 and two opposite side surfaces 210 of the fin structure 202. In the fin structure 202, the side surfaces 210 are connected to two opposite edges of the top surface 208. For example, the dielectric layer 206 may be formed by using a deposition process or a thermal oxidation process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process. The fin structure 202 and the dielectric layer 206 are formed from different materials, such that the dielectric layer 206 has an etching selectivity with respect to the fin structure 202 during an operation of etching the fin structure 202.

[0036] At operation 304, as shown in FIG. 2C and FIG. 3C, a dummy gate 212 is formed on a first portion 214 of the dielectric layer 206 by using, for example, a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a plasma-enhanced chemical vapor deposition process. In some exemplary examples, the dummy gate 212 extends from one of the side surfaces 210 to the other one of the side surfaces 210 through the top surface 208 of the fin structure 202, such that a cross-section of the dummy gate 212 is in an inverted U-shape. In some exemplary examples, the dummy gate 212 is formed from polysilicon.

[0037] At operation 306, as shown in FIG. 2D and FIG. 3D, two spacers 216a and 216b are respectively formed on two opposite sidewalls 218a and 218b of the dummy gate 212 by using for example, a deposition process and an etching process. The deposition process may be a chemical vapor deposition process or a physical vapor deposition process. The etching process may be an etching back process. In some examples, an operation of forming the spacers 216a and 216b includes forming the spacers 216a and 216b on two second portions 220a and 220b of the dielectric layer 206 respectively, and exposing two third portions 222a and 222b of the dielectric layer 206. In the dielectric layer 206, the second portion 220a is located between the first portion

214 and the third portion 222a, and the second portion 220b is located between the first portion 214 and the third portion 222b. For example, the second portions 220a and 220b are closely adjacent to opposite sides of the first portion 214 respectively, and the third portions 222a and 222b are closely adjacent to the second portions 220a and 220b respectively, such that the second portion 220a is sandwiched between the first portion 214 and the third portion 222a, and the second portion 220b is sandwiched between the first portion 214 and the third portion 222b.

[0038] Referring to FIG. 2D again, each of the spacers 216a and 216b extends from one of the side surfaces 210 to the other one of the side surfaces 210 through the top surface 208 of the fin structure 202, such that a cross-section of each of the spacers 216a and 216b is in an inverted U-shape. In some examples, the spacers 216a and 216b and the fin structure 202 are formed from different materials, such that the spacers 216a and 216b have an etching selectivity with respect to the fin structure 202 during an operation of etching the fin structure 202. In some exemplary examples, the spacers 216a and 216b, the dielectric layer 206 and the fin structure 202 are formed from different materials. For example, the spacers 216a and 216b may be formed from silicon nitride, the fin structure 202 may be formed from silicon, and the dielectric layer 206 may be formed from silicon oxide.

[0039] At operation 308, as shown in FIG. 3D, a first etching operation is performed on the dielectric layer 206 and the fin structure 202 to remove the third portions 222a and 222b and a portion of each of the second portions 220a and 220b of the dielectric layer 206, and two first portions 224a and 224b of the fin structure 202 underlying the third portions 222a and 222b and the portions of the second portions220a and 220b of the dielectric layer 206. In some examples, the first etching operation is a high bias etching operation. The first etching operation may be performed by using a dry etching technique. As shown in FIG. 2E and FIG. 3E, after the first etching operation is completed, the spacers 216a and 216b respectively protrude from the first portions 220a and 220b of the dielectric layer 206, so as to form two first recesses 226a and 226b in the spacers 216a and 216b respectively.

[0040] At operation 310, referring to FIG. 3D and FIG. 3E simultaneously, a second etching operation is performed on the fin structure 202 to remove two second portions 228a and 228b of the fin structure 202 which are respectively adjacent to the first portions 224a and 224b of the fin structure 202. As shown in FIG. 2F and FIG. 3F, after the second etching operation is completed, the remaining second portions 220a and 220b of the dielectric layer 206 protrude from two opposite ends of the fin structure 202 to respectively form second recesses 230a and 230b in the dielectric layer 206. The second recesses 230a and 230b respectively communicate with the first recesses 226a and 226b. In some examples, the second etching operation is a high selectivity etching operation, and the dielectric layer 206 has an etching selectivity with respect to the fin structure 202 during the second etching operation. Thus, a cross-section of each of the remaining second portions 220a and 220b of the dielectric layer may be in an inverted U-shape. The second etching operation may be performed by using a dry etching technique.

[0041] At operation 312, referring to FIG. 2F and FIG. 3F again, after the second etching operation is completed, a wet clean operation may be optionally performed on the first recesses 226a and 226b and the second recesses 230a and 230b to remove particles, products and/or contaminants from the first recesses 226a and 226b and the second recesses 230a and 230b. During the wet clean operation, the dummy gate 212 can be effectively protected by the second portions 220a and 220b of the dielectric layer 206, thereby preventing the dummy gate 212 from extruding.

[0042] At operation 314, as shown in FIG. 2G and FIG. 3G, a source 232 may be formed in the first recess 226a and the second recess 230a on the substrate 200, and a drain 234 may be formed in the first recess 226b and the second recess 230b on the substrate 200 by using an epitaxy process. For example, the source 232 may be formed to fill the first recess 226a and the second recess 230a and protrude from the spacer 216a, such that the source 232 may cover a portion of an outer surface 236a of the spacer 216a and a portion of the surface 204 of the substrate 200. The drain 234 may be formed to fill the first recess 226b and the second recess 230b and protrude from the spacer 216b, such that the drain 234 may cover a portion of an outer surface 236b of the

spacer 216b and a portion of the surface 204 of the substrate 200. In some exemplary examples, each of the source 232 and the drain 234 is formed to include a silicon germanium layer.

[0043] At operation 316, referring to FIG. 2F and FIG. 2G simultaneously, after the epitaxy process is completed, the dummy 212 are replaced with a metal gate 238 to complete a FinFET 240. In some examples, an operation of replacing the dummy gate 212 includes removing the dummy gate 212 to form a recess between the spacers 216a and 216b and expose the first portion 214 of the dielectric layer 206, and forming the metal gate 238 fill the recess and cover the first portion 214 of the dielectric layer 206. For example, an operation of removing the dummy gate 212 may be performed using a dry etching technique or a wet etching technique. An operation of forming the metal gate 238 may be performed by using a deposition process and a patterning process, in which the deposition process may be a chemical vapor deposition process or a physical vapor deposition process, and the patterning process may include a chemical mechanical polishing process.

[0044] In accordance with an embodiment, the present disclosure discloses a method for manufacturing a FinFET. In this method, a fin structure is formed on a substrate. A dielectric layer is formed on a top surface and two side surfaces of the fin structure, in which the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials. A dummy gate is formed on a first portion of the dielectric layer. Two spacers are respectively formed on two opposite sidewalls of the dummy gate. An operation of forming the spacers includes forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, in which each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer. A first etching operation is performed on the dielectric layer and the fin structure to remove the third portions and a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers. A second etching

operation is performed on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, in which the second recesses respectively communicate with the first recesses.

[0045] In accordance with another embodiment, the present disclosure discloses a method for manufacturing a FinFET. In this method, a fin structure is formed on a substrate. A dielectric layer is formed on a top surface and two side surfaces of the fin structure, in which the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials. A dummy gate is formed on a first portion of the dielectric layer. Two spacers are respectively formed on two opposite sidewalls of the dummy gate. An operation of forming the spacers includes forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, in which each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer. A first etching operation is performed on the dielectric layer and the fin structure to remove the third portions of the dielectric layer, a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions of the dielectric layer and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers. A second etching operation is performed on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses. A wet clean operation is performed on the first recesses and the second recesses. An epitaxy operation is performed on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate.

[0046] In accordance with yet another embodiment, the present disclosure discloses a FinFET. The FinFET includes a substrate, a fin structure, a dielectric layer, a metal

gate, two spacers, a source and a drain. The fin structure is disposed on the substrate. The dielectric layer is disposed on the fin structure and covers two opposite side surfaces of the fin structure, in which the dielectric layer includes two first portions protruding from the side surfaces of the fin structure, such that two first recesses are formed in the dielectric layer, and the first recesses are opposite to each other. The metal gate is disposed on a second portion of the dielectric layer, in which the second portion is sandwiched between the first portions of the dielectric layer. The spacers are disposed on the first portions of the dielectric layer respectively, in which the spacers respectively protrude from the first portions of the dielectric layer, such that two second recesses are formed in the spacers. The source is disposed in one of the first recesses and one of the second recesses on the substrate. The drain is disposed in the other one of the first recesses and the other one of the second recesses on the substrate.

[0047] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the fin structure to remove the third portions and a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the third portions and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers; and

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses.

2. The method of claim 1, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

3. The method of claim 1, wherein the operation of forming the spacers forms the spacers from silicon nitride.

4. The method of claim 1, wherein an operation of forming the dummy gate forms the dummy gate from polysilicon.

5. The method of claim 1, the method further comprising performing a wet clean operation on the first recesses and the second recesses after the second etching operation is completed.

6. The method of claim 1, the method further comprising performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate after the second etching operation is completed.

7. The method of claim 6, wherein the epitaxy operation forms the source and the drain each of which comprises a silicon germanium (SiGe) layer.

8. The method of claim 6, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

9. A method for manufacturing a FinFET, the method comprising:

forming a fin structure on a substrate;

forming a dielectric layer on a top surface and two side surfaces of the fin structure, wherein the side surfaces are connected to two opposite edges of the top surface, and the fin structure and the dielectric layer are formed from different materials;

forming a dummy gate on a first portion of the dielectric layer;

forming two spacers respectively on two opposite sidewalls of the dummy gate, wherein an operation of forming the spacers comprises forming the spacers respectively on two second portions of the dielectric layer and exposing two third portions of the dielectric layer, wherein each of the second portions of the dielectric layer is located between the first portion and one of the third portions of the dielectric layer;

performing a first etching operation on the dielectric layer and the fin structure to remove the third portions of the dielectric layer, a portion of each of the second portions of the dielectric layer, and two first portions of the fin structure underlying the

third portions of the dielectric layer and the portions of the second portions of the dielectric layer, thereby forming two first recesses respectively in the spacers;

performing a second etching operation on the fin structure to remove two second portions of the fin structure which are respectively adjacent to the first portions of the fin structure, thereby forming two second recesses in the dielectric layer, wherein the second recesses respectively communicate with the first recesses;

performing a wet clean operation on the first recesses and the second recesses; and

performing an epitaxy operation on the substrate to form a source in one of the first recesses and one of the second recesses on the substrate, and to form a drain in the other one of the first recesses and the other one of the second recesses on the substrate.

10. The method of claim 9, wherein an operation of forming the fin structure forms the fin structure from silicon, and an operation of forming the dielectric layer forms the dielectric layer from silicon oxide.

11. The method of claim 9, wherein the operation of forming the spacers forms the spacers from silicon nitride.

12. The method of claim 9, wherein an operation of forming the dummy gate forms the dummy gate from polysilicon.

13. The method of claim 9, wherein the epitaxy operation is performed to form the source and the drain each of which comprises a silicon germanium (SiGe) layer.

14. The method of claim 9, wherein an operation of forming the fin structure is performed by recessing the substrate.

15. The method of claim 9, the method further comprising replacing the dummy gate with a metal gate after the epitaxy operation is completed.

16. A FinFET comprising:

a substrate;

a fin structure on the substrate;

a dielectric layer which is disposed on the fin structure and covers two opposite side surfaces of the fin structure, wherein the dielectric layer comprises two first portions protruding from the side surfaces of the fin structure such that two first recesses are formed in the dielectric layer, and the first recesses are opposite to each other;

a metal gate on a second portion of the dielectric layer, wherein the second portion is sandwiched between the first portions of the dielectric layer;

two spacers on the first portions of the dielectric layer respectively, wherein the spacers respectively protrude from the first portions of the dielectric layer such that two second recesses are formed in the spacers;

a source which is disposed in one of the first recesses and one of the second recesses on the substrate; and

a drain which is disposed in the other one of the first recesses and the other one of the second recesses on the substrate.

17. The FinFET of claim 16, wherein the fin structure is formed from silicon, and the dielectric layer is formed from silicon oxide.

18. The FinFET of claim 16, wherein the spacers are formed from silicon nitride.

19. The FinFET of claim 16, wherein the source and the drain are formed from silicon germanium.

20. The FinFET of claim 16, wherein each of the source and the drain comprises an epitaxy layer.

ABSTRACT

A FinFET includes a substrate, a fin structure, a dielectric layer, a metal gate, two spacers, a source and a drain. The fin structure is disposed on the substrate. The dielectric layer is disposed on the fin structure and covers two opposite side surfaces of the fin structure. The dielectric layer includes two first portions protruding from the side surfaces of the fin structure, such that two opposite first recesses are formed in the dielectric layer. The metal gate is disposed on a second portion of the dielectric layer which is sandwiched between the first portions. The spacers are disposed on the first portions of the dielectric layer and protrude from the first portions of the dielectric layer respectively, such that two second recesses are formed in the spacers. The source and drain are respectively disposed in the first recesses and the second recesses on the substrate.

TSMC Exhibit 1064
Page 110 of 110