

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Review of: )  
U.S. Patent No. 9,318,609 )  
Issued: Apr. 19, 2016 )  
Application No.: 14/620,209 )  
Filing Date: Feb. 12, 2015 )

For: **Semiconductor Device With Epitaxial Structure**

**DECLARATION OF STEPHEN BRADLEY IN SUPPORT OF  
PETITION FOR *INTER PARTES* REVIEW OF  
UNITED STATES PATENT NO. 9,318,609**

I, Stephen Bradley, hereby declare as follows:

1. I am an attorney with Jones Day, in the Atlanta office, and am counsel for Petitioner Taiwan Semiconductor Manufacturing Company Ltd. (“TSMC”) in the above-captioned action. I submit this declaration in support of TSMC’s Petition for *Inter Partes* Review of U.S. Patent No. 9,318,609. I have personal knowledge of the facts set forth herein unless otherwise indicated.

2. Attached as Exhibit 1001 to TSMC’s Petition is a true and correct copy of U.S. Patent No. 9,318,609 B2.

3. Attached as Exhibit 1002 to TSMC’s Petition is a true and correct copy of the publicly available prosecution history of U.S. Patent No. 9,318,609 downloaded from the USPTO’s Patent Center ([patentcenter.uspto.gov](http://patentcenter.uspto.gov)).

4. Attached as Exhibit 1003 to TSMC's Petition is a true and correct copy of Dr. Jack Lee's Declaration in Support of TSMC's Petition.
5. Attached as Exhibit 1004 is a true and correct copy of U.S. Patent No. 9,166,022 B2.
6. Attached as Exhibit 1005 is a true and correct copy of U.S. Patent No. 9,281,378 B2.
7. Attached as Exhibit 1006 is a true and correct copy of U.S. Patent No. 8,809,139 B2.
8. Attached as Exhibit 1007 is a true and correct copy of a technical paper titled "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors" by T. Ghani et al. This paper was published in 2003 in the IEEE International Electron Devices Meeting 2003, pages 11.6.1-11.6.3.
9. Attached as Exhibit 1008 is a true and correct copy of excerpts from "CMOS Nanoelectronics" by Nadine Collaert, published in 2012. The excerpts are screenshots from eBook version of the publication made available via Google Play Books at the following URL:  
  
[https://play.google.com/store/books/details/Nadine\\_Collaert\\_CMOS\\_Nanoelectronics?id=srnNBQAAQBAJ&hl=en\\_US](https://play.google.com/store/books/details/Nadine_Collaert_CMOS_Nanoelectronics?id=srnNBQAAQBAJ&hl=en_US).
10. Attached as Exhibit 1013 is a true and correct copy of a technical

paper titled “Folded-channel MOSFET for deep-sub-tenth micron era” by D. Hisamoto et al. The paper was published in 1998 in the International Electron Devices Meeting 1998 – Technical Digest, pages 1032-1034.

11. Attached as Exhibit 1014 is a true and correct copy of a technical paper titled “Sub 50-nm FinFET: PMOS” by X. Huang et al. The paper was published in 1999 in the International Electron Devices Meeting 1999 – Technical Digest, pages 67-70.

12. Attached as Exhibit 1015 is a true and correct copy of a technical paper titled “FinFET – a self-aligned double-gate MOSFET scalable to 20 nm” by D. Hisamoto et al. The paper was published in 2000 in IEEE Transactions on Electron Devices, Vol. 47, No. 12, pages 2320-2325.

13. Attached as Exhibit 1016 is a true and correct copy of a New York Times article titled “Intel Increases Transistor Speed by Building Upward” by J. Markoff. The article was published in 2011 and is available at the following URL: <https://www.nytimes.com/2011/05/05/science/05chip.html>.

14. Attached as Exhibit 1017 is a true and correct copy of an Intel presentation titled “Intel’s Revolutionary 22 nm Transistor Technology.” The presentation was published in 2011 and is available at the following URL: [https://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details\\_Presentation.pdf](https://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf).

15. Attached as Exhibit 1018 is a true and correct copy of an archived copy of a presentation titled “Intel Announces first 22nm Tri-Gate Transistors, Shipping in 2H 2011” written by A. Shimpi and published on the website AnandTech. The article was published on May 4, 2011 and a PDF copy was archived by the Internet Archive’s Wayback Machine on May 18, 2011. The Wayback Machine archived the PDF hosted at the URL <http://www.anandtech.com/print/4313/intel-announces-first-22nm-3d-trigate-transistors-shipping-in-2h-2011> on that date and the archived copy is available at the following URL:

<https://web.archive.org/web/20110518133030/http://www.anandtech.com:80/print/4313/intel-announces-first-22nm-3d-trigate-transistors-shipping-in-2h-2011>.

16. Attached as Exhibit 1019 is a true and correct copy of a technical paper titled “A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 Dry Patterning, and 100% Pb-free Packaging” by K. Mistry et al. The paper was published in 2007 in the 2007 IEEE International Electron Devices Meeting, pp. 247-250.

17. Attached as Exhibit 1021 is a true and correct copy of a technical paper titled “Key Differences for Process-Induced Uniaxial v. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs” by S. Thompson et al. The paper was published in 2004 in the Technical Digest of the 2004 IEEE International

Electron Devices Meeting, pages 221-224.

18. Attached as Exhibit 1022 is a true and correct copy of a technical paper titled “45nm High-k + Metal Gate Strain-Enhanced Transistors” by C. Auth et al. The paper was published in 2008 in 2008 Symposium on VLSI Technology, pages 128-129.

19. Attached as Exhibit 1023 is a true and correct copy of a technical paper titled “High-Performance Metal/High-k n- and p-MOSFETs with Top-Cut Dual Stress Liners Using Gate-Last Damascene Process on (100) Substrate” by S. Mayuzumi et al. The paper was published in 2009 in IEEE Transactions on Electron Devices, Vol. 56, No. 4, pages 620-626.

20. Attached as Exhibit 1025 is a true and correct copy of excerpts from “Microchip Manufacturing” by S. Wolf, published in 2004. The excerpts are scans from a physical copy of this publication.

21. Attached as Exhibit 1026 is a true and correct copy of the *curriculum vitae* of Dr. Jack Lee, Ph.D.

22. Attached as Exhibit 1027 is a true and correct copy of a presentation titled MOSFET Scaling bearing a date of 2/19/2003 and is available at the following URL: [https://intra.ece.ucr.edu/~rlake/EE203/ee612\\_Taur4.pdf](https://intra.ece.ucr.edu/~rlake/EE203/ee612_Taur4.pdf).

23. Attached as Exhibit 1028 is a true and correct copy of a paper titled “Chemical Mechanical Polish: The Enabling Technology” by J. Steigerwald, from

the 2008 IEEE International Electron Devices Meeting. The paper is accessible at the following URL: <https://ieeexplore.ieee.org/document/4796607>.

24. Attached as Exhibit 1029 is a paper titled “Nanoscale CMOS” by H. Wong et al. The paper was published in IEEE, Vol. 87, No. 4 in 1999.

25. Attached as Exhibit 1030 is a true and correct copy of a paper titled “Chemical Mechanical Planarization for Microelectronics Applications” by P. Zantye et al. The paper was published in Materials Science and Engineering R. 45 in 2004.

26. Attached as Exhibit 1031 is a true and correct copy of excerpts of a book titled “Physics of Semiconductor Devices” by S. Sze and K. Ng. The book was published in 2007.

I declare under penalty of perjury that the foregoing is true and correct.

Date: November 14, 2025

By: /s/ Stephen M. Bradley

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