



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/620,209	04/19/2016	9318609	NAUP1656USA1	3329

27765 7590 03/30/2016
 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
 P.O. BOX 506
 MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
 (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yu-Hsiang Hung, Tainan City, TAIWAN;
 UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN;
 Ssu-I Fu, Kaohsiung City, TAIWAN;
 Chung-Fu Chang, Tainan City, TAIWAN;
 Cheng-Guo Chen, Changhua County, TAIWAN;
 Chien-Ting Lin, Hsinchu City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 02/04/2016

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Bertha Chang	(Depositor's name)
/Bertha Chang/	(Signature)
03/11/2016	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/620,209	02/12/2015	Yu-Hsiang Hung	NAUP1656USA1	3329

TITLE OF INVENTION:

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$960	\$0	\$0	\$960	05/04/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
Picardat, Kevin M	2822	257-347000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- Change of correspondence address (or Change of Correspondence Address Form PTO/SB/122) attached.
 "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- 1 Winston Hsu
 2 Scott Margo
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:

- Issue Fee
 Publication Fee (No small entity discount permitted)
 Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- A check is enclosed.
 Payment by credit card. Form PTO-2038 is attached.
 The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/

Date 03/10/2016

Typed or printed name Winston Hsu

Registration No. 41526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	14620209
Filing Date:	12-Feb-2015
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Filer:	Winston Hsu/Bertha Chang
Attorney Docket Number:	NAUP1656USA1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	25154484
Application Number:	14620209
International Application Number:	
Confirmation Number:	3329
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Bertha Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA1
Receipt Date:	11-MAR-2016
Filing Date:	12-FEB-2015
Time Stamp:	03:48:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$960
RAM confirmation Number	6740
Deposit Account	503105
Authorized User	HSU, WINSTON

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)
 Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)
 Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP1656USA1_AN_1_NP072.pdf	335142 8763f9f731e9197e92b368911cdb564cbe37b6fd	no	1

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30499 2c911f024ca1963a4c2c16e948af513f9492f166	no	2
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Warnings:

Information:

Total Files Size (in bytes):			365641		
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 02/04/2016
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Table with 2 columns: EXAMINER (PICARDAT, KEVIN M), ART UNIT (2822), PAPER NUMBER

DATE MAILED: 02/04/2016

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

14/620,209 02/12/2015 Yu-Hsiang Hung NAUPI656USA1 3329
TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

Table with 7 columns: APPLN. TYPE, ENTITY STATUS, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.
If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.
If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".
For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 02/04/2016
 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
 P.O. BOX 506
 MERRIFIELD, VA 22116

Certificate of Mailing or Transmission
 I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/620,209	02/12/2015	Yu-Hsiang Hung	NAUPI656USA1	3329

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	05/04/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
PICARDAT, KEVIN M	2822	257-347000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____</p> <p>(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____</p> <p>3 _____</p>
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : Individual Corporation or other private group entity Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
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5. **Change in Entity Status** (from status indicated above)

Applicant certifying micro entity status. See 37 CFR 1.29

Applicant asserting small entity status. See 37 CFR 1.27

Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Values: 14/620,209, 02/12/2015, Yu-Hsiang Hung, NAUP1656USA1, 3329

27765 7590 02/04/2016
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

PICARDAT, KEVIN M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 02/04/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/620,209	Applicant(s) HUNG ET AL.	
	Examiner KEVIN M. PICARDAT	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to amendment filed on 28 December 2015.
 A declaration(s)/affidavit(s) under 37 CFR 1.130(b) was/were filed on _____.
2. An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. The allowed claim(s) is/are 1-10. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/oph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) All b) Some *c) None of the:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Examiner's Amendment/Comment |
| 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. <input type="checkbox"/> Other _____. |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

The following is an examiner's statement of reasons for allowance: Examiner agrees with applicant's arguments, with regard to the amended claim, filed on 28 December 2015.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

The drawings were received on 28 December 2015. These drawings are acceptable.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. PICARDAT whose telephone number is (571)272-1841. The examiner can normally be reached on Monday-Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

Search Notes 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 21/8234, 845, 823821; 27/1211; 29/7851, 0653, 161, 66795, 6681, 7848, 7855	10-01-15	KMP
Updated above, see search history	1-27-16	KMP


CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	347, 351, 369, 327, 344	10-01-15	KMP
Updated	above		

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: listed subs	10-01-15	KMP
EAST: inventor name search	10-01-15	KMP
Reviewed parent app.	10-01-15	KMP
See search history	10-01-15	KMP
Updated above, see search history	1-27-16	KMP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
See search	history	1-27-16	KMP


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Issue Classification 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

CPC						
Symbol					Type	Version
H01L		29		7851	F	2013-01-01
H01L		29		7848	I	2013-01-01
H01L		29		6681	I	2013-01-01
H01L		29		7855	I	2013-01-01
H01L		21		8234	I	2013-01-01
H01L		21		845	I	2013-01-01
H01L		27		1211	I	2013-01-01
H01L		29		0653	I	2013-01-01
H01L		29		161	I	2013-01-01
H01L		29		66795	I	2013-01-01

CPC Combination Sets					
Symbol		Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	10	
/KEVIN M PICARDAT/ Primary Examiner.Art Unit 2822	01/27/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

Issue Classification 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant																<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original						
	1																				
	2																				
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	9																				
	10																				

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 10	
/KEVIN M PICARDAT/ Primary Examiner.Art Unit 2822 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 9



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BIB DATA SHEET

CONFIRMATION NO. 3329

SERIAL NUMBER 14/620,209	FILING or 371(c) DATE 02/12/2015 RULE	CLASS 438	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. NAUP1656USA1	
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN; INVENTORS Yu-Hsiang Hung, Tainan City, TAIWAN; Ssu-I Fu, Kaohsiung City, TAIWAN; Chung-Fu Chang, Tainan City, TAIWAN; Cheng-Guo Chen, Changhua County, TAIWAN; Chien-Ting Lin, Hsinchu City, TAIWAN; ** CONTINUING DATA ***** This application is a DIV of 13/913,511 06/09/2013 PAT 8993384 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/24/2015					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged /KEVIN M PICARDAT/ Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 1
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES					
TITLE SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE					
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	40	hung-yu-hsiang	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:05
L2	57	fu-ssu-i	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:05
L3	37	chang-chung-fu	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:06
L4	33	chen-cheng-guo	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:06
L5	189	lin-chien-ting	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:06
L6	243	1 2 3 4 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:06
L7	491628	fin or finfet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:07
L8	83	6 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:07
L9	103349	epitaxial near layer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:08
L10	35	8 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:08
L11	3879	7 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:08
L12	80541	isolation near (structure or layer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:08
L13	1005	11 and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:09
L14	705941	sidewall	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:09
L15	773	13 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:09
L16	66190	height near difference	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:09
L17	39	15 and 16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:09
L18	289	h01I27/1211	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L19	24498	h01I21/8234	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L20	228	h01I21/845	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L21	250	h01I21/823821	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L22	243	h01I29/7851	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10


L23	476	h01I29/0653	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L24	1385	h01I29/161	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L25	1218	h01I29/66795	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:10
L26	193	h01I29/6681	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:11
L27	571	h01I29/7848	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:11
L28	76	h01I29/7855	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:11
L29	28070	18 19 20 21 22 23 24 25 26 27 28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:11
L30	784	29 and 7 and 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:12
L31	245	30 and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:12
L32	201	31 and 14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:12
L33	7	32 and 16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2016/01/27 13:12

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L34	17111	(epitaxial near layer).clm.	US-PGPUB; USPAT	OR	ON	2016/01/27 13:14
L35	60795	(fin or finfet).clm.	US-PGPUB; USPAT	OR	ON	2016/01/27 13:14
L36	15334	(isolation near (structure or layer)).clm.	US-PGPUB; USPAT	OR	ON	2016/01/27 13:14
L37	52	(isolation near2 under near2 gate).clm.	US-PGPUB; USPAT	OR	ON	2016/01/27 13:16
L38	426	34 and 35	US-PGPUB; USPAT	OR	ON	2016/01/27 13:17
L39	59	38 and 36	US-PGPUB; USPAT	OR	ON	2016/01/27 13:17
L40	2	39 and 37	US-PGPUB; USPAT	OR	ON	2016/01/27 13:17

1/ 27/ 2016 1:17:55 PM

C:\Users\kpicardat\Documents\EAST\Workspaces\kevin.wsp

<i>Index of Claims</i> 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant				<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
CLAIM		DATE							
Final	Original	10/01/2015	01/27/2016						
	1	✓	=						
	2	✓	=						
	3	✓	=						
	4	✓	=						
	5	✓	=						
	6	✓	=						
	7	✓	=						
	8	✓	=						
	9	✓	=						
	10	✓	=						

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

Appl. No. : 14/620,209 Confirmation No. 3329
First Named Inventor : Yu-Hsiang Hung
Filed : February 12, 2015
TC/A.U. : 2822
Examiner : Picardat, Kevin M
Docket No. : NAUP1656USA1
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of October 08, 2015, please amend the above-identified application as follows:

5 **Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

Amendments to the Drawings begin on page 4 of this paper.

Remarks/Arguments begin on page 5 of this paper.

REPLACEMENT SHEET

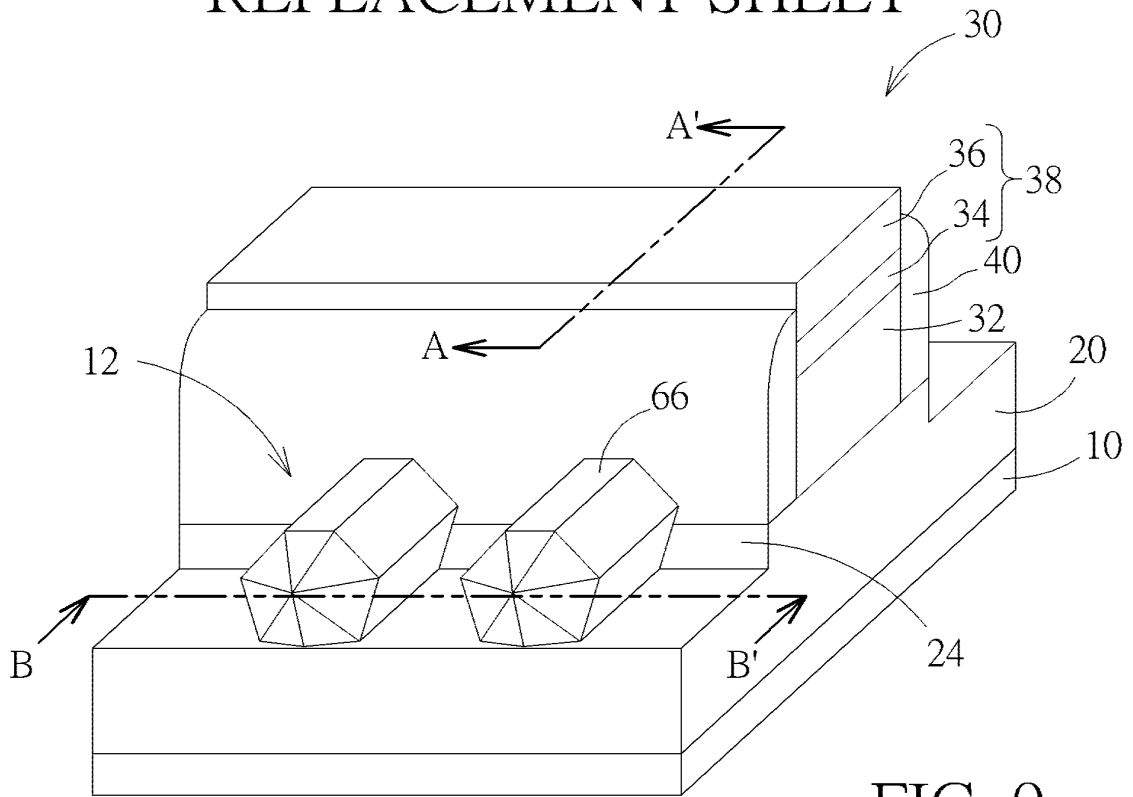


FIG. 9

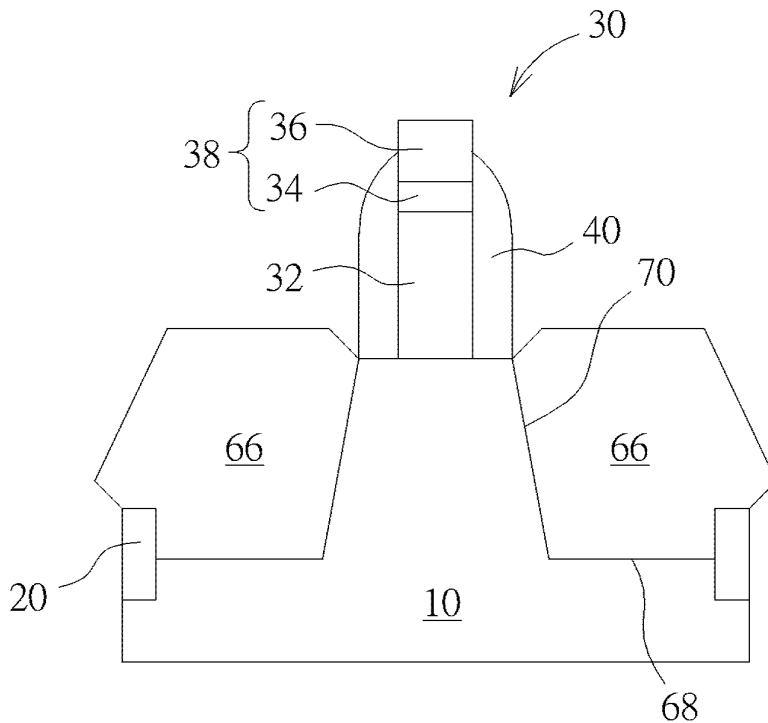


FIG. 10

REPLACEMENT SHEET

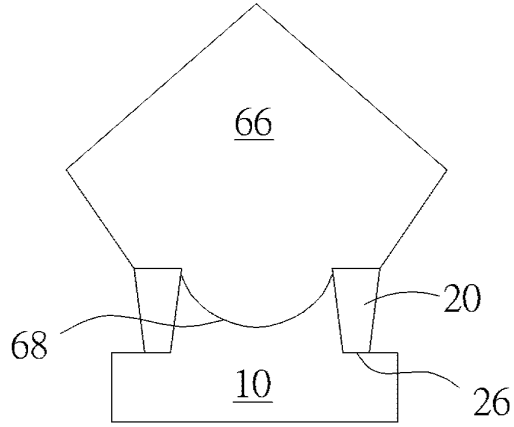


FIG. 11

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5 **Listing of Claims:**

Claim 1 (currently amended): A semiconductor device, comprising:

a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;

10 an isolation structure, disposed on the surface of the substrate and surrounding the fin structure;

a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure, wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface,
15 and the first top surface is higher than the second top surface; and

an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

20 Claim 2 (original): The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

25 Claim 3 (original): The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

Claim 4 (original): The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

30 Claim 5 (original): The semiconductor device according to claim 1, further comprising

a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

5 Claim 6 (original): The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

10 Claim 7 (original): The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.

15 Claim 8 (original): The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.

Claim 9 (original): The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.

20 Claim 10 (original): The semiconductor device according to claim 1, further comprising:

another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and
25 a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

Electronic Acknowledgement Receipt

EFS ID:	24451768
Application Number:	14620209
International Application Number:	
Confirmation Number:	3329
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Jessie Su
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA1
Receipt Date:	28-DEC-2015
Filing Date:	12-FEB-2015
Time Stamp:	01:03:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2440802.PDF	693546 <small>0288350bdo7864555a25c05fce191802f6f4597a</small>	no	6

Warnings:

Information:

2	Amendment/Req. Reconsideration-After Non-Final Reject	2440801.PDF	82739 <small>9a5a0ee4740c9c2b7e71967c9a4f83d297a b7fcd</small>	no	1
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2440800.PDF	68838 <small>e377ed4685831295b931b219016952c060 42d108</small>	no	2
Warnings:					
Information:					
4	Claims	2440799.PDF	86688 <small>92866dad3bb8ce54043a06f78138a5239b8 ca943</small>	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			931811		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Amendments to the Drawings:

Attachment:	Replacement Sheet	2 page(s)
	Annotated Sheet Showing Changes	0 page(s)
	New Sheet	0 page(s)

5

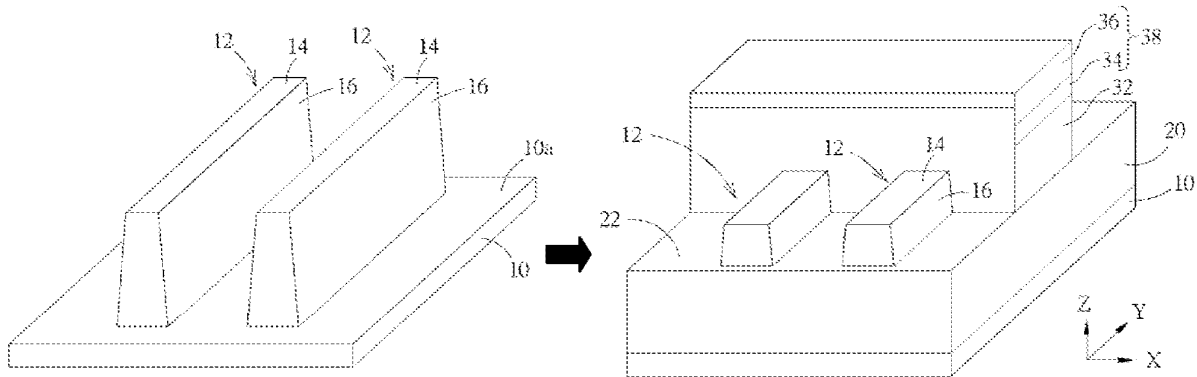
REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

▲ Amendments to the claims

In this response, the independent method Claim 1 is amended. The amendment of Claim 1 can be supported by the originally-filed specification, for example paragraphs [0026]. The newly-added features in the amendment may also be disambiguously derived
10 from the originally-filed FIGs. 1-2. No new matter is introduced. Reconsideration of the instant application is politely requested.

[0026] ... The **isolation structure 20** may have the configuration shown in FIG. 2. At this stage, a lower portion of each fin structure 12 is embedded in the isolation structure 20 and each fin structure 12 exposed out of the isolation
15 structure 20 may have a first height H1.



▲ Amendments to the drawings

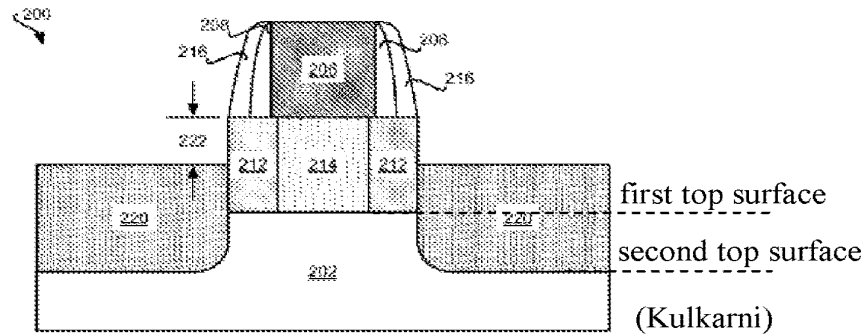
In this response, the FIG.10 and the FIG.11 are amended to shown correct and reasonable structural changes during the process. The amendment of Claim 1 can be
20 supported by logical deduction from FIGs. 7-8 in the originally-filed specification and would not introduce any new mater or alter/expand any current limitations of claims.

▲ Rejections of claims 1-10 and 12-20 under 35 U.S.C. §103

Claims 1-10 are rejected under 35 U.S.C. §102 as being anticipated by *Kulkarni*

et al. US 2012/0193713.

In re Claim 1: *Kulkarni* et al. discloses a finFET structure including a fin structure (212/214), protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces; an **isolation structure (202)**,
5 surrounding the fin structure; a gate structure (206), overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure (although the figures don't show the gate on the side surfaces that is because they only show a cross section and gates in finFET structure are well known to cross perpendicular to the fin and extend down the sides of the fin structure),
10 wherein the isolation structure (202) under the gate structure (206) has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is **higher** than the second top surface; and an epitaxial layer (220), disposed at one side of the gate structure and in direct contact with the fin structure, also disclosed is the height difference of 10-15 nanometers, which is 100-150 angstroms (see figs.2D-F and related text).
15



RESPONSE

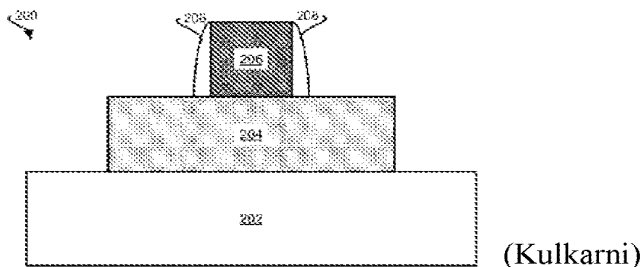
The Applicant has acknowledged that the current limitations recited in method independent Claim 1 may not sufficiently distinguish the claimed structure from the one
20 disclosed in the cited references, i.e. *Kulkarni*. For this reason, the instant Claim 1 is appropriately amended as follows:

“A semiconductor device, comprising: a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces; an isolation structure, disposed on the surface of the substrate and

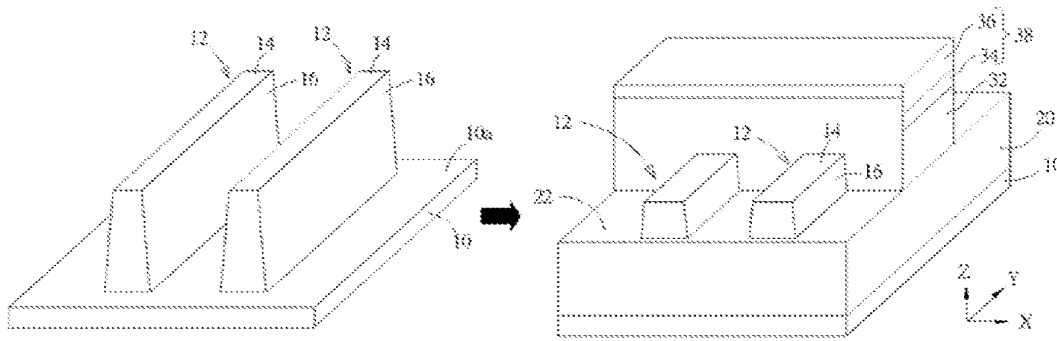
5 surrounding the fin structure; a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure, wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.”

The following argument is made accordingly on the basis of above-identified amended Claim 1:

10 (1) There is a fundamental and essential difference between the feature of *Kulkarni* and the present invention. As shown in the figure below, in *Kulkarni*, the **buried oxide 202** referred by the Examiner as the **isolation structure** is actually an oxide region buried in the substrate, likes the isolator portion in SOI (silicon-on-isolator) substrate. The fin structure 204 is formed from the silicon portion of SOI on the isolator, thus it is described in *Kulkarni*'s publication that the fin 204 is **on top of** the buried oxide 202 instead of protrudes from the buried oxide 202, Para.[0019]. In *Kulkarni*'s case, the fin 204 is **not** surrounded by the buried oxide 202.



20 In comparison thereto, in the present invention as the figure shown below, the fin structure is **not** formed **on top of** isolation structure (20). Instead, it is formed from the surface of substrate 10 and is surrounded by the isolation structure (20). This is quite difference from the configuration of *Kulkarni*, which the fin structure is formed on top of the isolator and is not surrounded thereby.



(present invention)

Additionally, since the isolation structure (20) of the present invention is not a buried oxide, it is formed on the substrate 10, while the isolator 202 in *Kulkarni* is a buried oxide, which is bound to be formed in the substrate (or be a portion of the substrate itself). Thus *Kulkarni* doesn't teach the feature of "an isolation structure disposed on the surface of the substrate and surrounding the fin structure" in amended Claim 1.

Conclusively, in accordance with three main differences between Ref. *Hempell/Ando* and the present invention: (1) the buried oxide in *Kulkarni* is not disposed on the surface of the substrate and doesn't surround the fin structure, *Kulkarni* don't disclose or obviously anticipate the technical features of limitations as required by amended Claim 1. Reconsideration and allowance of amended Claim 1 is respectfully requested.

As claims 2-10 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Reconsideration of claims 2-10 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/620,209	Filing Date 02/12/2015	<input type="checkbox"/> To be Mailed
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ENTITY: LARGE SMALL MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
<input type="checkbox"/> BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A	
<input type="checkbox"/> SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A	
<input type="checkbox"/> EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A	
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	minus 3 =	*	X \$ =	
<input type="checkbox"/> APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	12/28/2015	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	* 10	Minus	** 20	= 0	X \$80 = 0
	Independent <small>(37 CFR 1.16(h))</small>	* 1	Minus	***3	= 0	X \$420 = 0
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>					
					TOTAL ADD'L FEE	0

	(Column 1)	(Column 2)	(Column 3)	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR			
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	X \$ =
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	X \$ =
	<input type="checkbox"/> Application Size Fee <small>(37 CFR 1.16(s))</small>					
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>					
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
 /CAROLYN THOMAS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
14/620,209 02/12/2015 Yu-Hsiang Hung NAUP1656USA1 3329

27765 7590 10/08/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

PICARDAT, KEVIN M

ART UNIT PAPER NUMBER

2822

NOTIFICATION DATE DELIVERY MODE

10/08/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims 1-10 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Kulkarni et al. US 2012/0193713.

Kulkarni et al. discloses a finFET structure including a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces; an isolation structure, surrounding the fin structure; a gate structure (206), overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure (although the figures don't

Art Unit: 2822

show the gate on the side surfaces that is because they only show a cross section and gates in finFET structures are well known to cross perpendicular to the fin and extend down the sides of the fin structure), wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface (218), and the first top surface is higher than the second top surface; and an epitaxial layer(220), disposed at one side of the gate structure and in direct contact with the fin structure, also disclosed is the height difference of 10-15 nanometers, which is 100-150 angstroms (see figs. 2D-F and related text).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. PICARDAT whose telephone number is (571)272-1841. The examiner can normally be reached on Monday-Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M. PICARDAT/
Primary Examiner, Art Unit 2822

Search Notes 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 21/8234, 845, 823821; 27/1211; 29/7851, 0653, 161, 66795, 6681, 7848, 7855	10-01-15	KMP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	347, 351, 369, 327, 344	10-01-15	KMP

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: listed subs	10-01-15	KMP
EAST: inventor name search	10-01-15	KMP
Reviewed parent app.	10-01-15	KMP
See search history	10-01-15	KMP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 3329

SERIAL NUMBER 14/620,209	FILING or 371(c) DATE 02/12/2015 RULE	CLASS 438	GROUP ART UNIT 2822	ATTORNEY DOCKET NO. NAUP1656USA1	
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN; INVENTORS Yu-Hsiang Hung, Tainan City, TAIWAN; Ssu-I Fu, Kaohsiung City, TAIWAN; Chung-Fu Chang, Tainan City, TAIWAN; Cheng-Guo Chen, Changhua County, TAIWAN; Chien-Ting Lin, Hsinchu City, TAIWAN; ** CONTINUING DATA ***** This application is a DIV of 13/913,511 06/09/2013 PAT 8993384 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/24/2015					
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No 35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No Verified and Acknowledged /KEVIN M PICARDAT/ Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 6	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 1
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES					
TITLE SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE					
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8765533	B2	2014-07-01	Hsieh	
	2	6043138		2000-03-28	Ibok; Effiong E.	all
	3	6492216		2002-12-10	Yeo; Yee-Chia	all
	4	6921963		2005-07-26	Krivokapic; Zoran	all
	5	7087477		2006-08-08	Fried; David M.	all
	6	7091551		2006-08-15	Anderson; Brent A.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7250658		2007-07-31	Doris; Bruce B.	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

9	7309626		2007-12-18	leong; Mei-Kei	all
10	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
11	7470570		2008-12-30	Beintner; Jochen	all
12	7531437		2009-05-12	Brask; Justin K.	all
13	7569857		2009-08-04	Simon, legal representative; David	all
14	7525160		2009-04-28	Kavalleros	

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20040195624		2004-10-07	Liu, Chee-Wee;	all
	2	20050051825		2005-03-10	Fujiwara, Makoto;	all
	3	20060099830		2006-05-11	Walther; Steven R.;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

4	20060286729		2006-12-21	Kavalieros; Jack;	all
5	20070108528		2007-05-17	Anderson; Brent A.;	all
6	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
7	20080157208		2008-07-03	Fischer; Kevin J.;	all
8	20090124097		2009-05-14	Cheng; Kangguo;	all
9	20090242964		2009-10-01	Akil; Nader;	all
10	20090269916		2009-10-29	KANG; Inkuk;	all
11	20100048027		2010-02-25	Cheng; Kangguo;	all
12	20100072553		2010-03-25	XU; Jeff J.;	all
13	20100144121		2010-06-10	Chang; Cheng-Hung;	all
14	20100167506		2010-07-01	LIN; Simon Su-Hong;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

15	20120193713		2012-08-02	Kulkarni	
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1						

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.
	1	

EXAMINER SIGNATURE

Examiner Signature	/KEVIN PICARDAT/	Date Considered	10/01/2015
--------------------	------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2015-02-12
Name/Print	Winston Hsu	Registration Number	41,526

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("8993384").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/10/01 09:28
L2	29	("20040195624" "20050051825" "20060099830" "20060286729" "20070108528" "20070158756" "20080157208" "20090124097" "20090242964" "20090269916" "20100048027" "20100072553" "20100144121" "20100167506" "20120193713" "6043138" "6492216" "6921963" "7087477" "7091551" "7247887" "7250658" "7309626" "7352034" "7470570" "7525160" "7531437" "7569857" "8765533").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/10/01 09:29
L3	29	hung-yu-hsiang	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:05
L4	48	fu-ssu-i	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:05
L5	26	chang-chung-fu	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:05
L6	30	chen-cheng-guo	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:05
L7	174	lin-chien-ting	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:05
L8	219	3 4 5 6 7	US-PGPUB; USPAT;	OR	ON	2015/10/01 10:06


			USOCR; EPO; JPO; DERWENT			
L9	479742	fin or finfet	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:06
L10	68	8 and 9	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:06
L11	101019	epitaxial near layer	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:06
L12	29	10 and 11	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:06
L13	3506	9 and 11	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:07
L14	77723	isolation near (structure or layer)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:07
L15	908	13 and 14	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:08
L16	690910	sidewall	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:08
L17	693	15 and 16	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:08
L18	64202	height near difference	US- PGPUB; USPAT;	OR	ON	2015/10/01 10:10

			USOCR; EPO; JPO; DERWENT			
L19	35	17 and 18	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:10
L20	222	h01I27/1211	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L21	23592	h01I21/8234	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L22	164	h01I21/845	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L23	151	h01I21/823821	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L24	156	h01I29/7851	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L25	326	h01I29/0653	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:35
L26	1215	h01I29/161	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L27	897	h01I29/66795	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L28	128	h01I29/6681	US- PGPUB; USPAT;	OR	ON	2015/10/01 10:36

			USOCR; EPO; JPO; DERWENT			
L29	415	h01129/7848	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L30	60	h01129/7855	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L31	26448	20 21 22 23 24 25 26 27 28 29 30	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L32	2683	9 and 31	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L33	571	32 and 11	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:36
L34	183	33 and 14	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:37
L35	153	34 and 16	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:37
L36	148	35 not 19	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2015/10/01 10:38

10/ 1/ 2015 10:38:42 AM

C:\Users\kpicardat\Documents\EAST\Workspaces\kevin.wsp

<i>Index of Claims</i> 	Application/Control No. 14620209	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner KEVIN M PICARDAT	Art Unit 2822

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claims renumbered in the same order as presented by applicant
 CPA
 T.D.
 R.1.47

CLAIM		DATE							
Final	Original	10/01/2015							
	1	✓							
	2	✓							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
	8	✓							
	9	✓							
	10	✓							



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Table with 4 columns: APPLICATION NUMBER (14/620,209), FILING OR 371(C) DATE (02/12/2015), FIRST NAMED APPLICANT (Yu-Hsiang Hung), ATTY. DOCKET NO./TITLE (NAUP1656USA1)

CONFIRMATION NO. 3329

PUBLICATION NOTICE

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116



Title: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

Publication No. US-2015-0155386-A1
Publication Date: 06/04/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
14/620,209

APPLICATION AS FILED - PART I

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(j))	10	minus 20 = *
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

SMALL ENTITY

RATE(\$)	FEE(\$)
N/A	
N/A	
N/A	
TOTAL	

OR OTHER THAN SMALL ENTITY

RATE(\$)	FEE(\$)
N/A	280
N/A	600
N/A	720
x 80 =	0.00
x 420 =	0.00
	0.00
	0.00
TOTAL	1600

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(j))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

OR OTHER THAN SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(j))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

OR OTHER THAN SMALL ENTITY

RATE(\$)	ADDITIONAL FEE(\$)
x =	
x =	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.



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Table with 7 columns: APPLICATION NUMBER, FILING or 371(c) DATE, GRP ART UNIT, FIL FEE REC'D, ATTY. DOCKET NO, TOT CLAIMS, IND CLAIMS. Row 1: 14/620,209, 02/12/2015, 2812, 1600, NAUP1656USA1, 10, 1

CONFIRMATION NO. 3329

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



Date Mailed: 02/26/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections

Inventor(s)

Yu-Hsiang Hung, Tainan City, TAIWAN;
Ssu-I Fu, Kaohsiung City, TAIWAN;
Chung-Fu Chang, Tainan City, TAIWAN;
Cheng-Guo Chen, Changhua County, TAIWAN;
Chien-Ting Lin, Hsinchu City, TAIWAN;

Applicant(s)

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a DIV of 13/913,511 06/09/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper Authorization to Permit Access to Application by Participating Offices (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 02/24/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US 14/620,209

Projected Publication Date: 06/04/2015

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

**Title of Invention:
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF**

As the below named inventor, I hereby declare that:
This declaration is directed to:

- The attached application, or
- United States application number _____ filed on _____, or
- PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.
IN WITNESS WHEREOF, I have hereunto set hand and seal this MAY 02 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Yu-Hsiang Hung**

Date: 2013.05.02

Signature: Yu-Hsiang Hung

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

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Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ssu-I Fu**

Date: **JUN 03 2013**

Signature: Ssu-I Fu

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
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Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chung-Fu Chang**

Date: **JUN 03 2013**

Signature:

Chung-fu chang

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 6 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:

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IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Cheng-Guo Chen**

Date: **JUN 03 2013**

Signature: Cheng-Guo Chen

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

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- The attached application, or
- United States application number _____ filed on _____, or
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In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

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I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

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Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chien-Ting Lin**

Date: **JUN 03 2013**

Signature: Chien-Ting Lin

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

Practitioners associated with Customer Number: 27765

OR

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

The address associated with Customer Number: 27765

OR

<input type="checkbox"/>	Firm or Individual Name			
<input type="checkbox"/>	Address			
<input type="checkbox"/>	City			
<input type="checkbox"/>	Country			
<input type="checkbox"/>	Telephone		Email	

Assignee Name and Address:
UNITED MICROELECTRONICS CORP.
 No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
 The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	<i>Chia-Tsung Hung</i>	Date	SEP 26 2012
Name	Chia-Tsung Hung	Telephone	+886-3-5782258
Title	CHAIRMAN		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: UNITED MICROELECTRONICS CORP.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

UNITED MICROELECTRONICS CORP., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

- 1. The assignee of the entire right, title, and interest.
- 2. An assignee of less than the entire right, title, and interest (check applicable box):
 - The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
 - There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

- 3. The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

- 4. The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:
 - 1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
 - 2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet(s).

As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Winston Hsu/

02/12/2015

Signature

Date

Winston Hsu

41,526

Printed or Typed Name

Title or Registration Number

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

- The attached application, or
 United States application number _____ filed on _____, or
 PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WITNESS WHEREOF, I have hereunto set hand and seal this MAY 02 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: Yu-Hsiang Hung

Date: 2013.05.02

Signature: Yu-Hsiang Hung

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

**Title of Invention:
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As the below named inventor, I hereby declare that:
This declaration is directed to:

- The attached application, or
- United States application number _____ filed on _____, or
- PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ssu-I Fu**

Date: **JUN 03 2013**

Signature: Ssu-I Fu

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

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F#NPO-P0002E-US1201
DSC0-102U003310

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

**Title of Invention:
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF**

As the below named inventor, I hereby declare that:
This declaration is directed to:

- The attached application, or
- United States application number _____ filed on _____, or
- PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chung-Fu Chang**

Date: **JUN 03 2013**

Signature: Chung-fu Chang

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

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F#NPO-P0002E-US1201
DSC0-102U003310

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

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SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF**

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- United States application number _____ filed on _____, or
- PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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In consideration of the payment by **UNITED MICROELECTRONICS** having a postal address of **CORP.**

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

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IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1656USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Cheng-Guo Chen**

Date: **JUN 03 2013**

Signature: Cheng-Guo Chen

NPO#NAU-P1656-USA:0
CUST#UMCD-2012-0534

Page 8 of 10

F#NPO-P0002E-US1201
DSC0-102U003310

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

**Title of Invention:
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF**

As the below named inventor, I hereby declare that:
This declaration is directed to:

- The attached application, or
- United States application number _____ filed on _____, or
- PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUN 03 2013 (Date of signing)

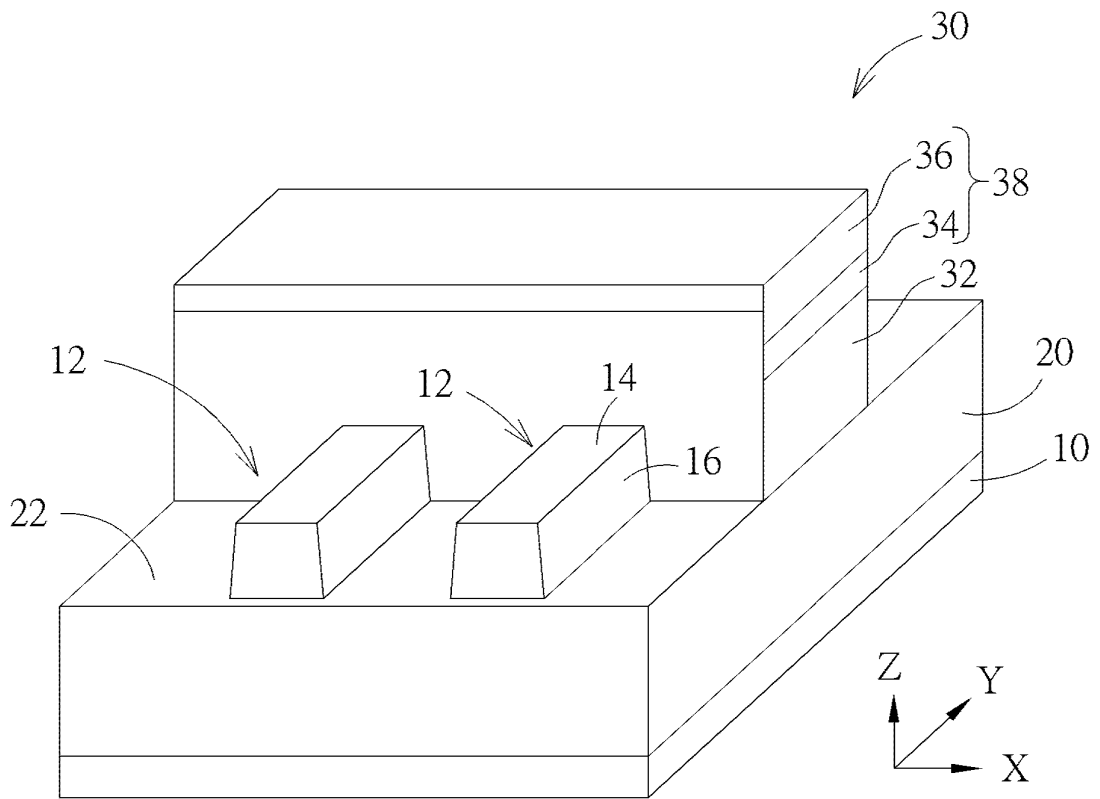
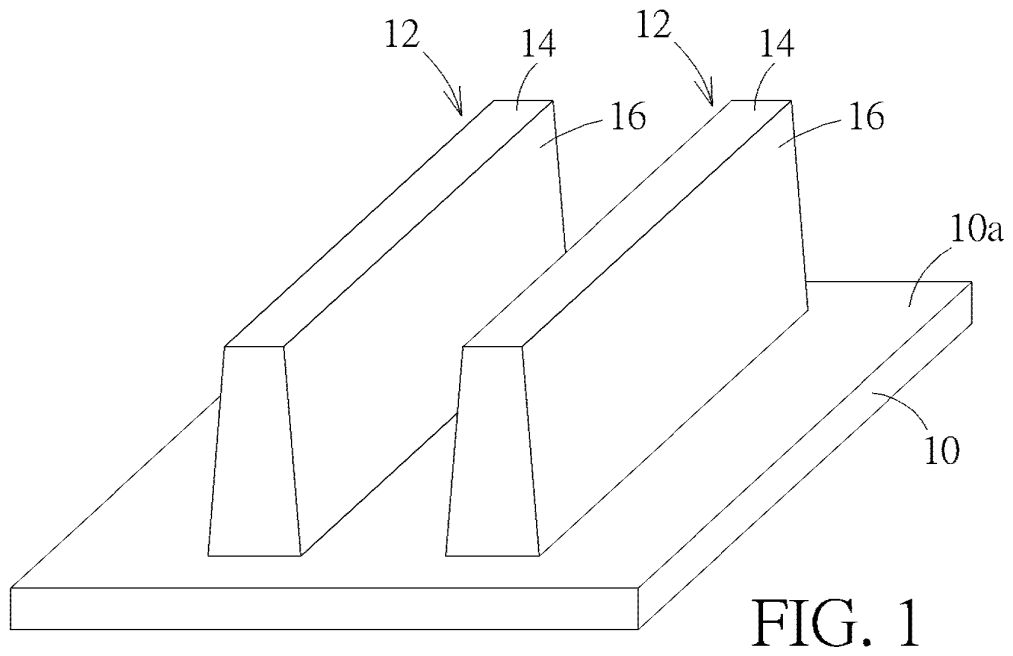
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chien-Ting Lin**

Date: **JUN 03 2013**

Signature: Chien-Ting Lin



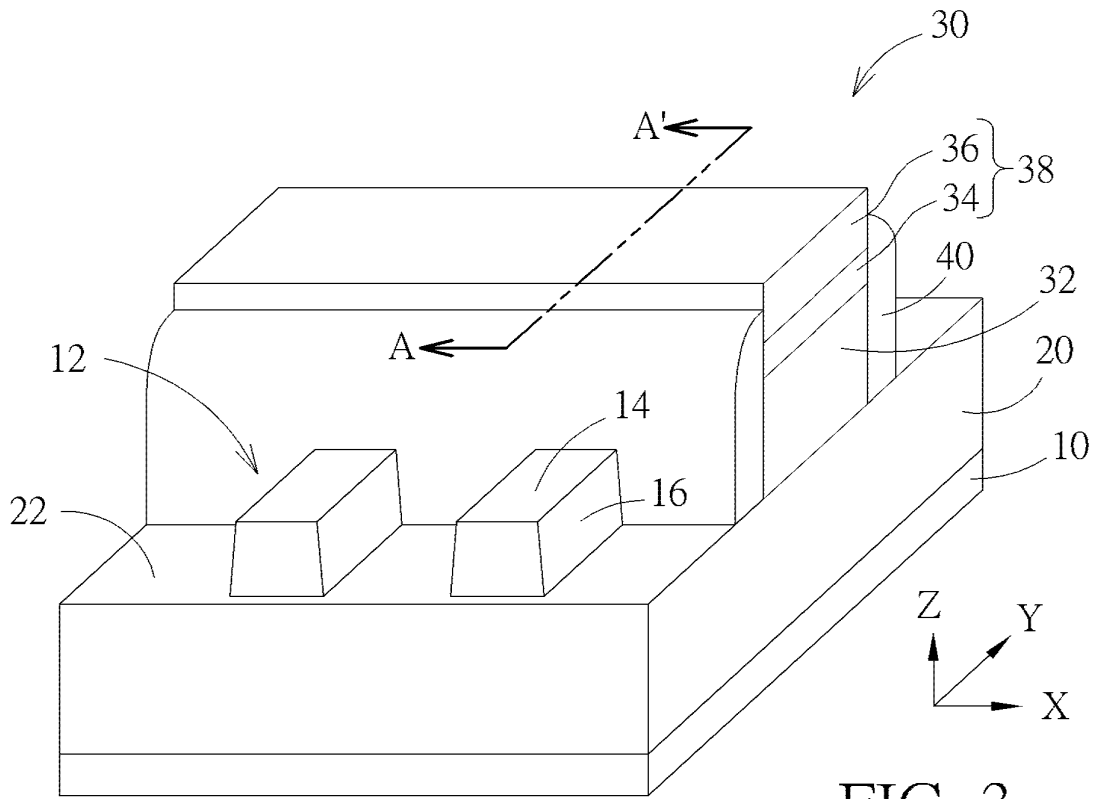


FIG. 3

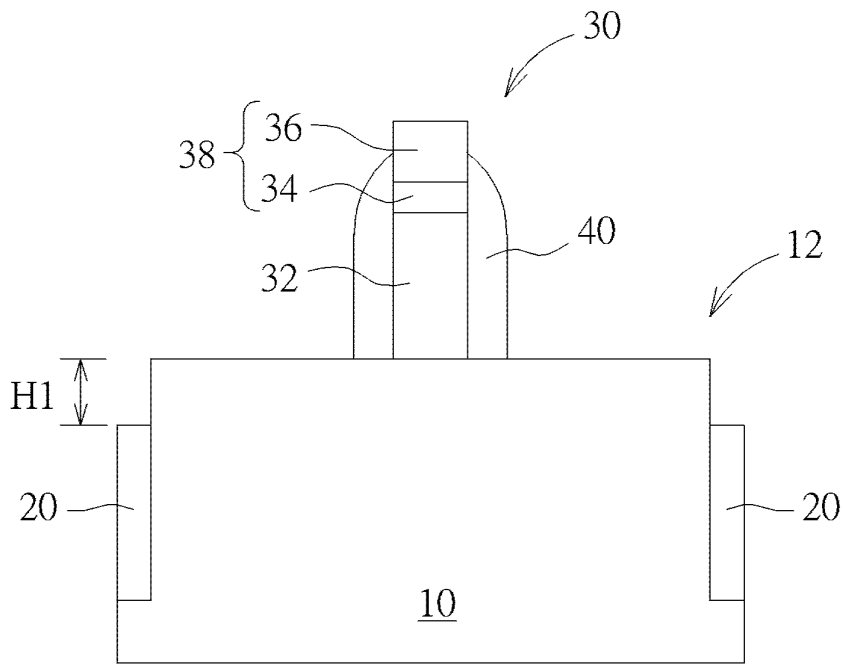


FIG. 4

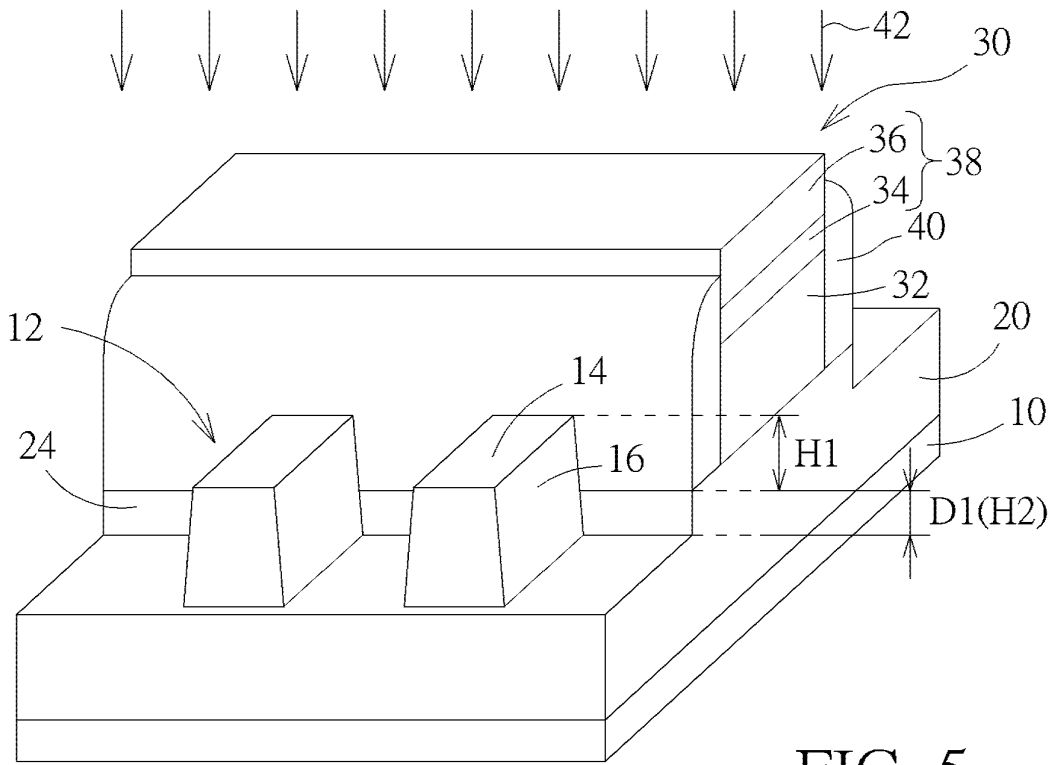


FIG. 5

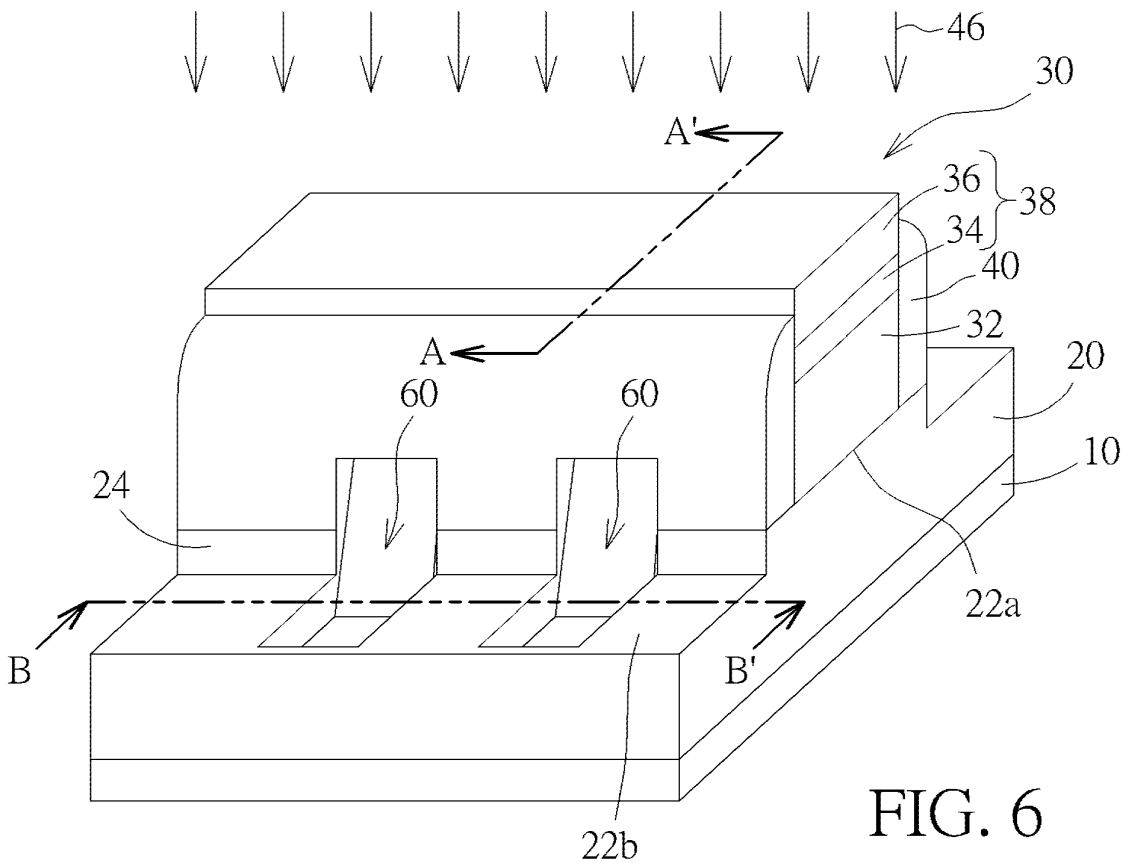


FIG. 6

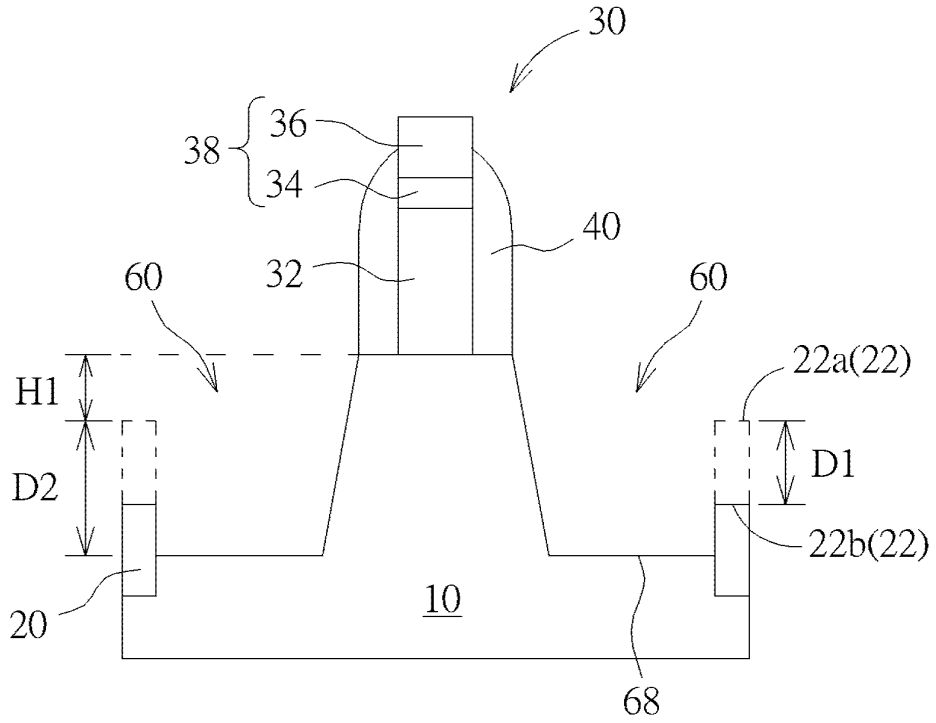


FIG. 7

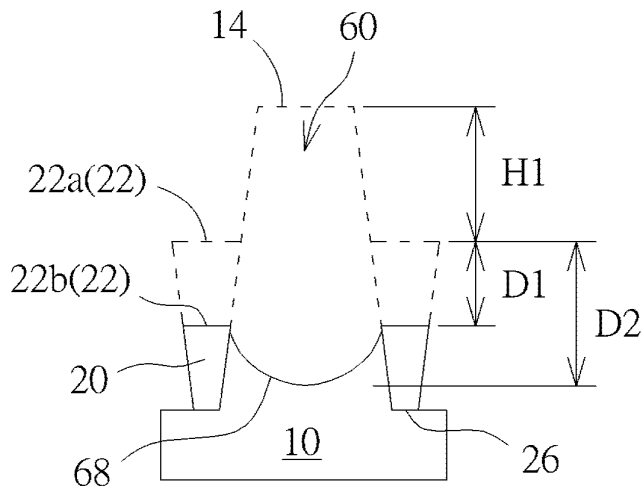


FIG. 8

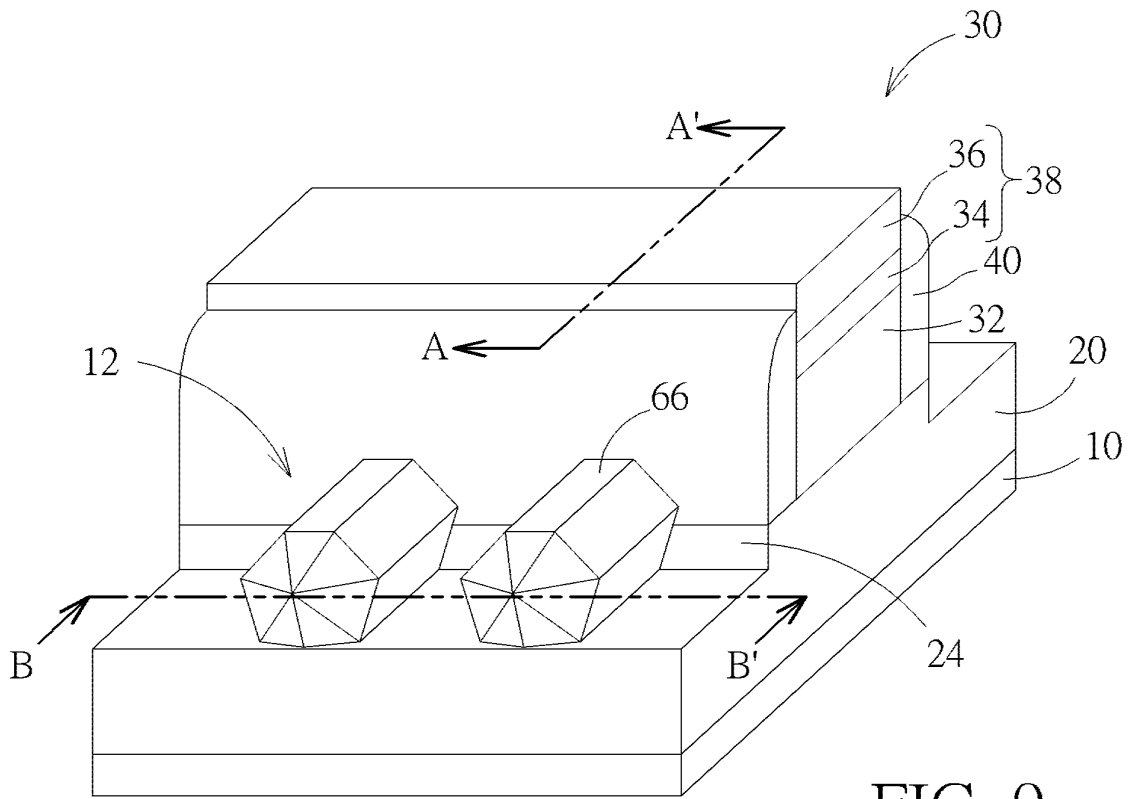


FIG. 9

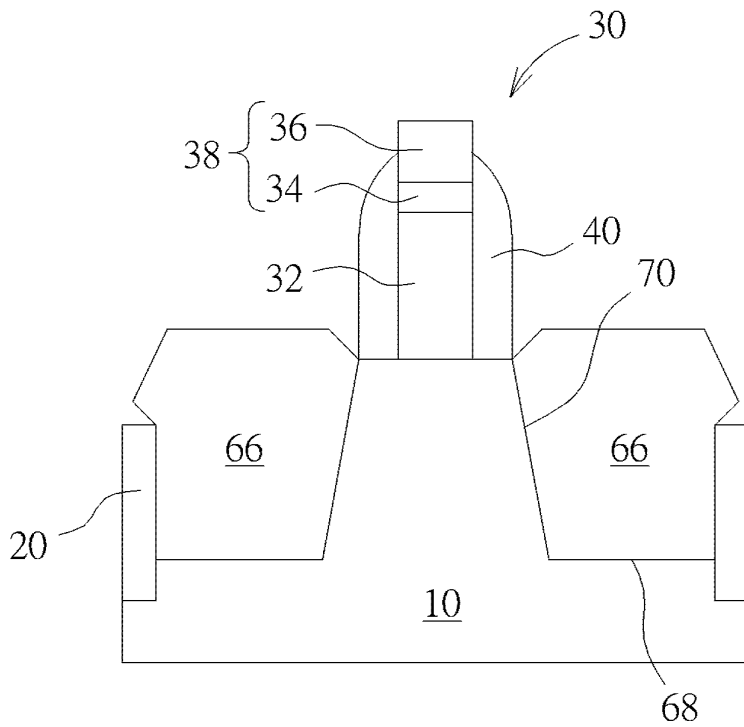


FIG. 10

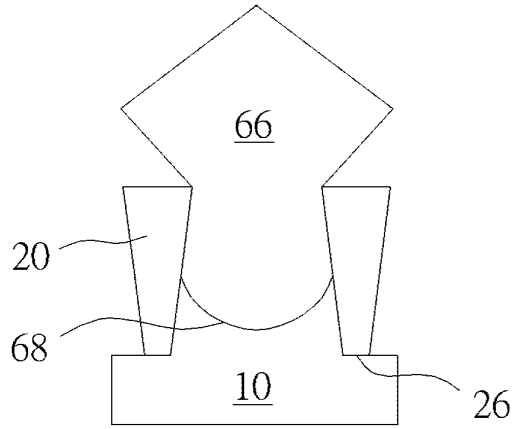


FIG. 11

Abstract of Disclosure

A semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface, and the isolation structure at two sides of the gate structure has a second top surface. The first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in direct contact with the fin structure.

Claims

What is claimed is:

1. A semiconductor device, comprising:
 - a fin structure, protruding from a surface of a substrate, wherein the fin structure comprises a top surface and two side surfaces;
 - an isolation structure, surrounding the fin structure;
 - a gate structure, overlaying the top surface and the two side surfaces of a portion of the fin structure and covering a portion of the isolation structure, wherein the isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, and the first top surface is higher than the second top surface; and
 - an epitaxial layer, disposed at one side of the gate structure and in direct contact with the fin structure.

2. The semiconductor device according to claim 1, wherein there is a height difference between the first top surface and second top surface, and the height difference ranges from 100 Angstroms to 250 Angstroms.

3. The semiconductor device according to claim 1, wherein the gate structure is a metal gate structure.

4. The semiconductor device according to claim 1, wherein the isolation structure under the gate structure comprises a sidewall and the epitaxial structure is in direct contact with the sidewall.

5. The semiconductor device according to claim 1, further comprising a recess formed at one end of the fin structure, wherein the epitaxial structure fills up the recess.

6. The semiconductor device according to claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the isolation structure.

7. The semiconductor device according to claim 6, wherein there is a height difference between the bottom surface of the epitaxial structure and the bottom surface of the isolation structure, and the height difference ranges from 100 Angstroms to 250 Angstroms.
8. The semiconductor device according to claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphide or phosphor-doped silicon carbide.
9. The semiconductor device according to claim 1, further comprising a spacer disposed on a sidewall of the gate structure.
10. The semiconductor device according to claim 1, further comprising:
another epitaxial structure, disposed at another side of the gate structure and in direct contact with the fin structure; and
a channel region, contiguous to the top surface and the side surfaces of the fin structure, and between the epitaxial structure and said another epitaxial structure.

Title

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE

Cross Reference To Related Applications

[0001] This application is a division of U.S. application Ser. No. 13/913,511, filed on Jun. 9, 2013, the disclosure of which is hereby incorporated herein by reference in its entirety.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates generally to the field of semiconductor devices, and more particularly to a semiconductor device with an epitaxial structure.

2. Description of the Prior Art

[0003] As semiconductor devices switching speeds continue to increase and operating voltage levels continue to decrease, the performances of metal-oxide-semiconductor field effect transistors (MOSFETs) and other types of transistors, such as bipolar junction transistors, need to be correspondingly improved. Currently, along with the development of the MOSFETs, one of the main goals in the industry is to increase the carrier mobility so as to further increase the operation speed of the MOSFETs.

[0004] In order to improve the device performances, crystal strain technology has been developed. Crystal strain technology is becoming more and more attractive as a means for getting better performances in the field of MOS transistor fabrication. Putting a strain on a semiconductor crystal alters the speed at which charges move through that crystal. Strains make the MOS transistors work better by enabling charge carriers, such as electrons or holes, to pass through the silicon lattice of the channel more easily. Currently, attempts have been made to use a strained silicon layer as a part of MOS transistors in which an epitaxial silicon germanium (SiGe) structure or an epitaxial silicon carbide (SiC) structure is formed. In this type

of MOS transistor, a biaxial tensile strain is induced in the epitaxy silicon layer due to the difference in lattice constants between SiGe or SiC and Si. As a result, the band structure is altered, and the carrier mobility is increased.

[0005] However, due to the continuous shrinkage in the size of the semiconductor devices, the aspect ratio of the epitaxial layer also gets higher, which often incur unwanted defects, such as void defects in the epitaxial layer. These defects inside the epitaxial layer reduce the stress required to be imposed onto the corresponding channel region. As a result, how to prevent the formation of the defects inside the epitaxial layer is an important issue.

Summary of the Invention

[0006] To this end, an object of the present invention is to provide a semiconductor device with an epitaxial layer so that stress imposed on the channel region can be increased.

[0007] According to a preferred embodiment of the invention, a semiconductor device is provided. The semiconductor device includes a fin structure, an isolation structure, a gate structure and an epitaxial structure. The fin structure protrudes from the surface of the substrate and includes a top surface and two sidewalls. The isolation structure surrounds the fin structure. The gate structure overlays the top surface and the two sidewalls of a portion of the fin structure, and covers a portion of the isolation structure. The isolation structure under the gate structure has a first top surface and the isolation structure at two sides of the gate structure has a second top surface, wherein the first top surface is higher than the second top surface. The epitaxial layer is disposed at one side of the gate structure and is in direct contact with the fin structure.

[0008] One feature of the present invention is to provide a semiconductor device with an epitaxial layer and a fabrication method thereof. Since the process for etching the isolation structure is

optionally carried out prior to and/or after the formation of the recess, the height of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial layer may be filled into the corresponding recess easily during the epitaxial growth process. Furthermore, since the epitaxial structure is not sealed during the epitaxial growth process, the void defects may be also avoided as a result.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010] FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention, wherein:

[0011] FIG. 1 is a schematic perspective diagram showing the semiconductor device at the beginning of the fabrication process;

[0012] FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a gate structure;

[0013] FIG. 3 is a schematic perspective diagram showing the semiconductor device after the formation of a spacer;

[0014] FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3;

[0015] FIG. 5 is a schematic perspective diagram showing the semiconductor device after etching the isolation structure;

[0016] FIG. 6 is a schematic perspective diagram showing the semiconductor device after etching fin structures;

[0017] FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6;

[0018] FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6;

[0019] FIG. 9 is a schematic perspective diagram showing the semiconductor device after the formation of an epitaxial layer;

[0020] FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9; and

[0021] FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9.

Detailed Description

[0022] In the following description, numerous specific details are given to provide a thorough understanding of the invention. It will, however, be apparent to one skilled in the art that the invention may be practiced without these specific details. Furthermore, some well-known system configurations and process steps are not disclosed in detail, as these should be well-known to those skilled in the art.

[0023] Likewise, the drawings showing embodiments of the apparatus are not to scale and some dimensions are exaggerated for clarity of presentation. Also, where multiple embodiments are disclosed and described as having some features in common, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0024] FIG. 1 to FIG. 11 are schematic diagrams showing a fabrication method of a semiconductor device according to a preferred embodiment of the present invention. Please refer to FIG.1. FIG. 1 is a schematic perspective view showing the semiconductor device of at the beginning of the fabrication process. As shown in FIG. 1, a substrate 10 is provided. The substrate 10 may be a semiconductor substrate such as a silicon substrate, a silicon containing substrate, a III-V semiconductor-on-silicon (such as GaAs-on-silicon) substrate, or a graphene-on-silicon substrate. Preferably, the substrate 10 is not a silicon-on-insulator (SOI) substrate. Still referring to FIG. 1, a plurality of fin structures 12 is disposed on the substrate 10. More precisely, the method for fabricating the fin structures 12 may include the following processes, but not limited thereto. First, a bulk substrate (not shown) is provided and a hard mask layer (not shown) is formed thereon. The hard mask layer is then patterned to

define the location for forming fin structures 12 in the bulk substrate. Afterwards, an etching process is performed to form fin structures 12 in the bulk substrate. After the above processes, the fabrication method for the fin structures 12 is complete. In this case, the fin structures 12 may be regarded as protruding from the surface 10a of the substrate and the compositions of the fin structures 12 and the substrate 10 may be the same, such as epitaxial silicon. In another case, when the substrate is chosen from a III-V semiconductor-on-silicon substrate rather than the above-mentioned bulk substrate, the main compositions of the fin structures may differ from that of the underlying substrate.

[0025] In this embodiment, the hard mask layer (not shown) is optionally removed in a later process after the formation of the fin structures 12, so that a tri-gate MOSFET can be formed in the following processes. There are three contact faces between each fin structure 12 and the following formed dielectric layer serving as a carrier channel region. Compared with planar MOSFETs, the tri-gate MOSFETs have wider channel width within the same channel length. When a driving voltage is applied, the tri-gate MOSFET may produce an on-current twice higher than conventional planar MOSFETs. In another embodiment, the hard mask layer (not shown) is reserved to form a fin field effect transistor (Fin FET), which is another kind of multi-gate MOSFET. Since the hard mask layer is reserved in the fin field effect transistor, there are only two contact surfaces between each fin structure 12 and the following formed dielectric layer.

[0026] Please refer to FIG. 2. FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure. An isolation structure 10 is formed on the substrate 10 between each fin structure 12 so as to electrically isolate subsequently-formed transistors from one another. The isolation structure 20 may have the configuration shown in FIG. 2. At this stage, a lower portion of each fin structure 12 is embedded in the isolation structure 20 and each fin structure 12 exposed out

of the isolation structure 20 may have a first height H1. The isolation structure 10, for example, may be a shallow trench isolation (STI) structure, which may be formed through a STI fabrication process. Since the fabrication process for the STI structure is well-known to those skilled in the art, the detailed description of this is therefore omitted, and is not limited thereto.

[0027] Still referring to FIG. 2, in a following step, a gate dielectric layer (not shown), a sacrificial electrode layer (not shown) and a cap layer (not shown) are sequentially formed to cover the substrate 10 and the fin structures 12. Then, the gate dielectric layer, the sacrificial electrode layer and the cap layer are patterned to form a stack structure. The stack structure may be regarded as a gate structure 30 including the gate dielectric layer (not shown), the sacrificial electrode layer 32 and the cap layer 38. The gate structure 30 crosses over two fin structures 12 and covers the isolation structure 20 between them. Specifically, the gate structure 30 may cover a top surface 14 and two side surfaces 16 of portions of each fin structure 12, and may cover a top surface 22 of portions of the isolation structure 20. Additionally, the gate structure 30 is preferably aligned with a first direction X, while the fin structures 12 are preferably aligned with a second direction Y and protruding from the substrate 10 along a third direction Z. In this embodiment, the first direction X, the second direction Y, and the third direction Z are mutually orthogonal to one another, but not limited thereto.

[0028] For the sake of clarity, only one gate structure 30 is depicted in FIG. 2 to FIG. 11. The number of which, however, may be increased depending on the requirements for different products. For example, more than one mutually parallel gate structure may be disposed on the substrate so that one fin structure may be concurrently covered by more than one gate structure. Besides, the same one gate structure 30 is preferably used as a gate for transistors with the same conductivity type, like gates for PMOS transistors or gates for NMOS

transistors.

[0029] In this embodiment, a gate-last for high-k last process is used so that the gate structure 30 may be regarded as a dummy gate structure. In other words, the gate dielectric layer will be replaced with a gate dielectric layer having a high dielectric constant in later processes and the sacrificial electrode layer 32 will be replaced with a conductive metal layer. Therefore, the material of the gate dielectric layer may be just a sacrificial material suitable for being removed in later processes. The sacrificial electrode layer 32 may be made of polysilicon, but it is not limited thereto. The cap layer 36 may be a single-layered or a multi-layered structure composed of a nitride layer or an oxide layer used to serve as a patterned hard mask. In this embodiment, the cap layer 36 is a double-layered structure composed of a bottom layer 34 and a top layer 34. The bottom layer 34 may be a nitride layer and the top layer 34 may be an oxide layer, but not limited thereto.

[0030] In the above paragraphs, a gate-last for high-k first process is used. However, the present embodiment may also adopt a gate-last for high-k last process. In this case, the gate dielectric layer is a gate dielectric layer having a high dielectric constant, which may be the group selected from hafnium oxide (HfO_2), hafnium silicate (HfSiO_4), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate (SrTiO_3), zirconium silicate (ZrSiO_4), hafnium zirconate (HfZrO_4), strontium bismuth tantalate ($\text{SrBi}_2\text{Ta}_2\text{O}_9$, SBT), lead zirconate titanate ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$, PZT) and barium strontium titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$, BST), but it is not limited thereto. Additionally, a barrier layer (not shown) may be formed on the gate dielectric layer to serve as an etching stop layer to protect the gate dielectric layer during the removal of the sacrificial electrode layer 32 and to prevent above disposed metals from diffusing downwards to the gate dielectric layer and from polluting the gate dielectric layer. The barrier layer (not shown) may be a single layer

structure or a multilayer structure composed of tantalum nitride (TaN) or titanium nitride (TiN) etc.

[0031] Please refer to FIG. 3 and FIG. 4, wherein FIG. 4 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 3. After the formation of the gate structure, a spacer 40 is formed on the sidewalls of the gate structure 30 to define the position of an epitaxial structure. In this embodiment, the spacers 40 are respectively formed on each side of the gate structure 30 and cover portions of the top surface 22 of the isolation structure 20. More precisely, the method for forming the spacers 40 may include the following steps. A material layer is deposited on the gate structure 30 and the substrate 10, and then an etching process is performed to form the spacers 40. The spacers 40 may be a single-layered structure, such as a silicon nitride layer or a silicon oxynitride layer, or a double-layered structure, such as a silicon oxide/silicon nitride layer, but not limited thereto. In this embodiment, the spacers 40 represent spacers for defining and forming an epitaxial structure, so that other spacers may be formed before/after the spacers 40 are formed to form a lightly doped source/drain region (as shown) or a source/drain region (as shown). For simplifying and clarifying the present invention, FIG.3 to FIG. 11 only depict the spacers 40 for forming the epitaxial structure.

[0032] Please refer to FIG. 5. FIG. 5 is a schematic perspective view showing the semiconductor device after etching the isolation structure. After the formation of the spacers 40, the isolation structure 20 exposed from the gate structure 30 and the spacers 40 may be further etched by a suitable etching process. In this way, a top surface 22 of portions of the isolation structure 20 may be etched down to a predetermined depth (also called a first depth D1) and a structure shown in FIG. 5 is obtained. More precisely, a first etching process 42, such as a wet etching or a dry etching process, may be carried out to selectively remove the isolation structure 20 rather than the gate structure 30 and the fin structures 12. Through this process, not only portions of the sidewalls of the isolation

structure 20 that are disposed under gate structure 30 and the spacers 40 may be exposed, but also portions of the fin structures 12 originally embedded in and in direct contact with the isolation structure 20 are exposed. At this time, the isolation structure 20 under the gate structure 30 and the spacers 40 may have a relatively high first top surface 22a, while the isolation structure 20 exposed from the gate structure 30 may have a relatively low second top surface 22b. There is a height difference H2 between the first top surface 22a and the second top surface 22b. For example, the height difference H2 may range from 100 Angstroms' to 250 Angstroms, preferably 150 Angstroms, but not limited thereto.

[0033] Please refer to FIG. 6 to FIG. 8. FIG. 6 is a schematic perspective view showing the semiconductor device after etching fin structures. FIG. 7 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 6. FIG. 8 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 6. As shown in FIG. 6 to FIG. 8, a second etching process 46 is carried out to etch the fin structures 12 under the gate structure 30 and the spacers 40. After the etching process, a recess 60 may be formed in each fin structure 12 at at least one side of the gate structure 30. Furthermore, according to this embodiment, the ends of the fin structures 12 at two sides of the gate structure 30 may respectively have a recess 60, and a bottom surface 68 of the recess 60 is preferably shallower than a bottom surface 26 of the isolation structure 20. More precisely, as shown in FIG. 7 and FIG. 8, there is a difference between the bottom surfaces 62 of the recesses 60 and the top surface 14 of the original fin structure 12, which height is equal to the first height H1 plus the second depth D2. During the second etching process 46, the top surface 22 of the isolation structure 20 at both sides of the gate structure 30 is also recessed down to a predetermined depth. This diminished value is equal to a first depth D1. Preferably, the second depth D2 is greater (also called deeper) than the first depth D1.

[0034] Furthermore, the above etching process may include at least

a dry etching step and/or at least a wet etching step. For example, the substrate 10 may be etched down to a predetermined depth through a dry etching step and then may be laterally etched to form a desired profile of the recess 60 through a wet etching step, but is not limited thereto. In this embodiment, the recess 60 has an upwardly-curved cross-sectional profile, but is not limited thereto, as the cross-sectional profile of the recess depends upon the specific requirements. Additionally, a wet cleaning process (not shown) may be performed optionally to clean the surface of the recess 60 after the etching. The wet cleaning process may include a dilute hydrofluoric acid (DHF) containing process, but it is not limited thereto.

[0035] It should be noted that, the timing for etching the isolation structure 20 exposed from the gate structure 30 and the spacers 40 and the timing for etching the fin structures 12 may be reversed. More precisely, according to the present embodiment, the fin structures 12 exposed from the gate structure 30 and the spacers 40 may be etched first and the isolation structure 20 not covered by the gate structure 30 and the spacers 40 are etched thereafter. In other words, one feature of the present invention is that, through etching the isolation structure 20, the height difference between the bottom surface 68 of each recess 60 and the top surfaces 22 of the isolation structure 20 at both sides of the gate structure 30 can be reduced. Therefore, the removal of the isolation structure 20 and the formation of the recess 60 may be carried out in either sequence and both can meet the needs of the present invention.

[0036] Please refer to FIG. 9 to FIG. 11. FIG. 9 is a schematic perspective view showing the semiconductor device after the formation of an epitaxial layer. FIG. 10 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 9. FIG. 11 is a schematic cross-sectional diagram taken along a line B-B' in FIG. 9. As shown in FIG. 9 to FIG. 11, an epitaxial growth process, such as a molecular beam epitaxy (MBE) process, a co-flow epitaxial growth process, a

cyclic selective epitaxial growth process or the likes, may be carried out in order to grow an epitaxial structure 60 in each corresponding recess 60. More precisely, each epitaxial structure 66 may completely cover the bottom surface 68 and sidewalls 70 of the corresponding recess 60. Furthermore, the composition of the epitaxial structure 66 may be correspondingly modified according to the conductivity types of the semiconductor devices. In this way, a certain stress may be imposed on the channel regions adjacent to the top surface 14 and the two sides of the fin structure 12. For example, in a P-type semiconductor device, the epitaxial structure 66 may be doped or un-doped silicon germanium layer so as to apply a compressive stress to the channel regions. Besides, the epitaxial structure 66 may include a multilayer or a surrounded structure with a different germanium concentration gradually varying from the inside to the outside or/and from bottom to top. For example, the epitaxial layer 66 may include epitaxial Si, at least a layer of epitaxial SiGe with a relatively low concentration of Ge, at least a layer of epitaxial SiGe with a relatively high concentration of Ge, an epitaxial Si layer and so forth, which are disposed sequentially from bottom to up. In another case, in an N-type semiconductor device, the composition of the epitaxial structure 66 may include silicon phosphorous (SiP), silicon carbide (SiC), phosphorus-doped silicon carbide or the likes, so as to provide a tensile stress to the channel regions.

[0037] Furthermore, regardless of the composition of the epitaxial structure 66, since the height difference between the bottom surface 68 of each recess 60 and the top surface 22b of the isolation structure 20 at two sides of the gate structure 30 has been reduced in the above processes, the epitaxial structure 66 may not be sealed during the following epitaxial growth process and the void defects may be avoided as a result. In other words, one feature of the present invention is that, through etching the isolation structure 20 at two sides of the gate structure 30, the epitaxial structure 66 may be formed with a desired height (also called depth) and without any void defects. Accordingly, the epitaxial structure may apply the required stress

to the channel regions thereby increasing the carrier mobility of the semiconductor device.

[0038] After the formation of the above epitaxial structures, the following semiconductor processes may be optionally carried out. For example, a high-k last replacement metal gate (RMG) process may be carried out so that the gate structure composed of polysilicon inside may be replaced with a metal gate structure. The RMG process may include the following processes: (1) depositing an interlayer dielectric to surround the gate structure; (2) removing the gate structure to leave a trench; (3) forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench; and (4) forming a conductive layer to fill up the trench. Afterwards, a contact formation process may be carried out to form a contact electrically connecting the epitaxial structure. Since the RMG process and the contact formation process are well-known to those skilled in the art, the detailed description of these is therefore omitted for the sake of clarity.

[0039] In the following paragraph, a modified embodiment of the above embodiment is disclosed and the description below is mainly focused on differences among each embodiment. In addition, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0040] Please refer to FIG. 3 and FIG. 5. According to this modified embodiment, after the formation of the spacers, the first etching process is also carried out to expose not only portions of the sidewalls of the isolation structure 20 disposed under the gate structure 30 and the spacers 40, but also to expose portions of the fin structures 12 originally embedded in and in direct contact with the isolation structure 20. Afterwards, with a slight difference from the process described in the above embodiment, the second etching process is not carried out in this modified embodiment so that no recess is formed in the fin structures. Finally, similarly to the

structure shown in FIG. 9, the epitaxial growth process is carried out to form the epitaxial structure 66 on the surface of the fin structure. The following processes are all similar to those described in the previous embodiment, the detailed description of which is therefore omitted for the sake of clarity. In this modified embodiment, since portions of the isolation structure 20 are removed, the epitaxial structure 66 may effectively apply stress to the corresponding channel regions.

[0041] It should be noted that, for the sake of clarity, only the non-planar FETs are described in the above paragraphs. However, planar FETs may also be formed without departing from the scope and spirit of the present invention. More precisely, in this case, the gate structure may be formed to cover a planar active region and portions of the isolation structures. Then, the active region and the isolation structure at two sides of the gate structure are etched sequentially. Finally, an epitaxial growth process is carried out. Similarly, through etching the isolation structure at two sides of the gate structure, the epitaxial structure may be formed with a desired height (also called depth) without void defects. Accordingly, the epitaxial structure may apply the required stress to the channel regions thereby increasing the carrier mobility of the semiconductor device.

[0042] To summarize, the present invention provides a semiconductor device. By performing the process for etching the isolation structure and associated with an optional recess, the difference in height between the bottom surface of the recess and the top surface of the isolation structure at two sides of the gate structure may be reduced. In this way, the epitaxial structure may not be sealed during the following epitaxial growth process and the void defects may be avoided. Accordingly, the epitaxial structure may apply a required stress to the channel regions and increase the carrier mobility of the semiconductor device.

[0043] Those skilled in the art will readily observe that numerous

modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Filer:	Winston Hsu/Hitomi Lin
Attorney Docket Number:	NAUP1656USA1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720

Pages:

Claims:

Miscellaneous-Filing:

Petition:

Patent-Appeals-and-Interference:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	21475224
Application Number:	14620209
International Application Number:	
Confirmation Number:	3329
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Kate Yeh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA1
Receipt Date:	12-FEB-2015
Filing Date:	
Time Stamp:	03:53:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2178683.PDF	1671397 <small>b98f4e9d57296548585632bf3a7765b2a0841e6f</small>	no	8

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	2178677.PDF	34947 a3c64c866a2c82a2e710fe23a51df32b2330 ce17	no	5
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Authorization to access Appl. by Trilateral Office	2178675.PDF	37258 8bb0a0c0490932072978aa7f07baffb176f4 18ae	no	1
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Warnings:					
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5	Power of Attorney	2178673.pdf	2385448 cd318041229bcc6b60d00421255bfc8cbd5 3023e	no	13
Warnings:					
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6	Drawings-only black and white line drawings	2178523.PDF	85204 4a7a93b34dd76e5c9a0d3fbfa8e9cde74d4 c25e1	no	6
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7	Abstract	2178522.PDF	24289 5123707b3d04b422d473528d1d3f9ddd45 3567e4	no	1
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8	Claims	2178521.PDF	27620 5f874e0367acecac34f7fb968b97b573dfa2 21a9	no	2
Warnings:					
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9	Specification	2178520.PDF	70311 be0880433b9b8d407334da7ddfae60a207 b758f9	no	14
Warnings:					
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10	Fee Worksheet (SB06)	fee-info.pdf	35096 49d43bd76edcf923219a0c877298d7bb006 8f739	no	2

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Total Files Size (in bytes):	4708727
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA1
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

<input type="checkbox"/>	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information:

Inventor 1					<input type="button" value="Remove"/>
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA1
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE		

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Legal Name				
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Postal Code		Country i	TW	
Inventor 5				<input type="button" value="Remove"/>

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City	Hsinchu City	State/Province		
Postal Code		Country i	TW	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1656USA1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

An Address is being provided for the correspondence information of this application.

Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE		
Attorney Docket Number	NAUP1656USA1	Small Entity Status Claimed	<input type="checkbox"/>
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1656USA1
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE		
Please Select One:	<input checked="" type="radio"/> Customer Number	<input type="radio"/> US Patent Practitioner	<input type="radio"/> Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13913511	2013-06-09
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1656USA1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p><input type="checkbox"/> NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
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Authorization to Permit Access:

<input checked="" type="checkbox"/> Authorization to Permit Access to the Instant Application by the Participating Offices
<p>If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.</p> <p>In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.</p> <p>In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.</p>

Applicant Information:

<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>
--

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1656USA1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE	

Applicant 1			<input type="button" value="Remove"/>
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p>			
<input type="button" value="Clear"/>			
<input checked="" type="radio"/> Assignee	<input type="radio"/> Legal Representative under 35 U.S.C. 117	<input type="radio"/> Joint Inventor	
<input type="radio"/> Person to whom the inventor is obligated to assign.		<input type="radio"/> Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor : <input type="text"/>			
If the Applicant is an Organization check here. <input checked="" type="checkbox"/>			
Organization Name	UNITED MICROELECTRONICS CORP.		
Mailing Address Information:			
Address 1	No.3, Li-Hsin Road 2,		
Address 2	Science-Based Industrial Park		
City	Hsin-Chu City	State/Province	
Country i	TW	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. <input type="button" value="Add"/>			

Assignee Information including Non-Applicant Assignee Information:

<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>	
Assignee 1	
<p>Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.</p>	
<input type="button" value="Remove"/>	
If the Assignee or Non-Applicant Assignee is an Organization check here. <input type="checkbox"/>	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1656USA1
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE	

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Winston Hsu/			Date (YYYY-MM-DD)	2015-02-12
First Name	Winston	Last Name	Hsu	Registration Number	41526
Additional Signature may be generated within this form by selecting the Add button.					<input type="button" value="Add"/>

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Yu-Hsiang Hung
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	NAUP1656USA1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8765533	B2	2014-07-01	Hsieh	
	2	6043138		2000-03-28	Ibok; Effiong E.	all
	3	6492216		2002-12-10	Yeo; Yee-Chia	all
	4	6921963		2005-07-26	Krivokapic; Zoran	all
	5	7087477		2006-08-08	Fried; David M.	all
	6	7091551		2006-08-15	Anderson; Brent A.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7250658		2007-07-31	Doris; Bruce B.	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

9	7309626		2007-12-18	leong; Mei-Kei	all
10	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
11	7470570		2008-12-30	Beintner; Jochen	all
12	7531437		2009-05-12	Brask; Justin K.	all
13	7569857		2009-08-04	Simon, legal representative; David	all
14	7525160		2009-04-28	Kavalieros	

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20040195624		2004-10-07	Liu, Chee-Wee;	all
	2	20050051825		2005-03-10	Fujiwara, Makoto;	all
	3	20060099830		2006-05-11	Walther; Steven R.;	all

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	
First Named Inventor	Yu-Hsiang Hung
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	NAUP1656USA1

4	20060286729		2006-12-21	Kavalieros; Jack;	all
5	20070108528		2007-05-17	Anderson; Brent A.;	all
6	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
7	20080157208		2008-07-03	Fischer; Kevin J.;	all
8	20090124097		2009-05-14	Cheng; Kangguo;	all
9	20090242964		2009-10-01	Akil; Nader;	all
10	20090269916		2009-10-29	KANG; Inkuk;	all
11	20100048027		2010-02-25	Cheng; Kangguo;	all
12	20100072553		2010-03-25	XU; Jeff J.;	all
13	20100144121		2010-06-10	Chang; Cheng-Hung;	all
14	20100167506		2010-07-01	LIN; Simon Su-Horng;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

15	20120193713		2012-08-02	Kulkarni	
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1						

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.
	1	

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Yu-Hsiang Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1656USA1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2015-02-12
Name/Print	Winston Hsu	Registration Number	41,526

Electronic Patent Application Fee Transmittal

Application Number:	14620209
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Filer:	Winston Hsu/Steffi Chang
Attorney Docket Number:	NAUP1656USA1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720

Pages:

Claims:

Miscellaneous-Filing:

Petition:

Patent-Appeals-and-Interference:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	21490566
Application Number:	14620209
International Application Number:	
Confirmation Number:	3329
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURE
First Named Inventor/Applicant Name:	Yu-Hsiang Hung
Customer Number:	27765
Filer:	Winston Hsu/Steffi Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1656USA1
Receipt Date:	12-FEB-2015
Filing Date:	
Time Stamp:	19:45:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1600
RAM confirmation Number	5905
Deposit Account	503105
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)
 Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	35400 f70d3d0b8dbcc8ebf84a33428bab2b087433b132	no	2

Warnings:

Information:

Total Files Size (in bytes):	35400
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.