

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,  
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,  
Patent Owner.

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Case No. IPR2025-01265  
U.S. Patent No. 8,993,384

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**PETITIONER'S OPPOSITION TO PATENT OWNER'S  
DISCRETIONARY DENIAL REQUEST**

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**Updated List of Petitioner Exhibits**

Ex.	Description
1001	U.S. Patent No. 8,993,384 (“384 patent”).
1002	Prosecution History of U.S. Patent No. 8,993,384.
1003	Declaration of Dr. Jack Lee, Ph.D.
1004	U.S. Patent No. 9,166,022 B2 (“Xu”).
1005	U.S. Patent 2012/0091538 A1 (“Lin”).
1006	U.S. Patent Pub. No. 2005/0148137 A1 (“Brask”).
1007	T. Ghani et al, <i>A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45 Nm Gate Length Strained Silicon CMOS Transistors</i> , IEEE International Electron Devices Meeting 2003, pp. 11.6.1-11.6.3 (2003).
1008	Excerpts from N. Collaert, <i>CMOS Nanoelectronics</i> (2012).
1009	A. Veloso et al., <i>Gate-Last vs. Gate-First Technology for aggressively scaled EOT Logic/RF CMOS</i> , Symposium on VLSI Technology – Digest of Technical Papers, pp. 34-35, (2011).
1010	M. Quirk and J. Serda, <i>Semiconductor Manufacturing Technology Instructor’s Manual</i> (2001) (archived Sep. 28, 2007).
1011	Excerpts from S. P. Muraka et al., <i>Interlayer Dielectrics for Semiconductor Technologies</i> (2003).
1012	Excerpts from D. Neaman, <i>Semiconductor Physics and Devices</i> (2012).
1013	D. Hisamoto et al., <i>Folded-channel MOSFET for deep-sub-tenth micron era</i> , International Electron Devices Meeting 1998 – Technical Digest, pp. 1032-1034, (1998).
1014	X. Huang et al., <i>Sub 50-nm FinFET: PMOS</i> , International Electron Devices Meeting 1999 – Technical Digest, pp. 67-70, (1999).
1015	D. Hisamoto et al., <i>FinFET – a self-aligned double-gate MOSFET scalable to 20 nm</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, pp. 2320-2325 (2000).
1016	J. Markoff, <i>Intel Increases Transistor Speed by Building Upward</i> , New York Times (2011).

1017	Intel, <i>Intel's Revolutionary 22 nm Transistor Technology</i> (2011).
1018	A. Shimpi, <i>Intel Announces first 22nm 3D Tri-Gate Transistors, Shipping in 2H 2011</i> , AnandTech (2011) (archived May 18, 2011).
1019	K. Mistry et al., <i>A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging</i> , 2007 IEEE International Electron Devices Meeting, pp. 247-250, (2007)
1020	U.S. Patent No. 7,525,160 B2 (“Kavalieros”)
1021	S. Thompson et al., <i>Key Differences for Process-Induced Uniaxial vs. Substrate-Induced Biaxial Stressed Si and Ge Channel MOSFETs</i> , Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 221-224 (2004).
1022	C. Auth et al., <i>45nm High-k + Metal Gate Strain-Enhanced Transistors</i> , 2008 Symposium on VLSI Technology, pp. 128-129
1023	S. Mayuzumi et al., <i>High-Performance Metal/High-k n- and p-MOSFETs With Top-Cut Dual Stress liners Using Gate-Last Damascene Process on (100) Substrates</i> , IEEE Transactions on Electron Devices, Vol. 56, No. 4, pp. 620-626, (2009)
1024	Excerpts from G. May and S. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2004).
1025	Excerpts from S. Wolf, <i>Microchip Manufacturing</i> , (2004).
1026	<i>Curriculum Vitae</i> of Dr. Jack Lee, Ph.D.
1027	Declaration of Stephen M. Bradley
1028-1100	Intentionally Left Blank
1101	Hsieh (U.S. Patent No. 8,735,553)
1102	Ching (U.S. Pub. No. 2014/0131776)
1103	Cho (U.S. Patent No. 8,853,037)
1104	Goto (U.S. Pub. No. 2014/0070328)
1105	van Dal (U.S. Pub. No. 2012/0319211)
1106	Liao (U.S. Patent No. 9,812,363)
1107	Chang (U.S. Patent No. 9,570,567)
1108	USPTO Class 257 Schedule

1109	USPTO Class 438 Definitions
1110	Xu-472 (U.S. Pub. No. 2012/0104472)
1111	TSMC Institution Decisions
1112	TSMC FWD Rate
1113	Baker (U.S. Patent No. 8,214,007)
1114	TSMC-Ansys Collaboration Press Release
1115	TSMC-Cadence Press Release
1116	'384 Patent Assignment to Marlin
1117	TSMC Technology Overview
1118	Intentionally Left Blank
1119	CNBC Transcript – US Commerce Secretary Howard Lutnick
1120	Removing Barriers to American Leadership in Artificial Intelligence
1121	Another Historic Investment Secured Under President Trump
1122	Tsai (U.S. Patent No. 10,263,108)
1123	Zhang (U.S. Patent No. 9,653,605)
1124	Nasdaq – This 1 Number May Ensure TSMC’s Market Dominance
1125	TSMC’s Resurgence: What Lies Ahead for the Architect of AI
1126	Decoding TSMC’s Contribution to the AI and 5G Ecosystem
1127	TSMC Annual Report 2024 (Excerpts)
1128	Yahoo! Finance Article on TSMC Fab 21
1129	Prosecution History of U.S. Patent No. 9,812,363
1130	Prosecution History of U.S. Patent No. 9,570,567
1131	Prosecution History of U.S. Patent No. 10,263,108

## **I. Introduction**

A core purpose of the PTAB under the American Invents Act (AIA) is to strengthen the integrity of the U.S. patent system by ensuring that only valid and properly granted patents remain in force. The challenged patent in the present proceeding, U.S. Patent No. 8,993,384, issued as a result of material Examiner error. To overcome a prior art rejection, Applicant amended the sole independent claim by adding a trivial sequencing limitation—merely specifying that the etching of the isolation structure occurs after the formation of the gate structure. Applicant represented that the applied prior art, Kavalieros and Hsieh, failed to teach this feature. The Examiner credited Applicant’s representation and allowed the claims. In doing so, the Examiner erred by overlooking core technical teachings in the Hsieh reference disclosing the added feature. Moreover, the Examiner’s search strategy fell far below the standard demanded by the Office resulting in the Examiner’s failure to identify numerous references disclosing the allegedly missing limitation. Referral is warranted to address these errors.

Additionally, the settled interests of TSMC and its customers outweigh any settled interests of the new Patent Owner, Marlin, and warrant referral. TSMC and its customers had a settled expectation of non-enforcement due to the lack of assertion by UMC, an alleged “primary” competitor of TSMC’s, during the first 8 years of the ’384 patent’s life. Indeed, Marlin fails to advance any evidence of prior

commercialization, licensing, or marking in the “technology space” where Marlin now seeks to enforce the patent. During this time of patent inactivity, TSMC invested billions of dollars to manufacture FinFET chips, including for American customers who expected to be able to integrate those chips into their own products without incident. Marlin, a foreign entity which only recently acquired the patent, has no comparable expectations.

Referral for consideration on the merits is warranted and is an efficient use of Board resources in view of the *Fintiv* factors because the ’384 patent is not currently asserted in a parallel litigation. There is, however, a threat of enforcement, as evidenced by Marlin’s claim of infringement and existing lawsuits in the ITC and district court. In response, TSMC diligently challenged the validity of the patent in the PTAB prior to any litigation to provide a true alternative to district court or ITC litigation. Moreover, this case involves complicated semiconductor technologies, and trained PTAB judges are best suited to adjudicate the merits of the Petition and to correct the past errors of this Office.

Finally, compelling national security, economic, and public interests make review of the ’384 patent an appropriate use of the Board’s resources. TSMC is the world’s largest chip maker, by some accounts providing around 90% of the world’s advanced chips (i.e., FinFETs). Ex. 1124, 2. Its advanced semiconductor technology, against which Marlin has asserted the ’384 patent, is vital to the U.S. supply chain,

with a wide range of applications including AI (e.g., NVIDIA's AI supercomputers), 5G, health care, and national security and defense. As key members of this Administration have acknowledged, promoting the development of semiconductors and the technology they enable (e.g., AI) is an important goal for the United States. Ex. 1119; Ex. 1120. Given TSMC's vital and strategic contribution to the U.S. supply chain, the Administration has a heightened interest in ensuring that the USPTO corrects its error in issuing this patent.

A holistic assessment of the facts, evidence, circumstances, and relevant considerations (detailed below) confirms that TSMC's Petition should be referred.

## **II. Referral Is Warranted In View Of Material Error By The Examiner.**

TSMC's petition should be referred to the Board to correct material errors in the examination process. First, the Examiner failed to properly consider that a reference applied during prosecution disclosed the purported novel amendment. Second, the Examiner's inadequate search failed to identify material prior art, including the references applied in TSMC's strong Petition. The severity of the Examiner's material errors here are as strong as, if not stronger than, the material errors that the Director has found justify referral. *See, e.g., Carbyne, Inc. v. TriTech Software Sys.*, IPR2025-00959, Paper-11, 2 (Oct. 3, 2025) (referring in part based on examiner error where reference "cited on an IDS during prosecution" "appears to disclose the purportedly missing claim limitations" leading to allowance).

**A. The Examiner materially erred by overlooking the teachings in the applied reference as well as references in the file wrapper.**

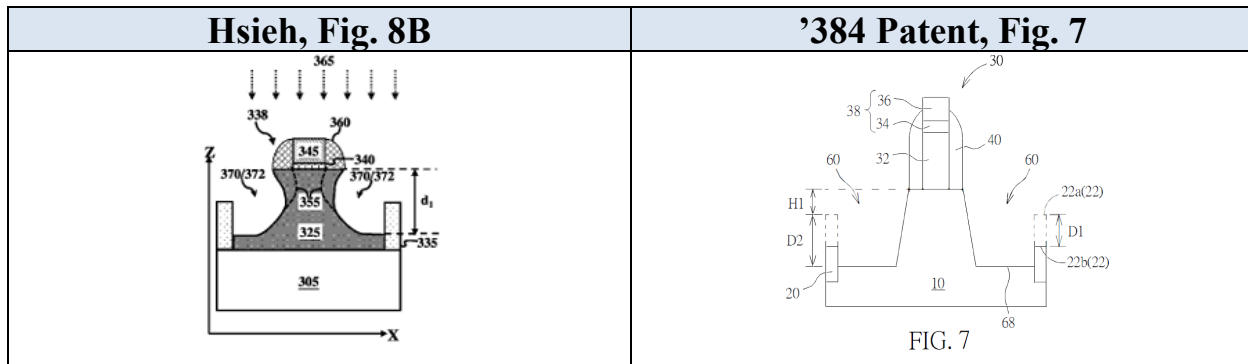
The merits are particularly strong due to errors made during prosecution, warranting referral to correct those mistakes. During prosecution, the sole Office Action rejected pending claims 11-13 and 15-18 as anticipated by Kavalieros (U.S. Patent No. 7,525,160) (Ex. 1020) and claims 14 and 19 as obvious over Kavalieros in view of Hsieh (U.S. Patent No. 8,765,533) (Ex. 1101). Ex. 1002, 88-90.

In response, the Applicant did not traverse the Examiner's rejection, effectively acquiescing that Kavalieros discloses the limitations of as-filed claim 11. Instead, Applicant amended claim 11 (issued claim 1) to recite "after the step of forming the gate structure, etching the isolation structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth." *Id.*, 103. In its companion remarks, Applicant argued that both Kavalieros **and** also Hsieh "fail[] to teach or suggest" this feature, contending that a POSITA "would not anticipate" this claimed feature, even if "refer[ring] to the cited references." *Id.*, 107-108. The Examiner allowed the amended claims, stating only that "Examiner agrees with applicant's arguments, with regard to the amended claims." *Id.*, 118.

The applicant misrepresented, or misunderstood, the teaching of the Hsieh reference. Specifically, the Hsieh reference, a TSMC patent relied upon by the Examiner, discloses this very feature subject of the amendment. In rejecting original claims 14 and 19, the Examiner cited only to "figs. 10A-13B and related text" of

Hsieh. *See* Ex. 1002, 3-4; Ex. 1101, 6:31-9:3 (discussing Figures 10A-13B and related text). By focusing on this limited disclosure, the Examiner overlooked the portion of Hsieh that is most relevant to the added claim limitation, which is a material error. *See Taiwan Semiconductor Manufacturing Co. Ltd., et al v. Marlin Semiconductor Ltd.*, IPR2025-00847, Paper-11, 3-4 (Sept. 3, 2025). Hsieh discloses a FinFET fabrication method that explicitly includes an etch process that removes “portions of the isolation feature 335” **after** the formation of the gate structure. Ex. 1101, 5:37-50. Specifically, after forming a gate structure 338 (*see id.*, Figs. 5A-7C, 4:21-5:34), “*an etching process removes ... portions of the isolation feature 335 to form source and drain recesses 372.*” *Id.*, 5:37-50.

Overlooking the teachings of Hsieh is particularly problematic since the etch process taught by Hsieh is virtually identical to the etch process disclosed in the '384 patent, as illustrated by the side-by-side figures below. The '384 patent discloses that “[d]uring the second etching process 46, the top surface 22 of the isolation structure 20 at both sides of the gate structure 30 is also recessed down to a predetermined depth.” Ex. 1001, 6:1-4. This recess of the isolation structure is at the very heart and alleged allowable subject matter of independent claim 1. Ex. 1001, 8:36-37, 40-42. Yet the Examiner failed to recognize that Hsieh’s highly similar etch process would achieve the same result as depicted in Figure 7 of the '384 patent, thus teaching the purportedly missing claim limitation.



Thus, this teaching of Hsieh when combined with Kavalieros, which Applicant acquiesced discloses the remaining features of as-filed claim 11, discloses every limitation of amended claim 11 (issued claim 1), rendering the claim obvious.

**B. The Examiner materially erred by conducting an inadequate search that failed to identify and apply material prior art.**

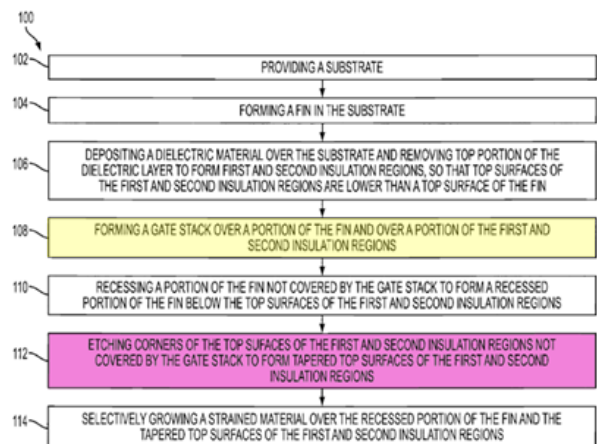
Aside from Hsieh, the art is replete with teachings of the alleged missing limitation, including the references raised in the Petition, which clearly teach this feature. Pet., 20-21, 67-68; Ex. 1102, Figs. 2-3, Ex. 1103, Figs. 11-12, Ex. 1104, Figs. 1A-1B, Ex. 1105, Figs. 3A-3B. The Examiner's failure to locate this art is the result of an inadequate and sub-standard prior art search. Even a minimally adequate search would have uncovered the prior art applied in the petition that discloses all limitations of claim 1 including the alleged missing limitation.

Search notes from the '384 patent's file wrapper indicate that, before issuing the Non-Final Rejection, the Examiner searched only within certain subclasses of a single USPC class (438). Ex. 1002, 94. The Examiner therefore failed to consider art classified in other relevant areas, such as class 257 which covers active solid-

state devices, including field effect devices (like FinFETs, the subject matter of the '384 patent). Ex. 1108, 1.

Compounding this error, the Examiner failed to search the most relevant subclasses within the searched class 438, which would have led to material prior art. For example, the Examiner did not search subclass 438/694 directed to relevant etching processes. Ex. 1109, 120. Had the Examiner properly searched this subclass, the Examiner would have found the Lin reference (Ex. 1005), a primary reference in the Petition that invalidates 7 out of 9 claims of the '384 patent (Pet., 43-79) and teaches the limitation that the Examiner deemed allowable.

Specifically, Lin discloses etching “corners of the top surfaces of the first and second insulation regions not covered by the gate stack . . . to form tapered top surfaces of the first and second insulation region.” Ex. 1005, ¶ [0013]. As Lin’s Figure 1 confirms, this etching process (magenta) is performed after forming a gate stack (yellow). Moreover, Lin explains that the etching process “make[s] it easier for growth precursors to reach the growth surface during selective growth of the strained material” grown in recesses between portions of the isolation structure. *Id.*, ¶ [0036]. Lin thus teaches the missing claim limitation: “after the step of forming the gate structure, etching the isolation



structure exposed from the gate structure until a top surface of the isolation structure is etched down to a first depth.” The Examiner erred not only in failing to identify and apply Lin, but in ignoring the advantages of such an etching step that a POSITA would have been motivated to apply to teachings of the applied art.

Additionally, even within the parameters of this deficient search, the Examiner failed to identify and apply material art that was returned. The search notes indicate that the Examiner searched subclass 438/294. Ex. 1002, 94. But the Examiner did not do so diligently as evidenced by U.S. Pub. No. 2012/0104472 (“Xu ’472”) (Ex. 1110)—the pre-grant publication of Xu (Ex. 1004), applied in the Petition—which sits within this subclass but was not applied by the Examiner. Like Ex. 1004, Xu ’472 renders obvious all claims of the ’384 patent and teaches the limitation that led to the patent’s allowance. *See Pet.*, 10-43.

In particular, Xu’s Figures 2 and 3 depict “an etching process [that] is applied to recess the isolation features 130.” Ex. 1004, 4:54-56. This process occurs after the formation of a gate structure (yellow) and etches a top surface of the isolation structure down to a first depth, as claimed:

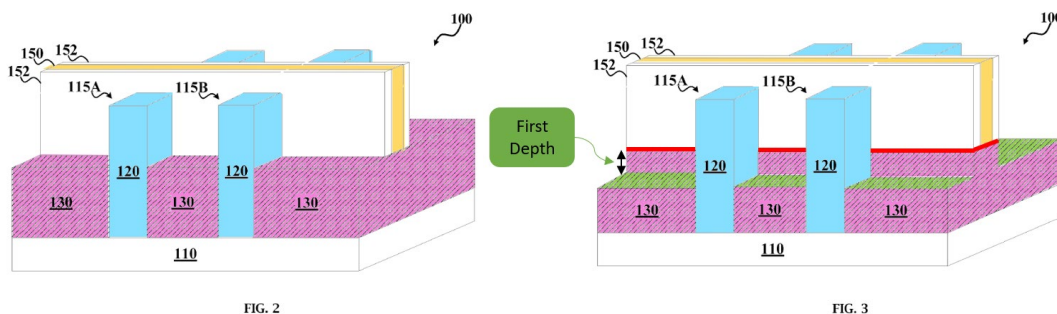


FIG. 2

FIG. 3

The Examiner’s failure to explain how the search of this subclass was limited, and his failure to include a complete search history in the patent’s file wrapper “indicate[s] that all documents having those symbols were reviewed.” MPEP § 719.05. Accordingly, the Examiner is presumed to have reviewed Xu ’472 but failed to apply it, which is a material error that warrants referral to the Board.

TSMC’s asserted art is not unique—*many* prior art references disclose the limitation that led to allowance. *E.g.*, Exs. 1102, 1103, 1104, 1005. For example, U.S. 2014/0131776 (“Ching”) (Ex. 1102), another TSMC reference, discloses an etch step wherein “top surfaces 22A of STI regions 22

are also recessed from the original top surface 22A’ of STI regions.” Ex. 1102, ¶ [0013]. As shown in annotated Fig. 3, this process etches isolation regions (pink) after the formation of a gate structure (yellow) down to a first depth, represented by the top surface of

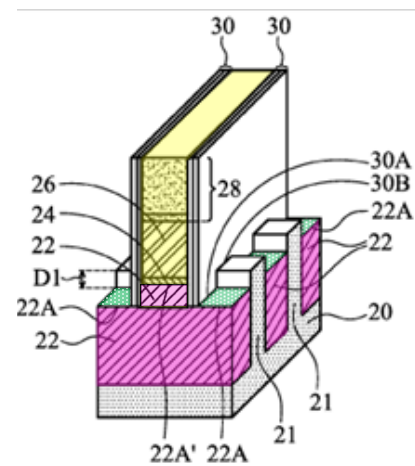


Fig. 3

the isolation (green). Accordingly, the claims should not have been allowed in view of this limitation, which was known in various prior art references that should have been used to reject the claim.

The Examiner’s deficient search process is further underscored by the search notes accompanying the subsequent notice of allowance. Ex. 1002, 124. The Examiner lists various CPC symbols purportedly used to search the prior art. But

none of these symbols match the CPC classifications applied to the '384 patent. *Compare id.* (“H01L/822, 8232, 9234, 8258”) *with* Ex. 1001 (listing H01L 29/7848, H01L 29/6681, H01L 29/7855, H01L 21/8234). Failure to even search the very areas where the patent itself is classified is emblematic of a poor search process that constitutes a material error warranting referral.

The Examiner’s compound, material error warrants referral to the Board. *See, e.g., Carbyne*, IPR2025-00959, Paper-11, 2 (referring in part based on examiner’s failure to apply reference cited on an IDS); *Azurity Pharmaceuticals, Inc. v. Helsinn Healthcare S.A.*, IPR2025-00945, Paper-11, 2-3 (Sep. 19, 2025) (referring 11-year-old patent based on examiner’s erroneous assessment of unexpected results); *TSMC*, IPR2025-00847, Paper-11, 3-4 (referring 15-year-old patent based on examiner’s failure to apply reference cited during prosecution).

### **III. Referral is Warranted Because of the Strength of the Petition, Which Invalidates All Claims Over Two Separate Primary References.**

The merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TSMC is a strong Petitioner (Ex. 1111; Ex. 1112) and presents two single-reference §103 grounds<sup>1</sup> against the sole independent claims—*Xu and Lin. Pet.*, 3-4, 20-21, 67-68. Marlin identifies no substantive deficiencies in

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<sup>1</sup> Petitioner notes that while the Petition grounds (filed July 8, 2025) present *Xu and Liu* “in view of the knowledge of a POSITA,” this knowledge is not being used to provide a missing limitation, but to demonstrate the knowledge of a POSITA and provide rationales for obviousness.



semiconductor industry, including TSMC's customers. Ex. 2104, 1. Marlin also cannot dispute that it has since asserted a set of its patents against TSMC in the ITC, seeking an exclusion order while good faith negotiations with TSMC remained open. The Petition should be referred to resolve this dispute before Marlin's enforcement of the '384 patent against TSMC or its customers disturbs the parties' well-settled expectations that the '384 patent remain dormant.

First, TSMC and its customers had settled expectations that the '384 patent would not be asserted due to the prior owner's inaction during the majority of the '384 patent's life. TSMC has been engaged in FinFET manufacture since 2013. Ex. 1117, 3. For over eight years after the March 31, 2015 issue date of the '384 patent, TSMC invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the FinFET technology, and its customers similarly invested significant resources into designs based on that technology. *See* Ex. 1121. During this time, the prior owner of the '384 patent, who Marlin claims is "TSMC's main competitor" (Paper-6, 3), remained silent and inactive. UMC's inactivity created settled expectations for TSMC and its customers that the patent would remain dormant. These expectations are reflected by TSMC's continuous manufacturing and extensive investment in this technology which began before the '384 patent issued and continued with no enforcement until Marlin's recent activities.

But Marlin’s activities cannot unwind the settled expectations of TSMC and its customers created by UMC’s longstanding inaction with the patent. In analogous bodies of law, the expectations of others would exceed those of a new property owner under such circumstances. *See* Restatement (First) of Prop. § 459 cmt. a (1993) (“Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance.”); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) (“[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.”).

Second, despite being the Patent Owner and holding such confidential information, Marlin has not presented any persuasive evidence that ’384 patent was ever “commercialized, asserted, marked, licensed, or otherwise applied” in the same “particular technology space” where it now seeks enforcement, which weighs against any claim by Marlin of “settled expectations.” *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasy, Inc.*, IPR2025-00531, Paper-10, 3 (July 17, 2025) (internal quotations omitted); *Home Depot U.S.A., Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper-11, 2-3 (Sep. 4, 2025).

The ’384 patent has not been asserted in litigation in any venue, against any party. Marlin alleges that UMC is “another Taiwanese semiconductor foundry” and

“TSMC’s main business competitor.” Paper-6, 1. Yet Marlin has not pointed to any evidence suggesting UMC enforced or demanded a license for the ’384 patent against TSMC (or anyone) during the 8 years UMC owned the patent.

Marlin also misleadingly argues that the ’384 patent “has been commercialized, at least in the form of licensing” with Intel Corporation and Samsung Electronics Co., Ltd. Paper-6, 4-5. Marlin did not produce these licenses in the present proceeding, instead supporting this statement only through a bare assertion by its corporate representative Paul Ahern without further context. Ex. 2104. Nowhere does Marlin or Mr. Ahren state when the license was entered, under what terms, or what products of Intel and Samsung Electronics are covered, let alone that the license was for products in the same technology space. Moreover, Marlin fails to put forth any evidence that these purported licenses were public or that its purported licensees marked their products in any way to evidence commercialization that would disturb TSMC’s settled expectations in its freedom to operate.

At bottom, when Marlin acquired patents that had never been asserted in any proceeding (including the ’384 patent) with the intention of enforcing them, the only reasonable expectation it could have is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 (“timing” of a property purchase and “knowledge of the purchaser” are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342,

1361-63 (Fed. Cir. 2019) (patent owners know their patents may be subject to post-issuance reconsideration proceedings); *see also* Brief for the Federal Respondent in Opposition, *Gesture Tech. Partners, LLC v. Apple Inc., et al.*, No. 24-1280, 14 (2025) (“[I]t was well understood at the founding that a patent system could include a practice of granting patents subject to potential cancellation in an executive proceeding.”) (quote and citation omitted). Marlin attempts to distract from this by attacking TSMC’s strong settled expectations, but these attempts are unpersuasive.

For example, relying on *iRythym Tech., Inc. v. Welch Allyn, Inc.*, IPR2025-00363, Marlin argues that TSMC’s alleged knowledge of the patent through prosecution of five of its own patents favors denial. Paper-6, 4. But Marlin’s argument is factually deficient and distinguishable. One of these patents does not cite to the ’384 patent or any of its family members. Ex. 1123. While family members of the ’384 patent (not the ’384 patent itself) are cited in three other U.S. patents, these references were cited by the Examiner (Exs. 1106, 1107, 1122), not in an IDS, as Marlin argues, and as was the case in *iRhythym*. Paper-6, 4; *iRythym*, Paper-10, 3. The basis for Marlin’s argument as to the final, German application is entirely unclear. Moreover, unlike in *iRhythym* where the Patent Owner in the IPR proceeding owned the patent at the time of issuance, the citations here occurred before Marlin acquired the patent. Ex. 1113 (U.S. Patent No. 8,214,007 issued to Welch Allyn, Inc.); Ex. 1129, 21; Ex. 1130, 48; Ex. 1131, 107. As described above,

TSMC has settled expectations, based on UMC's conduct, that the '384 patent would not be asserted.

Finally, Marlin also argues that licensing negotiations between the parties beginning in 2024 weigh against any claim of settled expectations by TSMC. Paper-6, 7 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc.* IPR2025-00693, Paper-13, 7). Marlin's reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding involving the challenged patents and the Petitioner did not even argue that the Examiner had materially erred during prosecution. *DataDome*, Paper-6, 7; Paper-39, 26-31. Both of these factors differ in the present case and weigh in favor of referral.

Moreover, TSMC filed this Petition just 11 months after receiving a demand, which was followed by a period of evaluation and good faith negotiations, and just 5 months after those negotiations discontinued by Marlin asserting patents against TSMC in court. TSMC was therefore far more diligent than the *DataDome* Petitioner who waited over two years after receiving an initial demand and 15 months after refusing a license to file its IPR Petition. *DataDome*, Paper-13, 7; *id.*, Pet'r. Ex. 1013 (January 11, 2023 letter seeking license on one of the challenged patents).

#### **V. Referral Is An Efficient Use Of Board Resources**

Additionally, referral here is warranted as an efficient use of Board resources in view of the *Fintiv* factors because there is no parallel litigation involving the '384

patent, making the PTAB the most efficient forum to resolve this dispute. *See, e.g., Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper-12, 2-3 (Aug. 12, 2025) (“[T]he parties are not involved in a parallel proceeding involving the challenged patents. As a result, there is no concern of inconsistent outcomes or significant duplication of efforts resulting from two proceedings operating in parallel.”). There is no other tribunal set to resolve the merits of this dispute and therefore no risk of duplicated efforts, inconsistent decisions, or unnecessary expense for the parties.

Marlin sidesteps this important fact, arguing it is not dispositive because the petitions in *Intel Corp. v. Proxense LLC* were still discretionarily denied despite having no *trial date*. Paper-6, 7-8 (citing IPR2025-00327, -00328, -00329, Paper-12, 2 (June 25, 2025)). However, in *Intel*, the Acting Director explained that the decision to discretionarily deny was based upon Petitioner’s failure to “provide any persuasive reasoning as to why an *inter partes* review is an appropriate use of Board resources.” *Intel*, Paper-12, 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources including to address the Examiner’s materially deficient examination and to resolve the parties’ dispute in an efficient manner that avoids “unnecessary and counterproductive litigation costs” before Marlin asserts this patent in a court against TSMC. November 2019 Consolidated Trial Guide, 56

(quoting H.R. Rep. No. 112-98, pt. 1, 40 (2010), 2011 U.S.C.C.A.N. 67, 69 (explaining the rationale underlying the AIA)).

Marlin has already alleged infringement of the '384 patent and shown a willingness to bring TSMC to Court. Referral of the Petition before litigation promotes the very ideals that underlie the IPR process and is therefore an appropriate use of Board resources. Moreover, with no parallel litigation and every factor weighing heavily in favor of institution other than the age of the patent, to deny referral here would be to create a brightline rule against IPR for older patents—which cannot be the intention of Deputy Director Stewart's March 26, 2025 Memorandum.

#### **VI. National Security, Economic, and Public Interest Considerations Warrant Referral**

Marlin acknowledges it has alleged infringement of the '384 patent by TSMC. Ex. 2014. Given Marlin's chosen forum for enforcement is the ITC, this threat to weaponize the '384 patent undermines the U.S. semiconductor supply chain, harming priorities that this Administration has made clear are vital to U.S. economic interests and national security. Ex. 1119, 3; Ex. 1120, 1. This makes *inter partes* review of the '384 patent an appropriate use of the Office's resources—indeed a compelling one. TSMC's FinFET fabrication capabilities are vital to leading U.S. companies (such as Apple, NVIDIA, and Amazon). More specifically, TSMC's FinFET technology at the accused 5 nm processing node supports U.S. advanced semiconductor research and development in industries including AI, health care, and

national security and defense. Ex. 1127, 18-19. Promoting these emerging industries is an important step in advancing the Administration's priorities. Ex. 1119, 3; Ex. 1120, 1. The threat proposed to these industries by Marlin's litigation tactics make this IPR an appropriate and efficient use of the Office's resources and expertise.

Indeed, the U.S. government has recognized the importance of AI to the national security, and TSMC is an important part of the American AI-dominance strategy. Ex. 1114; 1115. For example, TSMC "produces the advanced processors that Nvidia [], AMD [] and Apple [] rely on to bring AI to life," including, NVIDIA's next-generation Blackwell AI chips for NVIDIA's AI supercomputers. Ex. 1125, 2. Moreover, healthcare is a key area of projected growth in the AI semiconductor market, where the demand for "advanced chips—TSMC's specialty—will continue to surge." Ex. 1126, 5. Blocking or burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing "direct effects on future patient care" and "far-reaching consequences" for the development of life-saving medical technology. *Id.*

Marlin does not dispute the serious impact a ban on importing FinFET products into the United States would have to vital U.S. national security, public health, or economic interests. Instead, Marlin sets of a strawman—painting itself as protector of local industries. Paper-6, 10-11. The facts belie Marlin's pronouncement. Marlin does not practice the '384 patent, nor any patent it holds.

There is no evidence that Marlin, a foreign entity, has invested in the U.S. semiconductor technology space, except by trying to assert its recently acquired patents. Given Marlin's targeting of Intel for a license (Ex. 2104) and Marlin's assertion of its patents against U.S.-based companies (e.g., Apple, Qualcomm, Broadcom), Marlin's arguments that it is a protector of "local industry" ring hollow.

Finally, trying to cast TSMC as a "foreign entity" that "import[s] infringing products" and must be protected against twists the facts beyond recognition. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Ahern, that any product of TSMC infringes any patent in Marlin's portfolio, including the '384 patent. Additionally, Marlin ignores TSMC's commitment to invest \$165 billion in build manufacturing facilities in the United States in support of this Administration's goal to onshore advanced semiconductor manufacturing to bolster U.S. economic and national security interests. Ex. 1119, 3. Indeed, TSMC's Arizona facilities are already producing 4nm chips for American customers. Ex. 1128, 2. Marlin's enforcement campaign against TSMC seeks to damage the core supply chain of semiconductor chips from TSMC to the United States. National security, economic, and public interest considerations therefore warrant referral.

Dated: October 17, 2025

Respectfully submitted,

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*Lead Counsel for Petitioner*

**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that a copy of the foregoing opposition, including all Exhibits, was served on October 17, 2025 via email delivery directed to the attorneys of record for Patent Owner.

Date: October 17, 2025

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