Google Patents 104241360

Semiconductor device and manufacturing method thereof

Abstract

The invention discloses a semiconductor device and a manufacturing method thereof. The semiconductor device includes a fin-shaped protrusion structure, an insulation structure, a gate structure, and an epitaxial structure. The fin-shaped protrusion extends out of the surface of the substrate and has a top surface and two side surfaces. An insulating structure surrounds the fin-shaped protrusion structure. The gate structure covers the top surface and the two side surfaces of part of the fin-shaped protrusion structure and covers part of the insulation structure. The insulating structure under the gate structure has a first top surface, the insulating structures on both sides of the gate structure have a second top surface, and the first top surface is higher than the second top surface. The epitaxial structure is arranged on one side of the gate structure and directly contacts the fin-shaped protrusion structure.

Classifications

H10D30/62 Fin field-effect transistors [FinFET]

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Inventor: 洪裕祥, 傅思逸, 张仲甫, 陈正国, 林建廷

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Claims (19)

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translated from Chinese

1. A semiconductor device comprising: a fin-like protrusion structure extending from a surface of a substrate, wherein the fin-like protrusion structure has a top surface and two side surfaces; an insulating structure surrounding the fin-shaped protruding structure; The gate structure covers part of the top surface and the side surfaces of the fin-shaped protrusion structure, and covers part of the insulating structure, wherein the insulating structure located below the gate structure has a first top surface, and is located on the gate the insulating structure on both sides of the structure has a second top surface, and the first top surface is higher than the second top surface; and The epitaxial structure is disposed on one side of the gate structure and directly contacts the fin-shaped protrusion structure. 2. The semiconductor device according to claim 1, wherein a difference between the first top surface and the second top surface is between 100 angstroms and 250 angstroms. 3. The semiconductor device as claimed in claim 1, wherein the gate structure is a metal gate structure. 4. The semiconductor device according to claim 1, wherein the insulating structure under the gate structure has a sidewall, and the epitaxial structure directly contacts the sidewall. 5. The semiconductor device as claimed in claim 1, further comprising a groove formed at one end of the fin-shaped protrusion structure, wherein the epitaxial structure fills up the groove. 6. The semiconductor device as claimed in claim 5, wherein a bottom surface of the epitaxial structure is shallower than a bottom surface of the insulating structure. 7. The semiconductor device as claimed in claim 6, wherein a difference between the bottom surface of the epitaxial structure and the bottom surface of the insulating structure is between 100 angstroms and 250 angstroms. 8. The semiconductor device as claimed in claim 1, wherein the epitaxial structure comprises silicon germanium, silicon phosphorus or silicon phosphorus carbon. 9. The semiconductor device as claimed in claim 1, further comprising a spacer disposed on a sidewall of the gate structure. 10. The semiconductor device according to claim 1, further comprising: Another epitaxial structure is disposed on the other side of the gate structure and directly contacts the fin-shaped protrusion structure; The channel region is adjacent to the top surface and the side surfaces of the fin-like protrusion structure, and is located between the epitaxial structure and the other epitaxial structure. 11. A method of manufacturing a semiconductor device, comprising: forming a fin-like protrusion structure extending from a surface of a substrate, wherein the fin-like protrusion structure has a top surface and two side surfaces; forming an insulating structure surrounding the fin-shaped protruding structure; forming a gate structure, covering part of the top surface and the side surfaces of the protruding structure, and covering part of the insulating structure; etching the insulating structure exposed from the gate structure such that the top surface of the insulating structure reaches a first depth; forming a groove in the fin-like protrusion structure on one side of the gate structure; and An epitaxial structure is formed to fill the groove, wherein the bottom surface of the epitaxial structure has a second depth, and the second depth is deeper than the first depth. 12. The method of manufacturing a semiconductor device according to claim 11, wherein the insulating structure is a shallow trench isolation (STI). 13. The method of manufacturing a semiconductor device as claimed in claim 11, wherein the step of etching the insulating structure comprises wet etching or dry etching. 14. The method of manufacturing a semiconductor device as claimed in claim 11, wherein the gate structure is a dummy gate structure. 15. The method of manufacturing a semiconductor device as claimed in claim 11, wherein the step of forming the groove comprises wet etching or dry etching. 16. The method of manufacturing a semiconductor device as claimed in claim 11, wherein the epitaxial structure comprises silicon germanium, silicon phosphorus or silicon phosphorus carbon. 17 . The method of manufacturing a semiconductor device according to claim 11 , before etching the insulating structure, further comprising forming a spacer disposed on the sidewall of the gate structure. 18. The method of manufacturing a semiconductor device according to claim 17, wherein the step of forming the spacer comprises: Depositing a material layer over the entire surface to cover the gate structure and the fin-shaped protrusion structure in the direction; and The material layer is etched until the insulating structure is exposed. 19. The manufacturing method of a semiconductor device as claimed in claim 11, further comprising: depositing an interlayer dielectric layer to surround the gate structure; removing the gate structure to leave a trench; forming a gate dielectric layer to conformally cover the sidewalls and bottom of the trench; and A conductive layer is formed to fill up the trench.

Description

translated from Chinese

Semiconductor device and manufacturing method thereof

technical field

The invention relates to a semiconductor device, in particular to a semiconductor device with an epitaxial structure and a manufacturing method thereof.

Background technique

With the development of the semiconductor industry, the performance of switching speed and operating voltage of semiconductor devices has achieved significant progress. Therefore, the industry has increasingly stringent performance requirements for Metal-Oxide-Semiconductor Field Effect Transistor (MOS FET), bicarrier transistors and other transistor components. For current MOS transistors, increasing carrier mobility to increase the speed of MOS transistors has become a major issue in the field of semiconductor technology.

In order to achieve the above purpose, the industry has developed the so-called "strained silicon (strained-silicon) technology". The mobility of the channel increases, thereby achieving the purpose of making the MOS transistor operate faster. Among the currently known technologies, there are MOS transistors using strained silicon as a substrate, which utilizes the lattice constant of silicon germanium (SiGe) or silicon carbon (SiC) which is different from that of single crystal Si (single crystal Si) The characteristics of silicon germanium epitaxial layer or silicon carbon epitaxial layer produce structural strain to form strained silicon. Since the lattice constant of the silicon-germanium epitaxial layer or the silicon-carbon epitaxial layer is larger or smaller than that of silicon, this changes the band structure of silicon, which increases the mobility of carriers, thus increasing the MOS Transistor speed.

However, as the scale of semiconductor devices continues to shrink, the aspect ratio of the epitaxial layer also increases, resulting in unnecessary defects, such as void defects, often formed inside the epitaxial layer, thereby affecting the value of its stress. Therefore, how to prevent unnecessary defects in the epitaxial layer has become an important issue.

Contents of the invention

In view of this, an object of the present invention is to provide a semiconductor device with an epitaxial layer to increase the stress value applied to the channel region.

According to a preferred embodiment of the present invention, a semiconductor device is provided. The semiconductor device includes a fin-shaped protrusion structure, an insulating structure, a gate structure, and an epitaxial structure. The fin-shaped protruding structure extends out of the surface of the substrate and has a top surface and two side surfaces. The insulating structure surrounds the fin-shaped protruding structure. The gate structure covers part of the top surface and two side surfaces of the fin-shaped protrusion structure, and covers part of the insulating structure. The insulating structure located below the gate structure has a first top surface, and the insulating structures located on both sides of the gate structure have a second top surface, and the first top surface is higher than the second top surface. The epitaxial structure is disposed on one side of the gate structure and directly contacts the fin-like protrusion structure.

According to another preferred embodiment of the present invention, a method for fabricating a semiconductor device is provided, at least including the following steps. Firstly, a fin-like protrusion structure is formed, extending from a surface of a substrate, wherein the fin-like protrusion structure has a top surface and two side surfaces. Next, an insulating structure is formed to surround the protruding fin structure. A gate structure is then formed to cover part of the top surface and two side surfaces of the protruding structure, and cover part of the insulating structure. Etching exposes the insulating structure of the gate structure so that the top surface of the insulating structure reaches a first depth. Then a groove is formed in the fin-like protrusion structure on one side of the gate structure. Finally, an epitaxial structure is formed to fill the groove, wherein the bottom surface of the epitaxial structure has a second depth, and the second depth is deeper than the first depth.

The feature of the present invention is to provide a semiconductor device with an epitaxial structure (or called an epitaxial layer) and its manufacturing method. Since the insulating structures on both sides of the gate structure are selectively etched before and/or after forming the groove, the The height of the insulating structures on both sides of the groove is improved, so that the epitaxial structure can be easily filled in the groove during the epitaxial growth process, and there will be no cavity defects caused by early sealing.

Description of drawings

1 to 11 are schematic diagrams of a method for manufacturing a semiconductor device according to a preferred embodiment of the present invention, wherein:

1 illustrates a perspective view of a semiconductor device at an initial stage;

2 illustrates a perspective view of a semiconductor device after forming a gate structure;

3 illustrates a perspective view of a semiconductor device after forming a spacer;

Fig. 4 is a schematic cross-sectional view along the section line A-A' of Fig. 3;

5 illustrates a perspective view of a semiconductor device after etching an insulating structure;

6 illustrates a perspective view of the semiconductor device after etching the fin-shaped protrusion structure;

Fig. 7 is a schematic cross-sectional view along line A-A' of Fig. 6;

Fig. 8 is a schematic cross-sectional view along the section line B-B' in Fig. 6;

9 illustrates a perspective view of a semiconductor device after forming an epitaxial structure;

Figure 10 is a schematic cross-sectional view along the section line A-A' in Figure 9; and

Fig. 11 is a schematic cross-sectional view along line B-B' in Fig. 9 .

Symbol Description

Detailed ways

Hereinafter, specific implementations of the semiconductor device and its manufacturing method of the present invention are set forth, so that those skilled in the art can implement the present invention accordingly. For these specific implementation manners, reference may be made to corresponding drawings, so that these drawings

constitute a part of the implementation manners. Although the embodiments of the present invention are disclosed as follows, they are not intended to limit the present invention. Those skilled in the art may make some modifications and modifications without departing from the spirit and scope of the present invention.

1 to 11 are diagrams illustrating a method for fabricating a semiconductor device according to a preferred embodiment of the present invention. Please refer to FIG. 1 , which illustrates a perspective view of a semiconductor device at an initial stage. As shown in Figure 1, a substrate 10 is first provided, which can be, for example, a silicon substrate, a silicon-containing substrate, a silicon-on-silicon substrate of Group III and V semiconductors (such as GaAs-on-silicon), or a graphene silicon-on-silicon substrate (graphene -on-silicon) and other semiconductor substrates. Preferably, the substrate 10 does not include a silicon-on-insulator (SOI) substrate. Still as shown in FIG. 1 , a plurality of fin-like protrusion structures 12 are disposed on the substrate 10 . In detail, the method for preparing the above-mentioned fin-shaped protrusion structure 12 may include the following steps, but is not limited thereto. Firstly, a block substrate (not shown) is provided, a hard mask layer (not shown) is formed thereon, and it is patterned to define corresponding fins to be formed in the block substrate below. The position of the protruding structure 12. Next, an etching process is performed to form the fin-shaped protrusion structure 12 in the bulk substrate. In this way, the fabrication procedure of the fin-shaped protrusion structure 12 is completed. In this case, the fin-like protrusion structures 12 can be regarded as extending from a surface 10 a of the substrate 10 , and have the same composition as each other, such as single crystal silicon. On the other hand, when the substrate is not selected from the above-mentioned bulk substrate, but is selected from the III-V semiconductor silicon-coated substrate, the main composition of the fin-like protrusion structure will be different from the underlying substrate.

In this embodiment, the hard mask layer (not shown) may be selectively removed after the fin-like protrusion structure 12 is formed, so that there may be three direct contact surfaces between the fin-like protrusion structure 12 and the subsequently formed dielectric layer. (Contains two contact sides and one contact top surface). Therefore, a field effect transistor with such three direct contact surfaces is also called a tri-gate field effect transistor (tri-gate MOSFET). Compared with the planar field effect transistor, the tri-gate field effect transistor can have a wider carrier channel width under the same gate length by using the above three direct contact surfaces as the carrier flow channel, resulting in Double the drain drive current can be obtained under the same drive voltage. In addition, this embodiment can also keep the hard mask layer (not shown), and form another multi-gate field effect transistor (multi-gate MOSFET) with a fin structure in the subsequent manufacturing process - fin field Effect transistor (fin field effect transistor, Fin FET). In the FinFET, since the hard mask layer (not shown) remains, there are only two contact sides between the fin-like protrusion structure 12 and the dielectric layer to be formed later.

Please refer to FIG. 2 , which illustrates a perspective view of the semiconductor device after the gate structure is formed. An insulating structure 20 is formed on the substrate 10 between the fin-like protrusion structures 12 to electrically insulate the transistors formed subsequently, so as to form the insulating structure 20 shown in FIG. 2 . At this time, the lower portion of each fin-like protrusion structure 12 will be embedded in the insulating structure 20 , so that each fin-like protrusion structure 12 outside the insulating structure 20 will have a first height H1 . The insulating structure 20 is, for example, a shallow trench isolation (STI) structure, which is formed by, for example, a shallow trench isolation manufacturing process. The detailed formation method is well known to those skilled in the art, so it will not be described in detail, but the present invention This is not the limit.

Next, as shown in FIG. 2, a gate dielectric layer (not shown), a sacrificial electrode layer (not shown) and a capping layer (not shown) are sequentially formed from bottom to top to cover the substrate 10 and Fin-shaped protrusion structure 12. Subsequently, the capping layer (not shown), the sacrificial electrode layer (not shown) and the gate dielectric layer (not shown) are patterned to form a gate dielectric layer (not shown), a sacrificial The electrode layer 32 and a capping layer 38 are on the substrate 10 and the fin-like protrusion structure 12 . The gate dielectric layer, the sacrificial electrode layer 32 and the capping layer 38 can form a gate structure 30 to straddle the fin-like protrusion structures 12 and cover the insulating structure 20 between each fin-like protrusion structures 12 . According to this embodiment, the gate structure 30 straddles the two fin-shaped protrusion structures 12 to form a structure as shown in FIG. 2 . Specifically, the gate structure 30 covers part of the top surface 14 and two side surfaces 16 of each fin-like protrusion structure 12 , and covers part of the top surface 22 of the insulating structure 20 . In addition, the gate structure 30 preferably extends along a first direction X, and the fin-shaped protrusion structure 12 preferably extends along a second direction Y and protrudes from the substrate 10 along a third direction Z. The first direction X, the second direction Y and the third direction Z are orthogonal to each other, but not limited thereto.

In order to disclose the present invention clearly, only a single gate structure 30 is shown in FIGS. 2-11 , but the number thereof can also be increased according to different product requirements. For example, more than one gate structure parallel to each other can be disposed on the substrate, so that the same fin-like protrusion structure can be covered by more than one gate structure. In addition, the same gate structure 30 is preferably used as a gate of a transistor of the same conductivity type, such as a gate of a PMOS transistor or a gate of an NMOS transistor.

In this embodiment, a gate-last for high-k last (Gate-Last for High-K Last) manufacturing process is taken as an example, so the gate structure 30 can also be regarded as a dummy gate structure.). In other words, the gate dielectric layer will be replaced by a high-k gate dielectric layer in subsequent manufacturing processes, and the sacrificial electrode layer 32 will be replaced by a conductive metal layer. In this embodiment, the gate dielectric layer may only be a sacrificial material, such as an oxide layer, which is generally convenient to be removed in a subsequent manufacturing process. The composition of the sacrificial electrode layer 32 may be polycrystalline semiconductor material, such as polycrystalline silicon, but not limited thereto. The capping layer may include a single-layer or multi-layer structure composed of a nitride layer or an oxide layer, etc., as a patterned hard mask. In this embodiment, the cover layer 38 is a double-layer structure, which may include a bottom layer 34 and a top layer 36 from bottom to top, and the bottom layer 34 is, for example, a nitride layer, and the top layer 36 may be, for example, an oxide layer, This is not the limit.

The above is an introduction to the implementation of the post-high dielectric constant last gate manufacturing process, but this embodiment is not limited to this, it can also use a pre-high dielectric constant last gate (Gate-Last for High-K First)Craftsmanship. In this aspect, the gate dielectric layer can be a high dielectric constant gate dielectric layer, which can be selected from hafnium oxide (HfO_2), hafnium silicate ($HfSiO_4$) , hafnium silicon oxynitride (HfSiON), aluminum oxide (aluminum oxide, Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (tantalum oxide, Ta_2O_5), Yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate ($SrTiO_3$), zirconium silicate ($ZrSiO_4$), hafnium zirconate (hafniumzirconate , $HfZrO_4$), strontium bismuth tantalate ($SrBi_2Ta_2O_9$, SBT), lead zirconate titanate ($PbZr_xTi_{1-x}O_3$, PZT) and barium strontium titanate (bariumstrontium titanate, $BaxSr_{1-x}TiO_3$, BST), but the present invention is not limited thereto. In addition, a barrier layer (not shown) can be formed on the gate dielectric layer, which is used as an etch stop layer to protect the gate dielectric layer when removing the sacrificial electrode layer, and prevent subsequent The metal components diffuse down to contaminate the gate dielectric layer. The aforementioned barrier layer (not shown) may be, for example, a single-layer structure or a composite-layer structure of tantalum nitride (TaN), titanium nitride (TiN) and the like.

Please refer to FIG. 3 and FIG. 4 , wherein FIG. 4 is a schematic cross-sectional view along the section line A-A' in FIG. 3 . After forming the above-mentioned gate structure, as shown in FIGS. 3 and 4 , a spacer 40 can be formed on one sidewall of the gate structure 30 to define the position of the epitaxial structure to be formed subsequently. The spacer 40 in this embodiment is preferably formed on each side of the gate structure 30 , and the bottom thereof will cover part of the top surface 22 of the insulating structure 20 . In detail, the method for forming the spacer 40 may be, for example, first depositing a material layer (not shown) in the direction direction on the gate structure 30 and the substrate 10 , and then performing an etching process to form the spacer 40 . The structure of the spacer 40 may include a single-layer structure or a multi-layer structure, such as a single-layer structure composed of silicon nitride, silicon oxynitride, etc., or a double-layer structure composed of silicon oxide/silicon nitride, etc., but This is not the limit. The spacer 40 referred to in this embodiment is a spacer used to define and form an epitaxial structure, so before or after the formation of the spacer 40, other thinner spacers may be formed to form lightly doped source/drain An electrode region (not shown) or another thicker spacer is formed to form a source/drain region (not shown). In order to simplify and clearly disclose the present invention, FIGS. 3-11 only show the spacer 40 for forming the epitaxial structure.

Please refer to FIG. 5 , which illustrates a perspective view of the semiconductor device after etching the insulating structure. After forming the above-mentioned spacer 40, the insulating structure 20 not covered by the gate structure 30 and the spacer 40 can be further etched, so that the top surface 22 of part of the insulating structure 20 is lowered to a predetermined depth (or called a first depth D1), And form the structure as shown in FIG. 5 . In detail, a first etching process 42 , such as a wet etching process or a dry etching process, can be used to selectively remove the insulating structure 20 without removing the gate structure 30 and the fin-like protrusion structure 12 . In this way, in addition to exposing a portion of the sidewall 24 of the insulating structure 20 directly below the gate structure 30 and the spacer 40 , the portion originally embedded in the insulating structure 20 and in direct contact with the insulating structure 20 will also be exposed. Fin-shaped protrusion structure 12. At this time, the insulating structure 20 directly below the gate structure 30 and the spacer 40 has a higher first top surface 22a, while the insulating structure 20 not covered by the gate structure 30 has a lower first top surface 22a. There are two top surfaces 22b with a height difference H2 therebetween. For example, the height difference may be between 100 angstroms and 250 angstroms, preferably 150 angstroms, but not limited thereto.

Please refer to FIGS. 6 to 8. FIG. 6 shows a perspective view of the semiconductor device after etching the fin-shaped protrusion structure. FIG. 7 is a schematic cross-sectional view along the line AA' in FIG. FIG. 6 is a schematic cross-sectional view shown by section line BB'. As shown in FIGS. 6 to 8 , a second etching process 46 can be performed under the cover of the gate structure 30 and the spacer 40 to etch the fin-shaped protrusion structure 12 and the fins on at least one side of the gate structure 30 A groove 60 is formed in the protruding structure 12 . Further, in this embodiment, a groove 60 is formed in the fin-like protrusion structures 12 on both sides of the gate structure 30 , and the bottom surface 68 of the groove 60 is preferably not deeper than the bottom surface 26 of the insulating structure 20 . Specifically, as shown in FIG. 7 and FIG. 8 , there will be a difference between the bottom surface 68 of the groove and the top surface 14 of the original fin-shaped protrusion structure 12, which is equal to the first height H1 plus the second depth D2; and The top surface 22 of the insulating structure 20 located on both sides of the gate structure 30 is reduced by a value compared with that before the second etching process 46 , and the value is equal to the first depth D1 . Further, the second depth D2 is greater (or called deeper) than the first depth D1.

Furthermore, the above-mentioned etching may include at least one dry etching step or/and at least one wet etching step, for example, first etching the substrate 10 to a predetermined depth with a dry etching step, and then laterally etching with a wet etching step to form the desired The profile of the groove 60, but not limited thereto. In this embodiment, a section of the groove 60 has a concave section structure, but it is not limited thereto, and the groove 60 may have a different section structure according to actual needs. In addition, in this embodiment, a wet cleaning process (not shown) may be optionally performed to clean the surface of the etched groove 60 . The wet cleaning process may be, for example, a process containing dilute hydrofluoric acid (DHF), but the invention is not limited thereto.

It should be noted here that the manufacturing process timing of etching the insulating structure 20 not covered by the gate structure 30 and the spacer 40 and the manufacturing process timing of etching the fin-like protrusion structure 12 may be reversed. Specifically, in this embodiment, the fin-like protrusion structure 12 exposed from the gate structure 30 and the spacer 40 may be etched first, and then the insulating structure 20 not covered by the gate structure 30 and the spacer 40 is etched. In other words, since a feature of the present invention is to reduce the gap between the bottom surface 68 of the groove 60 and the top surface 22 of the insulating structure 20 on both sides of the gate structure 30 by etching the insulating structure 20, no matter what the etching sequence is, it can be achieve the desired purpose of this invention.

Please refer to FIGS. 9 to 11, wherein FIG. 9 shows a perspective view of a semiconductor device after forming an epitaxial structure, FIG. 10 is a schematic cross-sectional view along the line AA' in FIG. 9, and FIG. 9 is a schematic cross-sectional view drawn by section line BB'. As shown in Figures 9 to 11, an epitaxial growth process is performed, such as a molecular beam epitaxy (MBE), a co-flow epitaxial growth process (co-flow epitaxial growth process), a cycle selectivity An epitaxial structure 66 is formed in the corresponding groove 60 by the epitaxial growth process (cyclic selective epitaxial growth process) or other similar epitaxial process. Specifically, each epitaxial structure 66 can completely cover the bottom surface 68 and the sidewall 70 of the corresponding groove 60 . Furthermore, the composition of the epitaxial structure 66 can be varied according to semiconductor devices of different conductivity types, so that it can apply proper stress to the channel region adjacent to the top surface 14 and two side surfaces 16 of the fin-like protrusion structure 12 . For example, for a P-type semiconductor device, the epitaxial structure 66 is preferably a SiGe layer with or without dopants to provide a compressive stress to the channel region. Moreover, the epitaxial structure 66 may also have a cladding structure with different concentrations from the inside to the outside or/and from the bottom to the top. For example, the epitaxial structure may include, from bottom to top, epitaxial silicon, at least one epitaxial silicon germanium layer with relatively low germanium concentration, at least one epitaxial silicon germanium layer with relatively high germanium concentration, and an epitaxial silicon layer, and so on. On the other hand, for an N-type semiconductor device, the epitaxial structure 66 is preferably silicon-phosphorous (SiP), silicon-carbon (SiC), phosphorus-doped silicon-carbon, etc., so as to provide a tensile stress to the channel region. .

Furthermore, no matter what the composition of the epitaxial structure 66 is, since the gap between the bottom surface 68 of the groove 60 and the top surface 22b of the insulating structure 20 on both sides of the gate structure 30 can be reduced through the above etching process, during the epitaxy process, the epitaxial The structure 66 is less likely to be blocked by the insulating structure 22b to seal early and generate hole defects. In other words, a feature of the present invention is that by etching the insulating structures 20 on both sides of the gate structure 30 , the epitaxial structure 66 can maintain a desired height (or called depth) without generating hole defects. Therefore, the epitaxial structure can provide the stress required for the carrier channel, thereby effectively improving the carrier mobility.

After the above epitaxial structure is formed, a subsequent semiconductor manufacturing process, such as a post-metal gate replacement process with high dielectric constant, can be optionally performed to replace the gate structure 12 made of polysilicon with a metal gate structure. The manufacturing process may include: (1) depositing an interlayer dielectric layer to surround the gate structure; (2) removing the gate structure to leave a trench; (3) forming a gate dielectric layer, and (4) forming a conductive layer to fill up the trench. Afterwards, a contact plug manufacturing process is performed to form a contact plug electrically connected to the epitaxial structure. Since the above manufacturing process steps are known to those skilled in the art, they will not be repeated here.

According to the above, a semiconductor device and a manufacturing method thereof according to a preferred embodiment of the present invention are completed. A variant embodiment of the above-mentioned embodiment will be further introduced below, and to simplify the description, the following description will mainly focus on the differences, and will not repeat the similarities. In addition, the same components in each embodiment are marked with the same reference numerals, so as to facilitate mutual comparison among the embodiments.

Please refer to Figure 3 and Figure 5 first. According to this variant embodiment, after the spacer 40 is formed, a first etching process 42 may also be performed to expose a part of the sidewall 24 of the insulating structure 20 directly below the gate structure 30 and the spacer 40, and expose Part of the fin-shaped protrusion structure 12 that is originally embedded in the insulating structure 20 and directly contacts with the insulating structure 20 is exposed. Afterwards, different from the above-mentioned embodiment, this variant embodiment does not perform the second etching process, so no groove is formed in the fin-shaped protrusion structure 12 . Finally, as shown in FIG. 9 , an epitaxial growth process can be performed to form an epitaxial structure 66 on the surface of the fin-shaped protrusion structure 12 . Subsequent manufacturing processes are similar to the above-mentioned embodiments, and will not be repeated here. In this variant embodiment, part of the insulating structure 20 is removed first, so that the epitaxial structure 66 can effectively apply stress to the corresponding channel region.

It should be noted here that, for the sake of brevity, the above embodiments mainly use non-planar field effect transistors as targets of the present invention. However, the spirit of the present invention can also be applied to planar field effect transistors. Specifically, the gate structure can be used to cover a planar active region and part of the insulating structure, and the active region and the insulating structure on both sides of the gate structure are etched successively, and finally the epitaxial growth process is performed. Similarly, by etching the insulating structures on both sides of the gate structure, the subsequent epitaxial structure can obtain the required height

(or depth) without generating hole defects. Therefore, the epitaxial structure can provide the stress required for the planar carrier channel, thereby effectively improving the carrier mobility.

In summary, the present invention provides a semiconductor device structure and a manufacturing method thereof. By etching the insulating structures on both sides of the gate structure and selectively forming grooves, the gap between the bottom of the groove and the top of the insulating structures on both sides of the gate structure can be reduced. In the subsequent epitaxial process, the epitaxial structure is less likely to be blocked by the insulating structure, and the hole defects are sealed early, so it can provide the stress required for the carrier channel, thereby effectively improving the carrier mobility.

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CN102832236A *	2011-06-16	2012-12-19	台湾积体电路制造股份有限公司	Strained channel field effect transistor
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Family To Family Citations				

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US10784344B2	2017-09-28	2020-09-22	Samsung Electronics Co., Ltd.	Semiconductor devices and methods of manufacturing the same
Family To Family Citations				

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CN105845546B	2019-11-05	Epitaxial manufacturing process of illumination
CN104078363A	2014-10-01	Semiconductor device manufacturing method
CN103107139A	2013-05-15	Structure of field effect transistor with fin structure and manufacturing method thereof
TWI518790B	2016-01-21	Semiconductor device and method of making the same
TW201448120A	2014-12-16	Semiconductor device and fabrication method thereof
TWI528460B	2016-04-01	Method for fabricating field effect transistor with fin structure

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
CN201310252818.8A	2013-06-24	2013-06-24	Semiconductor device and method for fabricating the same

Applications Claiming Priority (1)

Application	Filing date	Title
CN201310252818.8A	2013-06-24	Semiconductor device and method for fabricating the same

Legal Events

Date	Code	Title	Description
2014-12-24	C06	Publication	
2014-12-24	PB01	Publication	
2016-06-15	C10	Entry into substantive examination	
2016-06-15	SE01	Entry into force of request for substantive examination	
2019-07-23	GR01	Patent grant	
2019-07-23	GR01	Patent grant	

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match
semiconductor		title,claims,abstract,description	58	0.000
manufacturing process		title,claims,abstract,description	31	0.000
substrate		claims,abstract,description	30	0.000
layer		claims,description	71	0.000
etching		claims,description	26	0.000
spacer group		claims,description	25	0.000
Silicon-germanium		claims,description	9	0.000
[Si].[Ge]		claims,description	7	0.000
dry etching		claims,description	5	0.000
material		claims,description	5	0.000
metal		claims,description	5	0.000

Concept	Sections	Count	Score
metal	claims,description	5	0.000
wet etching	claims,description	5	0.000
deposition	claims,description	4	0.000
isolation	claims,description	3	0.000
interlayer	claims,description	2	0.000
[P].[C].[Si]	claims	2	0.000
[Si].[P]	claims	2	0.000
insulation	abstract	2	0.000

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