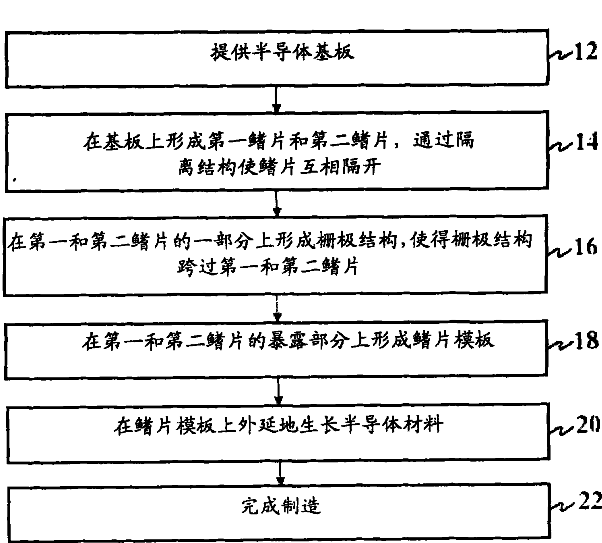
Google Patents 102468235

Fin-like field effect transistor (finfet) device and method of manufacturing same

Abstract

translated from Chinese

A FinFET device and method of fabricating the FinFET device are disclosed. An exemplary method includes providing a semiconductor substrate; forming a first fin structure and a second fin structure on the semiconductor substrate; forming a gate structure on a portion of the first fin structure and the second fin structure, such that the gate structure spans the through the first fin structure and the second fin structure; epitaxially growing the first semiconductor material on exposed portions of the first fin structure and the second fin structure, such that the first fin structure and the second fin structure the exposed portions are merged together; and epitaxially growing a second semiconductor material on the first semiconductor material.



CN102468235A

China

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Other languages: Chinese

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Worldwide applications

2010 • US 2011 • CN 2015 • US

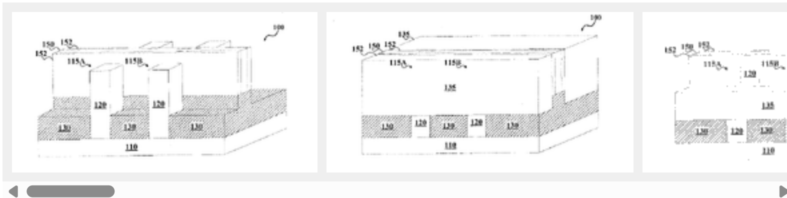
Application CN2011103243389A events

- 2011-10-19 • Application filed by Taiwan Semiconductor Manufacturing Co TSMC Ltd
- 2012-05-23 • Publication of CN102468235A
- 2014-05-28 • Application granted
- 2014-05-28 • Publication of CN102468235B
- Status • Active
- 2031-10-19 • Anticipated expiration

Info: Patent citations (22), Cited by (84), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Images (23)



Classifications

H10D84/834 Integrated devices formed in or on semiconductor substrates that comprise only semiconducting layers, e.g. on Si wafers or on GaAs-on-Si wafers characterised by the integration of at least one component covered by groups H10D12/00 or H10D30/00, e.g. integration of IGFETs of only field-effect components of only insulated-gate FETs [IGFET] comprising FinFETs

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Landscapes

Insulated Gate Type Field-Effect Transistor

Thin Film Transistor

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Claims (10)

Hide Dependent ^
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1. A method comprising: Provide semiconductor substrates; forming a plurality of fins on the semiconductor substrate, and isolating the fins from each other through an isolation structure; forming a gate structure on a portion of each fin such that the gate structure spans the plurality of fins; forming a fin template on the exposed portion of the fin; and A semiconductor material is grown epitaxially (epi) on the fin template. 2. The method of claim 1, wherein forming the fin templates includes epitaxially growing other semiconductor material on exposed portions of each of the fins such that the fins merge together. 3. The method of claim 2, further comprising etching back the isolation structure before forming the fin template. 4. The method of claim 3, further comprising: forming spacers on sidewalls of the gate structure; and Wherein etching back the isolation structure includes using an etching process that selectively etches the isolation structure. 5. The method of claim 2, wherein: epitaxially growing the semiconductor material on exposed portions of the fins includes epitaxially growing silicon; and Epitaxially growing the semiconductor material on the fin template includes epitaxially growing silicon germanium. 6. The method of claim 1, further comprising etching back the fin template prior to epitaxially growing the semiconductor material on the fin template. 7. The method of claim 6, wherein: the gate structure separates a source region and a drain region of each of the fins, the source region and the drain region of each fin defining a channel therebetween; and Etching back the fin template includes exposing a portion of the channel of each fin. 8. The method of claim 1, wherein forming the plurality of fins comprises forming fins having a first material portion and a second material portion, each of the fins comprising a gate structure separated by the gate structure. A source region and a drain region of each fin define a channel therebetween. 9. A method comprising: Provide semiconductor substrates; forming a first fin structure and a second fin structure on the semiconductor substrate; forming a gate structure over a portion of the first fin structure and the second fin structure such that the gate structure straddles the first fin structure and the second fin structure; epitaxially growing a first semiconductor material on exposed portions of the first fin structure and the second fin structure such that the exposed portions of the first fin structure and the second fin structure merge together; as well as A second semiconductor material is epitaxially grown on the first semiconductor material. 10. An integrated circuit device comprising: semiconductor substrate; a first fin and a second fin disposed on the semiconductor substrate; an isolation structure disposed between the first fin and the second fin such that the first fin and the second fin are isolated from each other; a gate structure positioned over a portion of the first fin and the second fin, the gate structure straddling the first fin and the second fin, thereby separating the first source and drain regions of the fin and said second fin; a first epitaxial semiconductor layer disposed on another portion of the first fin and the second fin; and a second epitaxial semiconductor layer disposed on the first epitaxial semiconductor layer, wherein the source region and the drain region of the first fin and the second fin comprise the first epitaxial semiconductor layer layer and a portion of the second epitaxial semiconductor layer.

Description

translated from Chinese

Fin field effect transistor (FINFET) device and method of manufacturing the same

Cross References to Related Applications

This disclosure is related to commonly-assigned U.S. Patent Application entitled Fin Field Effect Transistor (FINFET) Device and Method of Making Same, filed October 18, 2010, Attorney Docket No. 2010-0693/24061.1546, the entire contents of which are incorporated by reference Incorporated herein by reference.

technical field

Disclosed are a FinFET device and a method for manufacturing the FinFET device, and more particularly, the invention relates to a Fin Field Effect Transistor (FINFET) device and a method for manufacturing the same.

Background technique

As the semiconductor industry advances to nanotechnology process nodes in pursuit of high device density, high performance, and lower cost, manufacturing and design challenges have led to the development of three-dimensional designs such as fin field-effect transistors (FinFETs). Typical FinFETs are fabricated with thin "fins" (or fin structures) extending from a substrate, such as thin "fins" etched into the silicon layer of the substrate. The channel of a FinFET is formed in the vertical fins. The gate is provided on (or wound) the fin. It is advantageous to have gates on both sides of the channel so that the gates control the channel from both sides of the channel. FinFET devices also include stressed source/drain features to increase carrier mobility and improve device performance. Strained source/drain features typically use epitaxial (epi) silicon germanium (SiGe) in p-channel devices and epitaxial silicon (Si) in n-channel devices. FinFET devices offer many advantages, including reduced short channel effects and increased current flow. While existing FinFET devices and methods of fabricating FinFET devices have been generally adequate for their intended purposes, as devices continue to scale down, existing FinFET devices and methods of fabricating FinFET devices have been less than fully satisfactory in all respects.

Contents of the invention

Aiming at the problems in the prior art, the present invention provides a method. The method includes: providing a semiconductor substrate; forming a plurality of fins on the semiconductor substrate, and isolating the fins from each other through an isolation structure; forming a gate structure on a part of each fin, so that the gate structure spans A plurality of fins; forming a fin template on exposed portions of the fins; and epitaxially (epi) growing a semiconductor material on the fin template.

The method according to the present invention, wherein forming the fin template includes epitaxially growing other semiconductor material on the exposed portion of each of the fins, so that the fins are merged together.

The method according to the present invention further includes etching back the isolation structure before forming the fin template.

The method according to the present invention further includes: forming a spacer on a sidewall of the gate structure; and wherein etching back the isolation structure includes using an etching process for selectively etching the isolation structure.

The method of the present invention, wherein: epitaxially growing the semiconductor material on the exposed portion of the fin includes epitaxially growing silicon; and epitaxially growing the semiconductor material on the fin template includes epitaxially growing silicon germanium .

The method according to the present invention further includes etching back the fin template before epitaxially growing the semiconductor material on the fin template.

According to the method of the present invention, wherein: the gate structure separates the source region and the drain region of each fin, the source region and the drain region of each fin are defined between the channels of the fins; and etching back the fins includes exposing a portion of the channels of each fin.

The method of the present invention, wherein forming the plurality of fins includes forming fins having a first material portion and a second material portion, each of the fins including a source region separated by the gate structure and drain regions, the source and drain regions of each fin define a channel therebetween.

The method according to the present invention further includes completely removing the second material portion from the source region and the drain region of the fin before forming the fin template.

The method according to the present invention further includes removing the second material portion from source region and drain region portions of the fin prior to forming the fin template.

A method according to the present invention includes: providing a semiconductor substrate; forming a first fin structure and a second fin structure located on the semiconductor substrate; forming a fin structure located on the first fin structure and the second fin structure. a gate structure on a portion of the fin structure such that the gate structure straddles the first fin structure and the second fin structure; between the first fin structure and the second fin structure epitaxially growing a first semiconductor material on exposed portions of the structure such that exposed portions of the first fin structure and the second fin structure merge together; and epitaxially growing a second semiconductor material on the first semiconductor material .

The method according to the present invention further includes: forming an isolation structure between the first fin structure and the second fin structure, so that the first fin structure and the second fin structure isolating each other; and etching back said isolation structures prior to epitaxially growing said first semiconductor material.

The method according to the present invention further includes etching back the first semiconductor material before epitaxially growing the second semiconductor material.

The method according to the present invention, wherein: epitaxially growing the first semiconductor material includes epitaxially growing silicon; and epitaxially growing the second semiconductor material includes epitaxially growing silicon germanium.

The method according to the present invention further includes removing a portion of the first fin structure and the second fin structure before epitaxially growing the first semiconductor material.

The method according to the present invention, wherein: the first fin and the second fin comprise a first material portion and a second material portion, each of the first fin and the second fin having a source region and a drain region separated by the gate structure, the source region and the drain region of each fin defining a channel therebetween; and removing the portion of the first The fin and the second fin include completely removing portions of the second material from source and drain regions of the first fin and the second fin.

The method according to the present invention, wherein: the first fin and the second fin comprise a first material portion and a second material portion, each of the first fin and the second fin having a source region and a drain region separated by the gate structure, the source region and the drain region of each fin defining a channel therebetween; and removing the portion of the first The fin and the second fin include partially removing the second material portion from source and drain regions of the first fin and the second fin.

An integrated circuit device according to the present invention, comprising: a semiconductor substrate; a first fin and a second fin disposed on the semiconductor substrate; a fin disposed on the first fin and the second fin The isolation structure between the first fin and the second fin is isolated from each other; the gate structure placed on a part of the first fin and the second fin, the gate structure across the first fin and the second fin, thereby separating the source region and the drain region of the first fin and the second fin; disposed between the first fin and the second fin a first epitaxial semiconductor layer on another part of the second fin; and a second epitaxial semiconductor layer disposed on the first epitaxial semiconductor layer, wherein the first fin and the second fin The source and drain regions include a portion of the first epitaxial semiconductor layer and the second epitaxial semiconductor layer.

An integrated circuit device according to the present invention, wherein the source region and the drain region of each of the first fin and the second fin define a channel therebetween, the channel and the The first epitaxial semiconductor layer is in contact with the second epitaxial semiconductor layer.

The integrated circuit device of the present invention, wherein: the first and second fins comprise silicon; the first epitaxial semiconductor layer comprises silicon; and the second epitaxial semiconductor layer comprises silicon germanium.

Description of drawings

The present invention is better understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various components may be arbitrarily increased or decreased for clarity of discussion.

FIG. 1 is a flowchart illustrating a method of fabricating a Fin Field Effect Transistor (FinFET) device, according to various aspects of the present disclosure.

2-6 are perspective views illustrating a FinFET device at various stages of fabrication according to the method of FIG. 1 .

7 is a flowchart illustrating another method of fabricating a FinFET device in accordance with various aspects of the present disclosure.

8A , 9A, 10A and 11A are perspective views showing a FinFET device at various stages of fabrication according to the method of FIG. 7 .

8B, 9B, 10B, and 11B are schematic cross-sectional views of the FinFET devices shown in FIGS. 8A, 9A, 10A, and 11A, respectively.

8C, 9C, 10C, and 11C are schematic cross-sectional views of the FinFET devices shown in FIGS. 8A, 9A, 10A, and 11A, respectively.

12 is a flowchart illustrating yet another method of fabricating a FinFET device in accordance with various aspects of the present disclosure.

13A , 14A, 15A and 16A are perspective views of a FinFET device at various stages of fabrication according to the method of FIG. 12 .

Figures 13B, 14B, 15B and 16B are schematic cross-sectional views of the FinFET devices shown in Figures 13A, 14A, 15A and 16A, respectively.

13C, 14C, 15C, and 16C are schematic cross-sectional views of the FinFET devices shown in FIGS. 13A, 14A, 15A, and 16A, respectively.

Detailed ways

The following disclosure provides many different embodiments, or examples, for implementing different elements of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are of course examples only and are not intended to be limiting. For example, the following description of a first component being formed on a second component may include embodiments in which the first and second components are formed in direct contact, and may also include embodiments in which additional components are formed between the first and second components Between embodiments such that the first and second components are not in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in various embodiments. This repetition is for brevity only and does not in itself dictate a relationship between the various embodiments and/or structures discussed.

FIG. 1 is a flowchart of a method 10 of fabricating an integrated circuit device according to various embodiments of the present disclosure. In the illustrated embodiment, method 10 fabricates integrated circuit devices including fin field effect transistor (FinFET) devices. Method 10 begins at block 12 where a semiconductor substrate is provided. In block 14, a first fin and a second fin are formed on the semiconductor substrate. An isolation structure is formed to isolate the first and second fins. In block

16, a gate structure is formed on a portion of the first and second fins. A gate structure spans the first and second fins. In block 18, a fin template is formed on the exposed portions of the first and second fins. In block 20, semiconductor material is epitaxially grown on the fin template. Method 10 continues to block 22 where fabrication of the integrated circuit device is complete. Steps may be added before, during, and after method 10, and some of the described steps may be replaced or deleted for other embodiments of the method. The following discussion illustrates various embodiments of integrated circuit devices that may be fabricated according to method 10 of FIG. 1 .

2-6 provide various perspective views (partial or full) of FinFET device 100 at various stages of fabrication according to method 10 of FIG. 1 . The term FinFET device refers to any fin-based transistor, such as a fin multi-gate transistor. FinFET device 100 may be included in a microprocessor, a memory cell, and/or an integrated circuit device. 2-6 are simplified for clarity to better understand the inventive concept of the present disclosure. Additional components may be added to the FinFET device 100 , and some components described below may be replaced or deleted in other FinFET device 100 embodiments.

Referring to FIG. 2 , a FinFET device 100 includes a substrate (wafer) 110 . In the depicted embodiment, the substrate 110 is a bulk silicon substrate. Alternatively or additionally, the substrate 110 includes elemental semiconductors such as silicon or germanium in a crystalline structure; compound semiconductors such as silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; or combination. Alternatively, the substrate 110 is a silicon-on-insulator (SOI) substrate. The SOI substrate may be fabricated using isolation by implantation of oxygen (SIMOX), wafer bonding, and/or other suitable methods. Substrate 110 may include various doped regions and other suitable features.

FinFET device 100 includes fin structures 115A and 115B extending from substrate 110 . In the depicted embodiment, fin structures 115A and 115B include fins 120 . The fin 120 includes silicon (Si), and thus the fin 120 is also referred to as a Si fin. Fin structures 115A and 115B also include other material portions. Fin 120 includes a source region, a drain region, and a channel between the source and drain regions. The fins 120 are formed by performing photolithography and etching processes. Starting, for example, with substrate 110 , photolithography and etching processes form trenches in substrate 110 to form fins 120 extending from substrate 110 . The photolithography process may include photoresist coating (such as spin coating), soft baking, mask alignment, exposing, post-exposure baking, photoresist development, rinsing, drying (such as hard baking), other suitable processes or combinations thereof. For example, the fin portion 120 may be formed by blanket forming a photoresist layer (photoresist) on the substrate 110, exposing the photoresist to a pattern, performing a post-exposure bake process, and developing the photoresist to form a mask member including the photoresist. . The fins 120 may then be etched into the silicon substrate 110 using masking elements. The etching process can be a dry etching process, a wet etching process, other suitable etching processes, or a combination thereof. For example, the fins 120 may be etched into the substrate 110 using reactive ion etching (RIE). Alternatively, a photolithography process may be implemented or replaced by other methods, such as maskless lithography, electron beam writing, ion beam writing, and/or nanoimprinting techniques. The fin 120 may be formed through a double patterning lithography (DPL) process. DPL is a method of dividing a pattern into two staggered patterns to construct a pattern on a substrate. DPL allows for increased component (eg fin) density. Various DPL methods may be used including double exposure (eg, using two mask sets), forming spacers adjacent features and removing features to provide a spacer pattern, antifreeze, and/or other suitable processes. It should be noted that in the described embodiments the term “fin structure” refers to a single fin of FinFET device 100 . However, the term "fin structure" may also refer to all fins, and thus a fin structure may also refer to fin structures 115A and 115B as a whole. Further, although the embodiment shows two fins, the FinFET device 100 may also include fewer or more fins, depending on the design requirements of the FinFET device 100 .

Isolation features 130, such as shallow trench isolation (STI) structures, surrounding fin structures 115A and 115B (fin 120 in the illustrated embodiment) isolate fins 120 from each other and from other unillustrated integrated circuits. device isolation. Isolation features 130 are formed by partially filling trenches surrounding fins 120 with an insulating material such as silicon oxide, silicon nitride, silicon oxynitride, other suitable materials, or combinations thereof. The filled trench may have a multilayer structure, such as a thermal oxide liner layer filling the trench with silicon nitride. In the depicted embodiment, the isolation feature 130 includes an oxide material.

FinFET device 100 includes a gate structure 150 . The gate structure 150 spans the fin 120 , and in the illustrated embodiment, the gate structure 150 is formed in a middle portion of the fin 120 . The gate structure 150 may include a gate dielectric layer and a gate electrode. The gate dielectric layer includes dielectric materials such as silicon oxide, high-k dielectric materials, other suitable dielectric materials, or combinations thereof. Examples of high-k dielectric materials include HfO_2 , HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconia, alumina, hafnium dioxide-alumina (HfO_2 - Al_2O_3) alloys, other suitable high-k k Dielectric material or combination thereof. The gate electrode comprises polysilicon and/or metals comprising Al, Cu, Ti, Ta, W, Mo, TaN, Ni Si, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, other conductive materials, or combination. The gate structure 150 such as a gate electrode may be formed in a gate-first or gate-last process. The gate structure 150 may include many other layers such as cap layers, interfacial layers, diffusion layers, barrier layers, hard mask layers, or combinations thereof.

The gate structure 150 is formed by a suitable process such as deposition, photolithographic patterning and etching process. Deposition processes include chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), high-density plasma CVD (HDCVD), metal-organic CVD (MOCVD), remote plasma CVD (RPCVD), plasma Enhanced CVD (PECVD), low pressure CVD (LPCVD), atomic layer CVD (ALCVD), atmospheric pressure CVD (APCVD), electroplating, other suitable methods, or combinations thereof. Photolithographic patterning processes include photoresist coating (e.g. spin coating), soft bake, mask alignment, exposure, post exposure bake, photoresist development, cleaning, drying (e.g. hard bake), other suitable processes, or its combination. Alternatively, the photolithographic exposure process may be implemented or replaced by other methods such as maskless lithography, electron beam writing or ion beam writing. In yet another alternative embodiment, the photolithographic patterning process may implement nanoimprinting techniques. The etching process includes dry etching, wet etching and/or other etching methods.

Spacers 152 are placed on sidewalls of the gate structure 150 such as along the gate electrodes. The spacer 152 includes a dielectric material such as silicon oxide, silicon nitride, silicon oxynitride, other suitable materials, or combinations thereof. The spacer may include a multilayer structure such as a multilayer structure including a silicon nitride layer and a silicon oxide layer. The spacer is formed to a suitable thickness by a suitable process. For example, in the illustrated embodiment, the spacers 152 may be formed by depositing a silicon nitride layer and then dry etching the silicon nitride layer to form the spacers 152 shown in FIG. 2 . Before or after forming the spacers 152 , implantation, diffusion, and/or annealing processes may be performed to form lightly doped source and drain (LDD) features in the source and drain regions of the fin structures 115A and 115B.

Referring to FIG. 3 , a certain process is performed to form a recess on the isolation member 130 . For example, an etching process is performed to form a concave shape on the isolation part 130 . The etching process is a dry etching process, a wet etching process, other etching processes or a combination thereof. In the depicted embodiment, the etch process selectively etches the isolation features 130 and implements processing parameters that avoid etching the silicon nitride spacers 152 . For example, in the described embodiments, the etching process uses a hydrofluoric acid (HF) etching solution at a suitable concentration (eg, 100:1). In an embodiment, the HF solution forms the isolation member 130 into a concave shape of about 100 angstroms. Alternatively, other etching solutions may be used to effectively concave the isolation member 130 .

Referring to FIG. 4 , a fin template 135 is formed on the exposed portion of the fin 120 . For example, fin template 135 is formed by merging fins 120 of FinFET device 100 . In the depicted embodiment, fins 120 are incorporated together by epitaxially (epitaxially) growing semiconductor material on exposed portions of fins 120 in the source and drain regions of fin structures 115A and 115B. The semiconductor material is epitaxially grown by an epitaxial process until the fins 120 of the fin structures 115A and 115B are merged together to form a fin template 135 . The epitaxial process may use CVD deposition techniques such as vapor phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD), molecular beam epitaxy, and/or other suitable processes. Epitaxy processes can use gaseous and/or liquid precursors. In the illustrated embodiment, the fin template 135 may be silicon formed by a silicon epitaxial deposition process. The fin template 135 may be referred to as a bulk silicon-like template.

Alternatively, the fin template 135 may be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. The fin template 135 may be doped during deposition (growth) by adding impurities to the original material of the epitaxial process or in a deposition growth process in which impurities are subsequently added to the fin template 135 by an ion implantation process. For example, phosphorus can be doped into the epitaxial silicon fin template 135 (to form a Si:P epitaxial layer). A doped epitaxial layer may have a graded doping profile. A chemical mechanical polishing (CMP) process may be performed to planarize the fin template 135 . While fin 120 and fin template 135 are described separately, it should be understood that "fin template" may refer to only newly grown epitaxial semiconductor material (depicted as fin template 135) or newly grown epitaxial semiconductor material in combination with the original fin. (depicted as fins 120).

Referring to FIG. 5 , a process is performed to form recesses on the fin template 135 . For example, an etch process is performed on the fin template 135 to etch back the fin template 135 . The etching process is a dry etching process, a wet etching process, other etching processes or a combination thereof. In an example, the etching process uses a mixture of HBr, Cl_2 and O_2 . Alternatively, other etch process mixtures may be used to effectively recess the fin template 135 . The radio frequency (RF) bias power for the etch process may be from about 30 watts (W) to about 400 watts (W). Fin template 135 is effectively etched back exposing the channels of fin structures 115A and 115B as shown in FIG. 5 . This ensures that the subsequently formed raised source and drain features (semiconductor material 160) can effectively introduce stress into the channels of fin structures 115A and 115B.

Referring to FIG. 6 , semiconductor material 160 is epitaxially grown on fin template 135 . In the illustrated embodiment, the semiconductor material is epitaxially grown on the exposed fin template 135 in the source and drain regions of the fin structures 115A and 115B. Epitaxially grown semiconductor material 160 creates channel stress for fin structures 115A and 115B. The epitaxial process may use CVD deposition techniques (such as vapor phase epitaxy (VPE)) and/or ultra-high vacuum CVD (UHV-CVD), molecular beam epitaxy, and/or other suitable processes. Epitaxy processes can use gaseous and/or liquid precursors. In the illustrated embodiment, semiconductor material 160 is silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. Alternatively, the semiconductor material 160 may be silicon formed by a silicon epitaxial deposition process. The semiconductor material 160 may be doped during the deposition (growth) process by adding impurities to the original material in the epitaxy process or in the growth process of the semiconductor material 160 by adding impurities to the semiconductor material 160 later by the ion implantation process. A CMP process may be performed to planarize the semiconductor material 160 . Semiconductor material 160 may be referred to as raised source and drain features of the source and drain regions of fin structures 115A and 115B. It should be noted that the fin template 135 in the source and drain regions of the fin structures 115A and 115B may also be considered as part of the raised source and drain features. Before or after forming semiconductor material 160 , implantation, diffusion, and/or annealing processes may be performed to form heavily doped source and drain (HDD) features in the source and drain regions of fin structures 115A and 115B.

Conventional FinFET devices form raised source and drain features (eg, semiconductor material 160) on unmerged fins, such as fin 120 shown in FIG. 2 . As technology nodes continue to scale down, the width of unmerged fins such as fin 120 continues to decrease, eg, to about 15 nm and lower. It has been observed that raised source and drain features grown on the exposed surfaces of the unmerged fins (eg, along the width of the unmerged fins) provide insufficient stress due to technology node downgrades. For example, the stress provided by raised source and drain features formed on an unmerged fin tends to relax along the width of the unmerged fin. These occur because of spacers (in other words, free space) between adjacent unmerged fins. As the stress (stress) relaxes across the fin width, defects and dislocations may occur in the raised source and drain features, negatively impacting device performance. Instead, the disclosed method 10 incorporates the fins 120 together to form the fin template 135 of the FinFET device 100 in order to address the inherent stress relaxation problems of conventional FinFET devices. Method 10 provides a self-aligned source/drain template growth scheme that can be easily implemented into integrated circuit processing and provides maximum raised source and drain features for ever-improving FinFET device performance. In particular, fin template 135 provides planar source and drain regions for forming raised source/drain features in the source and drain regions of fin structures 115A and 115B. This approach provides stress relaxation along the fin width and achieves planar channel stress. Thus the disclosed FinFET device 100 can provide maximum stress to the channels of the fin structures 115A and 115B with limited (or sometimes no) defects and/or dislocations.

FinFET device 100 may include additional features formed by subsequent processes. For example, suicide features may be formed in the source and drain regions of the fin structures 115A and 115B. The silicide features may be formed by a silicide process such as a self-aligned silicide (aligned silicide) process. Various contacts/vias/lines and multi-layer interconnection features such as metal layers and interlayer dielectrics are formed on the substrate 110 , and these features are configured to connect the various components or structures of the FinFET device 100 . Additional components may provide electrical connections to device 100 including gate structure 150 . For example, multilayer interconnects include vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. Various interconnect components may use various conductive materials including copper, tungsten and/or suicide. In one embodiment, the copper-related multilayer interconnect structure is formed using a damascene process and/or a dual damascene process.

FIG. 7 is a flowchart of a method 30 of fabricating an integrated circuit device according to various aspects of the present disclosure. In the depicted embodiment, method 30 fabricates integrated circuit devices including fin field effect transistor (FinFET) devices. Method 30 begins at block 32 where a semiconductor substrate is provided. In block 34, a first fin structure and a second fin structure are formed on the semiconductor substrate. More specifically, first material portions of the first and second fin structures are formed on the semiconductor substrate, and second material portions of the first and second fin structures are formed on the first material portion. In block 36, a gate structure is formed on a portion of the first and second fin structures. The gate structure spans the first and second fin structures, dividing the source and drain regions of the first and second fin structures. A channel is defined between the source and drain regions of the first and second fin structures. At block 38, the second material portion is completely removed from the source and drain regions of the first and second fin structures. At block 40, the first material portions of the source and drain regions of the first and second fin structures are bonded together to form a fin template. At block 42, a third material portion is formed on the fin template in the source and drain regions of the first and second fin structures. Method 30 continues to block 44 where fabrication of the integrated circuit device is complete. Additional steps may be provided before, during, and after method 30, and some of the above-described steps may be replaced or eliminated in other embodiments of the method.

8A-8C, 9A-9C, 10A-10C, and 11A-11C provide various views (partial or full) of FinFET device 200 at various stages of fabrication according to method 30 of FIG. The term FinFET device refers to any fin-based transistor such as a fin-based, multi-gate transistor. FinFET device 200 may be included in microprocessors, memory cells, and/or other integrated circuit devices. In the depicted embodiment, FinFET device 200 is a p-channel metal oxide semiconductor (PMOS) FinFET device. 8A-8C , 9A-9C , 10A-10C , and 11A-11C are simplified for clarity to better understand the inventive concepts of the present disclosure. Additional components may be added in FinFET device 200 , and some of the components described below may be replaced or deleted in other embodiments of FinFET device 200 .

FIG. 8A is a perspective view of a FinFET device 200, FIG. 8B is a schematic cross-sectional view of a FinFET device 200 taken along line 8B-8B in FIG. 8A , and FIG. 8C is taken along line 8C-8C in FIG. A schematic cross-sectional view of a FinFET device 200 taken away. FinFET device 200 includes a substrate (wafer) 210 . In the depicted embodiment, the substrate 210 is a bulk silicon substrate. Alternatively or additionally, substrate 210 includes elemental semiconductors, such as silicon or germanium in a crystalline structure; compound semiconductors, such as silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide ; or a combination thereof. Optionally, the substrate 210 is a silicon-on-insulator (SOI) substrate. The SOI substrate may be fabricated using isolation by implantation of oxygen (SIMOX), wafer bonding, and/or other suitable methods. Substrate 210 may include various doped regions and other suitable features.

FinFET device 200 includes fin structures 215A and 215B extending from substrate 210 . In the depicted embodiment, fin structures 215A and 215B include fin portions 220 and 230 . Fin portion 220 includes silicon (Si), and fin portion 230 includes silicon germanium (SiGe). The SiGe concentration of the fin portion 230 can be represented by $Si_{1-x}Ge_X$, where x represents the atomic percentage of the Ge composition. In the described embodiment, x is less than or equal to 1 and greater than or

equal to zero. 8C is a schematic cross-sectional view of FinFET device 200 taken along the channel of fin structure 215A, showing source region S and drain region D of fin structure 215A. A channel region C is defined between the source and drain regions. Fin structure 215B similarly includes source, drain and channel regions. It should be noted that the term "fin structure" in the described embodiments refers to a single fin of the FinFET device 200 . However, the term "fin structure" may also refer to fins in general, and thus, fin structures may also refer to fin structures 215A and 215B in general. Further, although the described embodiment shows two fins, the FinFET device 200 may include fewer or more fins, depending on the design requirements of the FinFET device 200 .

Fin structures 215A and 215B including fin portions 220 and 230 are formed by a suitable process. In one embodiment, fin structures 215A and 215B are formed by performing a photolithography and etching process to form fin portion 220 and performing an epitaxial growth process to form fin portion 230 . For example, starting from substrate 210 , photolithography and etching processes form trenches in substrate 210 to form fin portions 220 (referred to as Si fin portions) of fin structures 215A and 215B extending from substrate 210 . The photolithography process may include photoresist coating (such as spin coating), soft baking, mask alignment, exposing, post-exposure baking, photoresist development, rinsing, drying (such as hard baking), other suitable processes or combinations thereof. For example, the fin portion 220 may be formed by forming a photoresist layer (photoresist) over the substrate 210, exposing the photoresist to a pattern, performing a post-exposure bake process, and developing the photoresist to form a mask member including the photoresist. . The fin portion 220 may then be etched into the silicon substrate 210 using a masking element. The etching process can be a dry etching process, a wet etching process, other suitable etching processes, or a combination thereof. For example, fin portion 220 may be etched into silicon substrate 210 using reactive ion etching (RIE). Alternatively, a photolithography process may be implemented or replaced by other methods, such as maskless lithography, electron beam writing, ion beam writing, and/or nanoimprinting techniques. The fin portion 220 may be formed through the DPL process as described above.

After the fin portion 220 is etched into the substrate 210 , an insulating layer may be formed on the substrate 210 including on the fin portion 220 . The insulating layer fills the trenches in the substrate 210 . A portion of the insulating layer is then removed to form an opening in the insulating layer exposing the top surface of the fin portion 220 . Semiconductor material may be epitaxially grown on exposed surfaces of fin portions 220 to form fin portions 230 of fin structures 215A and 215B. The epitaxial process may use CVD deposition techniques such as vapor phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD), molecular beam epitaxy, and/or other suitable processes. The epitaxy process may use gaseous and/or liquid precursors that interact with the components of the fin portion 220 (in other words, with the Si fin portion 220). In the depicted embodiment, fin portion 230 includes silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. Alternatively, fin portion 230 may comprise epitaxially grown silicon. The fin portion 230 may be doped during the deposition (growth) process by adding impurities to the original material of the epitaxial process or in the deposition growth process in which the fin portion 230 is subsequently added by an ion implantation process. For example, phosphorus can be doped into the epitaxial silicon fin portion (to form a Si:P epitaxial layer). A doped epitaxial layer may have a graded doping profile. A chemical mechanical polishing (CMP) process may be performed to planarize the fin portion 230 . Then, the remaining insulating layer is subjected to an etch-back process or a CMP process, thereby forming an isolation component (such as the isolation component 240).

In another example, fin structures 215A and 215B are formed by performing a photolithography and etching process to form fin portion 220 and a condensation process to form fin portion 230 . The condensation process may be implemented as described in US Patent Application Serial No. 12/702,862, entitled SiGeFinFET Notched Bottom by Condensation Method, filed February 9, 2010, the entire contents of which are incorporated herein by reference. For example, starting from substrate 210 , photolithography and etching processes form trenches in substrate 210 to form fin portions 220 (referred to as Si fin portions) of fin structures 215A and 215B extending from substrate 210 . Photolithography and etching processes are similar to those described above. Then, an insulating layer filling the trenches may be formed on the substrate 210 . An etch-back process may be performed on the insulating layer to form isolation features (eg, isolation features 240). A semiconductor material is then epitaxially grown on the exposed fin portion 220 . For example, SiGe is grown on the exposed fin portion 220 by an epitaxial process, similar to the epitaxial process described above. Then, the SiGe condensation process causes Ge from the SiGe material to diffuse into the fin portion 220 (Si fin) to form the fin portion 230 . An etch back process or a CMP process is then performed on the isolation features.

Isolation features 240 such as shallow trench isolation (STI) structures surrounding fin structures 215A and 215B isolate fin structures 215A and 215B from each other and from other unillustrated integrated circuit devices. Isolation feature 240 is formed by filling the trenches surrounding fin structures 215A and 215B with an insulating material such as silicon oxide, silicon nitride, silicon oxynitride, other suitable material portions, or combinations thereof. The filled trench may have a multilayer structure, such as a thermal oxide liner layer filling the trench with silicon nitride.

FinFET device 200 includes a gate structure 250 . Gate structure 250 spans fin structures 215A and 215B, and in the depicted embodiment, gate structure 250 is formed in the middle of fin structures 215A and 215B. Gate structure 250 may include a gate dielectric layer and a gate electrode. The gate dielectric layer includes dielectric materials such as silicon oxide, high-k dielectric materials, other suitable dielectric materials, or combinations thereof. Examples of high-k dielectric $_{\text{materials}}$ include $_{HfO2}$, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconia, alumina, hafnium dioxide-alumina ($_{HfO2}$ - $_{Al2O3}$) alloys, other suitable high-k k Dielectric material or combination thereof. The gate electrode comprises polysilicon and/or metals comprising Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, other conductive materials, or combinations thereof things. The gate structure 250 such as a gate electrode may be formed in a gate-first or gate-last process. The gate structure 250 may include many other layers such as cap layers, interfacial layers, diffusion layers, barrier layers, hard mask layers, or combinations thereof.

The gate structure 250 is formed by suitable processes such as deposition, photolithographic patterning and etching processes. Deposition processes include CVD, PVD, ALD, HDCVD, MOCVD, RPCVD, PECVD, LPCVD, ALCVD, APCVD, electroplating, other suitable methods, or combinations thereof. Photolithographic patterning processes include photoresist coating (e.g. spin coating), soft bake, mask alignment, exposure, post exposure bake, photoresist development, cleaning, drying (e.g. hard bake), other suitable processes, or its combination. Alternatively, the photolithographic exposure process may be implemented or replaced by other methods such as maskless lithography, electron beam writing or ion beam writing. In yet another alternative embodiment, the photolithographic patterning process may implement nanoimprinting techniques. The etching process includes dry etching, wet etching and/or other etching methods.

Spacers (not shown) are placed on the sidewalls of the gate structure 250 such as along the gate electrodes. The spacer is similar to the spacer 152 described above with respect to FIG. 2 . For example, spacer 152 includes a dielectric material such as silicon oxide, silicon nitride, silicon oxynitride, other suitable materials, or combinations thereof. The spacer may include a multilayer structure such as a multilayer structure including a silicon nitride layer and a silicon oxide layer. The spacer is formed to a suitable thickness by a suitable process. For example, the spacers may be formed by depositing layers of silicon nitride and silicon oxide, and then dry etching the layers to form the spacers. Before or after forming the spacers, implantation, diffusion, and/or annealing processes may be performed to form LDD features in the source and drain regions of the fin structures 215A and 215B.

FIG. 9A is a perspective view of a FinFET device 200, FIG. 9B is a schematic cross-sectional view of a FinFET device 200 taken along line 9B-9B in FIG. 9A , and FIG. 9C is taken along line 9C-9C in FIG. 9A. A schematic cross-sectional view of a FinFET device 200 taken away. In FIGS. 9A-9C , fin portion 230 is completely removed from the source and drain regions of fin structures 215A and 215B. More specifically, the etching process completely removes fin portion 230 from the source and drain regions of fin structures 215A and 215B thereby exposing fin portion 220 . The etching process is a dry etching process, a wet etching process, other etching processes or a combination thereof. In an embodiment, the etching process uses a mixture of HBr, Cl_2 and O_2 . Alternatively, other etch process mixtures may be used to effectively remove fin portion 230 . The radio frequency (RF) bias power for the etch process may be from about 30 watts (W) to about 400 watts (W). Photolithography and etching processes may be performed to provide a protective layer over various components of FinFET device 200 (eg, gate structure 250 and/or isolation features 240) so that the protected components are not affected by the etching process. As shown in FIG. 9C , fin portion 230 defined by gate structure 250 remains in the channel of fin

structures 215A and 215B. The removed fin portions 230 form channels in the source and drain regions of the fin structures 215A and 215B. The channel sidewalls may be defined by fin portion 220 , isolation features 240 , remaining fin portion 230 in the channel region, and/or a protective layer (if formed). In the depicted embodiment, the depth (d_1) of the trench extends from the initial top surface of the fin portion 230 to the exposed top surface of the fin portion 220 . If a protective layer is provided, d_1 may extend from the top surface of the protective layer to the exposed top surface of the fin portion 220 . Other methods of determining trench depth may also be used.

10A is a perspective view of a FinFET device 200, FIG. 10B is a schematic cross-sectional view of a FinFET device 200 taken along line 10B-10B in FIG. A schematic cross-sectional view of a FinFET device 200 taken away. In FIGS. 10A-10C , fin portions 220 in the source and drain regions of fin structures 215A and 215B are merged together to form fin template 280 . For example, fin template 280 may be formed by a process similar to that described above with respect to FIG. 5 . In the depicted embodiment, semiconductor material is epitaxially (epitaxially) grown on exposed fin portions 220 of the source and drain regions until fin portions 220 of fin structures 215A and 215B merge together to form fin template 280 . The epitaxial process may use CVD deposition techniques (eg, VPE and/or UHV-CVD), molecular beam epitaxy, and/or other suitable processes. Epitaxy processes can use gaseous and/or liquid precursors. In the depicted embodiment, the fin template 280 may be silicon formed by a silicon epitaxial deposition process. Alternatively, the fin template 280 may be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. The fin template 280 may be doped during the deposition (growth) process by adding impurities to the original material of the epitaxy process or in the deposition growth process in which the fin template 280 is subsequently added with an ion implantation process. For example, phosphorus can be doped into the epitaxial silicon fin template 280 (to form a Si:P epitaxial layer). A doped epitaxial layer may have a graded doping profile. A chemical mechanical polishing (CMP) process may be performed to planarize the fin template 280 . Although fin template 280 and fin portion 220 are described separately, it should be understood that "fin template" may refer to only newly grown epitaxial semiconductor material (depicted as fin template 280) or newly grown epitaxial semiconductor material in combination with the original fin. material (depicted as fins 220). Similar to fin template 135 described above with respect to FIGS. 2-6 , fin template 280 may minimize stress relaxation along the width of fin structures 215A and 215B, maximize stress on the channels of fin structures 215A and 215B and Improve device performance.

11A is a perspective view of a FinFET device 200, FIG. 11B is a schematic cross-sectional view of a FinFET device 200 taken along line 11B-11B in FIG. 11A , and FIG. A schematic cross-sectional view of a FinFET device 200 taken away. In FIGS. 11A-11C , fin portion 285 is formed on fin template 280 , providing fin structures 215A and 215B with fin portion 285 . For example, semiconductor material is grown epitaxially (epitaxially) on the fin template 285 . The epitaxial process may use CVD deposition techniques (eg, VPE and/or UHV-CVD), molecular beam epitaxy, and/or other suitable processes. The epitaxy process may use gaseous and/or liquid precursors that interact with components of the fin template 280 , in other words, with the Si fin template 280 . In the illustrated embodiment, the fin template 280 may be silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. The SiGe concentration of the fin portion 285 can be represented by $Si_{1-y}Ge_y$, where y represents the atomic percent of the Ge composition. In the described embodiment, y is less than or equal to 1 and greater than or equal to 0. The fin portion 285 may be doped during the deposition (growth) process by adding impurities to the original material for the epitaxial process or in a deposition growth process in which impurities are subsequently added to the fin portion 285 by an ion implantation process. A doped epitaxial layer may have a graded doping profile. A CMP process may be performed to planarize the fin portion 285 . Further, implantation, diffusion, and/or annealing processes may be performed to form HDD features in the source and drain regions of the fin structures 215A and 215B before or after the fin portion 285 is formed.

As shown in FIGS. 11A-11C , fin structures 215A and 215B include fin portion 220 , fin portion 230 , fin template 280 and fin portion 285 . More specifically, the source and drain regions of fin structures 215A and 215B include fin portion 220 , fin template 280 and fin portion 285 . The channel of fin structures 215A and 215B includes fin portion 220 and fin portion 230 . Fin templates 280 and/or fin portions 285 in the sources and drains of fin structures 215A and 215B optionally refer to stressed source and drain features of FinFET device 200 . In the depicted embodiment, fin portion 220 includes Si, fin template 280 includes Si, fin portion 230 includes $Si_{1-x}Ge_x$, and fin portion 285 includes $Si_{1-y}Ge_y$. Fin portion 285 provides compressive stress to the channels of fin structures 215A and 215B, thereby increasing hole mobility in PMOS FinFET device 200 . In the illustrated embodiment, y and x are independent of each other in the PMOS FinFET device 200 . Thus, fin portion 285 can include any Ge concentration and still achieve the compressive stress required for a PMOS FinFET device. By forming the fin portion 285 on the Si fin portion (fin template 280), the compressive stress is achieved independent of the SiGe concentration of the channel. For example, compressive stress from Si fin template 280 on $Si_{1-y}Ge_y$ fin portion 285 causes fin portion 285 to push/compress channel/fin portion 230, thereby providing uniaxial stress to the trench of FinFET device 200 road.

FinFET device 200 may include additional features that may be formed by subsequent processing. For example, suicide features may be formed in the source and drain regions of the fin structures 215A and 215B. The silicide features may be formed by a silicide process such as a self-aligned silicide (aligned silicide) process. Various contacts/vias/lines and multi-layer interconnection features such as metal layers and interlayer dielectrics are formed on the substrate 110 , and these features are configured to connect the various components or structures of the FinFET device 100 . Additional components may provide electrical connections to device 200 including gate structure 250 . For example, multilayer interconnects include vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. Various interconnect components may use various conductive materials including copper, tungsten and/or suicide. In one embodiment, the copper-related multilayer interconnect structure is formed using a damascene process and/or a dual damascene process.

FIG. 12 is a flowchart of a method 50 of fabricating an integrated circuit device according to various aspects of the present disclosure. In the depicted embodiment, method 50 fabricates integrated circuit devices including FinFET devices. Method 50 begins at block 52 where a semiconductor substrate is provided. In block 54, a first fin structure and a second fin structure are formed on the semiconductor substrate. More specifically, first material portions of the first and second fin structures are formed on the semiconductor substrate, and second material portions of the first and second fin structures are formed on the first material portion. In block 56, a gate structure is formed on a portion of the first and second fin structures. The gate structure spans the first and second fin structures, dividing the source and drain regions of the first and second fin structures. A channel is defined between the source and drain regions of the first and second fin structures. At block 58, the second material portion is partially removed from over the source and drain regions of the first and second fin structures. At block 60, remaining portions of the second material of the source and drain regions of the first and second fin structures are bonded together to form a fin template. At block 62, a third material portion is formed on the fin template in the source and drain regions of the first and second fin structures. Method 50 continues to block 64 where fabrication of the integrated circuit device is complete. Additional steps may be provided before, during, and after method 50, and some of the steps described above may be replaced or eliminated in other embodiments of the method.

13A-13C, 14A-14C, 15A-15C, and 16A-16C are various views (partial or full) of a FinFET device 400 at various stages of fabrication according to the method 50 of FIG. 12 . FinFET device 400 may be included in a microprocessor, memory cell, and/or other integrated circuit device. In the depicted embodiment, FinFET device 400 is an NMOS FinFET device. The FinFET devices 400 of FIGS. 13A-13C , 14A-14C, 15A-15C and 16A-16C are in many respects similar to those of FIGS. 8A-8C , 9A-9C, 10A-10C and The FinFET device 200 of FIGS. 11A-11C is similar. Therefore, for clarity and conciseness, the same reference numerals are used to identify FIGS. - Similar components in Figure 15C and Figures 16A-16C. 13A-13C, 14A-14C, 15A-15C, and 16A-16C are simplified for clarity to better understand the inventive concepts of the present disclosure. Additional components may be added to FinFET device 400 , and some of the components described below may be replaced or deleted in other embodiments of FinFET device 400 .

13A is a perspective view of a FinFET device 400, FIG. 13B is a schematic cross-sectional view of a FinFET device 400 taken along line 13B-13B in FIG. A schematic cross-sectional view of a FinFET device 400 taken away. FinFET device 400 includes substrate 210 , fin structures 215A and 215B including fin portions 220 and 230 , isolation feature 240 , and gate structure 250 . Fin structures 215A and 215B include a source, a drain, and a channel defined between the source and drain regions.

14A is a perspective view of a FinFET device 400, FIG. 14B is a schematic cross-sectional view of a FinFET device 400 taken along line 14B-14B in FIG. A schematic cross-sectional view of a FinFET device 400 taken away. In FIGS. 14A-14C , fin portion 230 is removed from the source and drain regions of fin structures 215A and 215B. In contrast to FinFET device 200 in FIGS. 9A-9C , in the depicted embodiment, the etch process partially removes fin portion 230 from the source and drain regions of fin structures 215A and 215B. The etching process is a dry etching process, a wet etching process, other etching processes or a combination thereof. In an example, the etching process uses a mixture of HBr, Cl_2 and O_2 . Alternatively, other etch process mixtures may be used to partially remove fin portion 230 . The radio frequency (RF) bias power for the etch process may be from about 30 watts (W) to about 400 watts (W). Photolithography and etching processes may be performed to provide a protective layer over various components of FinFET device 400 (eg, gate structure 250 and/or isolation features 240) so that the protected components are not affected by the etching process. As shown in FIG. 14C , fin portions 230 defined by gate structures 250 remain in the channels of fin structures 215A and 215B, and some fin portions 230 remain in the source and drain regions. The removed fin portions 230 form channels in the source and drain regions of the fin structures 215A and 215B. The channel sidewalls may be defined by the remaining fin portions 230 (in the source, drain, and channel regions), isolation features 240, and/or protective layers (if formed). In the depicted embodiment, the depth (d_2) of the trench extends from the initial top surface of the fin portion 230 to the exposed top surface of the fin portion 230 . If a protective layer is provided, d_2 may extend from the top surface of the protective layer to the exposed top surface of the fin portion 230 . Depth d_1 refers to the depth of the trenches in the source and drain regions of FinFET device 200 . Considering d_1 and d_2 , the trench (or groove) of FinFET device 200 is deeper than that of FinFET device 400 . As will be described below, the trench depth can be controlled to obtain various source and drain features for the fin structure, so that different kinds of channel pressure can be obtained for different FinFET devices.

15A is a perspective view of a FinFET device 400, FIG. 15B is a schematic cross-sectional view of a FinFET device 400 taken along line 15B-15B in FIG. A schematic cross-sectional view of a FinFET device 400 taken away. In FIGS. 15A-15C , fin portions 230 in the source and drain regions of fin structures 215A and 215B are merged together to form fin template 290 . For example, fin template 290 may be formed by a process similar to that described above with respect to FIGS. 10A-10C . In the depicted embodiment, semiconductor material is epitaxially (epitaxially) grown on the remaining fin portion 230 in the source and drain regions. The semiconductor material is epitaxially grown until fin portions 220 of fin structures 215A and 215B are merged together to form fin template 290 . Although the fin template 290 and the remaining fin portions 230 in the source and drain regions are depicted separately, "fin template" may refer to just the newly grown epitaxial semiconductor material (depicted as fin template 290) or to the original The newly grown epitaxial semiconductor material of the fin assembly (depicted as fin portion 230 remaining in the source and drain regions). The epitaxial process may use CVD deposition techniques (eg, VPE and/or UHV-CVD), molecular beam epitaxy, and/or other suitable processes. Epitaxy processes can use gaseous and/or liquid precursors. In the depicted embodiment, the fin template 290 includes silicon germanium (SiGe) formed by a silicon germanium epitaxial deposition process. Alternatively, fin template 290 may comprise epitaxially grown silicon. The fin template 290 may be doped during the deposition (growth) process by adding impurities to the original material of the epitaxy process or in the deposition growth process in which the fin template 290 is subsequently added with an ion implantation process. A doped epitaxial layer may have a graded doping profile. A CMP process may be performed to planarize the fin template 290 . While fin template 280 and fin portion 220 are described separately, similar to fin template 135 described above with respect to FIGS. 2-6 , fin template 290 can minimize stress relaxation along the width of fin structures 215A and 215B. , maximize the stress on the channels of the fin structures 215A and 215B and improve device performance.

16A is a perspective view of a FinFET device 400, FIG. 16B is a schematic cross-sectional view of a FinFET device 400 taken along line 16B-16B in FIG. A schematic cross-sectional view of a FinFET device 400 taken away. In FIGS. 16A-16C , fin portion 295 is formed on fin template 290 , providing fin structures 215A and 215B with fin portion 295 . For example, semiconductor material is grown epitaxially (epitaxially) on the fin template 290 . The epitaxial process may use CVD deposition techniques (eg, VPE and/or UHV-CVD), molecular beam epitaxy, and/or other suitable processes. Epitaxy processes can use gaseous and/or liquid precursors. In the depicted embodiment, fin portion 295 includes epitaxially grown SiGe. The SiGe concentration of the fin portion 295 can be represented by $Si_{1-z}Ge_z$, where z represents the atomic percent of the Ge composition. In such embodiments, z is less than or equal to 1 and greater than or equal to zero. Alternatively, fin portion 295 may comprise epitaxially grown Si. The fin portion 295 may be doped during the deposition (growth) process by adding impurities to the original material for the epitaxial process or in a deposition growth process in which impurities are subsequently added to the fin portion 295 by an ion implantation process. A doped epitaxial layer may have a graded doping profile. A CMP process may be performed to planarize the fin portion 295 . Further, implantation, diffusion, and/or annealing processes may be performed to form HDD features in the source and drain regions of the fin structures 215A and 215B before or after the fin portion 295 is formed.

As shown in FIGS. 16A-16C , fin structures 215A and 215B include fin portion 220 , fin portion 230 , fin template 290 , and fin portion 295 . More specifically, the source and drain regions of fin structures 215A and 215B include fin portions 220 , 230 , 290 and 295 . The channels of fin structures 215A and 215B include fin portions 220 and 230 . The fin portions 230 , 290 and/or 295 in the source and drain regions optionally refer to the stressed source and drain features of the FinFET device 400 . In the depicted embodiment, fin portion 220 includes Si, fin portions 230 and 290 include $Si_{1-x}Ge_x$, and fin portion 295 includes $Si_{1-z}Ge_z$, where z is less than x. Fin portions 230 , 290 , and 295 provide tensile stress to the channels of fin structures 215A and 215B, thereby providing electron mobility in the channel of NMOS FinFET device 400 .

FinFET device 400 may include additional features formed by subsequent processes. For example, suicide features may be formed in the source and drain regions of fin structures 215A and 215B, particularly on fin portion 295 . The silicide features may be formed by a silicide process such as a self-aligned silicide (aligned silicide) process. Various contacts/vias/lines and multi-layer interconnect features such as metal layers and interlayer dielectrics are formed on the substrate 210 and configured to connect the various components or structures of the FinFET device 400 . Additional components may provide electrical connections to device 400 including gate structure 250 . For example, multilayer interconnects include vertical interconnects, such as conventional vias or contacts, and horizontal interconnects, such as metal lines. Various interconnect components may use various conductive materials including copper, tungsten and/or suicide. In one embodiment, the copper-related multilayer interconnect structure is formed using a damascene process and/or a dual damascene process.

Accordingly, the present disclosure provides integrated circuit devices that exhibit maximum stress in their channels, and methods of fabricating integrated circuit devices with maximum stress. Maximum stress can be achieved by incorporating fin templates into integrated circuit devices. It should be understood that different embodiments may have different advantages, and that no one advantage is necessarily required by any embodiment. It should also be noted that FinFET device 100 , PMOS FinFET device 200 and/or NMOS FinFET device 400 may be fabricated in a single integrated circuit device using methods 10 , 30 , 50 described above. Referring to FinFET devices 200 and 400, by controlling the source and drain trench depths (eg d_1 and d_2) of the epitaxial source and drain features, stress can be obtained and optimized for both PMOS and NMOS FinFET devices. For example, as described above, fin portion 230 is completely removed from the source and drain regions of fin structures 215A and 215B in FinFET device 200 , while it is removed from the source and drain regions of fin structures 215A and 215B in FinFET device 400 . Fin portion 230 is partially removed from the drain region. This provides different starting substrates for forming the fin template, so that different types of stress can be obtained. Accordingly, the trench depth can be adjusted to independently optimize the performance of each FinFET device in the integrated circuit device. Further, fin templates in PMOS and NMOS FinFET devices can minimize stress relaxation along the width of the fin structure.

This disclosure provides many different embodiments. For example, the present disclosure provides methods of fabricating integrated circuit devices. In an embodiment, the method includes providing a semiconductor substrate; forming a plurality of fins on the semiconductor substrate, the fins are isolated from each other by an isolation structure; forming a gate structure on a portion of each fin, such that the gate structure spans multiple forming a fin template on the exposed portion of the fin; and epitaxially (epitaxially) growing semiconductor material on the fin template. Forming the fin templates may include epitaxially growing other semiconductor material on the exposed portions of each fin such that the fins merge together. The method may also include etching back the isolation structure prior to forming the fin template. The method also includes forming spacers on sidewalls of the gate structure. The etch back of the isolation structures may use an etch process that selectively etches

the isolation structures. In an example, epitaxially growing the semiconductor material on the exposed portion of the fin includes epitaxially growing silicon, and epitaxially growing the semiconductor material on the fin template includes epitaxially growing silicon germanium.

The method also includes etching back the fin template prior to epitaxially growing the semiconductor material on the fin template. In an example, a gate structure separates a source region and a drain region of each fin, wherein a channel is defined between the source and drain of each fin. Etching back the fin template may include exposing a portion of the channel of each fin. In an example, forming the plurality of fins includes forming fins having a first material portion and a second material portion, each fin including a source region and a drain region separated by a gate structure, wherein each fin has a The source and drain regions define a channel therebetween. The method may include completely removing portions of the second material from the source and drain regions of the fin prior to forming the fin template and/or partially removing the second material portion from the drain and source regions of the fin prior to forming the fin template. material part.

In another embodiment, a method includes providing a semiconductor substrate; forming a first fin structure and a second fin structure on the semiconductor substrate; forming a gate structure on a portion of the first fin structure and the second fin structure, making the gate structure straddle the first fin structure and the second fin structure; epitaxially growing the first semiconductor material on the exposed portions of the first fin structure and the second fin structure, so that the first fin structure and the second fin structure merging the exposed portions of the fin structure together; and epitaxially growing a second semiconductor material on the first semiconductor material. The method also includes forming an isolation structure between the first fin structure and the second fin structure such that the first fin structure and the second fin structure are isolated from each other, and etching back the isolation structure before epitaxially growing the first semiconductor material. The method also includes etching back the first semiconductor material prior to epitaxially growing the second semiconductor material. In an example, epitaxially growing the first semiconductor material includes epitaxially growing silicon, and epitaxially growing the second semiconductor material includes epitaxially growing silicon germanium. The method may include removing a portion of the first fin structure and the second fin structure prior to epitaxially growing the first semiconductor material. In an example, the first fin and the second fin include a first material portion and a second material portion, each of the first fin and the second fin having a source region and a drain separated by a gate structure region, and the source and drain regions of each fin define a channel therebetween. In this example, removing portions of the first and second fins may include completely removing portions of the second material from source and drain regions of the first and second fins and/or removing portions of the second material from the first and second fins. The portion of the second material is removed from the source and drain regions of the fin and the second fin.

Integrated circuit devices are formed by the methods described herein. In an embodiment, an integrated circuit device includes a semiconductor substrate; a first fin and a second fin disposed on the semiconductor substrate; an isolation structure disposed between the first fin and the second fin such that the first fin isolated from the second fin; a gate structure placed on a portion of the first fin and the second fin, the gate structure straddling the first fin and the second fin, thereby separating the first fin and the second fin the source and drain regions of the fin; the first epitaxial semiconductor layer placed on the other part of the first fin and the second fin; and the second epitaxial semiconductor layer placed on the first epitaxial semiconductor layer, wherein the first The source and drain regions of the fin and the second fin include a portion of the first epitaxial semiconductor layer and the second epitaxial semiconductor layer. The source and drain regions of each first and second fin define a channel therebetween. The channel may be in contact with the first epitaxial semiconductor layer and the second epitaxial semiconductor layer. In an example, the first fin and the second fin include silicon, the first epitaxial semiconductor layer includes silicon, and the second epitaxial semiconductor layer includes silicon germanium.

The components of several embodiments are discussed above so that those of ordinary skill in the art may better understand the various aspects of the invention. It should be understood by those skilled in the art that the present invention can be easily used as a basis to design or modify other processes and structures for achieving the same purpose and/or achieving the same advantages as the embodiments presented herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention, and that they could make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention.

Patent Citations (22)

Publication number	Priority date	Publication date	Assignee	Title
US7190050B2 *	2005-07-01	2007-03-13	Synopsys, Inc.	Integrated circuit on corrugated substrate
US20090101978A1 *	2007-10-17	2009-04-23	Anderson Brent A	Fin-type field effect transistor structure with merged source/drain silicide and method of forming the structure
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US6706571B1	2002-10-22	2004-03-16	Advanced Micro Devices, Inc.	Method for forming multiple structures in a semiconductor device
KR100513405B1	2003-12-16	2005-09-09	삼성전자주식회사	Method for forming fin field effect transistor
US7244640B2	2004-10-19	2007-07-17	Taiwan Semiconductor Manufacturing Company, Ltd.	Method for fabricating a body contact in a Finfet structure and a device including the same
US7265008B2	2005-07-01	2007-09-04	Synopsys, Inc.	Method of IC production using corrugated substrate
US7605449B2	2005-07-01	2009-10-20	Synopsys, Inc.	Enhanced segmented channel MOS transistor with high-permittivity dielectric isolation material
US8466490B2	2005-07-01	2013-06-18	Synopsys, Inc.	Enhanced segmented channel MOS transistor with multi layer regions
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US7898037B2	2007-04-18	2011-03-01	Taiwan Semiconductor Manufacturing Company, Ltd.	Contact scheme for MOSFETs

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US8883597B2	2007-07-31	2014-11-11	Taiwan Semiconductor Manufacturing Company, Ltd.	Method of fabrication of a FinFET element
US8283231B2	2008-06-11	2012-10-09	Taiwan Semiconductor Manufacturing Company, Ltd.	finFET drive strength modification
US7910453B2	2008-07-14	2011-03-22	Taiwan Semiconductor Manufacturing Company, Ltd.	Storage nitride encapsulation for non-planar sonos NAND flash charge retention
US8153493B2	2008-08-28	2012-04-10	Taiwan Semiconductor Manufacturing Company, Ltd.	FinFET process compatible native transistor
US7862962B2	2009-01-20	2011-01-04	Taiwan Semiconductor Manufacturing Company, Ltd.	Integrated circuit layout design
US7989355B2	2009-02-12	2011-08-02	Taiwan Semiconductor Manufacturing Company, Ltd.	Method of pitch halving
US8053299B2	2009-04-17	2011-11-08	Taiwan Semiconductor Manufacturing Company, Ltd.	Method of fabrication of a FinFET element
US9166022B2	2010-10-18	2015-10-20	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin-like field effect transistor (FinFET) device and method of manufacturing same

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CN103199010A *	2012-01-09	2013-07-10	台湾积体电路制造股份有限公司	FinFET and its method of formation
CN103515283A *	2012-06-25	2014-01-15	中国科学院微电子研究所	Semiconductor device manufacturing method
CN103515209A *	2012-06-19	2014-01-15	中芯国际集成电路制造(上海)有限公司	Fin field effect transistor and formation method thereof
CN103811325A *	2012-11-13	2014-05-21	中芯国际集成电路制造(上海)有限公司	Fin type field effect transistor forming method
CN103996709A *	2013-02-20	2014-08-20	台湾积体电路制造股份有限公司	Method for inducing strain in finfet channels
CN104241360A *	2013-06-24	2014-12-24	联华电子股份有限公司	Semiconductor device and manufacturing method thereof
CN104934468A *	2014-03-17	2015-09-23	中芯国际集成电路制造(上海)有限公司	Grid electrode and manufacturing method therefor
CN105047698A *	2014-03-26	2015-11-11	三星电子株式会社	Semiconductor device
CN108022842A *	2016-11-03	2018-05-11	联华电子股份有限公司	Semiconductor element and manufacturing method thereof
CN108231887A *	2016-12-21	2018-06-29	三星电子株式会社	Semiconductor devices
CN108389905A *	2017-02-03	2018-08-10	中芯国际集成电路制造(上海)有限公司	Semiconductor structure and forming method thereof
CN109003899A *	2017-06-06	2018-12-14	中芯国际集成电路制造(北京)有限公司	The forming method of semiconductor structure and forming method thereof, fin formula field effect transistor
CN109427670A *	2017-08-28	2019-03-05	台湾积体电路制造股份有限公司	The epitaxial structure and method that surrounding is wrapped up
US10411129B2	2014-03-26	2019-09-10	Samsung Electronics Co., Ltd.	Methods of fabricating semiconductor devices
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US8415718B2	2009-10-30	2013-04-09	Taiwan Semiconductor Manufacturing Company, Ltd.	Method of forming epi film in substrate trench
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US8942030B2	2010-06-25	2015-01-27	Taiwan Semiconductor Manufacturing Company, Ltd.	Structure and method for SRAM cell circuit
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US9130058B2	2010-07-26	2015-09-08	Taiwan Semiconductor Manufacturing Company, Ltd.	Forming crown active regions for FinFETs
US9166022B2	2010-10-18	2015-10-20	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin-like field effect transistor (FinFET) device and method of manufacturing same
US8367498B2 *	2010-10-18	2013-02-05	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin-like field effect transistor (FinFET) device and method of manufacturing same
US8633076B2	2010-11-23	2014-01-21	Taiwan Semiconductor Manufacturing Company, Ltd.	Method for adjusting fin width in integrated circuitry
US9472550B2	2010-11-23	2016-10-18	Taiwan Semiconductor Manufacturing Company, Ltd.	Adjusted fin width in integrated circuitry
US8796124B2	2011-10-25	2014-08-05	Taiwan Semiconductor Manufacturing Company, Ltd.	Doping method in 3D semiconductor device
US8759184B2	2012-01-09	2014-06-24	Taiwan Semiconductor Manufacturing Company, Ltd.	FinFETs and the methods for forming the same
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US8853037B2 *	2012-03-14	2014-10-07	GlobalFoundries, Inc.	Methods for fabricating integrated circuits
US8586455B1 *	2012-05-15	2013-11-19	International Business Machines Corporation	Preventing shorting of adjacent devices
US8669147B2	2012-06-11	2014-03-11	Globalfoundries Inc.	Methods of forming high mobility fin channels on three dimensional semiconductor devices
EP2682983B1 *	2012-07-03	2016-08-31	Imec	CMOS device comprising silicon and germanium and method for manufacturing thereof
US9142400B1	2012-07-17	2015-09-22	Stc.Unm	Method of making a heteroepitaxial layer on a seed area
US9728464B2	2012-07-27	2017-08-08	Intel Corporation	Self-aligned 3-D epitaxial structures for MOS device fabrication
CN103594512B *	2012-08-16	2017-09-05	中国科学院微电子研究所	Semiconductor device and manufacturing method thereof
US9082853B2	2012-10-31	2015-07-14	International Business Machines Corporation	Bulk finFET with punchthrough stopper region and method of fabrication
US9349837B2	2012-11-09	2016-05-24	Taiwan Semiconductor Manufacturing Company, Ltd.	Recessing STI to increase Fin height in Fin-first process
US9443962B2	2012-11-09	2016-09-13	Taiwan Semiconductor Manufacturing Company, Ltd.	Recessing STI to increase fin height in fin-first process
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US9006786B2 *	2013-07-03	2015-04-14	Taiwan Semiconductor Manufacturing Company, Ltd.	Fin structure of semiconductor device
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CN103117227B	2013-02-05	2015-11-25	华为技术有限公司	The preparation method of multiple-grid fin field effect pipe
US20140239395A1 *	2013-02-25	2014-08-28	International Business Machines Corporation	Contact resistance reduction in finfets
US9171952B2	2013-05-30	2015-10-27	Globalfoundries U.S. 2 Llc	Low gate-to-drain capacitance fully merged finFET
US9000498B2 *	2013-06-28	2015-04-07	Stmicroelectronics, Inc.	FinFET with multiple concentration percentages

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US9059002B2	2013-08-27	2015-06-16	International Business Machines Corporation	Non-merged epitaxially grown MOSFET devices
US8878300B1 *	2013-09-18	2014-11-04	Stmicroelectronics, Inc.	Semiconductor device including outwardly extending source and drain silicide contact regions and related methods
EP3050088A4	2013-09-25	2017-05-03	Intel Corporation	Isolation well doping with solid-state diffusion sources for finfet architectures
KR102175854B1 *	2013-11-14	2020-11-09	삼성전자주식회사	Semiconductor device and method of manufacturing the same
US9312273B2	2013-12-02	2016-04-12	International Business Machines Corporation	Structure and method to reduce crystal defects in epitaxial fin merge using nitride deposition
US9496282B2	2013-12-02	2016-11-15	International Business Machines Corporation	Structure and method to reduce crystal defects in epitaxial fin merge using nitride deposition
US9087900B1	2014-01-07	2015-07-21	Samsung Electronics Co., Ltd.	Semiconductor device and method for fabricating the same
KR102151768B1 *	2014-01-27	2020-09-03	삼성전자주식회사	Semiconductor device and method of manufacturing the same
US9525046B2 *	2014-03-17	2016-12-20	Semiconductor Manufacturing International (Shanghai) Corporation	Metal gate stack structure and manufacturing method
US9472572B2	2014-05-06	2016-10-18	Globalfoundries Inc.	Fin field effect transistor (finFET) device including a set of merged fins formed adjacent a set of unmerged fins
US10079283B2	2014-07-17	2018-09-18	E Ink Holdings Inc.	Manufacturing method of a transistor
EP3238264A4 *	2014-12-23	2018-08-22	Intel Corporation	Apparatus and methods of forming fin structures with sidewall liner
WO2016105412A1 *	2014-12-24	2016-06-30	Intel Corporation	Apparatus and methods of forming fin structures with asymmetric profile
US10032912B2 *	2014-12-31	2018-07-24	Stmicroelectronics, Inc.	Semiconductor integrated structure having an epitaxial SiGe layer extending from silicon-containing regions formed between segments of oxide regions
US9406529B1	2015-03-05	2016-08-02	International Business Machines Corporation	Formation of FinFET junction
US9954107B2	2015-05-05	2018-04-24	International Business Machines Corporation	Strained FinFET source drain isolation
KR102373622B1 *	2015-05-11	2022-03-11	삼성전자주식회사	Semiconductor device
US9754941B2	2015-06-03	2017-09-05	Globalfoundries Inc.	Method and structure to form tensile strained SiGe fins and compressive strained SiGe fins on a same substrate
US9548361B1	2015-06-30	2017-01-17	Stmicroelectronics, Inc.	Method of using a sacrificial gate structure to make a metal gate FinFET transistor
US9455331B1	2015-07-10	2016-09-27	International Business Machines Corporation	Method and structure of forming controllable unmerged epitaxial material
TWI655774B	2015-08-12	2019-04-01	聯華電子股份有限公司	Semiconductor device and method for fabricating the same
US9679899B2	2015-08-24	2017-06-13	Stmicroelectronics, Inc.	Co-integration of tensile silicon and compressive silicon germanium
US11222947B2	2015-09-25	2022-01-11	Intel Corporation	Methods of doping fin structures of non-planar transistor devices
CN106611787A *	2015-10-26	2017-05-03	联华电子股份有限公司	Semiconductor structure and manufacturing method thereof
US9449882B1	2015-10-29	2016-09-20	Taiwan Semiconductor Manufacturing Co., Ltd.	Semiconductor device and manufacturing method thereof
US9530669B1 *	2015-11-30	2016-12-27	International Business Machines Corporation	Method of making a semiconductor device having a semiconductor material on a relaxed semiconductor including replacing a strained, selective etchable material, with a low density dielectric in a cavity
TWI728966B *	2016-01-20	2021-06-01	聯華電子股份有限公司	Semiconductor device and method for fabricating the same
US10157748B2 *	2016-02-08	2018-12-18	Taiwan Semiconductor Manufacturing Co., Ltd.	Fin profile improvement for high performance transistor
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DE102017124223B4	2017-08-30	2022-02-24	Taiwan Semiconductor Manufacturing Co. Ltd.	Semiconductor structure with fins and isolation fins and method for their manufacture

US10943830B2	2017-08-30	2021-03-09	Taiwan Semiconductor Manufacturing Co., Ltd.	Self-aligned structure for semiconductor devices
US10304848B2	2017-09-01	2019-05-28	Taiwan Semiconductor Manufacturing Co., Ltd.	Flash memory structure with reduced dimension of gate structure
US10422746B2 *	2017-12-13	2019-09-24	International Business Machines Corporation	Nanoscale surface with nanoscale features formed using diffusion at a liner-semiconductor interface
US10707333B2	2018-07-30	2020-07-07	Taiwan Semiconductor Manufacturing Co., Ltd.	Semiconductor device and manufacturing method thereof

* Cited by examiner, † Cited by third party, ‡ Family to family citation

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Publication	Publication Date	Title
US10818661B2	2020-10-27	Fin-like field effect transistor (FinFET) device and method of manufacturing same
US11735650B2	2023-08-22	Structure and method for FinFET device with buried sige oxide
US10090300B2	2018-10-02	Fin-like field effect transistor (FinFET) device and method of manufacturing same
US9601598B2	2017-03-21	Method of manufacturing a fin-like field effect transistor (FinFET) device
US9153670B2	2015-10-06	Semiconductor device and fabricating the same
US8445340B2	2013-05-21	Sacrificial offset protection film for a FinFET device
CN103715258B	2016-08-17	Source/drain stack stressor for semiconductor device
US8466027B2	2013-06-18	Silicide formation and associated devices
KR20130137068A	2013-12-16	Method of making a finfet device
CN105023944A	2015-11-04	FinFET device with high-K metal gate stack
US9847392B1	2017-12-19	Semiconductor device and method for fabricating the same
US9502561B1	2016-11-22	Semiconductor devices and methods of forming the same

Priority And Related Applications

Applications Claiming Priority (2)

Application	Filing date	Title
US12/917,902	2010-11-02	Fin-like field effect transistor (FinFET) device and method of manufacturing same
US12/917,902	2010-11-02	

Legal Events

Date	Code	Title	Description
2012-05-23	C06	Publication	
2012-05-23	PB01	Publication	
2012-07-04	C10	Entry into substantive examination	
2012-07-04	SE01	Entry into force of request for substantive examination	
2014-05-28	C14	Grant of patent or utility model	
2014-05-28	GR01	Patent grant	

Concepts

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Silicon-germanium	claims,description	37	0.000
silicon	claims,description	35	0.000
silicon	claims,description	35	0.000
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