(e.g., one or more) of remaining electrodes among the electrodes by connecting the at least a portion of the remaining electrodes to the driving circuit **2340**. As illustrated in FIG. **23**, the electrodes include electrodes A**1**, A**2**, A**3**, B**1**, B**2**, B**3**, C**1**, C**2**, and C**3**, and the electrode router **2320** allocates, to the electrodes, a positive electrode SE**1+** and a negative electrode SE− of a first sensing channel, a positive electrode SE**2+** and a negative electrode SE**2−** of a second sensing channel, and a working electrode WE and a counter electrode CE of the stimulating channel.

As described above, the processor controls the electrode router **2320** to control a connection among the sensing circuit **2330**, the driving circuit **2340**, and the electrode interface **2310**. For example, the processor allocates at least a portion of the electrodes to the sensing channel of the electrode router, and at least a portion of remaining electrodes among the electrodes to the stimulating channel of the electrode router **2320**. For another example, the processor allocates at least a portion of the electrodes to the sensing channel of the electrode router **2320**, and at least another portion of the electrodes to the stimulating channel of the electrode router **2320**, based on an electrical signal detected from a target. Such a dynamic channel allocation performed based on the electrical signal detected from the target will be described in detail with reference to FIGS. **24** and **25**.

FIGS. **24** and **25** are diagrams illustrating examples of a differential signal based on an allocation of electrode channels.

As described above, a processor may allocate a sensing channel to at least a portion of electrodes, and a stimulating channel to at least a portion of remaining electrodes among the electrodes.

For example, as illustrated in FIG. **24**, in response to an electrical signal detected from a target **2490** including a threshold value or greater of common noise, the processor allocates the channels to the electrodes to arrange electrodes belonging to a same channel to be adjacent to each another on a substrate.

As illustrated in FIG. **24**, in a case in which electrodes allocated to a same channel are arranged adjacent to each other, common noise is removed from a differential signal **2440** associated with a first signal **2420** detected from a positive channel **2411** of the sensing channel and a second signal **2430** detected from a negative channel **2412** of the sensing channel. Thus, the processor may obtain a signal that is robust against the common noise by arranging electrodes of a same channel to be adjacent to each other in response to the threshold value or greater of common noise being detected.

For another example, as illustrated in FIG. **25**, in response to the electrical signal detected from a target **2590** including common noise of a value less than the threshold value, the processor allocates the channels to the electrodes to arrange electrodes belonging to a same channel not to be adjacent to each other on the substrate.

As illustrated in FIG. **25**, in a case in which electrodes allocated to a same channel are arranged not to be adjacent to each other, an amplitude of a differential signal **2540** associated with a first signal **2520** detected from a positive channel **2511** of a sensing channel and a second signal **2530** detected from a negative channel **2512** of the sensing channel is amplified. Thus, in response to the common noise being low (e.g., less than the threshold value), the processor may obtain an amplified electrical signal by arranging electrodes of a same channel to be far apart from each other.

As described above, a processor of a wireless device, a communication device, and an electrode device may dynamically map channels to be allocated to linearly arranged electrodes based on a period and an amplitude of an electrical signal detected from a target being observed. Thus, after the wireless device is inserted in an object, the wireless device may determine an optimal electrode arrangement without being separated from the object.

In addition to detection, in terms of stimulation, the wireless device, the communication device, and the electrode device may apply an electrical signal to the target through a current path having a higher signal-to-noise ratio (SNR). Thus, power to be used for electrostimulation applied to the target may be adjusted, and thus power efficiency may be improved.

FIGS. **26** and **27** are diagrams illustrating another example of a configuration of a communication device **2600**.

Referring to FIG. **26**, the communication device **2600** includes a first chip package **2601**, a second chip package **2602**, a motion sensor **2660**, a coil **2670**, and a battery **2690**. The first chip package **2601** and the second chip package **2602** may be embodied in a form of a single chip. However, the form is not limited to the example provided above, and thus the first chip package **2601** and the second chip package **2602** may be embodied in a form of separate chips.

The first chip package **2601** may be a chip configured to operate at a voltage less than or equal to a first threshold voltage. The voltage less than or equal to the first threshold voltage may also be referred to as a low voltage. In an example, a first transceiver circuit **2652**, a processor **2651**, and a sensing circuit **2654** that are included in the first chip package **2601** operate at such a low voltage. For example, when the first threshold voltage is designed to be 2 volts (V), the first chip package **2601** applies a low voltage of 1.8V to the first transceiver circuit **2652**, the processor **2651**, and the sensing circuit **2654**.

However, examples are not limited to the example described above. For example, the first chip package **2601** may be configured to operate in a first voltage range. The first voltage range may be a range of the low voltage less than or equal to the first threshold voltage.

For example, when the first voltage range is designed to be 1.6V to 2V, the first chip package **2601** applies a low voltage of 1.7V or 1.9V to the first transceiver circuit **2652**, the processor **2651**, and the sensing circuit **2654**. The first chip package **2601** operating at the low voltage may operate mainly to transmit a signal.

The second chip package **2602** may be a chip configured to operate at a voltage greater than or equal to a second threshold voltage. The voltage greater than or equal to the second threshold voltage may also be referred to as a high voltage. The second threshold voltage may be greater than the first threshold voltage. In an example, a second transceiver circuit **2653**, a driving circuit **2655**, and a power management circuit **2657** that are included in the second chip package **2602** operate at such a high voltage. For example, when the second threshold voltage is designed to be 11V, the second chip package **2602** applies a high voltage of 12V to the second transceiver circuit **2653**, the driving circuit **2655**, and the power management circuit **2657**.

However, examples are not limited to the example described above. For example, the second chip package **2602** may be embodied to operate in a second voltage range. The second voltage range may be a range of the high voltage greater than or equal to the second threshold voltage. For example, when the second voltage range is designed to be 11V to 13V, the second chip package **2602** applies a high voltage of 11.5V or 12.5V to the second transceiver circuit **2653**, the driving circuit **2655**, and the power management circuit **2657**. The second chip package **2602** operating at the high voltage may operate mainly to manage a voltage.

In FIG. **26**, a solid line arrow indicates power transfer, and a broken line arrow indicates signal transfer. As illustrated, power received through the coil **2670** is transferred to the battery **2690** through the second transceiver circuit **2653**. The power management circuit **2657** provides the power received from the battery **2690** to the remaining circuits. Also, a signal received through the coil **2670** is transferred to the processor **2651** through the first transceiver circuit **2652**. The processor **2651** processes the signal and transfers the processed signal to other circuits, or processes a signal transferred from the other circuits.

In an example, the communication device **2600** reduces power consumption by applying, to the first chip package **2601**, a voltage less than a voltage applied to the second chip package **2602**.

The motion sensor **2660** senses a motion of the communication device **2600**. The motion sensor **2660** is embodied as, for example, an acceleration sensor and a geomagnetic field sensor. The motion sensor **2660** may measure an acceleration applied to the communication device **2600**.

The processor **2651**, the first transceiver circuit **2652**, and the second transceiver circuit **2653**, the sensing circuit **2654**, the driving circuit **2655**, the power management circuit **2657**, the coil **2670**, and the battery **2690** may operate or be configured as described with reference to FIGS. **13** and **14**.

FIG. **27** illustrates a stacked structure of a communication device **2700** corresponding to the communication device **2600** of FIG. **26**.

Referring to FIG. **27**, the communication device **2700** includes a structure in which a substrate **2709**, a coil **2770**, a first chip package **2701**, a second chip package **2702**, and a battery **2790** are stacked in a sequential order. For example, as illustrated, the components of the communication device **2700** are stacked on a first surface of the substrate **2709** in an order of the first chip package **2701**, the second chip package **2702**, and the battery **2790**. In addition, a motion sensor may be stacked in a layer including the battery **2790**, or stacked on the battery **2790**.

A discrete element **2710** is stacked on a second surface of the substrate **2709** that is opposite to the first surface on which the first chip package **2701**, the second chip package **2702**, and the battery **2790** are staked. The discrete element **2710** is, for example, a decoupling capacitor.

The coil **2770**, the first chip package **2701**, the second chip package **2702**, and the battery **2790** may operate or be configured as described with reference to the first chip package **2601**, the second chip package **2602**, and the battery **2690** of FIG. **26**, and the substrate **2709** may be the same as the substrate **560** described above with reference to FIG. **5**.

The processors **320**, **1250**, **1351**, **1451**, and **2651** in FIGS. **1**, **12**, **13**, **14**, and **26**, respectively, and other components that perform the operations described in this application are implemented by hardware components configured to perform the operations described in this application that are performed by the hardware components. Examples of hardware components that may be used to perform the operations described in this application where appropriate include controllers, sensors, generators, drivers, memories, comparators, arithmetic logic units, adders, subtractors, multipliers, dividers, integrators, and any other electronic components configured to perform the operations described in this application. In other examples, one or more of the hardware components that perform the operations described in this application are implemented by computing hardware, for example, by one or more processors or computers. A processor or computer may be implemented by one or more processing elements, such as an array of logic gates, a controller and an arithmetic logic unit, a digital signal processor, a microcomputer, a programmable logic controller, a field-programmable gate array, a programmable logic array, a microprocessor, or any other device or combination of devices that is configured to respond to and execute instructions in a defined manner to achieve a desired result. In one example, a processor or computer includes, or is connected to, one or more memories storing instructions or software that are executed by the processor or computer. Hardware components implemented by a processor or computer may execute instructions or software, such as an operating system (OS) and one or more software applications that run on the OS, to perform the operations described in this application. The hardware components may also access, manipulate, process, create, and store data in response to execution of the instructions or software. For simplicity, the singular term "processor" or "computer" may be used in the description of the examples described in this application, but in other examples multiple processors or computers may be used, or a processor or computer may include multiple processing elements, or multiple types of processing elements, or both. For example, a single hardware component or two or more hardware components may be implemented by a single processor, or two or more processors, or a processor and a controller. One or more hardware components may be implemented by one or more processors, or a processor and a controller, and one or more other hardware components may be implemented by one or more other processors, or another processor and another controller. One or more processors, or a processor and a controller, may implement a single hardware component, or two or more hardware components. A hardware component may have any one or more of different processing configurations, examples of which include a single processor, independent processors, parallel processors, single-instruction single-data (SISD) multiprocessing, single-instruction multiple-data (SIMD) multiprocessing, multiple-instruction single-data (MISD) multiprocessing, and multiple-instruction multiple-data (MIMD) multiprocessing.

Instructions or software to control computing hardware, for example, one or more processors or computers, to implement the hardware components and perform the methods as described above may be written as computer programs, code segments, instructions or any combination thereof, for individually or collectively instructing or configuring the one or more processors or computers to operate as a machine or special-purpose computer to perform the operations that are performed by the hardware components and the methods as described above. In one example, the instructions or software include machine code that is directly executed by the one or more processors or computers, such as machine code produced by a compiler. In another example, the instructions or software includes higher-level code that is executed by the one or more processors or computer using an interpreter. The instructions or software may be written using any programming language based on the block diagrams and the flow charts illustrated in the drawings and the corresponding descriptions in the specification, which disclose algorithms for performing the operations that are performed by the hardware components and the methods as described above.

The instructions or software to control computing hardware, for example, one or more processors or computers, to implement the hardware components and perform the methods as described above, and any associated data, data files, and data structures, may be recorded, stored, or fixed in or on one or more non-transitory computer-readable storage media. Examples of a non-transitory computer-readable storage medium include read-only memory (ROM), random-access memory (RAM), flash memory, CD-ROMs, CD-Rs, CD+Rs, CD-RWs, CD+RWs, DVD-ROMs, DVD-Rs, DVD+Rs, DVD-RWs, DVD+RWs, DVD-RAMs, BD-ROMs, BD-Rs, BD-R LTHs, BD-REs, magnetic tapes, floppy disks, magneto-optical data storage devices, optical data storage devices, hard disks, solid-state disks, and any other device that is configured to store the instructions or software and any associated data, data files, and data structures in a non-transitory manner and provide the instructions or software and any associated data, data files, and data structures to one or more processors or computers so that the one or more processors or computers can execute the instructions. In one example, the instructions or software and any associated data, data files, and data structures are distributed over network-coupled computer systems so that the instructions and software and any associated data, data files, and data structures are stored, accessed, and executed in a distributed fashion by the one or more processors or computers.

While this disclosure includes specific examples, it will be apparent to one of ordinary skill in the art that various changes in form and details may be made in these examples without departing from the spirit and scope of the claims and their equivalents. The examples described herein are to be considered in a descriptive sense only, and not for purposes of limitation. Descriptions of features or aspects in each example are to be considered as being applicable to similar features or aspects in other examples. Suitable results may be achieved if the described techniques are performed in a different order, and/or if components in a described system, architecture, device, or circuit are combined in a different manner, and/or replaced or supplemented by other components or their equivalents. Therefore, the scope of the disclosure is defined not by the detailed description, but by the claims and their equivalents, and all variations within the scope of the claims and their equivalents are to be construed as being included in the disclosure.

What is claimed is:

1. A communication device, comprising:

a coil disposed around a core area of the communication device;

a processor disposed only in the core area and configured to establish communication with an external device through the coil; and

a discrete element disposed on the coil and connected to the processor through a via, wherein the discrete element comprises any one or any combination of any two or more of a capacitor, an inductor, and a resistor.

2. The communication device of claim **1**, wherein the processor is disposed in a layer distinguished from the coil.

3. The communication device of claim **1**, wherein the discrete element comprises a passive electronic component configured to separate voltages, by electrically decoupling circuits of circuits in a chip including the processor.

4. The communication device of claim **1**, wherein the discrete element is connected to a chip comprising the processor through the via, and is arranged in an outer edge ring area of the coil in a layer distinguished from the coil.

5. The communication device of claim **1**, further comprising:

a first transceiver circuit configured to transmit and receive, through the coil, a signal of a first bandwidth; and

a second transceiver circuit configured to transmit and receive, through the coil, a signal of a second bandwidth that is different from the first bandwidth,

wherein the first transceiver circuit and the second transceiver circuit are included in a chip comprising the processor.

6. The communication device of claim **5**, wherein

the first transceiver circuit is configured to operate at a voltage less than or equal to a first threshold voltage, and

the second transceiver circuit is configured to operate at a voltage greater than or equal to a second threshold voltage that is greater than the first threshold voltage.

7. The communication device of claim **1**, further comprising:

an electrode router circuit connected to electrodes of an electrode device,

wherein the electrode router circuit is included in a chip comprising the processor.

8. The communication device of claim **7**, wherein

the electrode router circuit is configured to connect a first electrode among the electrodes to a sensing circuit, and connect a second electrode among the electrodes to a driving circuit,

the sensing circuit is configured to detect, through the first electrode, an electrical signal corresponding to a point to which the first electrode is attached, and

the driving circuit is configured to apply, through the second electrode, an electrical signal to a point to which the second electrode is attached.

9. The communication device of claim **8**, wherein

the sensing circuit is configured to operate at a voltage less than or equal to a first threshold voltage, and

the driving circuit is configured to operate at a voltage greater than or equal to a second threshold voltage that is greater than the first threshold voltage.

10. The communication device of claim **1**, wherein the coil comprises

a first partial coil configured to resonate in a first bandwidth, and

a second partial coil configured to resonate in a second bandwidth that is different from the first bandwidth, and

the first partial coil and the second partial coil share a loop.

11. The communication device of claim **10**, wherein

the first partial coil comprises a loop configured to generate a magnetic field in a first direction, and

the second partial coil comprises a loop configured to generate an electric field in the first direction.

12. The communication device of claim **1**, further comprising:

an embedded element disposed in a layer distinguished from a layer comprising the coil and a layer including the processor, and connected to the processor through the via, wherein the embedded element comprises either one or both of a capacitor or an inductor; and

a motion sensor configured to sense a motion of the communication device.

13. The communication device of claim **1**, wherein a chip comprising the processor is spaced from the coil by a distance greater than or equal to a threshold distance.

14. The communication device of claim **1**, wherein the processor is connected to electrodes of an electrode device arranged to cover a target area associated with an object, and is configured to receive an electrical signal from or provide an electrical signal to some of the electrodes.

15. The communication device of claim **14**, wherein the processor is configured to allocate a sensing channel configured to receive the electrical signal from the electrodes using one or more electrodes among the electrodes, and allocate a stimulating channel configured to provide an electrical signal to the target area using one or more remaining electrodes among the electrodes, based on the received electrical signal.

16. A communication device, comprising:

a coil disposed around a core area of the communication device;

a processor disposed in the core area and configured to establish communication with an external device through the coil;

a discrete element disposed on the coil and connected to the processor through a via, wherein the discrete element comprises any one or any combination of any two or more of a capacitor, an inductor, and a resistor, which is connected to a chip comprising the processor through the via; and

an electrode router circuit connected to electrodes of an electrode device, wherein

the electrode router circuit is configured to connect a first electrode among the electrodes to a sensing circuit, and connect a second electrode among the electrodes to a driving circuit,

the sensing circuit is configured to detect, through the first electrode, an electrical signal corresponding to a point to which the first electrode is attached, and

the driving circuit is configured to apply, through the second electrode, an electrical signal to a point to which the second electrode is attached.

17. The communication device of claim **16**, wherein the electrode router circuit is included in a chip comprising the processor.

18. A communication device, comprising:

a coil disposed around a core area of the communication device;

a processor disposed in the core area and configured to establish communication with an external device through the coil,

wherein the processor is connected to electrodes arranged to cover a target area associated with an object, and is configured to receive an electrical signal from or provide an electrical signal to some of the electrodes, and

wherein the processor is configured to allocate a sensing channel configured to receive the electrical signal from the electrodes using one or more electrodes among the electrodes, and allocate a stimulating channel configured to provide an electrical signal to the target area using one or more remaining electrodes among the electrodes, based on the received electrical signal; and

a discrete element disposed on the coil and connected to the processor through a via, wherein the discrete element comprises any one or any combination of any two or more of a capacitor, an inductor, and a resistor, which is connected to a chip comprising the processor through the via.

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