



(19) **United States**

(12) **Patent Application Publication**
NAGAI et al.

(10) **Pub. No.: US 2012/0145552 A1**

(43) **Pub. Date: Jun. 14, 2012**

(54) **ELECTROPLATING METHOD**

(52) **U.S. Cl. 205/131**

(76) **Inventors:** Mizuki NAGAI, Tokyo (JP);
Yusuke Tamari, Tokyo (JP);
Shingo Yasuda, Tokyo (JP)

(57) **ABSTRACT**

(21) **Appl. No.: 13/313,154**

An electroplating method includes: preparing a substrate having via holes formed in a surface; immersing the substrate in a pretreatment solution to carry out pretreatment of the substrate; immersing the substrate in a plating solution without applying a voltage between the substrate and an anode, thereby replacing the pretreatment solution in the via holes with the plating solution; carrying out first-step electroplating of the substrate while controlling the voltage, applied between the substrate and the anode, to be equal to or higher than a voltage which is necessary for an electric current, appropriate to fill a plated metal into the via holes, to flow stably between the substrate and the anode; and carrying out second-step electroplating of the substrate while controlling the electric current, flowing between the substrate and the anode, at an electric current appropriate to fill the plated metal into the via holes.

(22) **Filed: Dec. 7, 2011**

(30) **Foreign Application Priority Data**

Dec. 8, 2010 (JP) 2010-273658

Publication Classification

(51) **Int. Cl.**
C25D 5/02 (2006.01)
C25D 5/34 (2006.01)

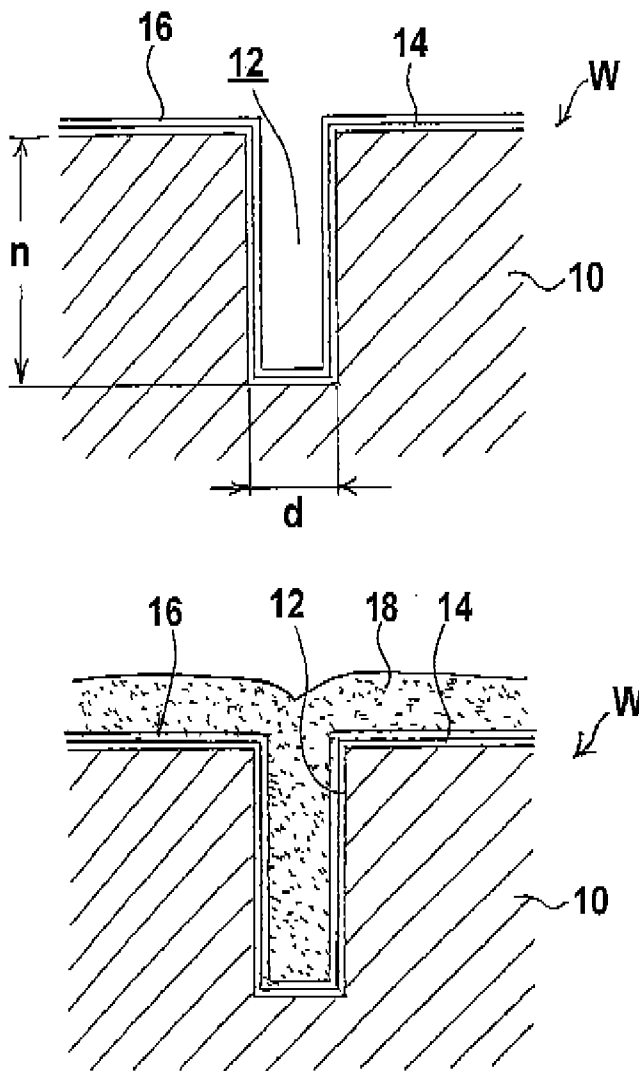


FIG. 1A

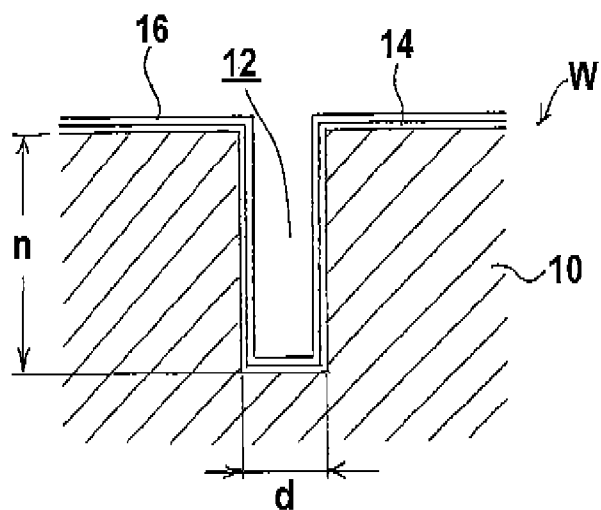


FIG. 1B

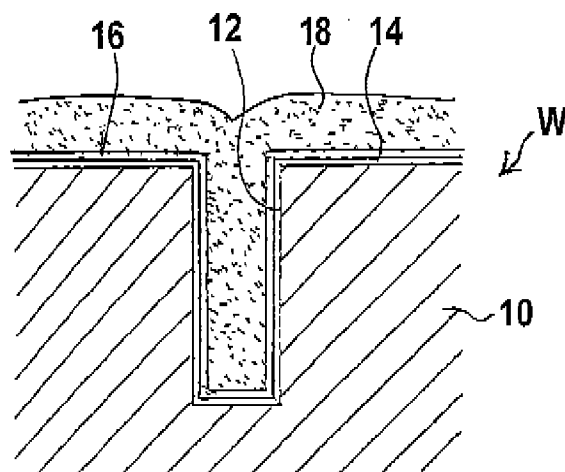


FIG. 1C

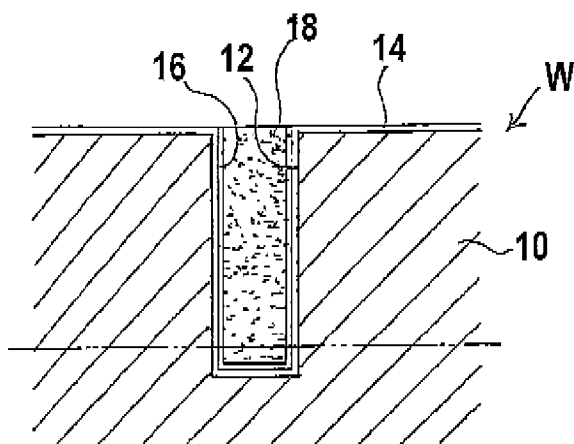


FIG. 2

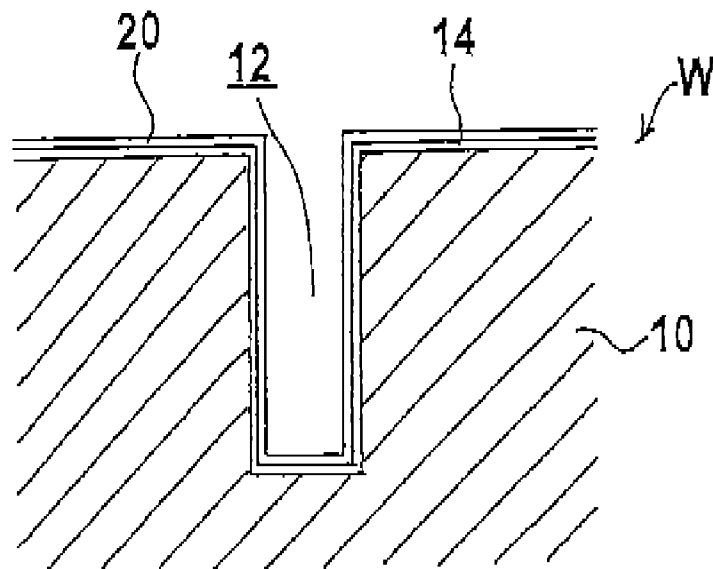


FIG. 3

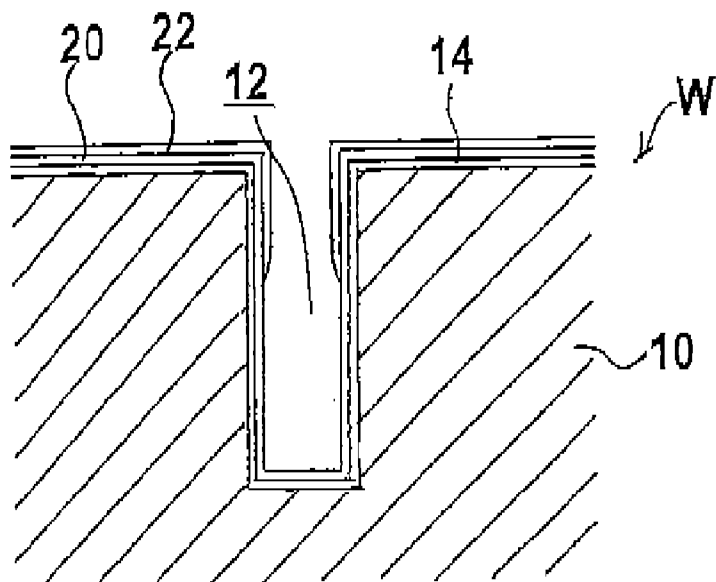


FIG. 4

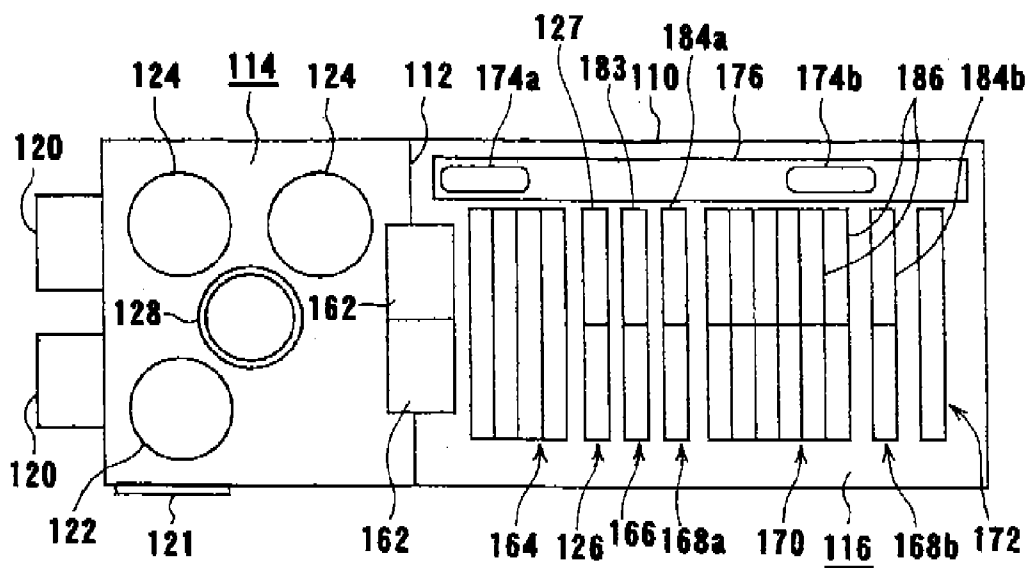


FIG. 5

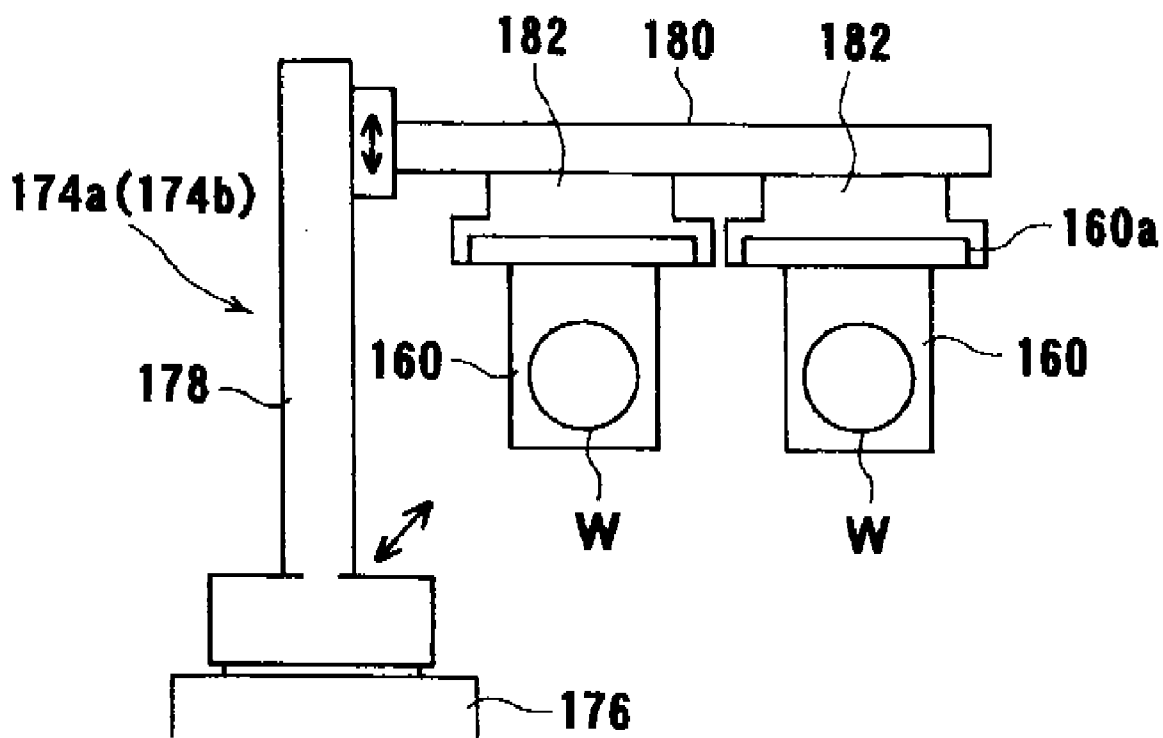


FIG. 7

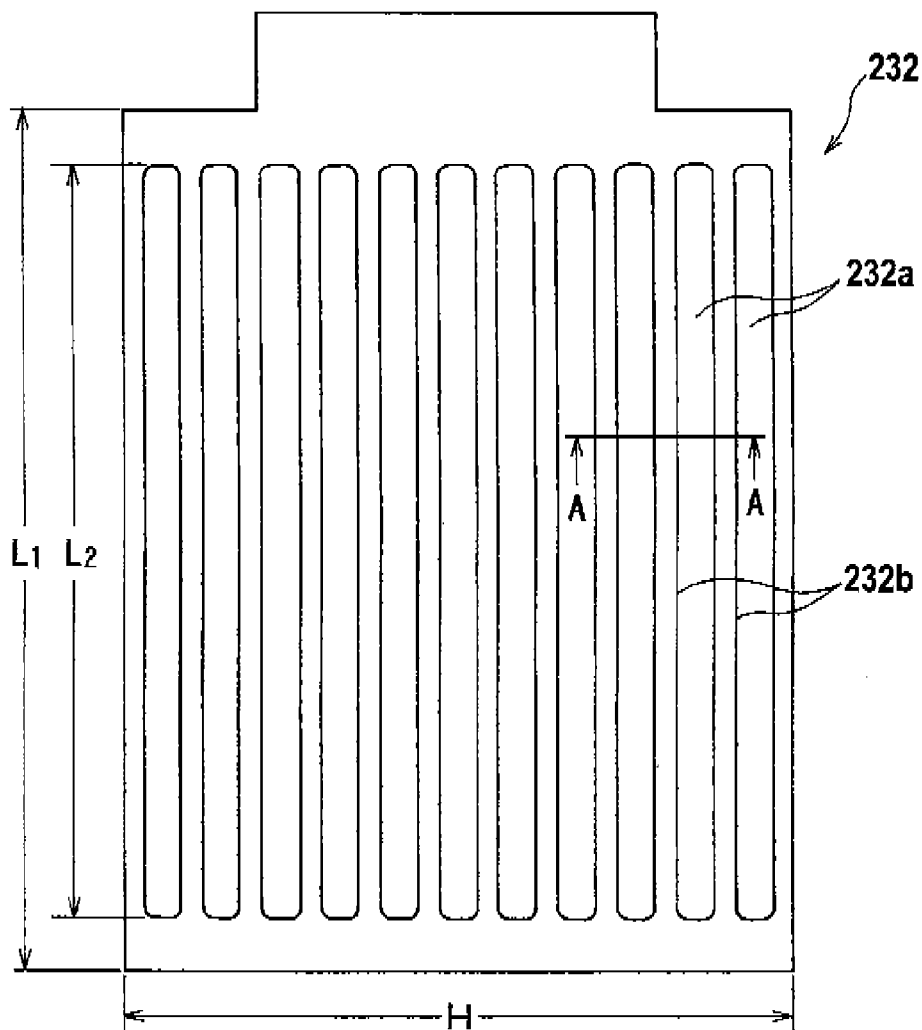
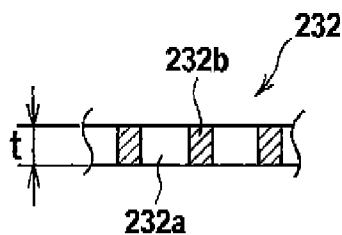


FIG. 8



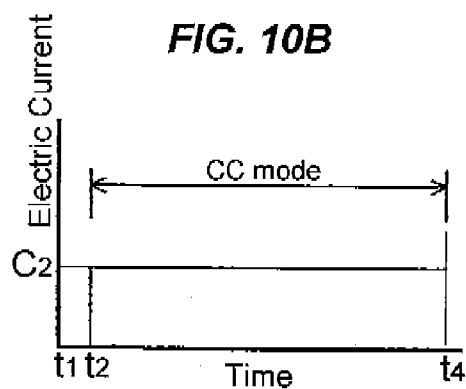
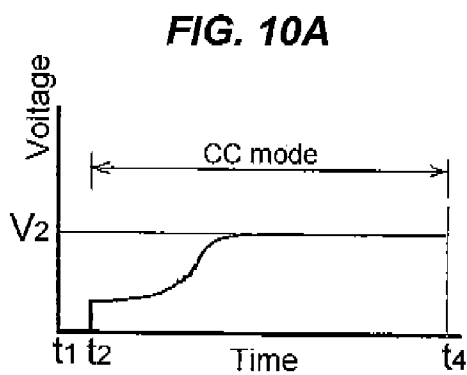
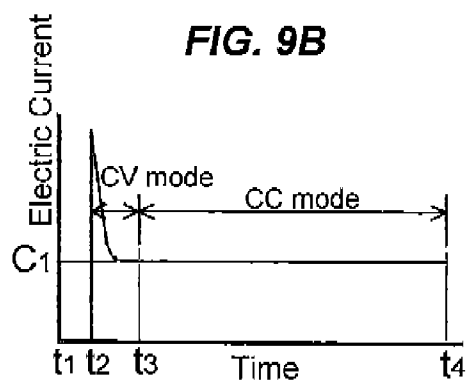
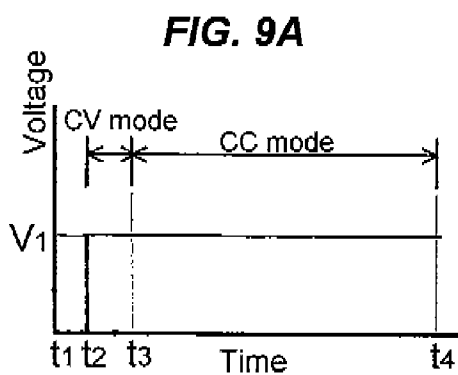


FIG. 11A

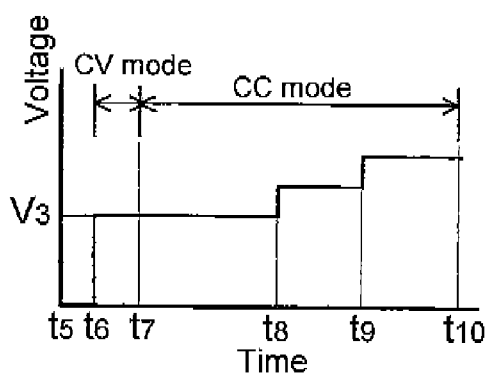


FIG. 11B

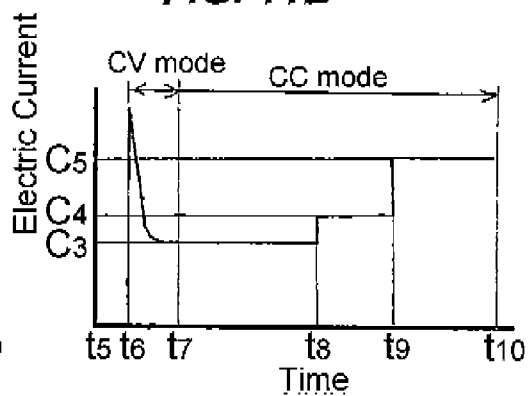


FIG. 12A

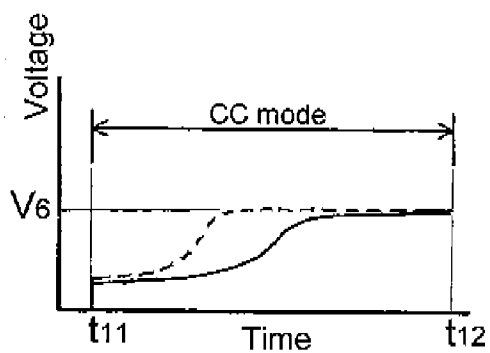


FIG. 12B

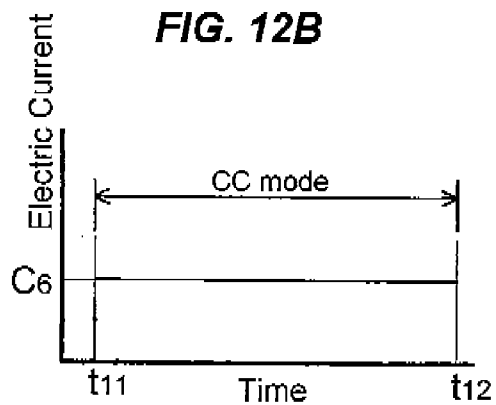


FIG. 13

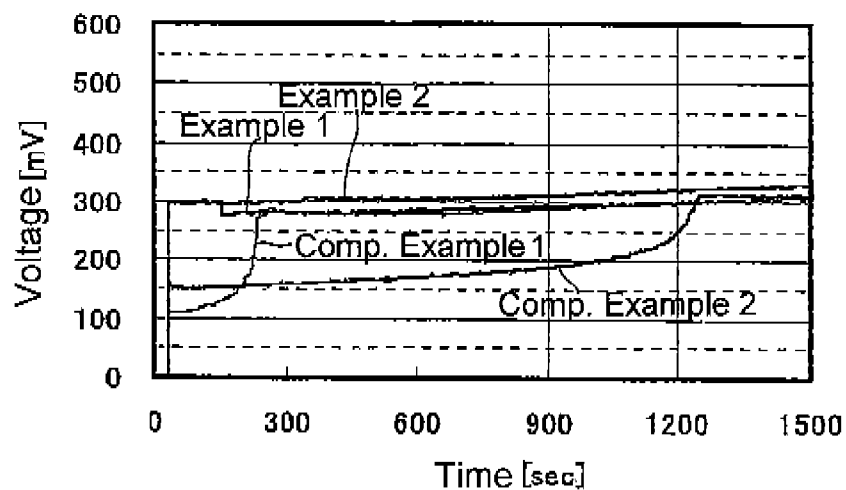


FIG. 14

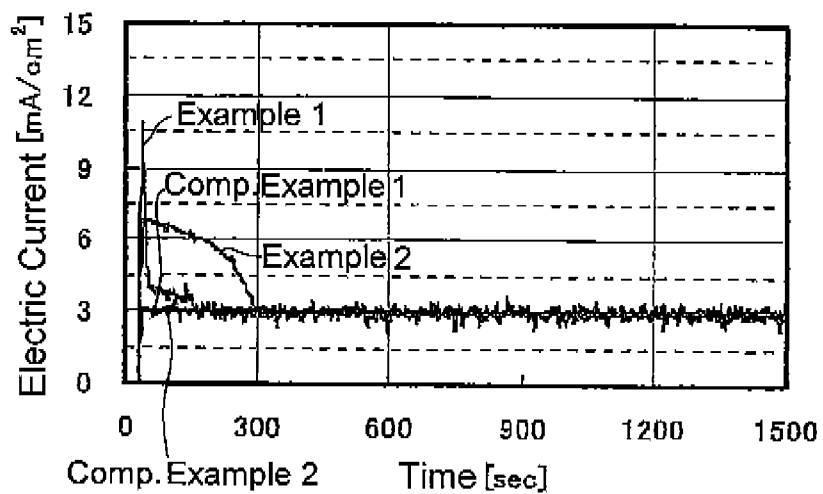


FIG. 15

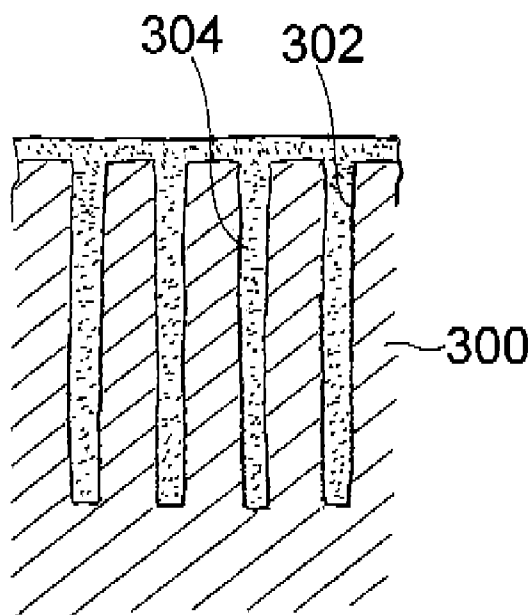


FIG. 16

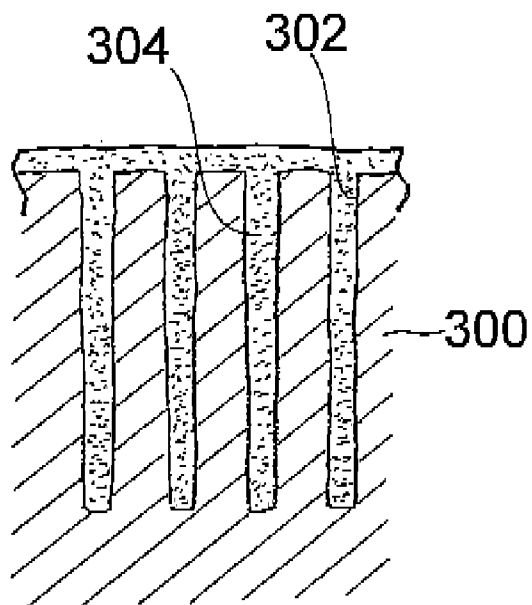


FIG. 17

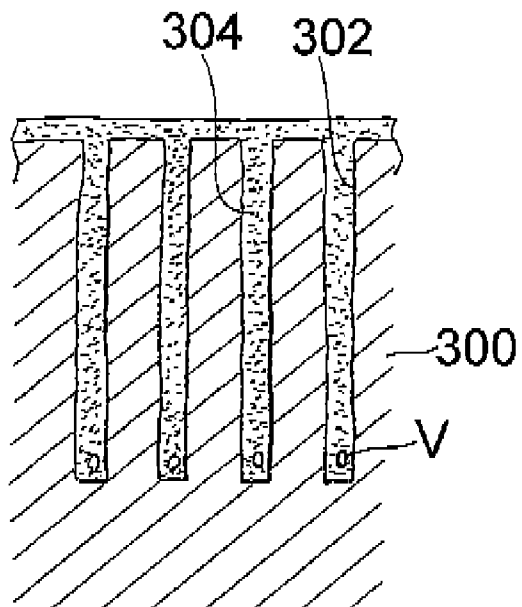
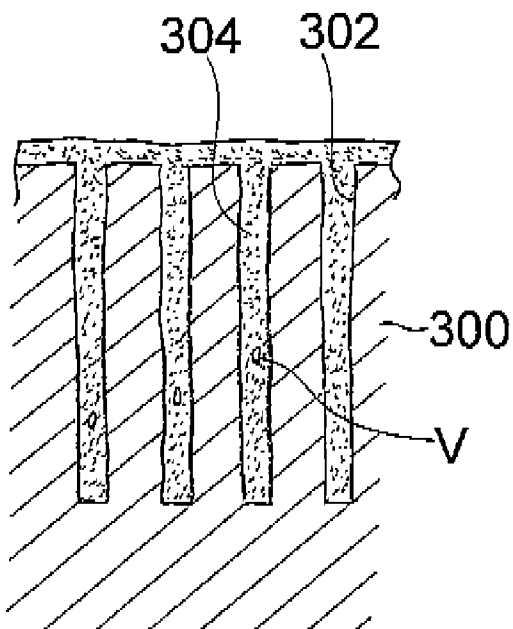


FIG. 18



ELECTROPLATING METHOD

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an electroplating method, and more particularly to an electroplating method which is useful for tilling a metal, such as copper, into via holes in the manufacturing of a substrate, such as a semiconductor substrate or the like, which has a number of through-vias (via plugs) vertically penetrating in its interior, and which can be used in so-called three-dimensional packaging of semiconductor chips.

[0003] 2. Description of the Related Art

[0004] A technique of forming through-vias of a metal such as copper, vertically penetrating through a semiconductor substrate, is known as a method to electrically connect the layers of a multi-layer stack of semiconductor substrates. FIGS. 1A through 1C are diagrams illustrating, in a sequence of process steps, a process for producing a substrate having through-vias of copper that vertically penetrate through the substrate. First, as shown in FIG. 1A, a substrate W is prepared by forming a plurality of upwardly-opening via holes 12 in a base 10, such as a silicon wafer, e.g., by using the lithography/etching technique, and thereafter forming, e.g., by PVD, a barrier layer 14 of a metal such as Ti (titanium) on an entire surface of the base 10, including interior surfaces of the via holes 12, and then forming a copper seed layer 16 on a surface of the barrier layer 14. The diameter "d" of the via holes 12 is, for example, 2 to 50 μm , in particular 10 to 20 μm , and the depth "h" of the via holes 12 is, for example, 20 to 150 μm .

[0005] Besides Ti, other metals, such as Ta (tantalum) and W (tungsten), or a nitride thereof, can be used for the barrier layer 14. This holds true for the following description.

[0006] Next, copper electroplating is carried out on the surface of the substrate W using the copper seed layer 16 as a cathode, thereby filling a plated metal (copper) 18 into the via holes 12 and depositing the plated metal 18 on the surface of the copper seed layer 16, as shown in FIG. 1B.

[0007] Thereafter, as shown in FIG. 1C, the extra copper seed layer 16 and the extra plated metal 18 on the base 10 are removed, e.g. by chemical mechanical polishing (CMP). Further, the back surface side of the base 10 is polished away, e.g., to the position shown by the two-dot chain line in FIG. 1C, thereby exposing a bottom face of the plated metal 18 embedded in the via holes 12. The substrate W having therein through-vias of copper (plated metal 18), vertically penetrating through the substrate W, can be produced in this manner.

[0008] The aspect ratio, i.e., the depth-to-diameter ratio, of the via holes 12 is generally high. In addition, the via holes 12 generally have a large depth. In order to completely fill copper (plated metal) into such via holes 12, having a deep high-aspect ratio, by electroplating without producing defects such as voids in the embedded plated metal, it is usually necessary to perform the electroplating in a bottom-up manner of allowing the plated metal to grow preferentially from the bottoms of the via holes 12. Such bottom-up plating is generally carried out by using a plating solution containing various additives such as SPS (bis(3-sulfopropyl)disulfide) as a plating accelerator, PEG (polyethylene glycol) as a suppressor, and PEI (polyethylene imine) as a leveler. These additives exert their effects after they are adsorbed onto a surface of a substrate.

[0009] The step coverage of a thin film formed by PVD is generally low. Therefore, in order to form a continuous copper seed layer 16 by PVD on the surface of the barrier layer 14, it is necessary to form the copper seed layer 16 with a fairly large thickness, e.g., about 800 to 1000 nm. There is, therefore, a demand for the formation of a thinner seed layer.

[0010] In this regard, Japanese Patent Laid-Open Publication No. 2007-247062 describes a method which comprises forming an auxiliary metal layer (seed layer) 20 of Ru (ruthenium) by conformal CVD on a surface of a barrier layer 14 of Ti or the like, which has been formed, e.g., by sputtering on an entire surface of a substrate W, including interior surfaces of via holes 12, as shown in FIG. 2, and carrying out copper electroplating with the auxiliary metal layer 20 as a cathode to till the plated metal (copper) into the via holes 12. Japanese Patent Laid-Open Publication No. 2008-244298 proposes to additionally form a copper seed layer 22 on a surface of an auxiliary metal layer 20 of Ru, as shown in FIG. 3. FIG. 3 illustrates the copper seed layer 22 having a thickness of about 100 to 300 nm, formed by common PVD.

[0011] The applicant has proposed a plating method which comprises forming an initial plated film by passing a direct current between a seed layer and an anode at a current density of 4 to 20 A/dm^2 for 0.1 to 5 seconds, and subsequently forming a secondary plated film by passing a direct current between the seed layer and the anode at a current density of 0.5 to 5 A/dm^2 (see Japanese Patent No. 3641372). The applicant has also proposed to apply a step voltage, which changes in a stepwise fashion with time, between a substrate and an anode in via-filling electroplating (see Japanese Patent Laid-Open Publication No. 2005-97732). The applicant has also proposed a plating method which involves adsorbing additives in a plating solution onto a surface ruthenium film of a substrate by keeping the substrate surface in contact with the plating solution for a predetermined time, and thereafter carrying out electroplating of the substrate surface to form a plated film on the surface of the ruthenium film (see Japanese Patent Laid-Open publication No. 2009-30167). Further, Japanese Patent No. 3780302 proposes a plating method which comprises first carrying out electroplating at a cathode current density of 5 to 10 A/dm^2 for 10 seconds to 5 minutes, and subsequently carrying out electroplating at a cathode current density of 0.5 to 3 A/dm^2 for 15 to 180 minutes.

SUMMARY OF THE INVENTION

[0012] The thickness of a plated metal (plated film) formed by electroplating is proportional to the current density during plating. Therefore, when filling a plated metal into via holes by electroplating, it is common practice to control an electric current so that an electric current, which is appropriate for the filling of the metal into the via holes, will flow between an anode and a seed layer that covers the via holes. Further, a plating solution containing various additives, as described above, is generally used for such via-filling plating.

[0013] However, despite the use of a plating solution containing additives, it has been quite difficult for electroplating to fill a plated metal, such as copper, securely into deep high-aspect ratio via holes 12 as shown in FIG. 2, covered with an auxiliary metal layer (seed layer) 20 of Ru, without producing defects such as voids in the embedded plated metal. For via holes covered with a copper seed layer, a plated metal may be filled into the via holes without the formation of voids by carrying out plating at a predetermined current density. On the other hand, when plating is carried out to fill a

plated metal (copper) into via holes covered with an auxiliary metal layer (seed layer) of Ru, voids are likely to be formed in the plated metal embedded in the via holes.

[0014] When a copper seed layer **22** having a thickness of about 100 to 300 nm, for example, is formed by common PVD on a surface of an auxiliary metal layer (seed layer) **20** of Ru, the copper seed layer **22** cannot cover the entire surface of the auxiliary metal layer **20**, and the auxiliary metal layer **20** of Ru will be exposed in the bottoms of via holes **12**, as shown in FIG. 3. When via-filling electroplating of such a substrate is carried out using the auxiliary metal layer **20** and the copper seed layer **22** as a cathode to fill a plated metal into the via holes **12**, voids will be formed in the plated metal embedded in the via holes **12**. This may be because the sheet resistance of the auxiliary metal layer **20** is higher than that of the copper seed layer **22**, and the plated metal will not deposit uniformly on the surface of the auxiliary metal layer **20**.

[0015] The present invention has been made in view of the above situation. It is therefore an object of the present invention to provide an electroplating method which makes it possible to securely fill a plated metal, such as copper, into via holes without producing defects, such as voids, in the embedded plated metal even when the via holes are covered with an auxiliary metal layer of, e.g., Ru, having a lower electrical conductivity than a copper seed layer, or when an auxiliary metal layer of, e.g., Ru is partly exposed in the via holes.

[0016] In order to achieve the above object, the present invention provides an electroplating method comprising: preparing a substrate having via holes formed in a surface; immersing the substrate in a pretreatment solution to carry out pretreatment of the substrate; immersing the substrate in a plating solution without applying a voltage between the substrate and an anode disposed opposite the substrate, thereby replacing the pretreatment solution in the via holes with the plating solution; carrying out first-step electroplating of the substrate while controlling the voltage, applied between the substrate and the anode, to be equal to or higher than a voltage which is necessary for an electric current, appropriate to fill a plated metal into the via holes, to flow stably between the substrate and the anode; and then carrying out second-step electroplating of the substrate while controlling the electric current, flowing between the substrate and the anode, at an electric current appropriate to fill the plated metal into the via holes.

[0017] When the first-step electroplating is carried out while controlling the voltage to be equal to or higher than a voltage which is necessary for an electric current, appropriate to fill a plated metal into via holes, to flow stably between a substrate and an anode, the electric current flowing between the substrate and the anode is temporarily high at the initial stage of plating. Therefore, an additive for suppressing plating is preferentially adsorbed onto those portions of the surface of an auxiliary metal layer of, e.g., Ru where a plated film has begun to grow. This promotes the growth of a plated film on those portions of the surface of the auxiliary metal layer where the growth of a plated film has not yet started, making it possible to deposit the plated metal uniformly on the surface of the auxiliary metal layer. After the plated metal begins to deposit uniformly on the surface of the auxiliary metal layer, the electric current, which is appropriate to fill the plated metal into the via holes, flows stably between the substrate and the anode. Then, the second-step electroplating is carried out while controlling the electric current at the electric current which is appropriate to fill the plated metal into the via holes.

The second-step electroplating is carried out at the controlled current for a period of time necessary to deposit the intended amount of plating. This electroplating method allows the plated metal, such as copper, to deposit preferentially in the bottoms of the via holes, i.e., in a bottom-up manner, making it possible to fill the plated metal into the via holes without producing defects, such as voids, in the plated metal embedded in the via holes.

[0018] The substrate is immersed in the plating solution preferably for 10 to 60 seconds without applying a voltage between the substrate and the anode.

[0019] If a substrate, e.g., having a copper seed layer that covers via holes, is immersed in a plating solution for too long a time without applying a voltage between the substrate and an anode, the copper seed layer will be damaged by the plating solution. Thus, the time for immersing the substrate in the plating solution without applying a voltage between the substrate and the anode is preferably about 10 to 20 seconds when the substrate has small-size via holes (e.g., 10 to 50 μm), and about 20 to 60 seconds when the substrate has large-size via holes (e.g., 100 μm).

[0020] The first-step electroplating may be carried out, for example, for one second to ten minutes.

[0021] By carrying out the first-step electroplating for such a period of time, the plated metal can be deposited uniformly on the surface of an auxiliary metal layer of, e.g., Ru, and the electric current, flowing between the substrate and the anode, can be stabilized.

[0022] The second-step electroplating may be carried out in such a manner that the electric current, flowing between the substrate and the anode, is changed in a stepwise fashion.

[0023] As the plated metal gradually deposits in the via holes with the progress of electroplating, the aspect ratio of the unfilled portion of each via hole gradually changes (decreases). The lower the aspect ratio is, the easier is via-filling plating at a high current with stable bottom-up growth of a plated film. Accordingly, the plating time can be shortened and the productivity can be increased by stepwise changing (increasing) the electric current, flowing between the substrate and the anode, in response to change in the degree of filling of the plated metal into the via holes, i.e., change in the aspect ratio of the unfilled portion of each via hole.

[0024] In a preferred aspect of the present invention, the plated metal is copper, and a metal other than copper is exposed on at least part of surfaces of the via holes. The metal other than copper is, for example, ruthenium (Ru) or cobalt (Co), or an alloy thereof.

[0025] The plated metal, such as copper, can be filled into the via holes, with Ru, Co or an alloy thereof being exposed on at least part of their surfaces, without producing defects such as voids in the embedded plated metal.

[0026] The present invention makes it possible to securely fill a plated metal, such as copper, into deep high-aspect ratio via holes without producing defects, such as voids, in the embedded plated metal even when the via holes are covered with an auxiliary metal layer of, e.g., Ru, having a lower electrical conductivity than a copper seed layer, or when an auxiliary metal layer of, e.g., Ru is partly exposed in the via holes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIGS. 1A through 1C are diagrams illustrating, in a sequence of process steps, a process for producing a substrate having through-vias of copper that vertically penetrate through the substrate;

[0028] FIG. 2 is a cross-sectional diagram illustrating the formation of an auxiliary metal layer on a barrier layer which covers an entire surface, including surfaces of via holes, of a substrate;

[0029] FIG. 3 is a cross-sectional diagram illustrating the successive formation of an auxiliary metal layer and a copper seed layer on a barrier layer which covers an entire surface, including surfaces of via holes, of a substrate;

[0030] FIG. 4 is an overall layout plan view of a plating facility for carrying out an electroplating method of the present invention;

[0031] FIG. 5 is a schematic view of a second transfer robot provided in the plating facility shown in FIG. 4;

[0032] FIG. 6 is a schematic cross-sectional view of a plating apparatus provided in the plating facility shown in FIG. 4;

[0033] FIG. 7 is a plan view of a stirring paddle (stirring tool) provided in the plating apparatus shown in FIG. 6;

[0034] FIG. 8 is a cross-sectional view taken along line A-A of FIG. 7;

[0035] FIG. 9A is a graph showing the relationship between time and a voltage applied between an anode and a substrate, and FIG. 9B is a graph showing the relationship between time and an electric current flowing between the anode and the substrate, the relationships being observed in electroplating carried out according to an embodiment of the present invention;

[0036] FIG. 10A is a graph showing the relationship between time and a voltage applied between an anode and a substrate, and FIG. 10B is a graph showing the relationship between time and an electric current flowing between the anode and the substrate, the relationships being observed in electroplating of the surface of the substrate shown in FIG. 3, carried out at a controlled current;

[0037] FIG. 11A is a graph showing the relationship between time and a voltage applied between an anode and a substrate, and FIG. 11B is a graph showing the relationship between time and an electric current flowing between the anode and the substrate, the relationships being observed in electroplating carried out according to another embodiment of the present invention;

[0038] FIG. 12A is a graph showing the relationship between time and a voltage applied between an anode and a substrate, and FIG. 12B is a graph showing the relationship between time and an electric current flowing between the anode and the substrate, the relationships being observed in electroplating of the surface of the substrate shown in FIG. 2, carried out at a controlled current;

[0039] FIG. 13 is a graph showing the relationships between time and a voltage applied between an anode and a substrate sample, observed in Examples 1 and 2, and Comp. Examples 1 and 2;

[0040] FIG. 14 is a graph showing the relationships between time and an electric current flowing between the anode and the substrate sample, observed in Examples 1 and 2, and Comp. Examples 1 and 2;

[0041] FIG. 15 is a diagram illustrating via holes of a substrate sample after filling a plated metal (copper) into the via holes in Example 1;

[0042] FIG. 16 is a diagram illustrating via holes of a substrate sample after filling a plated metal (copper) into the via holes in Example 2;

[0043] FIG. 17 is a diagram illustrating via holes of a substrate sample after filling a plated metal (copper) into the via holes in Comp. Example 1; and

[0044] FIG. 18 is a diagram illustrating via holes of a substrate sample after filling a plated metal (copper) into the via holes in Comp. Example 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0045] Preferred embodiments of the present invention will now be described with reference to the drawings. The following description illustrates an exemplary case where copper electroplating of a surface of a substrate is carried out to fill copper (plated metal) into via holes provided in the surface of the substrate, thereby forming through-vias of copper in the substrate.

[0046] FIG. 4 is an overall layout plan view of a plating facility for carrying out an electroplating method of the present invention. This plating facility is designed so as to automatically perform all plating processes including pre-treatment of a substrate, plating, and post-treatment of the plating, in a successive manner. The interior of an apparatus frame 110 having an armored panel attached thereto is divided by a partition plate 112 into a plating space 116 for performing a plating process of a substrate and treatments of the substrate to which a plating solution is attached, and a clean space 114 for performing other processes, i.e., processes not directly involving a plating solution. Two substrate holders 160 (see FIG. 5) are arranged in parallel, and substrate attachment/detachment stages 162 to attach a substrate to and detach a substrate from each substrate holder 160 are provided as a substrate delivery section on a partition portion partitioned by the partition plate 112, which divides the plating space 116 from the clean space 114. Loading/unloading ports 120, on which substrate cassettes storing substrates are mounted, are connected to the clean space 114. Further, the apparatus frame 110 has a console panel 121 provided thereon.

[0047] In the clean space 114, there are disposed an aligner 122 for aligning an orientation flat or a notch of a substrate with a predetermined direction, two cleaning/drying devices 124 for cleaning a plated substrate and rotating the substrate at a high speed to spin-dry the substrate. Further, a first transfer robot 128 is disposed substantially at the center of these processing devices, i.e., the aligner 122 and the cleaning/drying devices 124, to thereby transfer and deliver a substrate between the processing devices 122, 124, the substrate attachment/detachment stages 162, and the substrate cassettes mounted on the loading/unloading ports 120.

[0048] The aligner 122 and the cleaning/drying devices 124 disposed in the clean space 114 are designed so as to hold and process a substrate in a horizontal state in which a front face of the substrate faces upward. The first transfer robot 128 is designed so as to transfer and deliver a substrate in a horizontal state in which a front face of the substrate faces upward.

[0049] In the plating space 116, in the order from the partition plate 112, there are disposed a stocker 164 for storing or temporarily storing the substrate holders 160, a pretreatment device 126 for carrying out a pretreatment (pre-wetting treatment) for cleaning the surface of the substrate with a pretreatment liquid, such as pure water (DIW) or the like, and enhancing a hydrophilicity of the surface of the substrate by wetting with the pretreatment liquid, an activation treatment device 166 for etching, for example, an oxide film, having a high electrical resistance, on a seed layer formed on the surface of the substrate with an inorganic acid solution, such as sulfuric acid or hydrochloric acid, or an organic acid solution, such as

citric acid or oxalic acid, to remove the oxide film, a first water-cleaning device 168a for cleaning the surface of the substrate with pure water, a plating apparatus 170 for carrying out plating, a second water-cleaning device 168b, and a blowing device 172 for dewatering the plated substrate. Two second transfer robots 174a, 174b are disposed beside these devices so as to be movable along a rail 176. One of the second transfer robots 174a transfers the substrate holders 160 between the substrate attachment/detachment stages 162 and the stocker 164. The other of the second transfer robots 174b transfers the substrate holders 160 between the stocker 164, the pretreatment device 126, the activation treatment device 166, the first water-cleaning device 168a, the plating apparatus 170, the second water-cleaning device 168b, and the blowing device 172.

[0050] As shown in FIG. 5, each of the second transfer robots 174a, 174b has a body 178 extending in a vertical direction and an arm 180 which is vertically movable along the body 178 and rotatable about its axis. The arm 180 has two substrate holder retaining portions 182 provided in parallel for detachably retaining the substrate holders 160. The substrate holder 160 is designed so as to hold a substrate W in a state in which a front face of the substrate is exposed while a peripheral portion of the substrate is sealed, and to be capable of attaching the substrate W to the substrate holder 160 and detaching the substrate W from the substrate holder 160.

[0051] The stocker 164, the pretreatment device 126, the activation treatment device 166, the water-cleaning devices 168a, 168b, and the plating apparatus 170 are designed so as to engage with outwardly projecting portions 160a provided at both ends of each substrate holder 160 to thus support the substrate holders 160 in such a state that the substrate holders 160 are suspended in a vertical direction. The pretreatment device 129 has two pretreatment tanks 127 for holding therein a pretreatment liquid, such as pure water (deaerated DIW) having, e.g., a dissolved oxygen concentration of not more than 2 mg/L or the like. As shown in FIG. 5, the arm 180 of the second transfer robot 174b holding the substrate holders 160, which are loaded with the substrates W, in a vertical state is lowered so as to engage with upper ends of the pretreatment tanks 127 to support the substrate holders 160 in a suspended manner. Thus, the pretreatment device 126 is designed so that the substrate holders 160 are immersed together with the substrates W in the pretreatment liquid in the pretreatment tanks 127 to carry out a pretreatment (pre-wetting treatment). The activation treatment device 166 has two activation treatment tanks 183 for holding a chemical liquid therein. As shown in FIG. 5, the arm 180 of the second transfer robot 174b holding the substrate holders 160, which are loaded with the substrates W, in a vertical state is lowered so as to engage with upper ends of the activation treatment tanks 183 to support the substrate holders 160 in a suspended manner. Thus, the activation treatment device 166 is designed so that the substrate holders 160 are immersed together with the substrates W in the chemical liquid in the activation treatment tanks 183 to carry out an activation treatment. The activation treatment tanks 183 can be omitted when the activation treatment is not necessary.

[0052] Similarly, the water-cleaning devices 168a, 168b have two water-cleaning tanks 184a and two water-cleaning tanks 184b which hold pure water therein, respectively, and the plating apparatus 170 has a plurality of plating tanks 186 which hold a plating solution therein. The water-cleaning devices 168a, 168b and the plating apparatus 170 are

designed so that the substrate holders 160 are immersed together with the substrates W in the pure water in the water-cleaning tanks 184a, 184b or the plating solution in the plating tanks 186 to carry out water-cleaning or plating in the same manner as described above. The arm 180 of the second transfer robot 174b holding the substrate holders 160, which are loaded with substrates W, in a vertical state is lowered, and air or inert gas is injected toward the substrates W mounted on the substrate holders 160 to blow away a liquid attached to the substrate holders 160 and the substrates W and to dewater the substrates W. Thus, the blowing device 172 is designed so as to carry out blowing treatment.

[0053] As shown in FIG. 6, each plating tank 186 provided in the plating apparatus 170 is designed so as to hold a predetermined amount of plating solution Q therein. The substrates W, which are held in a state such that the front faces (surfaces to be plated) are exposed while peripheral portions of the substrates are watertightly sealed by the substrate holder 160, are immersed in the plating solution Q in the plating tank 186 in a vertical direction. In this embodiment, a plating solution which, in addition to copper ions, a supporting electrolyte and halogen ions, contains various additives such as SPS (bis(3-sulfopropyl)disulfide) as a plating accelerator, PEG (polyethylene glycol) as a suppressor, and PEI (polyethylene imine) as a leveler, for example, is used as the plating solution Q. Sulfuric acid is preferably used as the supporting electrolyte, and chlorine ions are preferably used as the halogen ions.

[0054] An overflow tank 200 for receiving the plating solution Q that has overflowed an edge of the plating tank 186 is provided around an upper end of the plating tank 186. One end of a circulation piping 204, which is provided with a pump 202, is connected to a bottom of the overflow tank 200, and the other end of the circulation piping 204 is connected to a plating solution supply inlet 186a provided at a bottom of the plating tank 186. Thus, the plating solution Q in the overflow tank 200 is returned into the plating tank 186 by the actuation of the pump 202. Located downstream of the pump 202, a constant-temperature unit 206 for controlling the temperature of the plating solution Q and a filter 208 for filtering out foreign matter contained in the plating solution are interposed in the circulation piping 204.

[0055] A bottom plate 210, having a large number of plating solution passage holes therein, is installed in the bottom of the plating tank 186. The interior of the plating tank 186 is thus separated by the bottom plate 210 into an upper substrate processing chamber 214 and a lower plating solution distribution chamber 212. Further, a shield plate 216, extending vertically downward, is mounted to the lower surface of the bottom plate 210.

[0056] According to this plating apparatus 170, the plating solution Q is introduced into the plating solution distribution chamber 212 of the plating tank 186 by the actuation of the pump 202, flows into the substrate processing chamber 214 passing through the plating solution passage holes provided in the bottom plate 210, flows vertically approximately parallel to the surface of the substrate W held by the substrate holder 160, and then flows into the overflow tank 200.

[0057] An anode 220 having a circular shape corresponding to the shape of the substrate W is held by an anode holder 222 and provided vertically in the plating tank 186. When the plating solution Q is filled in the plating tank 186, the anode 220 held by the anode holder 222 becomes immersed in the

plating solution Q in the plating tank 186 and faces the substrate W held by the substrate holder 160 and disposed in the plating tank 186.

[0058] Further, in the plating tank 186, a regulation plate 224, for regulating the distribution of electric potential in the plating tank 186, is disposed between the anode 220 and the substrate W to be disposed at a predetermined position in the plating tank 186. In this embodiment, the regulation plate 224 is comprised of a cylindrical portion 226 and a rectangular flange portion 228, and is made of polyvinyl chloride that is a dielectric material. The cylindrical portion 226 has such an opening size and axial length as to sufficiently restrict broadening of electric field. A lower end of the flange portion 228 of the regulation plate 224 reaches the bottom plate 210.

[0059] Between the regulating plate 224 and the substrate W to be disposed at a predetermined position in the plating tank 186 is disposed a vertically-extending stirring paddle 232 as a stirring tool which reciprocates parallel to the surface of the substrate w to stir the plating solution Q between the substrate W and the regulating plate 224. By stirring the plating solution Q with the stirring paddle (stirring tool) 232 during plating, a sufficient amount of copper ions can be supplied uniformly to the surface of the substrate W.

[0060] As shown in FIGS. 7 and 8, the stirring paddle 232 is comprised of a rectangular plate-like member having a uniform thickness "t" of 3 to 5 mm, and has a plurality of parallel slits 232a that define vertically-extending strip-like portions 232b. The stirring paddle 232 is formed of, for example, a resin such as PVC, PP and PTFE, and SUS or titanium with a Teflon coating. It is preferred that at least part of the stirring paddle 232, which contacts the plating solution, be electrically isolated. The vertical length L1 of the stirring paddle 232 and the vertical length L2 of the slits 232a are sufficiently larger than the vertical size of the substrate W. Further, the stirring paddle 232 is so designed that the sum of its lateral length H and its reciprocation distance (stroke) is sufficiently larger than the lateral size of the substrate W.

[0061] It is preferred that the width and the number of the slits 232a be determined such that each strip-shaped portion 232b is as narrow as possible insofar as it has the necessary rigidity so that the strip-shaped portions 232b between the slits 232a can efficiently stir the plating solution and, in addition, the plating solution can efficiently pass through the slits 232a.

[0062] The plating apparatus 170 is provided with a plating power source 250 of which the positive pole is connected via a conducting wire to the anode 220 and the negative pole is connected via a conducting wire to the surface of the substrate W during plating. The plating power source 250 is connected to a control section 252, and the plating apparatus 170 is controlled based on signals from the control section 252.

[0063] A description will now be given of a sequence of plating operations, carried out in the plating facility shown in FIG. 4, to fill copper (plated metal) into the via holes 12 of a substrate W as shown in FIG. 3. The substrate W has been produced by a process comprising forming upwardly-opening via holes 12 in a base 10, such as a silicon wafer, forming a barrier layer 14 of Ti or the like on an entire surface of the substrate, forming an auxiliary metal layer 20 of Ru on a surface of the barrier layer 14, and forming a copper seed layer 22 having a thickness of about 100 to 300 nm on a surface of the auxiliary metal layer 20 by PVD. The step coverage of a thin, film formed by PVD is generally low. Accordingly, when the copper seed layer 22 having a thick-

ness of about 100 to 300 nm is formed by PVD, the copper seed layer 22 does not reach to the bottoms of the via holes 12, and the auxiliary metal layer 20 of Ru is exposed in the via holes 12.

[0064] First, the substrate W is placed, with its front surface (surface to be plated) facing upwardly, in a substrate cassette, and the substrate cassette is mounted on the loading/unloading port 120. One of the substrates W is taken out of the substrate cassette mounted on the loading/unloading port 120 by the first transfer robot 128 and placed on the aligner 122 to align an orientation flat or a notch of the substrate W with a predetermined direction. On the other hand, two substrate holders 160, which have been stored in a vertical state in the stocker 164, are taken out by the second transfer robot 174a, rotated through 90° so that the substrate holders 160 are brought into a horizontal state, and then placed in parallel on the substrate attachment/detachment stages 162.

[0065] The substrates W aligned the orientation flat or the notch thereof with a predetermined direction are transferred and loaded into the substrate holders 160 placed on the substrate attachment/detachment stages 162 in a state such that peripheral portions of the substrates are sealed. The two substrate holders 160, which have been loaded with the substrates W, are simultaneously retained, lifted, and then transferred to the stocker 164 by the second transfer robot 174a. The substrate holders 160 are rotated through 90° into a vertical state and lowered so that the two substrate holders 160 are held (temporarily stored) in the stocker 164 in a suspended manner. The above operation is carried out repeatedly in a sequential manner, so that substrates are sequentially loaded into the substrate holders 160, which are stored in the stocker 164, and are sequentially held (temporarily stored) in the stocker 164 at predetermined positions in a suspended manner.

[0066] On the other hand, the two substrate holders 160, which have been loaded with the substrates and temporarily stored in the stocker 164, are simultaneously retained, lifted, and then transferred to the pretreatment device 126 by the second transfer robot 174b. Each substrate w is immersed in a pretreatment liquid, such as pure water (DIW), held in the pretreatment tank 127 to thereby carry out a pretreatment (pre-wetting treatment). A dissolved oxygen concentration of pure water used as the pretreatment liquid is preferably controlled not more than 2 mg/L by using a vacuum deaerator or introducing inactive gas. Next, the two substrate holders 160, each loaded with the substrate W, are transferred to the activation treatment device 166 in the same manner as described above, where the substrates W are immersed in a solution of an inorganic acid such as sulfuric acid or hydrochloric acid, or a solution of an organic acid such as citric acid or oxalic acid, held in the activation treatment tanks 183 to etch away an oxide film having a high electrical resistance from the surface of the seed layer, thereby exposing a clean metal surface. As with pure water for use in the above-described pretreatment, the concentration of dissolved oxygen in an acid solution for use in the activation treatment may be controlled. After the activation treatment, the substrate holders 160, each loaded with the substrate W, are transferred to the first water-cleaning device 168a in the same manner as described above, where the surfaces of the substrates W are cleaned with pure water held in the first water-cleaning tanks 184a.

[0067] After the water cleaning, the two substrate holders 160, each loaded with the substrate W, are transferred to above the plating tanks 186 of the plating apparatus 170 in the same manner as described above. The plating tanks 186 have

been filled with a predetermined amount of the plating solution Q having a predetermined composition, the plating solution being circulated through the circulation system. The substrate holders 160 are then lowered to immerse the substrates W, held by the substrate holders 160, in the plating solution Q in the plating tanks 186. Each substrate W is disposed in the plating solution Q at a position facing the anode 220 held by the anode holder 222. Each anode 220 is to be connected to the plating power source 250 through the anode holder 222.

[0068] As shown in FIGS. 9A and 9B, the substrate W is immersed in the plating solution Q for a predetermined time (t_1 - t_2) without applying a voltage between the anode 220 and the copper seed layer (and the auxiliary metal layer 20) on the surface of the substrate, thereby replacing the pretreatment solution in the via holes 12 with the plating solution Q. By thus replacing the pretreatment solution in the via holes 12 with the plating solution Q, copper ions and additives can be prevented from becoming dilute in the bottoms of the via holes 12. This can prevent the plated metal from failing to deposit normally, thereby preventing the production of defects, such as voids, in the plated metal embedded in the via holes 12.

[0069] If the substrate W, having the copper seed layer 22 that covers the via holes 12, is immersed in the plating solution Q for too long a time without applying a voltage between the anode 220 and the copper seed layer 22, the copper seed layer 22 will be damaged by the plating solution Q. Thus, the time for immersing the substrate W in the plating solution Q without applying a voltage between the anode 220 and the copper seed layer 22 is preferably about 10 to 20 seconds when the substrate has small-size via holes (e.g., 10 to 50 μm), and about 20 to 50 seconds when the substrate has large-size via holes (e.g., 100 μm).

[0070] When a plating start time t_2 is reached, the positive pole of the plating power source 250 is connected to the anode 220, and the negative pole of the plating power source 250 is connected to the copper seed layer 22 (and the auxiliary metal layer 20) of the substrate W, and first-step electroplating is carried out for a predetermined time (t_2 - t_3) while controlling the voltage, applied between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at a voltage V_1 (CV mode) which is necessary for an electric current C_1 , appropriate to fill the plated metal into the via holes 12, to flow stably between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220. The "electric current appropriate to fill the plated metal into the via holes 12" herein refers to a current in such a range as to allow the plated metal to be filled into the via holes 12 without the formation of voids. The current range, which enables void-free via-filling plating, depends on the diameter and the depth of via holes. The use of the highest possible current in the current range is preferred from the viewpoint of increased productivity due to shortening of plating time.

[0071] When, unlike the method of carrying out the first-step electroplating at a controlled voltage, as shown in FIG. 9A, electroplating of the substrate W to fill the plated metal into the via holes 12 is carried out for a predetermined time (t_2 - t_4) while controlling the electric current, flowing between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at a current C_2 ($=C_1$) (CC mode) which is appropriate to fill the plated metal into the via holes 12, as shown in FIG. 10B, the voltage, applied between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode

220, initially takes a low value and gradually increases and, after the elapse of a certain period of time, reaches an approximately constant voltage V_2 , as shown in FIG. 10A. This voltage V_2 is used, in this embodiment, as a CV mode entry voltage V_1 ($=V_2$).

[0072] Maybe the reason why the initial voltage takes a low value when carrying out via-filling plating at a controlled current, as shown in FIG. 10B, is because a plated film does not grow uniformly on the surface of the auxiliary metal layer 20, and an electric current flows locally only in those portions of the surface of the auxiliary metal layer 20 where the plated film has begun to grow. The voltage increases gradually as plating progresses with time, and reaches a constant value as if the plated film begins to grow uniformly in the via holes. However, because the plated film does not grow uniformly microscopically, voids will exist in the plated metal embedded in the via holes.

[0073] On the other hand, when the first-step electroplating is carried out while controlling the voltage, applied between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at a voltage V_1 (CV mode) which is necessary for an electric current C_1 , appropriate to fill the plated metal into the via holes 12, to flow stably between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, as shown in FIG. 9A, the electric current flowing between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220 is temporarily high at the initial stage of plating, as shown in FIG. 9B. Therefore, an additive for suppressing plating is preferentially adsorbed onto those portions of the surface of the auxiliary metal layer 20 where a plated film has begun to grow. This promotes the growth of a plated film on those portions of the surface of the auxiliary metal layer 20 where the growth of a plated film has not yet started, making it possible to deposit the plated metal uniformly on the surface of the auxiliary metal layer 20 of Ru. After the plated metal (copper) begins to deposit uniformly on the surface of the auxiliary metal layer 20 of Ru, the electric current C_1 , which is appropriate to fill the plated metal into the via holes 12, becomes to flow stably between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220.

[0074] In this embodiment, the voltage is selected and controlled in the first-step electroplating so that the electric current C_1 , which is appropriate to fill the plated metal into the via holes 12, flows stably. This can prevent the current from becoming so low that the plating time becomes too long, or prevent the current from becoming so high that voids are formed in the plated metal embedded in the via holes 12. In the first-stage plating of this embodiment, the electric current becomes the Constant current C_1 appropriate for via-filling plating, even though the electric current significantly changes upon the start of plating. Accordingly, even when plating progresses on an auxiliary metal layer, such as an Ru layer, whose surface oxidation state can vary in a substrate or among substrates, variation of plating in the same substrate or among substrates can be minimized.

[0075] The plating time for the first-step electroplating is, for example, one second to ten minutes. By carrying out the first-step electroplating for such a period of time, the plated metal can be deposited uniformly on the surface of the auxiliary metal layer 20 of Ru, and the electric current, flowing between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, can be stabilized.

[0076] Next, second-step electroplating is carried out for a predetermined time (t_3 - t_4) while controlling the electric cur-

rent, flowing between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at the electric current C_1 (CC mode) which is appropriate to fill the plated metal into the via holes 12, as shown FIG. 9B. In the electroplating method of this embodiment, a high electric current is allowed to flow between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220 at the initial stage of the first-step electroplating (CV-mode plating), and the high electric current is then rapidly changed to the electric current C_1 appropriate to fill the plated metal into the via holes 12. The second-step electroplating (CC-mode plating) is carried out at the controlled constant current C_1 for a period of time necessary to deposit the intended amount of plating. This electroplating method allows the plated metal (copper) to deposit preferentially in the bottoms of the via holes 12, i.e., in a bottom-up manner, making it possible to fill the plated metal into the via holes 12 without producing defects, such as voids, in the embedded plated metal.

[0077] During the period from immersion of the substrate W in the plating solution Q until the completion of electroplating, the stirring paddle 232 is reciprocated parallel to the substrate W, as necessary, to stir the plating solution Q between the regulation plate 224 and the substrate W. If strong stirring of the plating solution is continued after the aspect ratio of the via holes has decreased, with the progress of plating, to such a level that the plating solution can easily reach the plated metal surface, it is likely that the growth of the plated film will slow down and it will take a long time to complete via-filling plating. In such a case, it is preferred to reduce the intensity of stirring of the plating solution when plating has progressed to a certain degree. Upon completion of the plating, the application of a voltage between the anode 220 and the copper seed layer 22 (and the auxiliary metal layer 20) of the substrate W is stopped. Thereafter, the two substrate holders 160, each loaded with the substrate W, are held again by the second transfer robot 174b and withdrawn from the plating tanks 186.

[0078] The two substrate holders 160 are then transferred to the second water-cleaning device 168b in the same manner as described above, where the surfaces of the substrates are cleaned by immersing the substrates in pure water held in the water-cleaning tanks 184b. Thereafter, the substrate holders 160, loaded with the substrates, are transferred to the blowing device 172 in the same manner as described above, where the plating solution and water droplets are removed from the substrate holders 160 by blowing air or an inert gas onto the substrate holders 160. Thereafter, the substrate holders 160, loaded with the substrates, are returned to the stocker 164 and are each suspended and held at a predetermined position in the stocker 164.

[0079] The second transfer robot 174b sequentially repeats the above operations to sequentially return substrate holders 160, each loaded with a substrate after plating, to predetermined positions in the stocker 164 and suspend the substrate holders 160 in the stocker 164. On the other hand, two substrate holders 160 loaded with substrates after plating, which have been returned to the stocker 164, are simultaneously gripped by the second transfer robot 174a, and are placed on the substrate attachment/detachment stages 162 in the same manner as described above.

[0080] The first transfer robot 128, disposed in the clean space 114, takes the substrate out of the substrate holder 160 on the substrate attachment/detachment stage 162 and transfers the substrate to one of the cleaning/drying devices 124. In

the cleaning/drying device 124, the substrate, which is held in a horizontal position with the front surface facing upwardly, is cleaned, e.g., with pure water and then spin-dried by rotating it at a high speed. Thereafter, the substrate is returned by the first transfer robot 128 to the substrate cassette mounted on the loading/unloading port 120, thereby completing the sequence of plating operations.

[0081] It is also possible to carry out the first-step electroplating while controlling the voltage, applied between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at a voltage V_1 (CV mode) higher than a voltage V_2 ($V_1 > V_2$) which is necessary for an electric current, appropriate to fill the plated metal into the via holes 12, to flow stably between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220.

[0082] FIGS. 11A and 11B illustrate an electroplating method according to another embodiment of the present invention. In this embodiment, a substrate W is first immersed in the plating solution Q for a predetermined time (t_5 - t_6) without applying a voltage between the anode 220 and the copper seed layer 22 (and the auxiliary metal layer 20) of the substrate W. Subsequently, first-step electroplating of the substrate W is carried out for a predetermined time (t_6 - t_7) while controlling the voltage, applied between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at a voltage V_3 (CV mode) which is necessary for an electric current C_3 , appropriate to fill the plated metal into the via holes 12, to flow stably between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220. Subsequently, CC-mode second-step electroplating of the substrate W is carried out while controlling the electric current, flowing between the copper seed layer 22 (and the auxiliary metal layer 20) and the anode 220, at stepwise increasing currents: an electric current C_3 for a predetermined time (t_7 - t_8), an electric current C_4 for a predetermined time (t_8 - t_9) and an electric current C_5 for a predetermined time (t_9 - t_{10}). The electric currents C_4 and C_5 are also appropriate to fill the plated metal into the via holes 12.

[0083] As the plated metal gradually deposits in the via holes 12 with the progress of electroplating, the aspect ratio of the unfilled portion of each via hole 12 gradually changes (decreases). The lower the aspect ratio is, the easier is via-filling plating at a high current with stable bottom-up growth of a plated film. Accordingly, the plating time can be shortened and the productivity can be increased by stepwise changing (increasing) the electric current, flowing between the substrate and the anode, in response to change in the degree of filling of the plated metal into the via holes 12, i.e., change in the aspect ratio of the unfilled portion of each via hole.

[0084] Also in the case of a substrate W having an auxiliary metal layer 20 of Ru, formed on a barrier layer 14 that covers the entire substrate surface including the interior surfaces of via holes 12, as shown in FIG. 2, a plated metal can be filled into the via holes 12 without producing defects, such as voids, in the embedded plated metal by the electroplating method of the present invention. In particular, the substrate W is first subjected to the above-described pretreatment by immersing the substrate W in the pretreatment solution. After the pretreatment, the substrate W is immersed in a plating solution without applying a voltage between the auxiliary metal layer 20 of the substrate W and the anode 220 disposed opposite the substrate W, thereby replacing the pretreatment solution in the via holes 12 with the plating solution. Subsequently, first-

step electroplating of the substrate W is carried out while controlling the voltage (CV mode), applied between the auxiliary metal layer 20 of the substrate w and the anode 220, to be equal to or higher than a voltage which is necessary for an electric current, appropriate to fill the plated metal into the via holes 12, to flow stably between the substrate W and the anode 220. Subsequently, second-step electroplating of the substrate W is carried out while controlling the electric current (CC mode), flowing between the auxiliary metal layer 20 of the substrate W and the anode 220, at an electric current which is appropriate to fill the plated metal into the via holes 12.

[0085] When, unlike the method of carrying out the first-step electroplating at a controlled voltage as shown in FIG. 9A, electroplating of the substrate W to fill the plated metal into the via holes 12 is carried out for a predetermined time (t_{11} - t_{12}) while controlling the electric current, flowing between the auxiliary metal layer 20 and the anode 220, at a current C_6 (CC mode) which is appropriate to fill the plated metal into the via holes 12, as shown in FIG. 12B, the voltage, applied between the auxiliary metal layer 20 and the anode 220, initially takes a low value and gradually increases and, after the elapse of a certain period of time, reaches an approximately constant voltage V_6 , as shown by the solid line in FIG. 12A. Therefore, a voltage to be equal to or higher than this voltage V_6 is used as a CV mode entry voltage.

[0086] Compared to the above-described case, shown by the broken line in FIG. 12A, where the CC-mode electroplating is carried out on the substrate having the copper seed layer 22 formed on the auxiliary metal layer 20, it takes a longer time in this case for the applied voltage to reach the constant voltage V_6 . This is because of the larger area of the auxiliary metal layer 20 as compared to the case where the copper seed layer 22 partly covers the auxiliary metal layer 20 in the via holes 12, as shown in FIGS. 2 and 3, on the other hand, the plated metal can be deposited uniformly on the auxiliary metal layer 20 shown in FIG. 2 by carrying out the CV-mode first-step electroplating for a longer period of time. After the plated metal begins to deposit uniformly on the surface of the auxiliary metal layer 20, an electric current, which is appropriate to fill the plated metal into the via holes 12, flows stably between the auxiliary metal layer 20 and the anode 220. By carrying out the second-step electroplating after the first-step electroplating while controlling the electric current (CC mode), the plated metal can be finally filled into the via holes 12 without producing a defect, such as a void, in the embedded plated metal.

[0087] The following examples illustrate the present invention in greater detail and are not intended to limit the present invention in any manner.

EXAMPLE 1

[0088] A substrate sample was produced by a process comprising: forming via holes, having a diameter of 7 μm and a depth of 85 μm , in a surface of a silicon wafer; forming a 100-nm thick Ti barrier layer by PVD on an entire wafer surface, including interior surfaces of the via holes; forming a 10-nm thick Ru layer as an auxiliary metal layer by CVD on a surface of the barrier layer; and forming a 100-nm thick copper seed layer by PVD on a surface of the auxiliary metal layer.

[0089] The sample was immersed in pure water (deaerated DIW), having a dissolved oxygen concentration of not more than 2 mg/L, for 1 to 10 minutes to carry out pretreatment

(pre-wetting treatment) of the sample. The sample after the pretreatment was immersed in a plating solution for 30 seconds without applying a voltage between an anode and the copper seed layer (and the auxiliary metal layer) of the sample. The plating solution had the following composition; copper sulfate pentahydrate 200 g/L; sulfuric acid 50 g/L; chlorine 50 mg/L; and additives in appropriate amounts. Next, while keeping the sample immersed in the plating solution, a voltage of 0.3 V was applied between the anode and the copper seed layer (and the auxiliary metal layer) of the sample for 2 minutes to carry out first-step electroplating in a CV mode. Subsequent to the first-step electroplating, second-step electroplating in a CC mode was carried out by passing an electric current at 0.3 A/dm² (ASD) between the anode and the copper seed layer (and the auxiliary metal layer) of the sample for 120 minutes.

EXAMPLE 2

[0090] A substrate sample was produced by a process comprising: forming via holes, having a diameter of 7 μm and a depth of 85 μm , in a surface of a silicon wafer; forming a 100-nm thick Ti barrier layer by PVD on an entire wafer surface, including interior surfaces of the via holes; and forming a 10-nm thick Ru layer as an auxiliary metal layer by CVD on a surface of the barrier layer.

[0091] The sample was immersed in pure water (deaerated DIW), having a dissolved oxygen concentration of not more than 2 mg/L, for 1 to 10 minutes to carry out pretreatment (pre-wetting treatment) of the sample. The sample after the pretreatment was immersed in the same plating solution as used in Example 1 for 30 seconds without applying a voltage between an anode and the auxiliary metal layer of the sample. Next, while keeping the sample immersed in the plating solution, a voltage of 0.3 V was applied between the anode and the auxiliary metal layer of the sample for 5 minutes to carry out first-step electroplating in a CV mode. Subsequent to the first-step electroplating, second-step electroplating in a CC mode was carried out by passing an electric current at 0.3 A/dm² (ASD) between the anode and the auxiliary metal layer of the sample for 120 minutes.

COMPARATIVE EXAMPLE 1

[0092] The same substrate sample as used in Example 1 was immersed in pure water (deaerated DIW), having a dissolved oxygen concentration of not more than 2 mg/L, for 1 to 10 minutes to carry out pretreatment (pre-wetting treatment) of the sample. The sample after the pretreatment was immersed in the same plating solution as used in Example 1 for 30 seconds without applying a voltage between an anode and the copper seed layer (and the auxiliary metal layer) of the sample. Next, while keeping the sample immersed in the plating solution, electroplating in a CC mode was carried out by passing an electric current at 0.3 A/dm² (ASD) between the anode and the copper seed layer (and the auxiliary metal layer) of the sample for 120 minutes.

COMPARATIVE EXAMPLE 2

[0093] The same substrate sample as used in Example 2 was immersed in pure water (deaerated DIW), having a dissolved oxygen concentration of not more than 2 mg/L, for 1 to 10 minutes to carry out pretreatment (pre-wetting treatment) of the sample. The sample after the pretreatment was immersed in the same plating solution as used in Example 1

for 30 seconds without applying a voltage between an anode and the auxiliary metal layer of the sample. Next, while keeping the sample immersed in the plating solution, electroplating in a CC mode was carried out by passing an electric current at 0.3 A/dm² (ASD) between the anode and the auxiliary metal layer of the sample for 120 minutes.

[0094] FIG. 13 shows the relationships between time and the voltage applied between the anode and the substrate sample, observed in Examples 1 and 2, and Comp. Examples 1 and 2. FIG. 14 shows the relationships between time and the electric current flowing between the anode and the substrate sample, observed in Examples 1 and 2, and Comp. Examples 1 and 2. As can be seen in FIG. 13, it takes time for the voltage to stabilize in Comp. Examples 1 and 2. Especially in Comp. Example 2 in which electroplating is carried out on the Ru layer, it takes a considerable time for the voltage to stabilize. As can be seen in FIG. 14, the high electric current at the initial stage of plating rapidly decreases to an electric current appropriate for via-filling plating in Examples 1 and 2.

[0095] FIGS. 15 and 16 illustrate via holes of the substrate sample after filling the plated metal (copper) into the via holes in Examples 1 and 2, respectively; and FIGS. 17 and 18 illustrate via holes of the substrate sample after filling the plated metal (copper) into the via holes in Comp. Examples 1 and 2, respectively.

[0096] As can be seen in FIGS. 15 and 16, the plated metal (copper) 304, free of defects such as voids, is embedded in the via holes 302 provided in the substrate sample 300 in Examples 1 and 2. In contrast, as can be seen in FIG. 17, voids v are formed in the bottom of the plated metal (copper) 304 embedded in the via holes 302 of the substrate sample 300 in Comp. Example 1. Further, as can be seen in FIG. 18, voids V are formed in the middle of the plated metal (copper) 304 embedded in the via holes 302 of the substrate sample 300 in Comp. Example 2. The results are summarized in Table 1 below.

TABLE 1

Plating conditions	State of plated metal embedded
Example 1	No void
Example 2	No void
Comp. Example 1	Voids formed in the bottoms of vias
Comp. Example 2	Voids formed in the middle of vias

[0097] While the present invention has been described with reference to preferred embodiments, it is understood that the present invention is not limited to the embodiments described above, but is capable of various changes and modifications within the scope of the inventive concept as expressed herein.

What is claimed is:

1. An electroplating method comprising:

preparing a substrate having via holes formed in a surface; immersing the substrate in a pretreatment solution to carry out pretreatment of the substrate;

immersing the substrate in a plating solution without applying a voltage between the substrate and an anode disposed opposite the substrate, thereby replacing the pretreatment solution in the via holes with the plating solution;

carrying out first-step electroplating of the substrate while controlling the voltage, applied between the substrate and the anode, to be equal to or higher than a voltage which is necessary for an electric current, appropriate to fill a plated metal into the via holes, to flow stably between the substrate and the anode; and then

carrying out second-step electroplating of the substrate while controlling the electric current, flowing between the substrate and the anode, at an electric current appropriate to fill the plated metal into the via holes.

2. The electroplating method according to claim 1, wherein the substrate is immersed in the plating solution for 10 to 60 seconds without applying a voltage between the substrate and the anode.

3. The electroplating method according to claim 1, wherein the first-step electroplating is carried out for one second to ten minutes.

4. The electroplating method according to claim 1, wherein the second-step electroplating is carried out in such a manner that the electric current, flowing between the substrate and the anode, is changed in a stepwise fashion.

5. The electroplating method according to claim 1, wherein the plated metal is copper, and a metal other than copper is exposed on at least part of surfaces of the via holes.

6. The electroplating method according to claim 5, wherein the metal other than copper is ruthenium or cobalt, or an alloy thereof.

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