































































































































































connect is connected to a second metal conductor of said plurality of metal conductors, wherein said second metal interconnect comprises a second copper layer; and

a first semiconductor chip under said first interconnection scheme, wherein said first semiconductor chip comprises a first metal bump on a first metal pad of said first semiconductor chip, wherein said first metal bump comprises a third copper layer with a thickness between 5 and 30 micrometers, wherein said first semiconductor chip is connected to a third metal interconnect of said second interconnection scheme through said first metal bump.

19. The chip package of claim 18, wherein said compound comprises a SiO<sub>2</sub> compound.

20. The chip package of claim 18, further comprising a first passive component under said first interconnection scheme.

21. The chip package of claim 18, wherein said first semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

22. The chip package of claim 18, wherein said first metal layer is a silver-containing layer.

23. The chip package of claim 18, wherein said solid layer further comprises a third region opposite to said second region, wherein said third region is between said first region and another edge of said solid layer, wherein said plurality of metal conductors in said third region.

\* \* \* \* \*

30