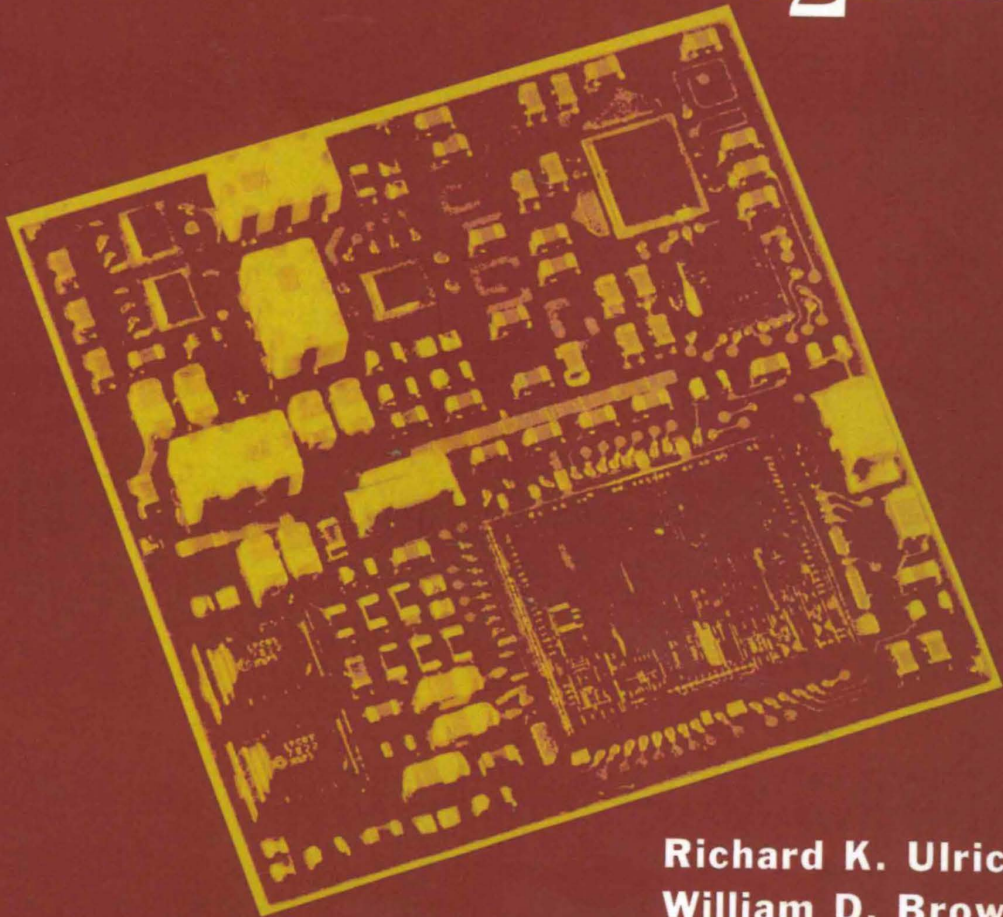


# ADVANCED ELECTRONIC PACKAGING

2<sup>nd</sup> Edition



**Richard K. Ulrich**  
**William D. Brown**

*IEEE Press Series on Microelectronic Systems*  
*Stuart K. Tewksbury and Joe E. Brewer, Series Editors*

Copyright © 2006 by the Institute of Electrical and Electronics Engineers, Inc. All rights reserved.

Published by John Wiley & Sons, Inc. Published simultaneously in Canada.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning, or otherwise, except as permitted under Section 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4470, or on the web at [www.copyright.com](http://www.copyright.com). Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, (201) 748-6011, fax (201) 748-6008, or online at <http://www.wiley.com/go/permission>.

**Limit of Liability/Disclaimer of Warranty:** While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. No warranty may be created or extended by sales representatives or written sales materials. The advice and strategies contained herein may not be suitable for your situation. You should consult with a professional where appropriate. Neither the publisher nor author shall be liable for any loss of profit or any other commercial damages, including but not limited to special, incidental, consequential, or other damages.

For general information on our other products and services or for technical support, please contact our Customer Care Department within the United States at (800) 762-2974, outside the United States at (317) 572-3993 or fax (317) 572-4002.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print, may not be available in electronic formats. For more information about Wiley products, visit our web site at [www.wiley.com](http://www.wiley.com).

*Library of Congress Cataloging-in-Publication Data is available.*

ISBN-13 978-0-471-46609-X

ISBN-10 0-471-46609-3

Printed in the United States of America

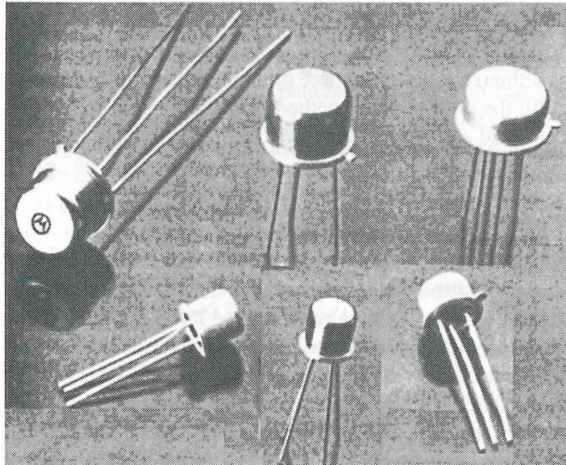
10 9 8 7 6 5 4 3 2 1

second-level interconnection is the connection between a package containing more than one chip, which are interconnected via an imbedded conductor network in a substrate, and a PWB. However, the substrate on which the chips are mounted prior to being inserted into a package actually qualifies as a PWB in the broadest sense of the definition of a PWB.

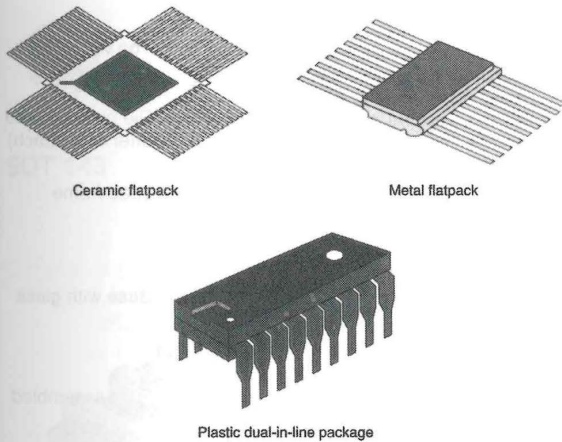
## 1.4 BRIEF HISTORY OF MICROELECTRONIC PACKAGING TECHNOLOGY

It is probably impossible to determine the exact date that electronic packaging began to be viewed as an engineering and science technology. However, microelectronics packaging technology began in earnest in response to the discovery of the transistor in the late 1940s and has continued to evolve to serve the increasing complexity and performance of ICs since that time. Early transistors were of the alloy structure and were housed in plastic packages, providing little in the way of protection for the device. However, once the military became interested in these new devices for high-reliability applications, the need for hermeticity to prevent transistor gain degradation and junction leakage current due to contamination and moisture led to the development of the metal transistor outline (TO) packages shown in Figure 1.5. These packages consist of a gold-plated metal base containing external leads (generally three or four leads for discrete transistors), commonly referred to as a header, and a metal lid that is sealed to the header by welding in an inert atmosphere, such as nitrogen or argon, to ensure that moisture and other contaminants are excluded from the ambient in which the electronic device must operate.

With the development of silicon planar technology, electronic packages were developed to accommodate the large number of I/O leads of ICs. Initially, ICs were merely packaged in higher pin count versions of the TO can, which quickly became inadequate to handle the more complex and higher I/O integrated circuits. Consequently, the 1960s saw a rapid proliferation of new packages for ICs. Because of cost considerations, the lack of standards for package design, and difficulty in mounting some packages onto PWBs, only



**Figure 1.5** Photograph of a selection of TO packages.



**Figure 1.6** Dual-in-line and flatpack packages.

the “flatpack” and dual-in-line package (DIP) survived. Examples of these two major types of IC packages are shown in Figure 1.6. It should be noted that the flatpack leads, which extend from all four sides, are essentially planar with the package, while those of the DIP are perpendicular to the body of the package and exit on two sides. This has some implications in terms of mounting to PWBs. In particular, the DIP is ideally suited for insertion mounting onto PWBs via plated through holes (PTHs) by automatic insertion machines and wave soldering, whereas the flatpack has to be mounted using special methods and tools. Consequently, the DIP became the primary package for ICs and, along with through-hole PWBs, has long dominated the electronics assembly market.

Packaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard. One of the early attempts to develop a low-cost, hermetic package resulted in the CerDIP, which was a DIP constructed of two pieces of sandwiched ceramic with the leads protruding from between the slabs of ceramic as shown in Figure 1.7. The two pieces of ceramic were held together using a low-melting-temperature glass, which also acted as a seal, thereby providing hermeticity. Unfortunately, the glass used originally outgassed moisture, which created reliability problems. The development of vitreous sealing glasses, which do not outgas moisture, coupled with performing the sealing operation in a nitrogen ambient reduced the reliability problem to a tolerable level.

Driven by the need to further reduce packaging costs, the industry pursued fully automated manufacturing of plastic DIPs. The result of this effort was a low-cost plastic package, which was transfer molded around an IC chip that had previously been die and wire bonded to a lead frame. Unfortunately, plastics are not hermetic because of their high permeability to moisture and poor adhesion to the metal leads, which provides a path for water vapor to access the IC. Furthermore, the resins and fillers either initially contained undesirable contaminants (e.g., Cl and Na) or they were polymerization by-products of the plastics, leading to degradation of the IC. These problems were eventually resolved by improving the encapsulant applied to the chip prior to plastic packaging and improvement in the properties of the plastics themselves.

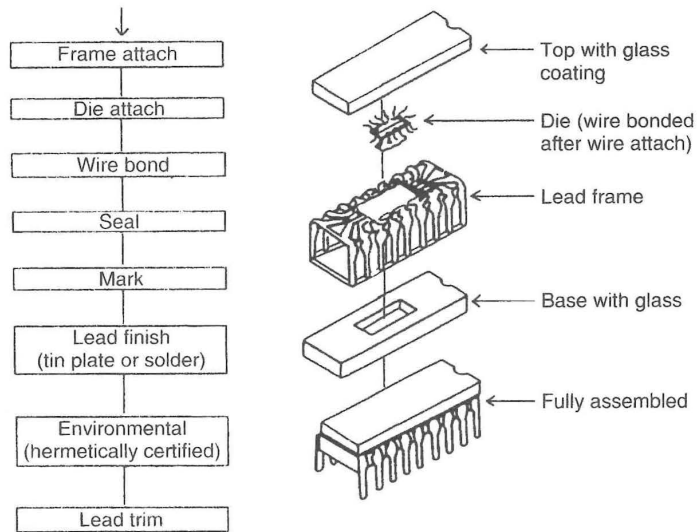


Figure 1.7 Assembly sequence for CERDIP.

The 1970s and 1980s saw the development of several types of IC packages, including surface-mount packages (SMPs), in response to a need for higher density PWBs. When mounted on a PWB, the SMP's leads do not penetrate the PWB like those of through-hole-mounted packages. Thus, they can be mounted on the side of a PWB containing conductor traces. Consequently, SMPs can be mounted on both sides of a PWB. Mounting of SMPs to PWBs is accomplished by reflow solder technology, which gave new life to the flatpack, actually the first surface-mount package. Also, small outline packages (SOPs), which resemble miniature versions of DIPs, as shown in Figure 1.8, were developed for use in surface-mount technology (SMT). The two types of small outline packages are the small outline transistor (SOT) and the small outline IC (SOIC) shown in Figure 1.9. This same period saw the development of chip carriers and quadpacks (or quad flatpacks). The chip carrier is available in both leadless and leaded versions, as well as with plastic and

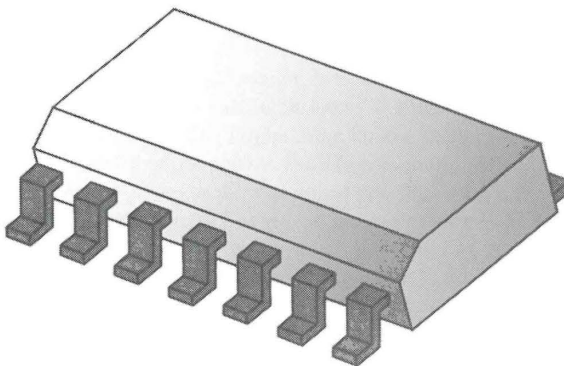
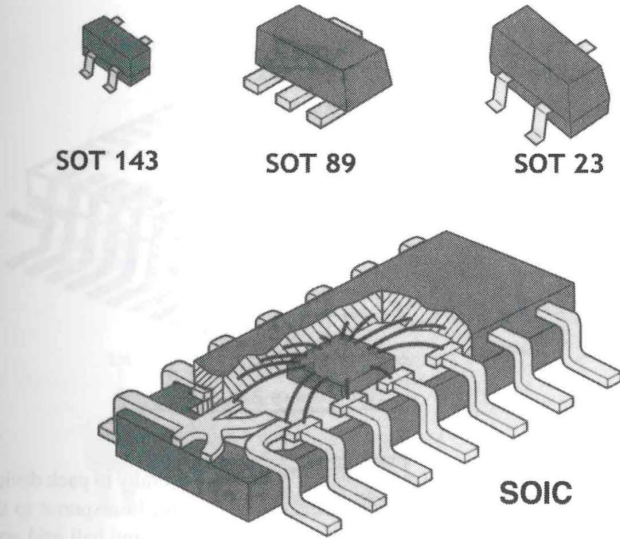
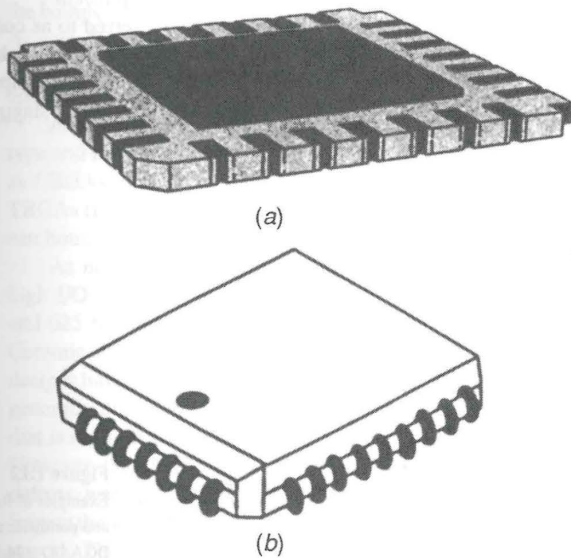


Figure 1.8 Small outline package (SOP).

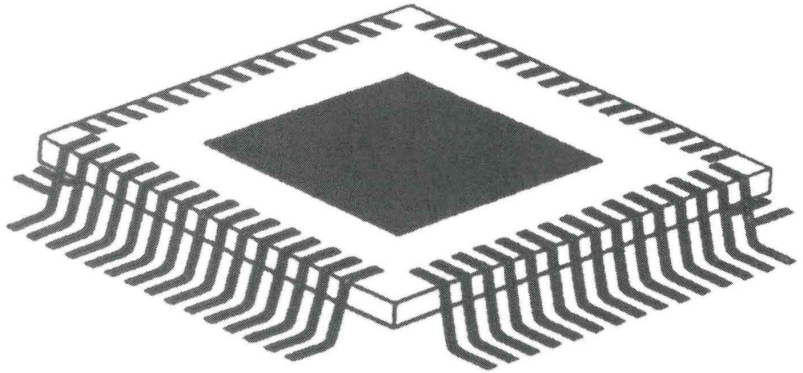


**Figure 1.9** Small outline transistor (SOT) and small outline integrated circuit (SOIC) packages.

ceramic bodies (see Fig. 1.10). These type packages conform very closely to the size of the ICs they contain and have leads on all four sides. The quadpack, one of the earliest plastic surface-mount IC packages, comes in a variety of sizes and lead configurations and also has leads on all four sides as shown in Figure 1.11. The terminal pitches vary from 0.3 to 1.0 mm (10 to 50 pins/cm<sup>2</sup>). Thus, the quadpack (I/O  $\approx$  300) is generally used when the chip I/O requirements are greater than can be addressed using a DIP (I/O  $\approx$  64 with 10 pins/cm<sup>2</sup>).



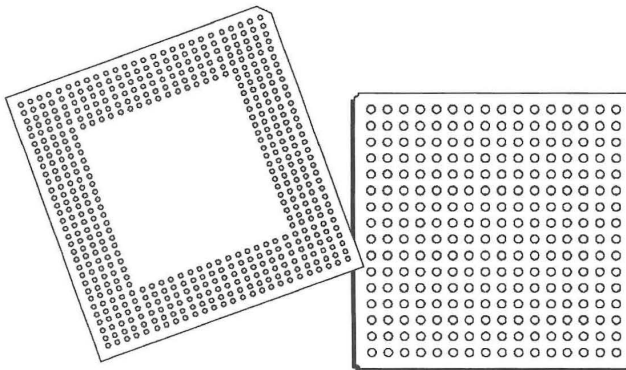
**Figure 1.10** (a) Ceramic leadless chip carrier and (b) plastic leadless chip carrier.



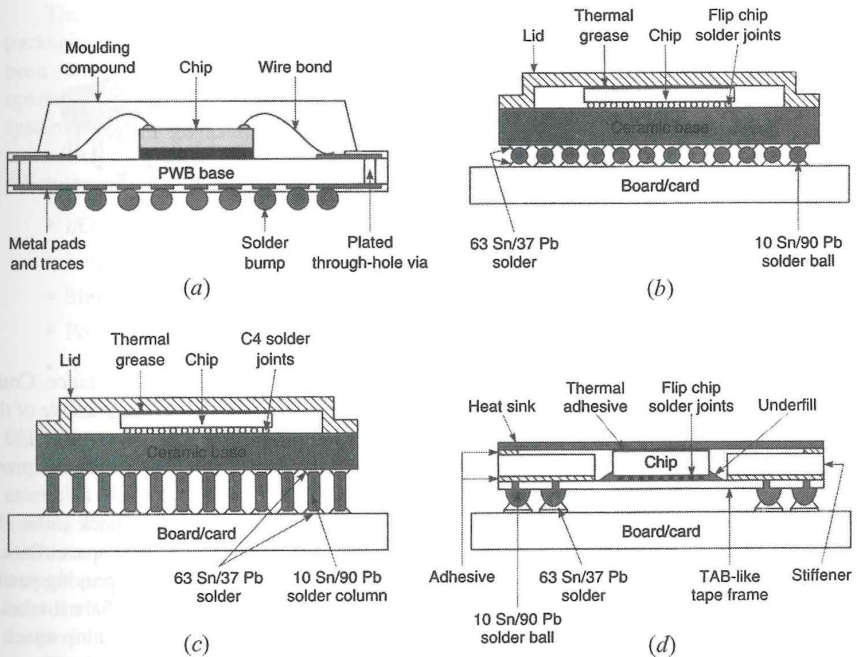
**Figure 1.11** Quad flatpack (or quadpack).

The ultimate goal for high-performance electronic systems is generally to pack devices as close together as possible in order to minimize circuit path length. In response to this need, the early 1990s saw the emergence of both pin grid array (PGA) and ball grid array (BGA) packages as a replacement for quad flatpacks (QFPs), primarily because of their high I/O density (the terminals are arrayed on part or all of the bottom of the package), minimum footprint, and shorter electrical paths, which means that they have better electrical performance. For QFPs, lead counts higher than 200 require lead spacings of 0.5 mm, and for 300 leads, the spacing approaches 0.3 mm. Unfortunately, as spacings become tighter, the yield falls exponentially with lead spacing. For I/Os greater than 250, the PGA and BGA have an advantage over the QFP in that they always occupy less space than a QFP. However, PGA and BGA construction is inherently more expensive than that of the QFP because of costs associated with the component carrier substrate. The primary terminal pitches of the BGA are 1.27 and 1.5 mm, yielding a mounting density of 40 to 60 pins/cm<sup>2</sup>.

The BGA package evolved from flip-chip technology, also referred to as controlled-collapse chip connect (C4), pioneered by IBM for ICs [6]. Thus, the BGA package can be identified by the solder bumps on the bottom of the package. The solder bumps can be arranged in a uniform full-matrix array (i.e., over the entire bottom surface), a staggered full



**Figure 1.12**  
Examples of full matrix  
and perimeter array  
BGA I/O solder bumps.

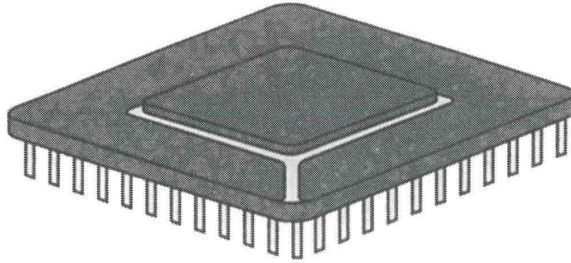


**Figure 1.13** Conceptual sketch of (a) plastic ball grid array, (b) ceramic ball grid array, (c) ceramic column grid array, and (d) tape ball grid array.

array, or around the perimeter in a multiple number of rows (see Fig. 1.12). No matter how the bumps are arranged, the result is a smaller footprint than that of conventional packages. As noted previously, for a given amount of real estate, the BGA package provides more I/O than QFPs. Thus, the BGA package is considered the package of choice for high-density and high-I/O ICs.

As is the case with other packages, BGAs have been broadly classified according to the type and form of the die carrier substrate material. Thus, the packages have been classified as CBGAs (ceramic), CCGAs (ceramic column), PBGAs (plastic), MBGAs (metal), and TBGAs (tape). These packages, some of which are conceptually illustrated in Figure 1.13, can house either a single chip or multiple chips.

As noted previously, one of the big advantages of BGA packages is that they offer high I/O. Typical I/O for several types of BGAs are 400 I/O PBGAs, 736 I/O TBGAs, and 625 I/O CBGAs, although BGA packages are available with more than 2000 leads. Ceramic column BGAs are available with I/Os greater than 1000. Current and planned designs have solder-bump-array pitches in the range of 40 to 150  $\mu\text{m}$ . The solder bumps are generally of tin-lead or tin-lead-silver composition. Thus, the BGA is a leadless package that is not susceptible to bent or skewed leads, which means that it can be easily handled. However, there are some aspects of BGA packages of concern. In particular, solder joint defects, warpage during reflow, a large variation in solder ball size, the inability to visually inspect the solder joints, reduced resistance to thermal cycling, and problems associated with rework. These can be overcome with good design, process development, and process control



**Figure 1.14** Pin grid array package.

so that the resulting yield makes inspection and rework of minor importance. Considering all the pluses and minuses, BGA still appears to be the surface-mount package of the future for both single-chip and multichip packaging. Similarly, the PGA package (I/O  $\approx$  600), illustrated in Figure 1.14, is used when the I/O requirement is higher than that provided by quadpacks.

There always has been and will continue to be motivation to pack more electronic functionality and higher speed performance into a smaller volume of space. Packaging of ICs is one area that offers attractive benefits for reducing size and improving performance by either eliminating the package or reducing the size to the point where it takes up very little more space than the IC. Elimination of the package [i.e., direct chip attach (DCA)] still presents some problems where full functionality and reliability testing are concerned. In other words, the ability to test and burn-in bare die has not yet reached the quality and reliability levels comparable to the same die in a package. Consequently, packaging ICs for testing and burn-in is still very attractive. In the late 1990s, the BGA concept was applied to a packaging technology referred to as chip-scale packaging (CSP) by reducing the terminal pitch to 1.0 mm or less for a mounting density greater than 100 pins/cm<sup>2</sup> [7, 8]. CSP contributed significantly to a reduction in the size, weight, and performance of products such as the cellular phone.

CSPs are essentially “packages” that ruggedize the IC for ease of handling, testing, and assembly. Thus, CSPs are a viable substitute for “known good die” (KGD) if low-cost test and burn-in methods are not available for bare die. CSPs, also referred to as slightly larger than IC carrier (SLICC), are generally defined as packages that are equal to or smaller than 1.2 times the bare die size. Microball grid array, miniball grid array, and micro-SMT packages fit this definition since they are of minimum size and employ direct surface mounting instead of wire bonds. In fact, in excess of 60 different chip-scale package types have been proposed over the years. The primary difference in the various types is the material layers, which serve as compliant members, space transformers, and mechanical protection, between the silicon and the bump array. These material layers serve to categorize the CSPs into tape carrier (flexible laminate), resin mold, ceramic carrier, silicon-based, rigid laminate, lead-on-chip (LOC), and lead frame types.

CSPs are designed to be flip-chip mounted using conventional equipment and solder reflow. Essentially, CSPs take advantage of the attributes of a flip chip in a surface-mountable package. Thus, CSPs offer a method for subjecting ICs to full functional and reliability testing using a packaging technology while essentially maintaining the size and performance of bare die.

The 1980s also marked the turning point in the way electronic engineers viewed IC packaging technology. As noted previously, for many years the electronics industry had been concentrating on increasing the performance of ICs (i.e., more circuitry/silicon area operating at higher speeds) with little consideration of the fact that ICs in an electronic system must communicate with each other through the packages that contain them. As a result of the trend toward higher circuit densities and operating speeds on a chip, the following effects became important considerations for packaging engineers:

- I/O requirements increased sharply.
- Signal transition time between chips became a factor limiting system speed.
- Signal integrity between silicon chips degraded.
- Power requirements per chip increased.
- A problem with heat dissipation was created.

All of these factors forced electronic packaging technology into the spotlight, resulting in a reconsideration of how ICs were being packaged. From this reconsideration evolved multichip packaging, for example, multichip module (MCM) packaging technology [5], examples of which are shown in Figure 1.15. Although the basic concept of a multichip module was not new (hybrid circuits had been around for nearly 50 years), in the late 1980s and throughout the 1990s interest was renewed in mounting a multiple number of ICs in a single package in order to take advantage of inherently shorter interconnection distances between ICs. Thus, the development of MCM technology became an industry effort to push the performance of electronic systems to higher and higher levels.

The simplest definition of an MCM is that of a single electronic package containing more than one IC. The ICs are interconnected through a substrate. Based on this simple definition, an MCM combines high-performance ICs with a custom-designed common substrate structure, which provides mechanical support for the chips and multiple layers of conductors to interconnect them. This arrangement takes better advantage of the performance of the ICs than does interconnecting individually packaged ICs because the interconnect length is much shorter. The really unique feature of MCMs is the complex substrate structure, which is fabricated using multilayer ceramics, polymers, silicon, metals, glass-ceramics, laminates, and the like. Thus, multichip modules are not really new. They have been in existence since the first multichip hybrid circuit was fabricated. Conventional PWBs utilizing chip on board (COB), a technique where ICs are mounted and wire bonded directly to the board (direct chip attach), have also existed for some time. However, if packaging efficiency (also called silicon density), defined as the percentage of area on an interconnecting substrate that is occupied by silicon, is the guideline used to define an MCM, then many hybrid and COB structures with less than 30% silicon density do not qualify as MCMs. The fundamental (or basic) intent of MCM technology is to provide an extremely dense conductor matrix for the interconnection of bare IC chips. Consequently, some companies designated their MCM products as high-density interconnect (HDI) modules and others dropped the MCM designation for multichip packages (MCP).

MCM technology, still a viable technology today, played a major role in the evolution of multichip packaging in the 1990s, which includes three-dimensional (3D) stacking of ICs within a single package [9–13]. Although chips can be stacked physically without connecting them to each other to save board space, present development efforts focus on interconnected, stacked chips. One of the first commercial efforts to stack chips within a single package mated flash memory with static random-access memory (SRAM). However,

## *Second Edition* focuses on current practices and advanced packaging technologies

*Advanced Electronic Packaging, Second Edition* reflects the changes in the electronic packaging industry, as well as feedback from students, engineers, and educators since the publication of the *First Edition* in 1999. Like the *First Edition*, each chapter is authored by one or more acknowledged experts and then carefully edited to ensure a consistent level of quality and approach throughout.

Readers familiar with the *First Edition* will note several key changes. For example, organic and ceramic substrates are now covered in separate chapters. There are new chapters on passive devices, RF and microwave packaging, electronic package assembly, and cost evaluation and assembly. In addition, readers have access to the latest information and findings in such topics as:

- Packaging materials and applications
- Analytical techniques for materials
- Fabrication technologies and package design
- Electrical, mechanical, and thermal considerations
- Modeling and simulations
- MEMS packaging
- Reliability
- Three-dimensional packaging

All the hallmarks of the *First Edition*, which became an industry standard and a popular graduate-level textbook, have been retained. Examples illustrate real-world applications, which are then reinforced by the extensive use of exercises to enable readers themselves to place their newfound knowledge into practice. In addition, references are provided that guide readers to more in-depth information and primary resources in specialized topics.

Fully updated, this comprehensive reference remains the preeminent graduate-level textbook in its field as well as an essential reference for engineers and scientists.

**RICHARD K. ULRICH, PhD**, is a professor of chemical engineering at the University of Arkansas. He is a book editor and columnist on embedded passive technology, an NEMI committee member, an associate editor of *IEEE Transactions on Advanced Packaging*, and past chairman of the Dielectric Science and Technology Division of the Electrochemical Society.

**WILLIAM D. BROWN, PhD**, is Associate Dean for Research, College of Engineering, and Distinguished Professor of Electrical Engineering, University of Arkansas. Since 1991, he has played an active role in sponsoring and guiding research at the University's High Density Electronics Center (HiDEC), which is dedicated to advancing the state of the art in electronics packaging materials and technologies.



Subscribe to our free Engineering eNewsletter at  
[www.wiley.com/ewnewsletters](http://www.wiley.com/ewnewsletters)

Visit [www.wiley.com/ieee](http://www.wiley.com/ieee)

