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(54) **PILLAR BUMP WITH BARRIER LAYER**

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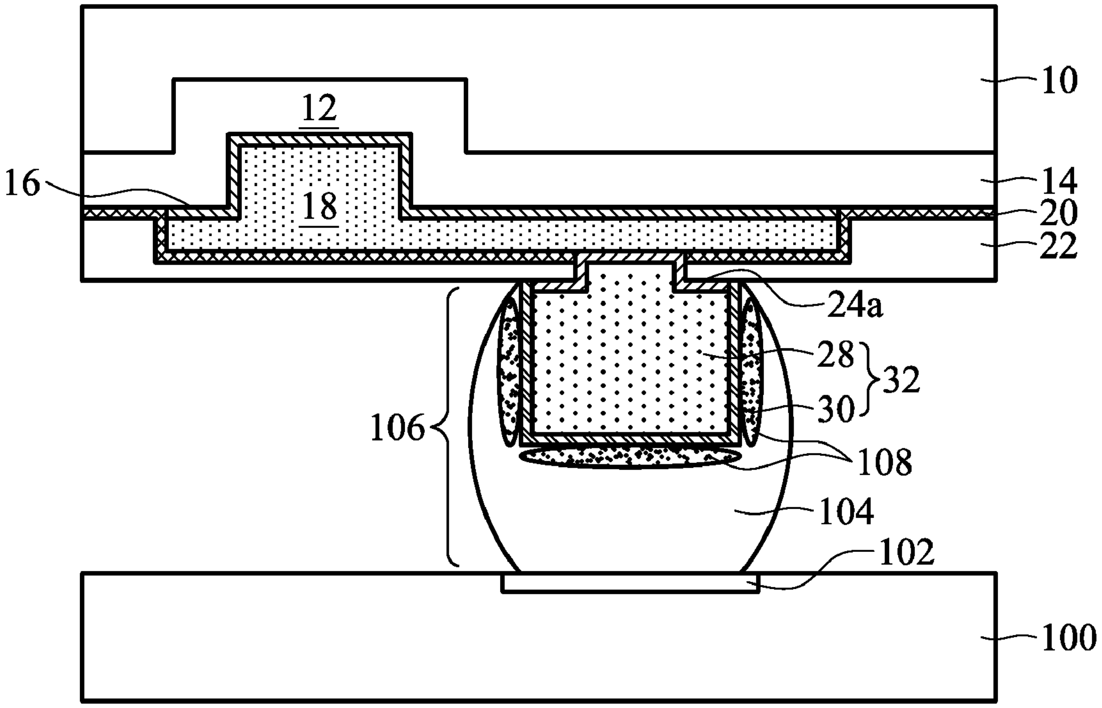
(57) **ABSTRACT**

A copper pillar bump has a surface covered with by a barrier layer formed of a copper-containing material layer including a group III element, a group IV element, a group V element or combinations thereof. The barrier layer depresses the copper diffusion and reaction with solder to reduce the thickness of intermetallic compound between the pillar pump and solder.



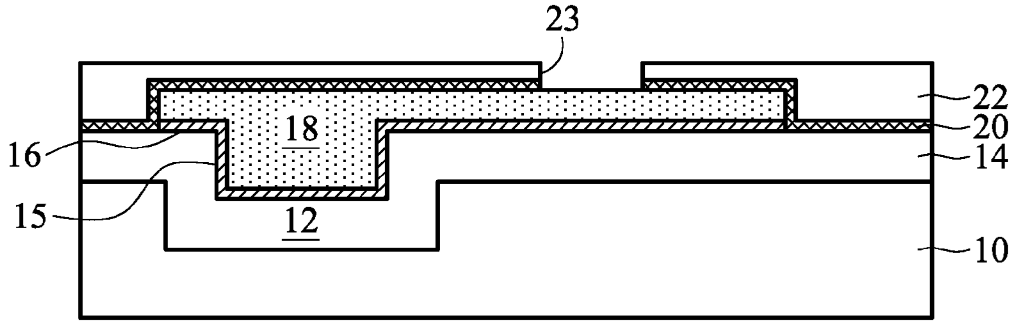


FIG. 1

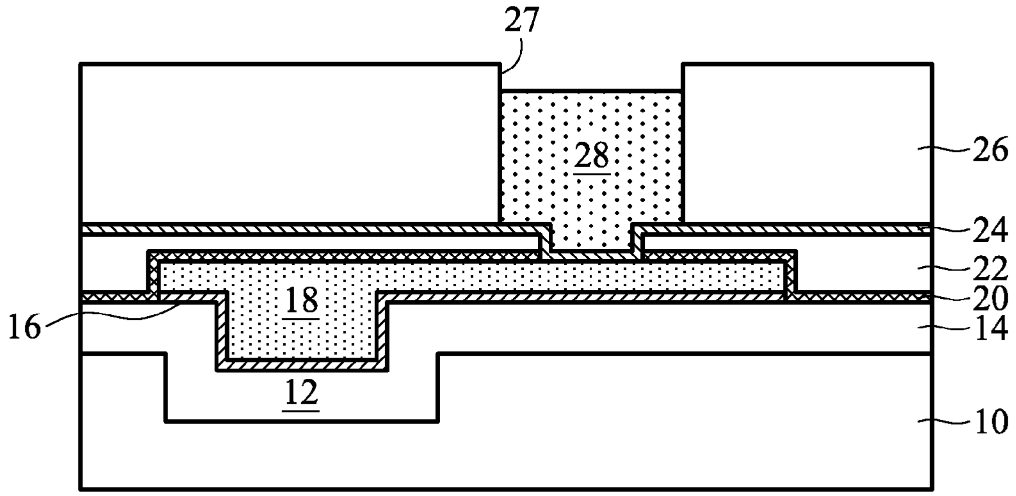


FIG. 2

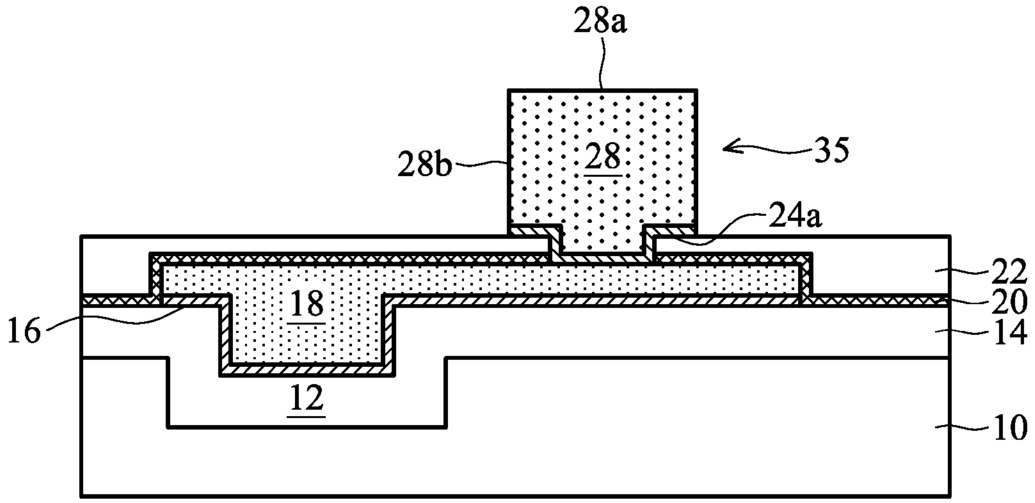

28a
35
28b
28
24a
22
20
18
16
14
12
10

FIG. 3

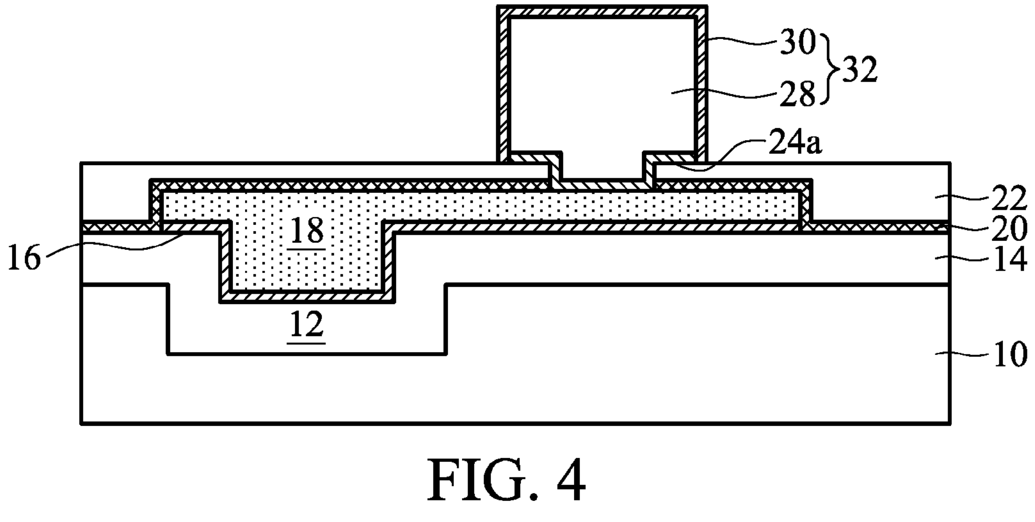

30
32
28
24a
22
20
18
16
14
12
10

FIG. 4

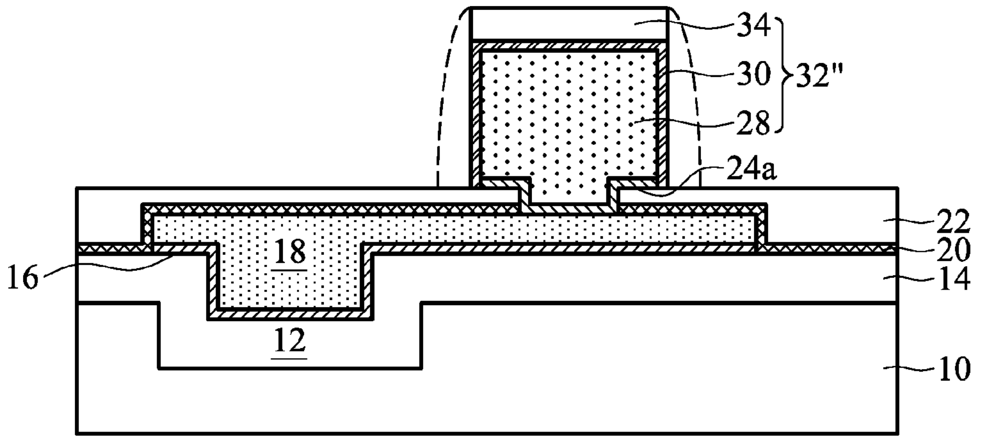

34
30
28
32"
24a
22
20
14
10
18
16
12

FIG. 5

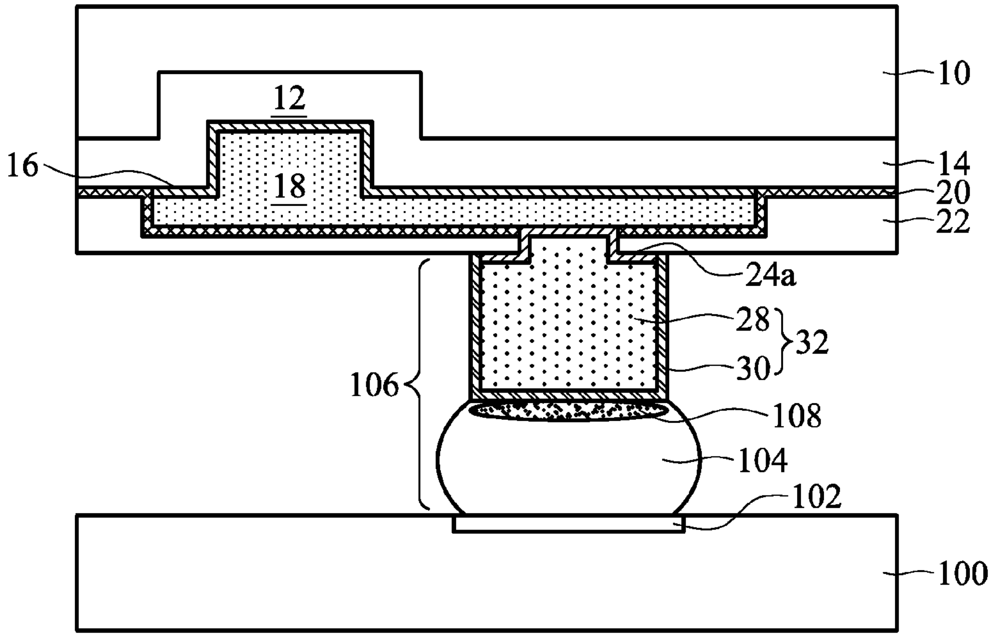

10
12
14
16
18
20
22
24a
28
30
32
106
108
104
102
100

FIG. 6

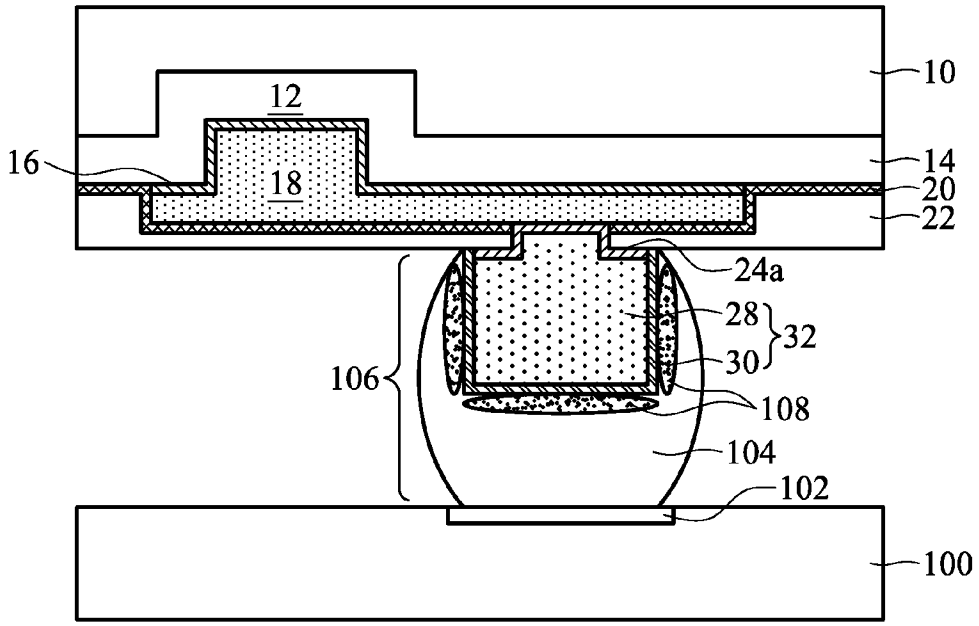


FIG. 7

PILLAR BUMP WITH BARRIER LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority of U.S. Provisional Patent Application Ser. No. 61/258,393, filed on Nov. 5, 2009, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to the fabrication of integrated circuit devices, and more particularly, to the fabrication of bump structures in integrated circuit devices.

BACKGROUND

[0003] Modern integrated circuits are made up of literally millions of active devices such as transistors and capacitors. These devices are initially isolated from each other, but are later interconnected together to form functional circuits. Typical interconnect structures include lateral interconnections, such as metal lines (wirings), and vertical interconnections, such as vias and contacts. Interconnections are increasingly determining the limits of performance and the density of modern integrated circuits. On top of the interconnect structures, bond pads are formed and exposed on the surface of the respective chip. Electrical connections are made through bond pads to connect the chip to a package substrate or another die. Bond pads can be used for wire bonding or flip-chip bonding.

[0004] Flip-chip packaging utilizes bumps to establish electrical contact between a chip's I/O pads and the substrate or lead frame of the package. Structurally, a bump actually contains the bump itself and a so-called under bump metallurgy (UBM) located between the bump and an I/O pad. An UBM generally contains an adhesion layer, a barrier layer and a wetting layer, arranged in this order on the I/O pad. The bumps themselves, based on the material used, are classified as solder bumps, gold bumps, copper pillar bumps and bumps with mixed metals. Recently, copper pillar bump technology is proposed. Instead of using solder bump, the electronic component is connected to a substrate by means of copper pillar bump, which achieves finer pitch with minimum probability of bump bridging, reduces the capacitance load for the circuits and allows the electronic component to perform at higher frequencies.

[0005] The Cu pillar bump flip-chip assembly has the following advantages: (1) better thermal/electric performance, (2) higher current carrying capacity, (3) better resistance to electromigration, thus longer bump life, (4) minimizing molding voids—more consistence gaps between Cu pillar bumps. Also, a lower cost substrate is possible by using Cu-pillar controlled solder spreading, eliminating lead-free teardrop design. However, there are concerns regarding the Intermetallic Compound (IMC) generated between the Cu pillar bump and the solder during annealing. When used with Sn solder material, sufficient Cu diffusion from Cu pillar bump into the solder forms thick IMC such as Cu_6Sn_5 and Cu_3Sn through the reaction between the diffused Cu and Sn in the solder. Thick IMC layers reduce mechanical strength of the Cu pillar bump because the IMC layers are brittle. The IMC becomes scallops and spalls off the interface. With thicker Sn solder, longer annealing process and abundant Cu source make Cu_3Sn thicker, and also the size of Cu_6Sn_5 becomes large. Total transfer of the ductile solder to harder IMC lowers the shear strength of the structure. The IMC formation will cause bump crack or unwanted stress, the thicker IMC also results in poor adhesion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The objects, features and advantages of this disclosure will become apparent by referring to the following detailed description of exemplary embodiments with reference to the accompanying drawings, wherein:

[0007] FIG. **1** to FIG. **4** are cross-sectional diagram depicting an exemplary embodiment of a Cu pillar bump process;

[0008] FIG. **5** is a cross-sectional diagram depicting an exemplary embodiment of a Cu pillar bump; and

[0009] FIG. **6** is a cross-sectional diagram depicting an exemplary embodiment of a flip-chip assembly; and

[0010] FIG. **7** is a cross-sectional diagram depicting an exemplary embodiment of a flip-chip assembly.

DETAILED DESCRIPTION

[0011] In the following description, numerous specific details are set forth to provide a thorough understanding of the disclosure. However, one having an ordinary skill in the art will recognize that the disclosure can be practiced without these specific details. In some instances, well-known structures and processes have not been described in detail to avoid unnecessarily obscuring the disclosure.

[0012] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. It should be appreciated that the following figures are not drawn to scale; rather, these figures are merely intended for illustration.

[0013] Herein, cross-sectional diagrams of FIG. **1** to FIG. **4** illustrate an exemplary embodiment of a Cu pillar bump process. At the outset, it is assumed that a pillar or bump is provided comprising copper. This pillar or bump may be applied directly on an electrical pad on a semiconductor chip for a flip chip assembly or other similar application.

[0014] In FIG. **1**, an example of a substrate **10** used for bump fabrication may comprise a semiconductor substrate as employed in a semiconductor integrated circuit fabrication, and integrated circuits may be formed therein and/or thereupon. The semiconductor substrate is defined to mean any construction comprising semiconductor materials, including, but is not limited to, bulk silicon, a semiconductor wafer, a silicon-on-insulator (SOI) substrate, or a silicon germanium substrate. Other semiconductor materials including group III, group IV, and group V elements may also be used. The substrate **10** may further comprise a plurality of isolation features (not shown), such as shallow trench isolation (STI) features or local oxidation of silicon (LOCOS) features. The isolation features may define and isolate the various microelectronic elements (not shown). Examples of the various microelectronic elements that may be formed in the substrate **10** include transistors (e.g., metal oxide semiconductor field effect transistors (MOSFET), complementary metal oxide semiconductor (CMOS) transistors, bipolar junction transistors (BJT), high voltage transistors, high frequency transistors, p-channel and/or n-channel field effect transistors (PFETs/NFETs), etc.); resistors; diodes; capacitors; inductors; fuses; and other suitable elements. Various processes are performed to form the various microelectronic elements including deposition, etching, implantation, photolithography, annealing, and other suitable processes. The microelectronic elements are interconnected to form the integrated circuit device, such as a logic device, memory device (e.g., SRAM), RF device, input/output (I/O) device, system-on-chip (SoC) device, combinations thereof, and other suitable types of devices.

[0015] The substrate **10** further includes inter-layer dielectric layers and a metallization structure overlying the integrated circuits. The inter-layer dielectric layers in the metallization structure include low-k dielectric materials, un-doped silicate glass (USG), silicon nitride, silicon oxynitride, or other commonly used materials. The dielectric constants (k value) of the low-k dielectric materials may be less than about 3.9, or less than about 2.8. Metal lines in the metallization structure may be formed of copper or copper alloys. One skilled in the art will realize the formation details of the metallization layers. A contact region **12** is a top metallization layer formed in a top-level inter-layer dielectric layer, which is a portion of conductive routs and has an exposed surface treated by a planarization process, such as chemical mechanical polishing (CMP), if necessary. Suitable materials for the conductive region **12** may include, but are not limited to, for example copper (Cu), aluminum (Al), AlCu, copper alloy, or other mobile conductive materials. In one embodiment, the contact region **12** is a metal pad region **12**, which may be used in the bonding process to connect the integrated circuits in the respective chip to external features.

[0016] FIG. **1** also illustrates a passivation layer **14** formed on the substrate **10** and patterned to form an opening **15** exposing a portion of the conductive region **12** for allowing subsequent post passivation interconnect processes. In one embodiment, the passivation layer **14** is formed of a non-organic material selected from un-doped silicate glass (USG), silicon nitride, silicon oxynitride, silicon oxide, and combinations thereof. In another embodiment, the passivation layer **14** is formed of a polymer layer, such as an epoxy, polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), and the like, although other relatively soft, often organic, dielectric materials can also be used.

[0017] A post passivation interconnect (PPI) process is then performed on the passivation layer **14**. Referring to FIG. **1**, layers **16** including an adhesion layer and a seed layer are formed on the passivation layer **14** to line the sidewalls and bottom of the opening **15**. The adhesion layer, also referred to as a glue layer, is blanket formed, covering the passivation layer **14** and the sidewalls and the bottom of opening **15**. The adhesion layer may include commonly used barrier materials such as titanium, titanium nitride, tantalum, tantalum nitride, and combinations thereof, and can be formed using physical vapor deposition, sputtering, and the like. The adhesion layer helps to improve the adhesion of the subsequently formed copper lines onto passivation layer **14**. The seed layer is blanket formed on the adhesion layer. The materials of the seed layer include copper or copper alloys, and metals such as silver, gold, aluminum, and combinations thereof may also be included. The seed layer may also include aluminum or aluminum alloys. In an embodiment, the seed layer is formed of sputtering. In other embodiments, other commonly used methods such as physical vapor deposition or electroless plating may be used. For clarity, the seed layer and the adhesion layer are shown as layers **16** in the drawings.

[0018] Also, a post passivation interconnect (PPI) line **18** is formed on the layers **16** to fill the opening **15**. Using a mask and a photolithography process, a conductive material fills the opening **15** of the passivation layer **14** and the opening of the mask followed by removing the mask and the exposed layers **16**. The conductive material formed on the layers **16** and filling the opening **15** serves as the PPI line **18**. The PPI line **18** may include, but is not limited to, for example copper, aluminum, copper alloy, or other mobile conductive materials. The PPI line **18** may further include a nickel-containing layer (not shown) on the top a copper-containing layer. The PPI formation methods include plating, electroless plating, sputtering, chemical vapor deposition methods, and the like. The PPI line **18** connects the contact region **12** to bump features. The PPI line **18** may also function as power lines, re-distribution lines (RDL), inductors, capacitors or any passive components. The PPI line **18** may have a thickness less than about 30 μm, for example between about 2 μm and about 25 μm. Then the exposed portions of the layers **16** including the adhesion layer and the seed layer are removed. The removal step may include a wet etching process or a dry etching process. In one embodiment, the removal step includes an isotropic wet etching using an ammonia-based acid, which may be a flash etching with a short duration.

[0019] Next, a dielectric layer **20**, also referred to as an isolation layer or a passivation layer, is formed on the exposed passivation layer **14** and the PPI line **18**. The dielectric layer **20** may be formed of dielectric materials such as silicon nitride, silicon carbide, silicon oxynitride or other applicable materials. The formation methods include plasma enhance chemical vapor deposition (PECVD) or other commonly used CVD methods. A polymer layer **22** is formed on the dielectric layer **16** through the steps of coating, curing, descum and the like. Lithography technology and etching processes such as a dry etch and/or a wet etch process are then performed to pattern the polymer layer **22**, thus an opening **23** is formed to pass through the polymer layer **22** and expose a portion of the PPI line **18** for allowing subsequent bump process. The polymer layer **22**, as the name suggests, is formed of a polymer, such as an epoxy, polyimide, benzocyclobutene (BCB), polybenzoxazole (PBO), and the like, although other relatively soft, often organic, dielectric materials can also be used. In one embodiment, the polymer layer **22** is a polyimide layer. In another embodiment, the polymer layer **22** is a polybenzoxazole (PBO) layer. The polymer layer **22** is soft, and hence has the function of reducing inherent stresses on respective substrate. In addition, the polymer layer **22** is easily formed to a thickness of tens of microns.

[0020] Referring to FIG. **2**, the formation of an under-bump-metallurgy (UBM) layer **24** that includes a diffusion barrier layer and a seed layer is performed on the resulted structure. The UBM layer **24** is formed on the polymer layer **22** and the exposed portion of the PPI line **18**, and lines the sidewalls and bottom of the opening **23**. The diffusion barrier layer, also referred to as a glue layer, is formed to cover the sidewalls and the bottom of the opening **23**. The diffusion barrier layer may be formed of tantalum nitride, although it may also be formed of other materials such as titanium nitride, tantalum, titanium, or the like. The formation methods include physical vapor deposition (PVD) or sputtering. The seed layer may be a copper seed layer formed on the diffusion barrier layer. The seed layer may be formed of copper alloys that include silver, chromium, nickel, tin, gold, and combinations thereof. In one embodiment, the UBM layer **24** includes a diffusion barrier layer formed of Ti and a seed layer formed of Cu.

[0021] Next, a mask layer **26** is provided on the UBM layer **24** and patterned with an opening **27** exposing a portion of the UBM layer **24** for Cu pillar bump formation. In one embodiment, the opening **27** is over the opening **23**. In another embodiment, the diameter of the opening **27** is greater or equal to the diameter of the opening **23**. The mask layer **26** may be a dry film or a photoresist film. The opening **27** is then partially or fully filled with a conductive material with solder wettability. In an embodiment, a copper (Cu) layer **28** is formed in the opening **27** to contact the underlying UBM layer **24**. As used throughout this disclosure, the term "copper (Cu) layer" is intended to include substantially a layer including pure elemental copper, copper containing unavoidable impurities, and copper alloys containing minor amounts of elements such as tantalum, indium, tin, zinc, manganese, chromium, titanium, germanium, strontium, platinum, magnesium, aluminum or zirconium. The formation methods may include sputtering, printing, electro plating, electroless plating, and commonly used chemical vapor deposition (CVD) methods. For example, electro-chemical plating (ECP) is carried out to form the Cu layer **28**. In an exemplary embodiment, the thickness of the Cu layer **28** is greater than 30 μm. In another exemplary embodiment, the thickness of the Cu layer **28** is greater than 40 μm. For example, the Cu layer **28** is of about 40-50 μm thickness, or about 40-70 μm thickness, although the thickness may be greater or smaller.

[0022] Next, as shown in FIG. **3**, the mask layer **26** is removed, exposing a portion of the UBM layer **24** outside the Cu layer **28**. In the case the mask layer **26** is a dry film, it may be removed using an alkaline solution. If the mask layer **26** is formed of photoresist, it may be removed using acetone, n-methyl pyrrolidone (NMP), dimethyl sulfoxide (DMSO), aminoethoxy ethanol, and the like. Then the exposed portion of the UBM layer **24** is etched to expose the underlying polymer layer **22** outside the Cu layer **28**, thus the UBM layer **24** underlying the Cu layer **28** remains. In an exemplary embodiment, the step of removing the UBM layer **24** is a dry etching or a wet etching. For example, an isotropic wet etching (often referred to as flash etching due to its short duration) using an ammonia-based acid is employed. Thus the Cu layer **28** having a top surface **28***a* and sidewall surfaces **28***b* protrudes from the polymer layer **22**, also referred to as a Cu pillar bump **28** hereinafter. In an exemplary embodiment, the thickness of the Cu pillar bump **28** is greater than 30 μm. In another exemplary embodiment, the thickness of the Cu pillar bump **28** is greater than 40 μm. For example, the Cu pillar bump **28** is of about 40-50 μm thickness, or about 40-70 μm thickness, although the thickness may be greater or smaller.

[0023] Next, as depicted in FIG. **4**, a barrier layer **30** is formed on the Cu pillar bump **28** to act as a diffusion barrier layer for preventing copper in the Cu pillar bump **28** to diffuse into bonding material, such as solder, that is used to bond the substrate **10** to external features. The barrier layer **30** may be also referred to as a protection layer, an antioxidation layer or an oxide resistant layer employed for preventing the surfaces **28***a* and **28***b* of the Cu pillar bump **28** from oxidation during subsequent processes. The barrier layer **30** may be formed through depleting surfaces of the Cu pillar bump **28** by selective thermal CVD method. In one embodiment, the barrier layer **32** is formed on the Cu pillar **28**, covering the top surface **28***a*, the sidewall surfaces **28***b*, or combinations thereof. The barrier layer **30** is a copper-containing material layer including a group III element, a group IV element, a group V element listed in the periodic table or any combination thereof. In one embodiment, the copper-containing material layer may include, but is not limited to, boron (B), germanium (Ge), silicon (Si), carbon (C), nitrogen (N), phosphorous (P) or combinations thereof. In some embodiments, the copper-containing material layer is a CuGeN layer, a CuGe layer, a CuSi layer, a CuSiN layer, a CuSiGeN layer, a CuN layer, a CuP layer, a CuC layer, a CuB layer, or combinations thereof using a selective CVD with gases containing B, Ge, Si, C, N, P or combinations thereof (e.g., B_2H_6, CH_4, SiH_4, GeH_4, NH_3, PH_3). For an example of forming a CuGeN layer, a deoxidize treatment step (NH_3 treatment) is performed followed by a GeH_4 CVD process. The barrier layer **30** becomes a diffusion barrier layer to passivate the Cu from the solder in subsequent joint process so that the IMC formation is controlled to become thinner and more uniform. Besides, the thickness of the barrier layer **30** is thin due to its formation is like a diffusion process. In one embodiment, the thickness of the barrier layer **30** is less than or equal to 10 nm. The combination of the Cu pillar bump **28** and the barrier layer **30** is referred to as a connection structure **32** for to bonding the substrate **10** to external features.

[0024] The connection structure **32** may further include a solder layer. Referring to FIG. **5**, an exemplary embodiment of forming a solder layer on the Cu pillar bump is depicted. After the formation of the barrier layer **30**, a solder layer **34** may be provided on the barrier layer **30**, in a position adjacent to the top surface **28***a* of the Cu pillar bump **28** adjacent to the sidewall surfaces of the Cu pillar bump **28** as depicted by a dotted line, or combination thereof. The solder layer **34** may be made of Sn, SnAg, Sn—Pb, SnAgCu (with Cu weight percentage less than 0.3%), SnAgZn, SnZn, SnBi—In, Sn—In, Sn—Au, SnPb, SnCu, SnZnIn, or SnAgSb, etc. The combination of the Cu pillar bump **28**, the barrier layer **30** and the solder layer **34** is referred to as another connection structure **32"** for to bonding the substrate **10** to external features.

[0025] The substrate **10** is then sawed and packaged onto a package substrate, or another die, with solder balls or Cu bumps mounted on a pad on the package substrate or the other die. FIG. **6** is a cross-sectional diagram depicting an exemplary embodiment of a flip-chip assembly.

[0026] The structure shown in FIG. **4** or FIG. **5** is flipped upside down and attached to another substrate **100** at the bottom. The substrate **100** may be a package substrate, board (e.g., a printed circuit board (PCB)), or other suitable substrate. The connection structure **32** or **32"** contacts the substrate **100** at various conductive attachment points, for example, a joint solder layer **104** on contact pads **102** and/or conductive traces, forming a joint structure **106** between the substrates **10** and **100**. An exemplary coupling process includes a flux application, chip placement, reflowing of melting solder joints, and cleaning of flux residue. The substrate **10**, the joint structure **106**, and the other substrate **100** may be referred to as a packaging assembly, or in the present embodiment, a flip-chip packaging assembly. During thermal cycling, the tin in the solder (joint solder layer **104** and/or solder layer **34**) tends to migrate through cracks or other defects and react with the barrier layer **30** and/or the Cu pillar bump **28** to form an intermetallic compound (IMC) layer **108** which may be observed between the solder joint **104** and the connection structure **32** or **32"**. The IMC layer **108** may include Cu, Sn and the material including a group III element, a group IV element, a group V element listed in the periodic table or any combination thereof. For example, The IMC layer may include a Cu—Sn—X IMC, wherein the X element may include, but is not limited to, boron (B), germanium (Ge), silicon (Si), carbon (C), nitrogen (N), phosphorous (P) or combinations thereof. The IMC thickness can be controlled to less than 2 μm with the diffusion barrier layer **30**. The barrier layer **30** depresses Cu diffusion from the Cu pillar BUMP **28** to the solder to control the IMC layer **108** to a thickness less than 2 μm, resulting in high strength and better adhesion. The thin IMC formation can induce less stress to decrease probability of bump cracking and contribute to better reliability of Cu pillar bump.

[0027] FIG. **7** is a cross-sectional diagram depicting an exemplary embodiment of a flip-chip assembly. Depending on the solder volume and substrate attaching processes, the joint solder layer **104** may cover at least a portion of the connection structure **32** or **32"**, for example the top portion and/or sidewall portions. When the joint solder layer **104** covers the sidewall portions of the connection structure **32** or **32"** as depicted, the IMC layer **108** is also observed between the sidewall portion of the connection structure **32** or **32"** and the joint solder layer **04**.

[0028] In the preceding detailed description, the disclosure is described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications, structures, processes, and changes may be made thereto without departing from the broader spirit and scope of the disclosure. The specification and drawings are, accordingly, to be regarded as illustrative and not restrictive. It is understood that the disclosure is capable of using various other combinations and environments and is capable of changes or modifications within the scope of inventive concepts as expressed herein.

What is claimed is:

1. An integrated circuit device, comprising:
a semiconductor substrate;
a bond pad region on the semiconductor substrate;
a copper pillar bump overlying and electrically connected to the bond pad region; and
a barrier layer on a surface of the copper pillar bump, wherein the barrier layer is a copper-containing material layer comprising at least one of a group III element, a group IV element and a group V element.

2. The integrated circuit device of claim **1**, wherein the barrier layer is a CuGeN layer.

3. The integrated circuit device of claim **1**, wherein the barrier layer is a copper-containing material layer comprising at least one of germanium (Ge), silicon (Si) and carbon (C).

4. The integrated circuit device of claim **1**, wherein the barrier layer is a copper-containing material layer comprising at least one of nitrogen (N) or phosphorus (P).

5. The integrated circuit device of claim **1**, wherein the barrier layer is a copper-containing material layer comprising boron (B).

6. The integrated circuit device of claim **1**, further comprising a solder layer on the barrier layer.

7. The integrated circuit device of claim **1**, further comprising:
a passivation layer overlying the semiconductor substrate and exposing a portion of the bond pad region;
an interconnect line formed on the passivation layer and electrically connected to the bond pad region; and
a polymer layer overlying the passivation layer and exposing a portion of the interconnect line;
wherein the copper pillar bump is formed overlying the polymer layer and electrically connected to the exposed portion of the interconnect line.

8. The integrated circuit device of claim **7**, wherein the interconnect line comprises copper.

9. The integrated circuit device of claim **7**, wherein the passivation layer comprises polybenzoxazole (PBO).

10. The integrated circuit device of claim **7**, wherein the polymer layer comprises polybenzoxazole (PBO).

11. A flip-chip assembly comprising:
a first substrate;
a second substrate;
a joint structure disposed between the first substrate and the second substrate;
wherein the joint structure comprises a connection structure between the first substrate and the second substrate and a joint solder layer between the connection structure and the second substrate; and
an intermetallic compound (IMC) layer between the connection structure and the joint solder layer, wherein the IMC layer has a thickness less than 2 μm.

12. The flip-chip assembly of claim **11**, wherein the connection structure comprises a copper pillar bump.

13. The flip-chip assembly of claim **12**, wherein the connection structure comprises a barrier layer on a surface of the copper pillar bump.

14. The flip-chip assembly of claim **13**, wherein the barrier layer is a copper-containing material layer comprising at least one of a group III element, a group IV element and a group V element.

15. The flip-chip assembly of claim **13**, wherein the barrier layer is a CuGeN layer.

16. The flip-chip assembly of claim **13**, wherein the copper-containing material layer comprises at least one of germanium (Ge), silicon (Si) or carbon (C).

17. The flip-chip assembly of claim **13**, wherein the copper-containing material layer comprises at least one of nitrogen (N) or phosphorus (P).

18. The flip-chip assembly of claim **13**, wherein the copper-containing material layer comprises boron (B).

19. The flip-chip assembly of claim **11**, wherein the first substrate comprises:
a passivation layer overlying the first substrate;
an interconnect line formed on the passivation layer; and
a polymer layer overlying the passivation layer and exposing a portion of the interconnect line;
wherein the connection structure is overlying and electrically connected to the exposed portion of the interconnect line.

20. The flip-chip assembly of claim **19**, wherein the interconnect line comprises copper, and the polymer layer comprises polybenzoxazole (PBO).

* * * * *