third metal bump connected to said second metal interconnect through a third opening in said second polymer layer; and

a second semiconductor chip under said first interconnection scheme and said first semiconductor chip, wherein said first interconnection scheme is between said first and second semiconductor chips, wherein said second semiconductor chip comprises a central-processing-unit (CPU) circuit block and a graphics-processing-unit (GPU) circuit block.

17. The chip package of claim **16**, further comprising a third semiconductor chip over said first interconnection scheme.

18. The chip package of claim **16**, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

19. The chip package of claim **16**, further comprising a third metal plug vertically in a third through via in said polymer layer, wherein a pitch between said first and third metal plugs is between 200 and 1000 micrometers.

20. The chip package of claim **16**, wherein said first polymer layer has a coefficient of expansion between 3 and 10 ppm/°C.

21. The chip package of claim **16**, further comprising a third semiconductor chip under said second semiconductor chip and multiple fourth metal bumps between said second and third semiconductor chips, wherein said second semiconductor chip comprises a first metal pad on a top surface of said second semiconductor chip and a second metal pad on a bottom surface of said second semiconductor chip, wherein said first metal pad is connected to said second metal pad through a through-silicon-via metal layer.

22. The chip package of claim **16**, further comprising a passive component over said first surface.

23. The chip package of claim **16**, wherein said first interconnection scheme comprise a third metal interconnect across over a sidewall of the second semiconductor chip.

24. The chip package of claim **16**, further comprising a third semiconductor chip under said first interconnection scheme, wherein said third semiconductor chip is a memory chip.

25. The chip package of claim **16**, wherein said second semiconductor chip comprises a third metal interconnect on a metal pad of said second semiconductor chip, wherein said third metal interconnect comprises a second metal layer on said metal pad and a fifth copper layer over said second metal layer, wherein said fifth copper layer has a thickness between 5 and 30 micrometers, wherein said third metal interconnect is connected to said a fourth metal interconnect of said first interconnection scheme.

26. The chip package of claim **16**, wherein a height is between a backside surface of said first semiconductor chip and a top surface of said second polymer layer is smaller than a thickness of said first metal bump.

27. The chip package of claim **16**, wherein said second semiconductor chip is coupled to said first semiconductor chip through said first interconnection scheme.

28. The chip package of claim **16**, wherein said first metal plug has a thickness between 100 and 300 micrometers.

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