wherein in said process that forms the first dielectric layer:

(i) the PVD and/or electroplating operation is non-conformal to cause the semiconductor material at the bottom of the opening to be accessible for said electroless plating and/or electroplating of the first conductive layer thereon; and/or

(ii) the first dielectric layer at the bottom of the opening is etched to make the semiconductor material at the bottom of the opening accessible for said electroless plating and/or electroplating of the conductive layer thereon, wherein the etch etches the entire surface of the first dielectric layer on the sidewalls of the opening but does not remove all of the first dielectric layer on the sidewalls of the opening.

53. The method of claim 52 wherein the first dielectric layer is formed by PVD.

54. The method of claim 52 further comprising removing material from a second surface of the body opposite to the first surface to expose the first conductive layer.

55. The method of claim 52 wherein the first conductive layer comprises:

a first sub-layer deposited by electroless plating onto the semiconductor material at the bottom of the opening; and

a second sub-layer deposited by electroplating onto the first sub-layer.

56. The method of claim 52 wherein the first conductive layer comprises:

a first sub-layer deposited by electroless plating and/or electroplating onto the bottom of the opening; and

a second sub-layer deposited by electroless plating and/or electroplating onto the first sub-layer;

wherein the first sub-layer is not solderable, and the second sub-layer is solderable; and

the method further comprises removing material from a second surface of the body opposite to the first surface to expose the second sub-layer.

57. The method of claim 56 further comprising soldering the exposed second sub-layer to a contact of an integrated circuit or a contact on a wiring substrate.

58. The method of claim 52 wherein the first conductive layer is deposited to at least a level of the first surface of the body so that the opening is filled when the first conductive layer has been deposited.

59. A manufacturing method comprising:

forming an opening in a first surface of a body which comprises semiconductor material;

forming a first dielectric layer in the opening;

forming a first layer over the first dielectric layer by a process that includes a non-conformal physical vapor deposition (PVD) and/or electroplating, wherein said non-conformal PVD and/or electroplating operation causes the first layer to form over at least a portion of the opening's sidewalls adjacent the first surface of the body but not over at least a portion of the opening's bottom surface;

etching the first dielectric layer by an etch selective to the first layer, to remove the first dielectric layer from at least said portion of the opening's bottom surface;

after etching the first dielectric layer, depositing a first conductive layer by a process that includes electroless plating and/or electroplating of the first conductive layer onto the semiconductor material at the bottom of the opening.

60. The method of claim 59 wherein the first layer is formed by PVD.

61. The method of claim 59 further comprising removing material from a second surface of the body opposite to the first surface to expose the first conductive layer.

62. The method of claim 59 wherein the first conductive layer comprises:

a first metal sub-layer deposited by electroless plating onto the semiconductor material at the bottom of the opening; and

a second metal sub-layer deposited by electroplating onto the first sub-layer.

63. The method of claim 59 wherein the first conductive layer comprises:

a first sub-layer deposited by electroless plating and/or electroplating onto the semiconductor material at the bottom of the opening; and

a second sub-layer deposited by electroless plating and/or electroplating onto the first sub-layer;

wherein the first sub-layer is not solderable, and the second sub-layer is solderable; and

the method further comprises removing material from a second surface of the body opposite to the first surface to expose the second sub-layer.

64. The method of claim 63 further comprising soldering the exposed second sub-layer to a contact of an integrated circuit or a contact on a wiring substrate.

65. The method of claim 59 wherein the first conductive layer is deposited to at least the first surface of the body to fill the opening.

66. The method of claim 59 further comprising removing the first layer after etching of the first dielectric layer.

67. A manufacturing method comprising:

forming an opening in a first surface of a body which comprises semiconductor material;

forming a first dielectric layer in the opening;

forming a first layer over the first dielectric layer by a process that includes a non-conformal physical vapor deposition (PVD) and/or electroplating, wherein said non-conformal PVD and/or electroplating operation causes the first layer to form over at least a portion of the opening's sidewalls adjacent the first surface of the body;

etching the first dielectric layer by an etch selective to the first layer, to remove the first dielectric layer from at least a portion of the opening's bottom surface;

after etching the first dielectric layer, depositing a first conductive layer by a process that includes electroless

plating and/or electroplating of the first conductive layer onto the semiconductor material at the bottom of the opening;

wherein in said process that forms the first layer:

(i) the PVD and/or electroplating operation is non-conformal to cause the first dielectric layer at the bottom of the opening to be accessible for being etched selectively to the first layer; and/or

(ii) the first layer is etched at the bottom of the opening to make the first dielectric layer at the bottom of the opening accessible for being etched, wherein the etch of the first layer etches the entire surface of the first layer in the opening but does not remove all of the first layer on the sidewalls of the opening.

68. The method of claim 67 wherein the first layer is formed by PVD.

69. The method of claim 67 further comprising removing material from a second surface of the body opposite to the first surface to expose the first conductive layer.

70. The method of claim 67 wherein the first conductive layer comprises:

a first metal sub-layer deposited by electroless plating onto the semiconductor material at the bottom of the opening; and

a second metal sub-layer deposited by electroplating onto the first sub-layer.

71. The method of claim 67 wherein the first conductive layer comprises:

a first sub-layer deposited by electroless plating and/or electroplating onto the semiconductor material at the bottom of the opening; and

a second sub-layer deposited by electroless plating and/or electroplating onto the first sub-layer;

wherein the first sub-layer is not solderable, and the second sub-layer is solderable; and

the method further comprises removing material from a second surface of the body opposite to the first surface to expose the second sub-layer.

72. The method of claim 71 further comprising soldering the exposed second sub-layer to a contact of an integrated circuit or a contact on a wiring substrate.

73. The method of claim 67 wherein the first conductive layer is deposited to at least the first surface of the body to fill the opening.

74. The method of claim 67 further comprising removing the first layer after etching of the first dielectric layer.

75. A manufacturing method comprising:

forming an opening in a first surface of a body which comprises semiconductor material;

forming a first dielectric layer in the opening;

forming a first conductive layer in the opening over the first dielectric layer;

forming a first layer over the first conductive layer by a process that includes a non-conformal physical vapor deposition (PVD) and/or electroplating, wherein said non-conformal PVD and/or electroplating operation causes the first layer to form over at least a portion of the opening's sidewalls adjacent the first surface of the body but not over at least a portion of the opening's bottom surface;

after forming the first layer, depositing a second conductive layer by a process that includes electroless plating or electroplating process of the second conductive layer onto the first conductive layer at the bottom of the opening.

76. The method of claim 75 wherein the first layer comprises metal deposited by PVD and/or electroplating, and the process that forms the first layer comprises anodizing the metal to form a non-conductive oxide.

77. The method of claim 76 wherein the metal has a higher electrochemical potential than a top surface of the first conductive layer.

78. The method of claim 76 wherein forming the second conductive layer comprises electroplating.

79. The method of claim 75 further comprising removing material from a second surface of the body opposite to the first surface to expose the first conductive layer.

80. The method of claim 75 wherein at least a bottom portion of the first conductive layer is not solderable, but at least one of the first and second conductive layers comprises a solderable layer; and

the method further comprises removing material from a second surface of the body opposite to the first surface to expose the solderable layer.

81. The method of claim 75 wherein the second conductive layer is deposited to at least the first surface of the body to fill the opening.

82. A manufacturing method comprising:

forming an opening in a first surface of a body which comprises semiconductor material;

forming a first dielectric layer in the opening;

forming a first conductive layer in the opening over the first dielectric layer;

forming a first layer over the first conductive layer by a process that includes a non-conformal physical vapor deposition (PVD) and/or electroplating, wherein said non-conformal PVD and/or electroplating operation causes the first layer to form over at least a portion of the opening's sidewalls adjacent the first surface of the body;

after forming the first layer, depositing a second conductive layer by a process that includes electroless plating and/or electroplating of the second conductive layer onto the first conductive layer at the bottom of the opening;

wherein in the process that forms the first layer:

(i) the PVD and/or electroplating operation is non-conformal to cause the first conductive layer at the bottom of the opening to be accessible for plating the second conductive layer thereon; and/or

(ii) the first layer is etched at the bottom of the opening to make the first conductive layer at the bottom of the opening accessible for the plating of the second

conductive layer thereon, wherein the etch of the first layer etches the entire first layer exposed in the opening but does not remove all of the first layer on the sidewalls of the opening.

83. The method of claim 82 wherein the first layer comprises metal deposited by PVD and/or electroplating, and the process that forms the first layer comprises anodizing the metal to form a non-conductive oxide.

84. The method of claim 83 wherein the metal has a higher electrochemical potential than a top surface of the first conductive layer.

85. The method of claim 82 wherein forming the second conductive layer comprises electroplating.

86. The method of claim 82 further comprising removing material from a second surface of the body opposite to the first surface to expose the first conductive layer.

87. The method of claim 82 wherein at least a bottom portion of the first conductive layer is not solderable, but at least one of the first and second conductive layers comprises a solderable layer; and

the method further comprises removing material from a second surface of the body opposite to the first surface to expose the solderable layer.

88. The method of claim 82 wherein the second conductive layer is deposited to at least the first surface of the body to fill the opening.

89. A structure comprising:

a body comprising semiconductor material;

an opening in the body;

a first dielectric layer over a sidewall of the opening;

a first conductive layer over the first dielectric layer;

a second dielectric layer over the first conductive layer over the sidewall of the opening, wherein the second dielectric layer does not completely cover the first conductive layer in the opening;

a second conductive layer over the second dielectric layer and the first conductive layer, wherein the second conductive layer physically contacts a portion of the first conductive layer in the opening but the second conductive layer is separated by the second dielectric layer from another portion of the first conductive layer over the sidewall of the opening.

90. The structure of claim 89 wherein the opening passes through the body.

91. The structure of claim 89 wherein the second dielectric layer comprises an oxide of a metal, and said metal is present in a non-oxidized state between the second dielectric layer and the first conductive layer.

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