Characterization and Elimination of Trench Dislocations

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Abstract

Trench dislocations in a 0.25um BiCMOS SRAM technology were traced to defects arising during S/D processing. It is argued that these defects coalesce to form dislocations, typically near the trench edge, under the combined influence of mechanical stress and high temperature processing. Process variables impacting the generation of these dislocations, including layout geometry; trench depth, profile, and densification; the presence of a liner under the gate spacer nitride; and S/D implant condition and anneal are studied. Based on this analysis, a defect-free BiCMOS process is proposed. It is shown that although the incidence of trench dislocations could be decreased by reducing the overall stress in the flow, eliminating S/D implant defects is the key to completely removing the trench dislocations.

Introduction

Controlling process-induced stress is an increasing concern with each succeeding generation of IC process. Increasing packing density and reducing feature size lead to higher wafer stress levels [1]. With the drive toward low thermal budget processing, the ability of materials to relieve stress by flow processes decreases as well. A number of recent publications have discussed silicon dislocations observed with the introduction of shallow trench isolation [2-4]. These papers have invoked mechanical stress as the primary cause of these dislocations and have identified methods to reduce stress in the silicon to eliminate these dislocations. However, they do not clearly identify the process step which is the source of these dislocations and reducing the stress alone does not always eliminate the defects completely. In this work, we demonstrate that point defects generated during heavy source/drain implantation form the nuclei for trench dislocations, which under the combined influence of mechanical stress and high temperature processing typically glide to the region of maximum stress. We also propose a defect free solution based on annealing the implant damage to ensure that any subsequent changes in the process or the layout do not regenerate these dislocations.

Description of Defects

This work was based on a 0.25μm BiCMOS SRAM technology with shallow trench isolation which was reported previously [5]. This triple poly/triple metal BiCMOS SRAM process consisted of buried layer and epitaxy followed by shallow trench isolation. The active pattern was defined using DUV lithography and etched to create 3500Å deep trenches. The trenches were filled with O_3-TEOS and annealed at high temperature prior to trench CMP. The gate stack consisted of poly-Si /WSi_x/ Si_3N_4 cap with Si_3N_4 spacers. Heavy dose arsenic n+ source/drain implants were followed by a poly-2 self-aligned contact formation. Poly-3 load resistor and backend processing for the contacts and metal layers completed the process. Figure 1 is a TEM cross-section of this technology.

Trench dislocations were observed in the memory array of this 0.25um 1Mb SRAM at the end of line. These dislocations were typically initiated near the bottom corner of the trench, terminating either at another trench corner or at the silicon surface, as shown in the cross-section and plan-view TEMs in Figure 2. In some instances, the dislocations were initiated and/or terminated in the n+ source drain regions. Wright-etching was used to highlight and quantify these defects as shown in Figure 3.

Stress Reduction

The initial attempts to eliminate the trench dislocations concentrated on identifying and reducing sources of stress throughout the process, based on recent literature [1-4]. Wafer curvature was monitored at different points in the process in order to extract the stress on the silicon substrate from various film stack materials (Figures 4 and 5). Based on this study three key areas were identified for stress reduction: (i) trench processing, (ii) gate stack composition, (iii) nitride spacer.

Trench processing - The trench fill O_3-TEOS densification anneal was compared for three temperatures. A lower temperature anneal gave 5X more defects than the baseline, while a higher temperature anneal resulted in 64% fewer defects (Figure-6a), consistent with published literature [2]. This effect can be attributed to the reduced volume change in well-densified fill oxide during subsequent heat steps. However, even the highest temperature (1200°C) anneal resulted in too many dislocations in the array.

Simulations were used to study the effect of trench depth and profile on stress. Several alternatives were investigated, including varying trench depth and sidewall profile from the nominal conditions of a 3500Å deep trench with 70° sidewalls. Stress contours are shown to peak at the bottom corner of the trench and the magnitude of the stress is greater for deeper trenches and more vertical profile (Figure 7).

Experimentally, it was found that shallower trenches had more dislocations than deeper trenches (Figure 6b), contrary to predictions from stress simulations. The number of dislocations was not modulated by trench profile either. These intriguing results will be discussed and explained in more detail later on in this paper.

Gatestack - The SRAM gate consists of a poly-Si /WSi_x/ Si_3N_4 stack. It was shown from the wafer curvature measurements that the tungsten silicide and nitride cap contribute significantly to the overall mechanical stress. To reduce the stress exerted by the gate stack, alternate stacks with the WSix replaced by polysilicon and the nitride cap replaced by TEOS were investigated. It was found that while the stress contribution due to the gatestack could be reduced, it's composition had no significant impact on the incidence of dislocations, as can be seen in Figure 8a.

Nitride spacers - An oxide liner under the nitride spacer is known to reduce the stress from the spacer on the underlying silicon, which could also prevent formation of trench dislocations. In this work, it was found that a TEOS liner reduced the incidence of dislocations by as much as 70% [Figure 8b]. However, while a TEOS liner reduced the local stress imparted by the nitride spacer and decreased the incidence of dislocations, they were not eliminated.

Defect Characterization

Since stress reduction alone did not completely eliminate the trench defects, efforts were redirected to understand these dislocations further.

Bitcell Layout - The influence of bitcell geometry on the dislocations was studied. A bitcell active geometry, defined along <111> planes, was found to be more susceptible to dislocations than an alternate layout which was defined with largely <100> planes. A schematic layout and top-view SEM comparing the two bitcells is shown in Figure 9a. The <111> bitcell, showed a 10X increase in the number of defects and a 100X increase in bitcell diode leakage relative to the <100> bitcell, as demonstrated in Figure 9b and 9c. By studying a range of other structures on the chip, it was found that both trench and gate or spacer edges were required since the dislocations only occurred where a gate crossed over active. Thus, generation of trench dislocations is sensitive to layout geometry.

Process Flow - The next step in understanding the cause of the dislocations was to identify the process steps responsible for defect creation (Table 1). The entire process flow was carefully dissected and short flow lots were run, eliminating one step at a time in the process. The trench dislocations were first observed following the high temperature RTA that was used to reduce poly-2-to-n+ active contact resistance. Varying the temperature, time and ramp rates for this RTA step were not found to have an appreciable impact on the incidence of trench dislocations. Although the dislocations first appeared following the poly-2 RTA step, the RTA itself was not solely responsible for the dislocations because, only cumulative processing through the poly-2 RTA including trench isolation and n+ source/drain implantation resulted in the defects. If LOCOS isolation were used instead of shallow trench or if the source/drain implants were eliminated, no dislocations were observed. This suggests that the stress-induced dislocations are not formed unless nucleation sites are provided in the form of implant damage.

The earlier observation that shallower trenches resulted in more dislocations than deeper trenches despite the lower stress also supports this conjecture. With shallower trenches the stress is higher in the silicon region with n+ source/drain implant damage and the peak stress point at the trench bottom corner is closer to the damaged silicon (Figure 7). This also illustrates that an overall lower stress in the silicon alone does not ensure a defect free process. The experimental observation that a more gradual trench profile did not reduce the incidence of dislocations, despite simulations indicating reduced mechanical stress, also lends support to the theory. We therefore conclude that defects generated during source/drain implant damage coalesce into dislocations under the influence of stress and thermal processing.

Defect Elimination

Efforts then focused on eliminating source/drain implant damage as the means to fix trench dislocation problems. In the first experiment, the source/drain implant energy was varied to modulate the amount and range of damage caused to the silicon lattice. Reducing implant energy reduced defectivity by 70%. Since published results show a reduction in end-of-range damage with lower energy implants, this result is consistent with the explanation that implant damage causes trench dislocations. Next, an oxidizing anneal which is known to eliminate spacer edge defects was included after n+ source/drain implantation. This oxidation step injects interstitials which diffuse to and annihilate the source/drain defects at the spacer edge. Without any other process changes, the inclusion of this anneal alone completely eliminated all dislocations in the silicon. Figure 10a summarizes the results of these experiments and figure 10b is a plan-view TEM of bitcells run with the S/D oxidizing anneal demonstrating the elimination of all trench dislocations. We propose therefore that including an oxidizing source/drain anneal ensures a trench dislocation free process solution for shallow trench isolation. Since this solution is based on eliminating the very sites for defect nucleation, subsequent changes in the process or the layout would not regenerate these defects.

Summary

Trench dislocations were observed after cumulative processing through a poly-2 RTA step in a 0.25um BiCMOS SRAM process. It is concluded that trench dislocations are caused by n+ source/drain implant nucleated defects that coalesce to form dislocations under the combined influence of mechanical stress and high temperature processing. It was found that while the incidence of trench dislocations could be decreased by reducing the overall mechanical stress, elimination of S/D defects by including an oxidizing anneal was the ultimate solution to the problem.

References

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[2] K. Ishimaru et al., Symp. on VLSI Tech., p123, 1997.
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[4] S. Park et al., IEDM Digest, p669, 1997.
[5] T. McNelly et al., IEDM Digest, p927, 1995.

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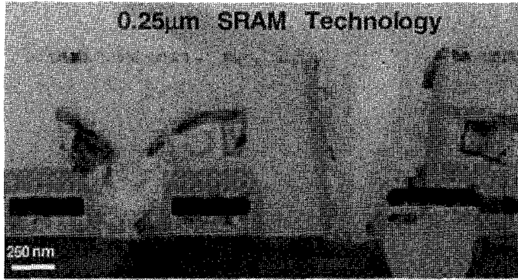

Figure 1: Cross-section of 0.25µm SRAM technology

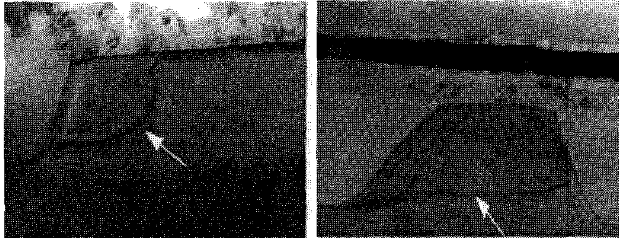
Figure 2: Cross-section TEMs of trench dislocations.

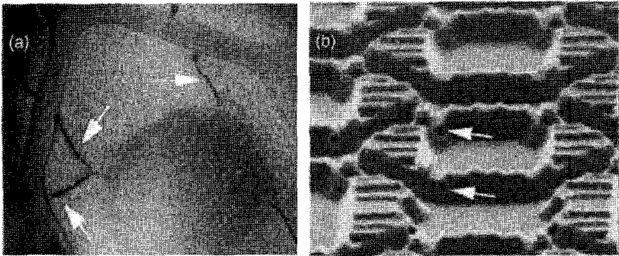

Figure 3: (a) Plan view TEM of trench dislocations. (b) SEM of trench dislocations after Wright etch.

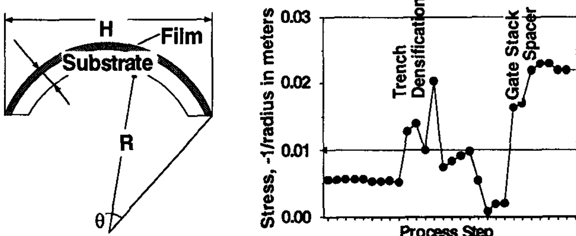

Figure 4: Stress measurements on product wafers

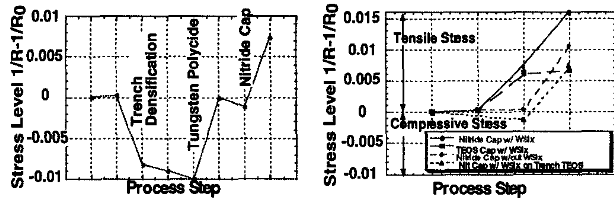

Figure 5: Stress measurements on unpatterned wafers

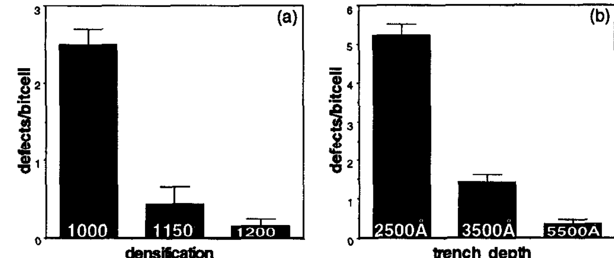

Figure 6: Effect of trench processing on trench dislocations

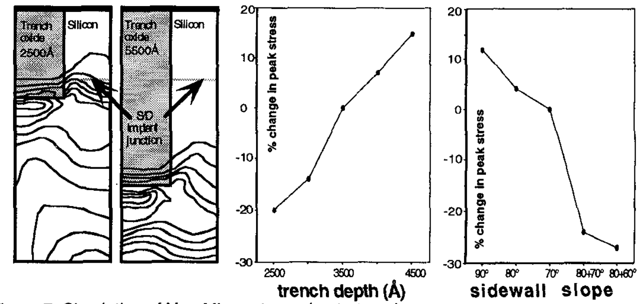

Figure 7: Simulation of Von-Mises stress due to trench process

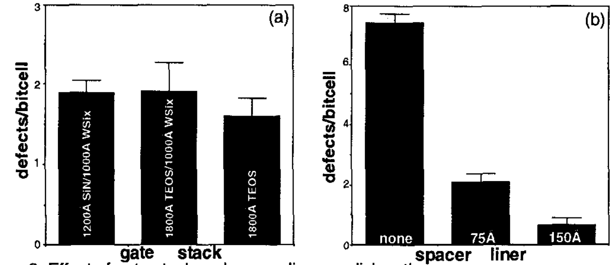

Figure 8: Effect of gate stack and spacer liner on dislocations

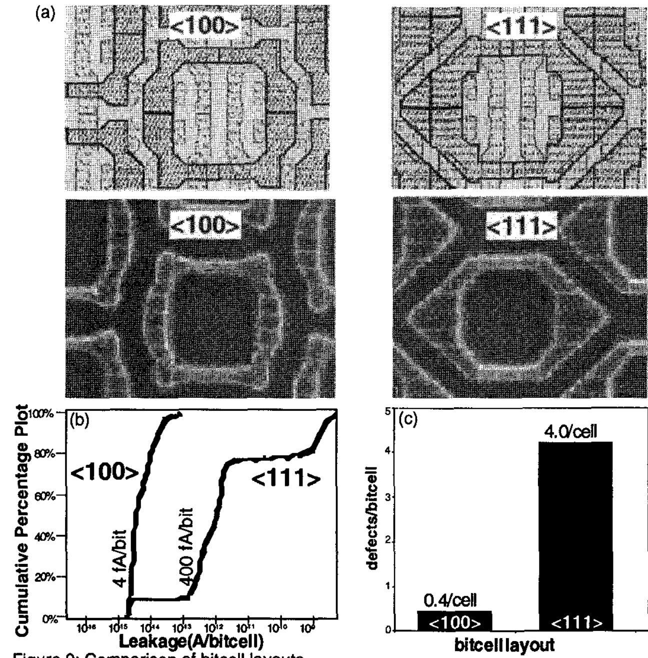

Figure 9: Comparison of bitcell layouts

- Buried Layer Formation & Epitaxy
- Active Photo & Etch
- Liner Oxide & O3-TEOS Trench Fill
- Trench Fill Anneal & Trench CMP
- Gate Stack Formation & Patterning
- Nitride Spacer Deposition & Etch
- N+S/D Implant
- Interpoly Dielectric Deposition
- Self-Aligned Contact Photo & Etch
- Poly-2 Deposition & RTA
- Poly-3 Processing
- Metallization

Table 1: Process flow

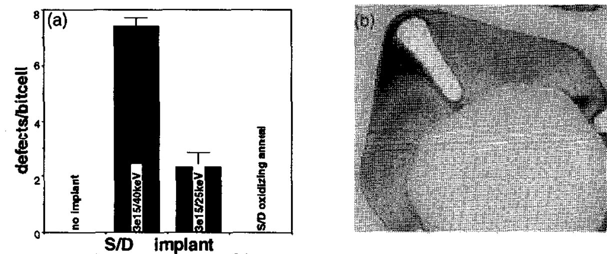

Figure 10: Effect of eliminating S/D defects

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