

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Marlin Semiconductor Ltd.,

Patent Owner.

Patent No. 8,076,194 B2
Filing Date: May 18, 2010
Issue Date: December 13, 2011

Title: METHOD OF FABRICATING METAL OXIDE SEMICONDUCTOR
TRANSISTOR

Inter Partes Review No. IPR2026-00061

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
DISCRETIONARY DENIAL REQUEST**

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Memorandum from John A. Squires, Under Secretary of Commerce
for Intellectual Property and Director of the United States Patent
and Trademark Office, to All PTAB Users (Mar. 11, 2026)17

I. Introduction

U.S. Patent No. 8,076,194 (“’194 patent”) issued because of material error by the Examiner during prosecution. The Office already found Examiner error during the prosecution of the parent patent, U.S. Patent No 7,745,847 (“’847 patent”), referring and instituting TSMC’s IPR. *See generally Taiwan Semiconductor Mfg. Co. Ltd. v. Marlin Semiconductor Ltd.*, IPR2025-00847, Paper 11 (Discretionary Decision, Sept. 3, 2025), Paper 12 (Institution, Oct. 9, 2025). The same material error was repeated here. As with the ’847 patent, the Examiner relied on U.S. Patent No. 6,815,770 (“Chien770”) to address only dependent-claim limitations, failing to recognize that Chien770 also teaches the allegedly novel limitations of the independent claims. This is substantially the same error the Office already found to warrant institution of the ’847 patent IPR.

Marlin has no response. Despite repeatedly citing to the ’847 patent proceedings (referred and instituted, to correct this examiner error), Marlin altogether failed to address this Examiner error in its discretionary denial request. *See* Paper 6, at 4, 5, 9, 10. TSMC’s petition should be referred to address these errors, consistent with the IPR proceedings instituted for the ’847 patent.

That alone warrants referral. But the settled interests of TSMC and its customers also outweigh any settled interests of the new Patent Owner, Marlin. This, too, warrants referral. TSMC and its customers had settled expectations of non-

enforcement because UMC, an alleged competitor of TSMC, failed to assert it for 11 years after the '194 patent issued. During that extended period of inactivity, TSMC invested billions of dollars to manufacture advanced semiconductor chips, including for American customers who expected to be able to integrate those chips into their own products without incident. Ex-1032, Ex-1035. Marlin, a foreign entity which only recently acquired the patent, has no comparable expectations.

Referral is also an efficient use of Board resources in view of the *Fintiv* factors because the '194 patent is not currently asserted in parallel litigation. There is, however, a threat of enforcement, as evidenced by Marlin's specific claim of infringement with respect to the '194 patent and existing lawsuits in the ITC and district court. In response, TSMC diligently challenged the validity of the patent in the PTAB prior to any litigation involving the '194 patent to provide a true alternative to district court or ITC litigation. Moreover, this case involves complicated semiconductor technologies, and trained PTAB judges are best suited to adjudicate the merits of the Petition and to correct the past errors of this Office.

Finally, compelling national security, economic, and public interests make review an appropriate use of the Board's resources. TSMC is the world's largest chip maker, by some accounts providing around 90% of the world's advanced chips (e.g., 7nm and smaller). *See* Ex-1034, at 2. Its advanced semiconductor technology, against which Marlin asserted the parent '847 patent, is vital to the U.S. supply chain

for advanced technologies. Given TSMC's \$165B investment to establish a strategic U.S. supply chain for advanced semiconductors, including current manufacturing of the accused 4nm process nodes in Arizona, the Administration has a heightened interest in ensuring that the USPTO corrects its error in issuing the '194 patent.

A holistic assessment of the facts, evidence, circumstances, and relevant considerations (detailed below) confirms that TSMC's Petition should be referred.

II. The Examiner Materially Erred by Overlooking Disclosures in Chien770, Applied as a Secondary Reference During Prosecution, Which Anticipates at Least Claims 1 and 5-8

As the Office already did for the IPR challenging the '847 patent (the parent of the '194 patent), TSMC's petition should be referred to the Board to correct material errors during prosecution. The Examiner applied Chien770 (Ex-1030) as a secondary reference in an obviousness rejection. The Examiner, however, failed to appreciate that Chien770 anticipates several claims. This failure is compounded by the fact that the Examiner made virtually the same error during the prosecution of the '847 patent. These failures constitute material errors and warrant referring the Petition for an institution decision on the merits. *See generally* IPR2025-00847, Paper 11 (Director, Sept. 3, 2025); *see also Carbyne, Inc. v. TriTech Software Sys.*, IPR2025-00959, Paper 11, at 2 (Oct. 3, 2025) (referring, in-part, based on examiner error where reference "cited on an IDS during prosecution" "appears to disclose the purportedly missing claim limitations" leading to allowance).

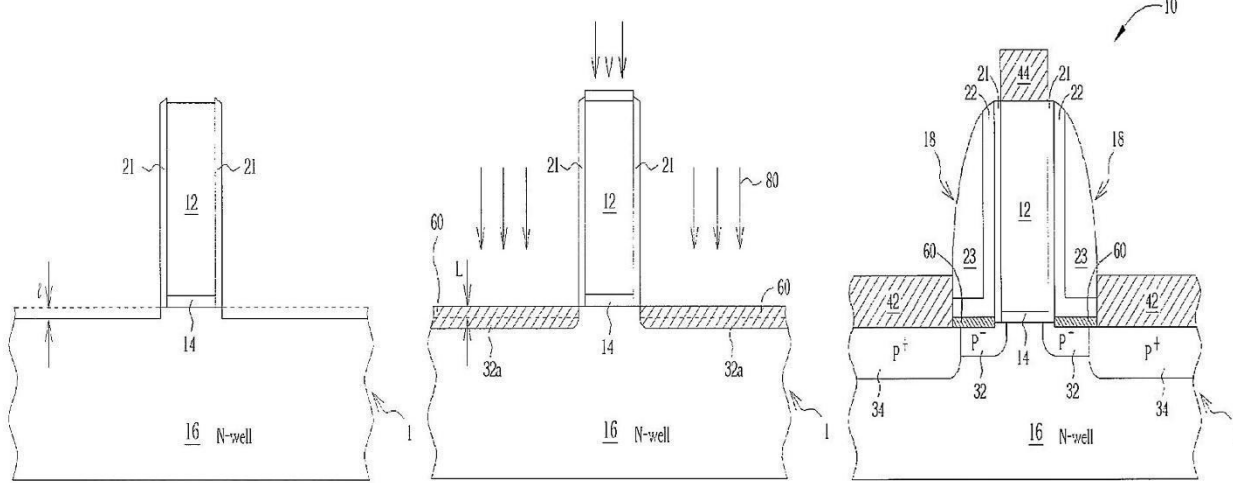
The Examiner considered, but overlooked, an anticipatory reference (Chien770) during prosecution. During prosecution, the Examiner rejected the initial claims as anticipated by Chen (U.S. Patent No. 7,381,623), and obvious based on Chen alone, Chen and Han (U.S. Patent No. 7,800,182), or Chen and Chien770. *See* Ex-1002, at 59-64. As with the parent '847 patent, however, Chien770 was cited for much less than it discloses. *See* IPR2025-00847, Paper 10, at 5-10. Chien770 was only cited for its disclosure that “the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer” (claims 5-6) and “a lightly doped drain disposed in the semiconductor substrate adjacent to the gate” (claim 8). Ex-1002, at 63.

In response, the applicant argued that Chen, the primary reference, did not disclose “after forming an epitaxial layer in the recess, a spacer is formed on the sidewall of the gate and on a portion of the epitaxial layer such that a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate” but did not address Chien770 directly. *See* Ex-1002, at 169-173. Subsequently, the Examiner added another reference, Zhang (U.S. Publication No. 2008/0203449), but again applied Chien770 only as a secondary reference. *See* Ex-1002, at 177-82. The applicant then swore behind Zhang, leading directly to the issuance of the '194 patent with no reasons given. *See* Ex-1002, at 200-18, 228-32.

The Examiner committed material error by allowing the '194 patent because

the allegedly missing limitation *was disclosed in Chien770*. It is in the Office’s and the public’s interest to correct this material error.

Chien770 explains and supports the allegedly missing claim feature, as shown below. First, as Fig. 6 shows, the substrate surface is etched to below the dotted line “to form recesses having a depth of approximately 50 to 100 angstroms ($l=50$ to 100 angstroms),” where “ l ” represents the recess depth. Chien770, at 4:14-19. Next, as Fig. 7 shows, Chien770 teaches that “an epitaxial process is then carried out to grow an epitaxial layer 60 in the recesses at both sides of the gate electrode 12.” *Id.* at 4:22-24. Epitaxial layer 60 has “a thickness L .” *Id.* at 4:25-26. The epitaxial layer preferably extends *above* the substrate surface, as Chien770 expressly discloses: “In accordance with the preferred embodiment of the present invention, $L \geq l$.” *Id.* at 4:26-28; *see also id.* at 4:14-28, Figs. 4, 6-7. Epitaxial layer 60 is therefore raised, as Fig. 4 shows, such that spacer 18 contacts it above the substrate’s surface.



Chien770, Fig. 6

Chien770, Fig. 7

Chien770, Fig. 4

And Chien770 does not disclose only this allegedly novel feature; it is

anticipatory. Consider Claim 1, for example:

<p>1[pre] A method of fabricating a MOS transistor, comprising:</p>	<p>“FIG. 5 to FIG. 12 are schematic cross-sectional diagrams showing <i>the fabrication of the MOS transistor</i> with ultra shallow junction S/D extensions according to the present invention.” (Chien770 at 2:40-43.)</p>
<p>1[a] providing a semiconductor substrate;</p>	<p>“First, as shown in FIG. 5, a <i>semiconductor substrate 1</i> preferably a single crystal silicon substrate is provided.” (Chien770 at 3:67-4:3.)</p>
<p>1[b] forming at least a gate on the semiconductor substrate;</p>	<p>“A gate oxide layer 14 and a polysilicon layer are sequentially formed on the semiconductor substrate 1. A conventional lithographic process and a dry etching process are then carried to define the poly <i>gate structure 12</i> with a line width to a sub-micron scale.” (Chien770 at 4:4-8.)</p>
<p>1[c] forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;</p>	<p>“After the definition of the gate electrode 12, an <i>offset spacer layer 21a</i> with a thickness of about 100 to 150 angstroms is <i>deposited on the gate electrode 12</i> and the surface of the semiconductor substrate 1.” (Chien770 at 4:8-12.)</p>
<p>1[d] forming at least a recess within the semiconductor substrate adjacent to the gate;</p>	<p>As shown in FIG. 6, the offset spacer layer 21a is etched back to form offset Spacers 21 on opposite sidewalls of the gate electrode 12. It is noted that <i>the etching also etches a thickness 1 of the</i></p>

	<p><i>semiconductor substrate 1 at both side of the gate electrode 12 to form recesses</i> having a depth of approximately 50 to 100 angstroms ($l=50$ to 100 angstroms). (Chien770 at 4:14-19.)</p>
<p>1[e] forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate; and</p>	<p>“As shown in FIG. 7, an epitaxial process is then carried out to <i>grow an epitaxial layer 60 in the recesses</i> at both sides of the gate electrode 12 on the semiconductor substrate 1. Preferably, the epitaxial layer 60 has a thickness L of 50 to 100 angstroms, more preferably, 75 angstroms. In accordance with the preferred embodiment of the present invention, $L \geq l$ [where L is the layer thickness and l is the recess depth].” (Chien770 at 4:22-28.)</p>
<p>1[f] forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate.</p>	<p>“[As shown in FIG. 8], a liner 22a and a silicon nitride layer 23a are deposited on the semiconductor substrate 1. As shown in FIG. 9, <i>the silicon nitride layer 23a and the liner 22a are anisotropically etched back to form spacers 18</i>. The spacer 18 consists of the of f set [sic] oxide spacer 21, the oxide liner 22, and the nitride spacer 23. The oxide liner 22 covers the offset oxide Spacer 21 and <i>its lower portion extends laterally to overlie the SiGe epitaxial layer 60.</i>” (Chien770 at 4:62-5:3.)</p>

The Examiner twice applied Chien770 to reject the claims, but only as a secondary reference. It was material error for the Examiner not to appreciate

Chien770's disclosures, which explicitly disclose the allegedly novel limitation. In fact, Chien770 discloses *every* limitation of at least claims 1 and 5-8. The Examiner thus should have rejected the claims based on Chien770.

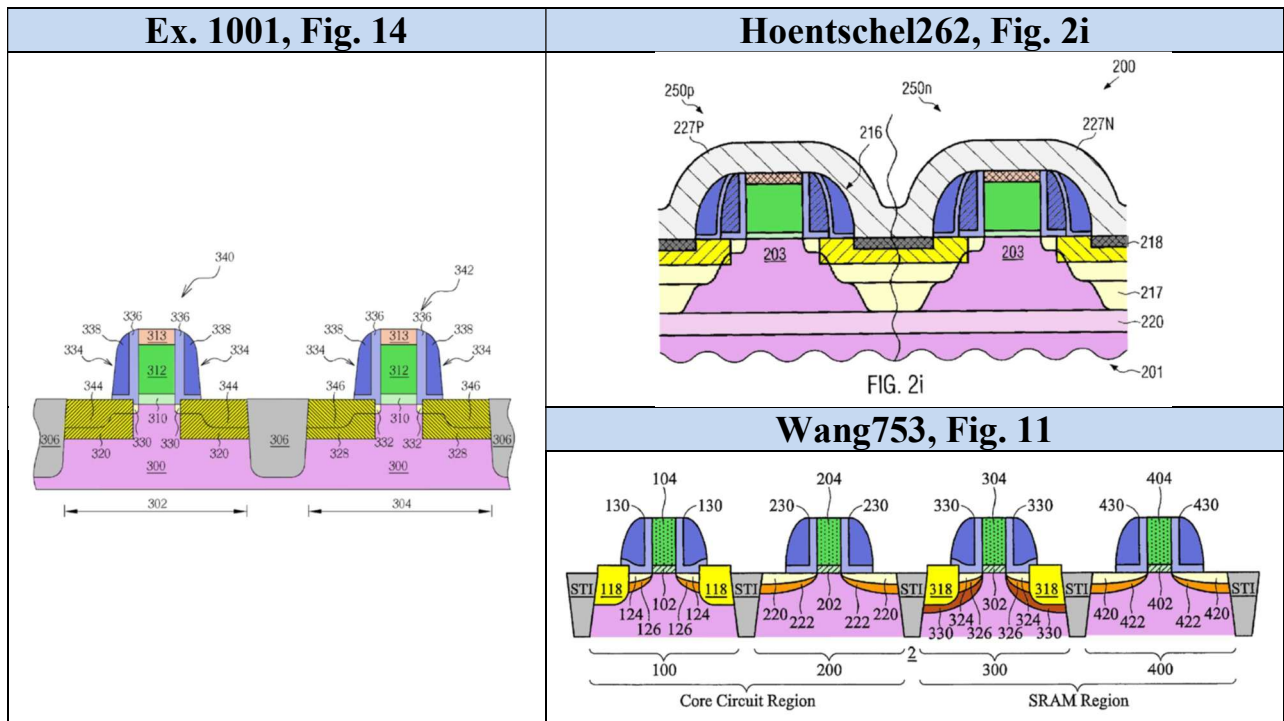
The severity of the Examiner's material error far exceeds other material errors that have justified referral. An overlooked anticipatory reference applied by the Examiner is an exceptional error that stands out. *See Anthony Inc. v. ControlTec, Inc.*, IPR2025-00559, Paper 12, at 2 (July 16, 2025) (referring to panel because examiner's failure to locate petition reference showed material error in prosecution); *Microsoft Corp. v. Partec Cluster Competence Ctr. GmbH*, IPR2025-00318, Paper 9, at 3 (June 12, 2025) (referring to the panel because "Petitioner appears to show a material error by the Office [by overlooking the teaching of several references] and it is an appropriate use of Office resources to review the potential error").

Finally, instituting IPR of the parent '847 patent in IPR2025-00847 independently supports referral and institution here. The '194 patent is part of the same patent family and shares the same core technology and prosecution history, including the same examination error already found material and worthy of referral. Instituting review of the '194 patent ensures consistent treatment of related patents and avoids the anomalous result of permitting claims in a continuation patent to stand where similar claims in the parent have already been referred and instituted. Ensuring consistency across a patent family, especially where the same error was

made during prosecution, is an appropriate and efficient use of Office resources.

III. Referral Is Warranted Because of the Strength of the Petition, Which Invalidates All Claims Over Two Separate Primary References

The merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TMSC presents two single-reference §§102/103 grounds—Honetschel262 and Wang753—each covering the majority of the '194 patent's claims. *See Pet.* at 1. Marlin identifies no substantive deficiencies in either primary reference, and while the Petition lays out the full method in detail the compelling merits of the Petition can be gleaned even just from the side-by-side figures below, which show the striking similarities between the alleged invention and the references (figures shown are final stages):



Moreover, the PTAB has already found a reasonable likelihood of success in

a related petition, IPR2025-00847, challenging the parent '847 patent's device claims. *See generally* IPR2025-00847, Paper 12. This weighs against discretionary denial of the '194 patent's similar method claims. *See generally Tesla v. Intel Ventures II LLC*, IPR2025-00217, Paper 9 (Jun. 13, 2025) (informative) (finding the Board's previous determination of a reasonable likelihood that similar claims of an ancestor patent were unpatentable counsels against discretionary denial).

IV. Referral Is Warranted Because the Settled Expectations of Petitioner and Others Outweigh Marlin's Alleged Expectations

Marlin's main contention in requesting denial is that the patent issued 14 years ago, allegedly creating "settled expectations" that, alone, effectively trump all other considerations. *See* Paper 6, at 2-8. Focusing the analysis solely on Marlin's expectations, without regard for the expectations of TSMC, its customers, and the public, is not balanced or fair. TSMC, its customers, and the public have "settled expectations" that heavily outweigh Marlin's alleged expectations.

After acquiring the '194 patent in June 2021 (*see* Ex-1031) Marlin began an enforcement campaign against the semiconductor industry, including TSMC's customers. *See* Ex-2104, at 1. This includes asserting patents against TSMC and its customers in the ITC to seek an exclusion order while good faith negotiations with TSMC remained open. The Petition should be referred to resolve this dispute before Marlin's enforcement of the '194 patent against TSMC or its customers disturbs the parties' well-settled expectations that the '194 patent will remain dormant.

First, TSMC and its customers had settled expectations that the '194 patent would not be asserted due to inaction during most of the '194 patent's life. TSMC had been producing the technology at issue in the ITC for over three years before Patent Owner acquired the '194 patent from UMC and over seven years before the Patent Owner first sued TSMC. *See* Ex-1032 (7nm Technology). During that time both Marlin and UMC, who Marlin claims is "TSMC's main competitor" (Paper 6, at 3), remained silent and inactive. This inactivity created settled expectations for TSMC and its customers that the patent would remain dormant. These expectations weigh against denial. *See generally Apple Inc. v. Ferid Allani*, IPR2025-00856, Paper-11 (Sep. 5, 2025) (informative) (declining to discretionarily deny institution based on Petitioner's expectations that the challenged patent not be asserted after 11 years of Patent Owner inaction).

UMC does not have a history of asserting its patents. According to Docket Navigator, UMC has been involved in a total of 19 patent actions since 1992 and is listed as a plaintiff/complainant in only 5 cases, none of which are after 2009. *See generally* Ex-1033. UMC's longstanding inactivity created settled expectations for TSMC and its customers that the patent would remain dormant.

Marlin's recent activity cannot unwind the settled expectations of TSMC and its customers created by UMC's longstanding inaction. In analogous bodies of law, the settled expectations of others would exceed those of a new property owner under

such circumstances. *See* Restatement (First) of Prop. § 459 cmt. a (1993) (“Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance.”); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) (“[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.”); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020).

Second, Marlin has not presented any persuasive evidence that the ’194 patent was ever “commercialized, asserted, marked, licensed, or otherwise applied” in the same “particular technology space” where it now seeks enforcement. *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasy, Inc.*, IPR2025-00531, Paper-10, at 3 (July 17, 2025) (internal quotations omitted). This weighs against any claim by Marlin of “settled expectations.” *See Home Depot U.S.A., Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper-11, 2-3 (Sep. 4, 2025) (informative). The ’194 patent has not been asserted in litigation in any venue, against any party. Marlin alleges that UMC is “TSMC’s main business competitor” (Paper 6, at 1), yet Marlin has not identified any evidence suggesting UMC enforced or demanded a license for the ’194 patent from TSMC (or anyone) during the 11 years UMC owned the patent.

Marlin argues that the ’194 patent “has been commercialized, at least in the form of licensing” with Intel Corporation and Samsung Electronics Co., Ltd. *See*

Paper 6, at 4-5. But Marlin supports this contention through a bare assertion by its corporate representative Garrett Dempsey that fails to provide any details regarding those licenses by which to assess their relevance or significance, including whether they practice specifically the '194 patent. *See* Ex-2104. And, regardless of their scope, it can be inferred that those licenses arose from Marlin's recent enforcement campaign, which began long after TSMC's settled expectations of non-enforcement had been established. Marlin's licensing-based arguments are therefore readily distinguishable from *Alliance Laundry Sys., LLC v. PayRange LLC*, where the Patent Owner submitted detailed evidence of the license terms, including covered patents and dollar amounts. *See* IPR2025-00950, Paper 1 (Sep. 19, 2025) (informative).

Moreover, Marlin fails to put forth any evidence that these purported licenses were public or that its purported licensees marked their products in any way to evidence commercialization that would disturb TSMC's settled expectations in freedom to operate. As best as TSMC can tell, news of this licensing campaign was not public until May 2025, after Marlin had already hauled TSMC into multiple tribunals. *See* Ex-1036; Ex-1037. Those news stories indicate that licenses were taken over Marlin's entire portfolio, containing hundreds of patents. *See id.* Marlin cannot reasonably infer settled expectations with respect to the validity and enforceability of the '194 patent from such a broad license. *See, e.g., Samsung Elecs. Co. Ltd. v. Wilus Inst. of Standards & Tech. Inc.*, IPR2025-00935, Paper 9, at 25

(July 30, 2025) (arguing for settled expectations based on patent pool licensing); *Wilus*, Paper 12, at 3 (Sept. 26, 2025) (referring petition to the Board).

When Marlin acquired patents (including the '194 patent) that had never been asserted in any proceeding, with the intention of enforcing them, Marlin's only reasonable expectation could be that the validity of those patents would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 (“timing” of a property purchase and “knowledge of the purchaser” are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (patent owners know their patents may be subject to post-issuance reconsideration proceedings).

Marlin attempts to deflect by alleging TSMC knew of the '194 patent through its own patent prosecutions, favoring denial under *iRhythm*. *See* Paper 6, at 4. But Marlin proves no such knowledge. Its vague reliance on the Google Patents “cited by” list appears to reference TSMC Patent No. 8,633,070. *See* Ex-2103 at 6. But the '070 patent does not cite the '194 patent; it cites only 2009/0039389, the application that led to the '847 parent. Ex-1038 ('070 patent). And that application was cited by the *Examiner*—not the applicant, as in *iRhythm*. *See* Paper 6, at 4; *iRhythm*, Paper 10, at 3. Even citation of an asserted patent during prosecution does not establish knowledge for indirect infringement or willfulness, particularly for a company like TSMC with tens of thousands of patents. *See, e.g., Spherix Inc. v. Juniper Networks*,

Inc., No. 1:14-CV-00578-SLR-SRF, 2015 WL 1517508, at *3 (D. Del. Mar. 31, 2015); *State Indus., Inc. v. A.O. Smith Corp.*, 751 F.2d 1226, 1236 (Fed. Cir. 1985) (“To willfully infringe a *patent*, the patent must exist and one must have knowledge of it.”). Citation of a mere parent application by an examiner in one of thousands of patents is likewise insufficient to disturb settled expectations of validity.

Finally, Marlin argues that licensing negotiations between the parties beginning in 2024 weigh against any claim of settled expectations by TSMC. *See* Paper 6, at 6-7 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc.* IPR2025-00693, Paper 13 (Aug. 14, 2025)). Marlin’s reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding involving the challenged patents. And second, *DataDome* did not argue that the Examiner had materially erred during prosecution. *See DataDome*, Paper 8, at 7; *id.*, Paper 12, at 26-31. Both of those factors differ in the present case and weigh in favor of referral.

Moreover, TSMC filed this Petition just over 9 months after Marlin asserted patents against TSMC in court. TSMC was more diligent than the *DataDome* Petitioner, who waited 15 months to file its IPR Petition. *See DataDome*, Paper 13; *DataDome*, Ex-1015 (December 1, 2023 letter refusing license); *DataDome*, Paper 5 (Petition filed March 14, 2025).

V. Referral Is an Efficient Use of Board Resources

Additionally, referral here is an efficient use of Board resources because there

is no parallel litigation involving the '194 patent, making the PTAB the most efficient forum to resolve this dispute. *See, e.g., Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper 12, at 2-3 (Aug. 12, 2025) (“[T]he parties are not involved in a parallel proceeding involving the challenged patents. As a result, there is no concern of inconsistent outcomes or significant duplication of efforts resulting from two proceedings operating in parallel.”); *Azurity Pharms., Inc. v. Helsinn Healthcare S.A.*, IPR2025-00945, Paper 11, at 2-3 (Sept. 19, 2025). No other tribunal is set to resolve the merits of this dispute, meaning there is no risk of duplicated efforts, inconsistent decisions, or unnecessary expenses for the parties.

Marlin argues this is not dispositive because petitions in *Intel Corp. v. Proxense LLC* were discretionarily denied despite having no *trial date*. *See* Paper 6, at 7 (citing IPR2025-00327, Paper 12, at 2 (June 25, 2025)). In *Intel*, however, the Acting Director explained that the discretionary decision to deny was based upon Petitioner’s failure to “provide any persuasive reasoning as to why an *inter partes* review is an appropriate use of Board resources.” *Intel*, Paper 12, at 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources, including to address the Examiner’s material errors, to ensure consistent results with the '847 patent proceeding, and to resolve the parties’ dispute in an efficient manner that avoids “unnecessary and counterproductive litigation costs” before Marlin asserts this patent in a court against TSMC.

Marlin has already indicated that it believes the '194 patent is infringed (*see* Ex-2014) and alleged in the ITC and district court that TSMC infringes the parent '847 patent (*see* Ex-1051). Referral before further litigation is an appropriate use of resources that promotes the ideals that underlie the IPR process. IPR is an efficient means to resolve the dispute over the validity of the '194 patent and to avoid “unnecessary and counterproductive litigation costs” before Marlin asserts this patent in a court against TSMC. *See* November 2019 Consolidated Trial Guide, at 56 (quoting H.R. Rep. No. 112-98, pt. 1, 40 (2010), 2011 U.S.C.C.A.N. 67, 69).

VI. National Security, Economic, and Public Interest Considerations Warrant Referral

The Office just yesterday issued new guidance noting it will consider whether the petitioner or patent owner manufactures products in the United States. *See generally* Memorandum from John A. Squires, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office, to All PTAB Users (Mar. 11, 2026). In short, TSMC does; Marlin, as a non-practicing entity based in Ireland, does not. And Marlin alleged through a claim chart that TSMC's 4nm, 5nm, and 7nm process technologies infringe the '194 patent, following with an ITC investigation asserting infringement of the '847 parent. *See generally* Ex-1051; Ex-2014. As further explained below, TSMC has committed to invest \$165 billion to onshore advanced semiconductor manufacturing to the U.S., and TSMC's newly built advanced manufacturing facilities are producing products

for U.S. customers using TSMC’s accused 4nm process.

This threat to weaponize the ’194 patent undermines the U.S. semiconductor supply chain, harming priorities that this Administration has made clear are vital to U.S. economic interests and national security. Ex-1039, at 3; Ex-1040, at 1; Ex-1047, at 40. As Secretary Lutnick explained in April 2025, “national security” is the “key” reason to “bring semiconductors home.” Ex-1039, at 3-4.

This makes *inter partes* review of the ’194 patent an appropriate use of the Office’s resources—indeed a compelling one. TSMC’s advanced semiconductor fabrication capabilities are vital to leading U.S. companies (such as Apple, NVIDIA, and AMD who are buying the chips made at TSMC’s Arizona fab). More specifically, TSMC’s advanced semiconductor technology is vital to the U.S. supply chain and supports U.S. advanced semiconductor research and development in industries including AI, health care, and national security and defense. *See* Ex-1041, at 18-19. Promoting these industries is an important step in advancing the Administration’s priorities. *See* Ex-1039, at 3; Ex-1040, at 1.

Indeed, the Administration has recognized AI’s importance to the national security, and TSMC is an important part of the American AI-dominance strategy. *See generally* Ex-1042; Ex-1043; Ex-1045. TSMC “produces the advanced processors that Nvidia [], AMD [] and Apple [] rely on to bring AI to life,” including NVIDIA’s next-generation Blackwell AI chips for NVIDIA’s AI supercomputers.

Ex-1044, at 2. Healthcare is also an area of projected growth in the AI semiconductor market, where the demand for “advanced chips—TSMC’s specialty—will continue to surge.” Ex-1045, at 5. Blocking or burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing “direct effects on future patient care” and “far-reaching consequences” for the development of life-saving medical technology. Ex-1048, at 4.

Marlin does not dispute the serious impact a ban on importing TSMC’s advanced semiconductors into the U.S. would have to vital national security, public health, or economic interests. Instead, Marlin sets up a strawman, painting itself as protector of local industry. *See* Paper 6, at 9-10. The facts belie Marlin’s claim. Marlin does not practice the ’194 patent or any other patent it holds. No evidence suggests that Marlin, a foreign entity, has invested in the U.S. semiconductor technology space, only that Marlin has tried to assert recently acquired patents. Given Marlin’s assertion of patents against U.S. companies (e.g., Apple, Qualcomm, Broadcom), Marlin’s claim to be a protector of “local industry” rings hollow.

Moreover, although Marlin is attempting to rely on its license to Intel as its domestic industry basis in the ITC investigation, Intel is not a willing participant and does not seem to want this supposed “protection.” *See, e.g.*, Ex-1050, at 1; Ex-1051, at 60-63, 76-77. From the outset, Marlin’s claim charts in the ITC admitted that Intel uses *TSMC* to manufacture advanced semiconductors for *Intel* products. *See, e.g.*,

Ex-1049, at 6-8 (noting “[t]he Domestic Industry Product contains a TSMC semiconductor die which TSMC manufactured” and basing its domestic industry allegations on products made using TSMC’s N5P technology). Marlin’s allegation of “protecting US domestic industry” boils down to this: Intel’s business needs to be protected from the technologies that TSMC uses to make products *for Intel*. Marlin is hurting, not protecting, Intel and other U.S. semiconductor companies.

Finally, Marlin’s attempt to cast TSMC as a foreign entity that “import[s] infringing products” is baseless. Paper 6, at 9. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Dempsey, that any product made by TSMC infringes the ’194 patent. And the fact that TSMC is headquartered in Taiwan is irrelevant. If Marlin wishes to debate which foreign entity (Marlin or TSMC) is helping U.S. industry, TSMC is happy to oblige. TSMC has committed to invest \$165 billion to build manufacturing facilities in the United States in support of this Administration’s goal to onshore advanced semiconductor manufacturing to bolster U.S. economic and national security interests. *See* Ex-1039, at 3. TSMC’s Arizona facilities are already producing 4nm chips for American customers. *See* Ex-1046, at 2. Meanwhile, Marlin’s enforcement campaign against TSMC seeks to interrupt TSMC’s investment in Arizona and damage the core supply chain of semiconductor chips to the United States. National security, economic, and public interest considerations thus favor referral.

Dated: March 12, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Petitioner's Opposition to Patent Owner's Discretionary Denial Request** was served on March 12, 2026, via e-mail directed to counsel of record for Patent Owner at the following:

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