UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,
v.
MARLIN SEMICONDUCTOR LIMITED,
Patent Owner.

Case No. IPR2026-00061
U.S. Patent No. 8,076,194 B2

DECLARATION OF JOSEPH MCALEXANDER

I. QUALIFICATIONS

1. I am a Registered Professional Engineer (#79454) and the President of M^{c}Alexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. OVERVIEW

4. The Petition alleges that Hoentschel262 (Grounds 1A-C) and Wang753 (Grounds 2A-C) anticipate or render obvious independent claims 1 and 10. I disagree.

5. In Grounds 1A-C, the Petition relies solely on Hoentschel262's statement that epitaxial growth can include "overfilling" to support its allegation that the top surface of the alleged epitaxial layer is above the surface of the semiconductor substrate. The Petition concedes that Hoentschel262 does not illustrate epitaxial layers above the substrate. The single word "overfilling" is insufficient to teach or suggest elements 1[e] and 10[e]. Moreover, even if the word "overfilling" was enough to suggest "the top surface of the epitaxial layer is above the surface of the semiconductor substrate," the Petition offers no explanation for how the rest of Hoentschel262's fabrication process could be modified to accommodate such raised epitaxial layers; and other fabrication steps would need to be altered in order to accommodate this change. Hoentschel262 does not even address how to accommodate such a modification. In the '194 patent, the solution to this problem "is to form the epitaxial layer before forming the spacer." EX1001, 7:15-16. This allows the spacers to be formed on top of raised epitaxial layers. In contrast, in the embodiment of Hoentschel262 that the Petition relies upon, part of the spacer is formed before the alleged recesses are etched and the alleged epitaxial layers are formed. As such, Hoentschel262's fabrication process is incompatible with raised epitaxial layers. The Petition fails to address this issue at all. As such, the Petition fails to establish that Hoentschel262 discloses or renders obvious

"wherein a contact surface of the [first] epitaxial layer and the spacer is above the surface of the semiconductor substrate."

6. In Grounds 2A-2C, the Petition relies solely on Wang753's non-scale drawings to support its allegation that the top surface of the alleged epitaxial layer is above the surface of the semiconductor substrate. I understand that the Federal Circuit has rejected as a matter of law an attempt to rely on non-scale drawings to establish and prove "proportions," "sizes," or "quantitative relationship" of elements in those drawings. Moreover, the Petition's interpretations of Wang753's figures are inconsistent with, and not supported by, Wang753's text and the figures themselves. Wang753 expressly describes that its "SiGe stressors" (the alleged epitaxial layer) are grown "***in*** recesses 116," rather than out of the recesses and above the substrate. Wang753's description is in direct contrast to the challenged '194 patent, which describes that its epitaxial layers are not merely grown "in" the recesses, they are further grown "higher than the surface of the semiconductor substrate:" "epitaxial layer 220 is grown in the recess 218 ***and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.***" EX1001 at 3:51-54 (emphasis added).

III. MATERIALS CONSIDERED

7. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including

U.S. Patent No. 8,076,194 B2 (the "'194 Patent"), the '194 Patent prosecution history, and the asserted prior art.

IV. UNDERSTANDING OF THE LAW

8. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

9. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

a. a method claim, which covers a process/activity, or

b. an apparatus claim, which covers a physical machine, etc.

10. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

11. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

12. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

13. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

14. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

15. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider

certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a "nexus") between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

16. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

17. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

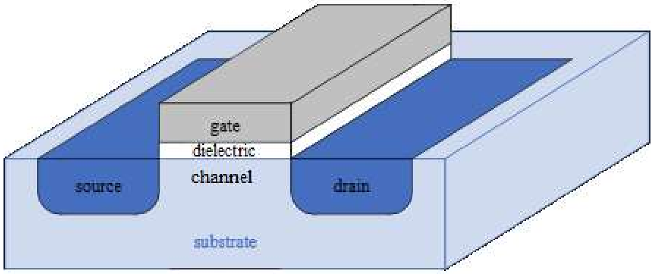
A. Basic Transistor Components

18. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). EX2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. EX2002 at 3.

19. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. EX2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. EX2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. EX2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. EX2002 at 31-34.

20. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See*,

e.g., EX2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



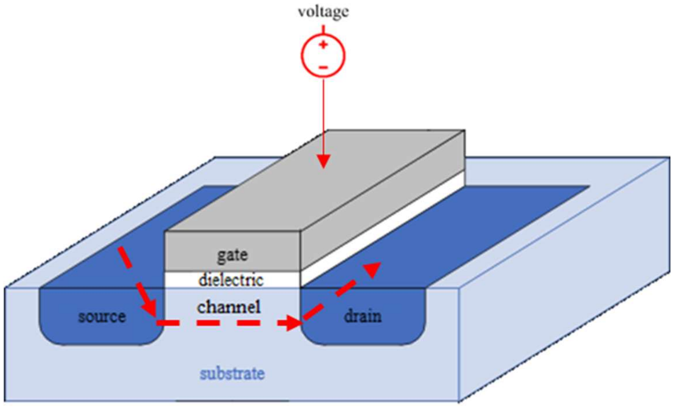
See, *e.g.*, EX2002 at 510-511.

21. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). EX2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). EX2002 at 510-511.

22. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. EX2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the "flow of charge" (current) between the gate and the channel, but the applied voltage results in the creation of a "field effect" in the channel. EX2002 at

510-511. This "field effect" either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). EX2002 at 510-511.

23. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.



See, *e.g.*, EX2002 at 510-511 (annotated).

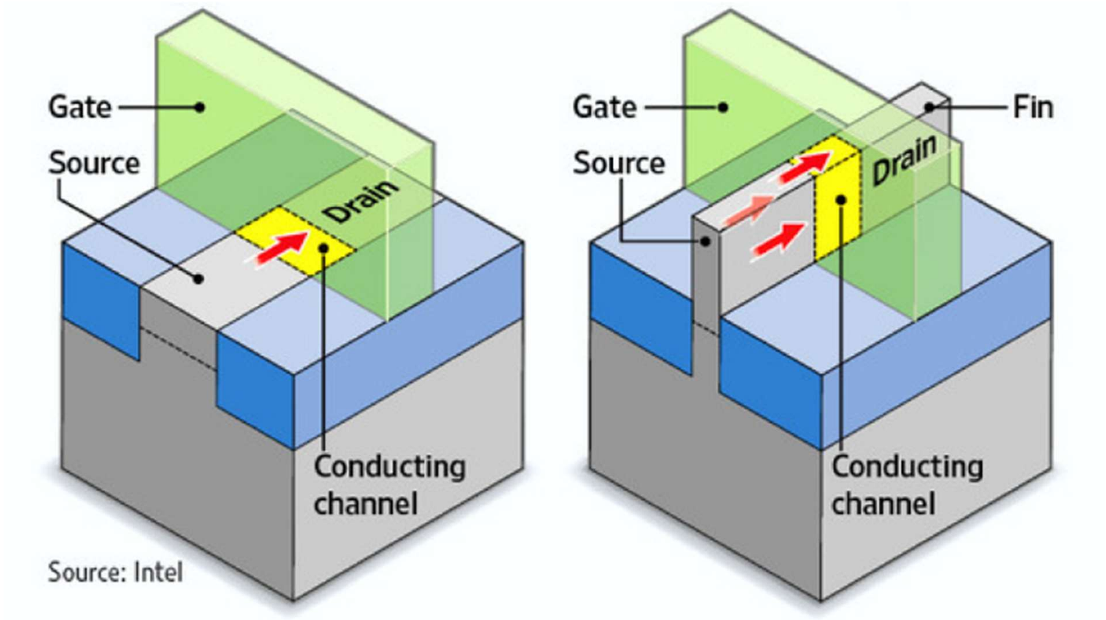
B. Planar vs. Three-Dimensional Transistors

24. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip

has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a "FinFET."

25. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a "planar" FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

26. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



Source: Intel

27. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor ("FinFET"), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

28. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

29. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

30. In the first stage, the semiconductor material itself is created. EX2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. EX2002 at 13.

31. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called "wafers." EX2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

32. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. EX2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. EX2002 at 14.

33. In the packaging stage, the wafer is separated into individual chips. EX2002 at 14-15.

2. The Wafer Fabrication Stage

34. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. EX2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* EX2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

35. **Layering** is the operation used to add thin layers to the semiconductor substrate. EX2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. EX2002 at 72.

36. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. EX2002 at 72.

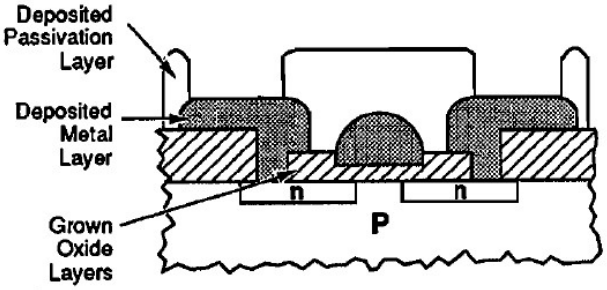


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

37. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. EX2002 at 72-73. This creates a pattern on the wafer surface. EX2002 at 72-73.

38. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. EX2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

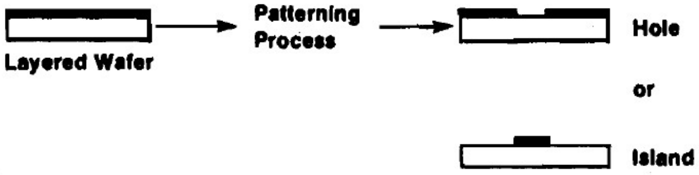


Figure 4.7 Patterning.

39. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

> These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

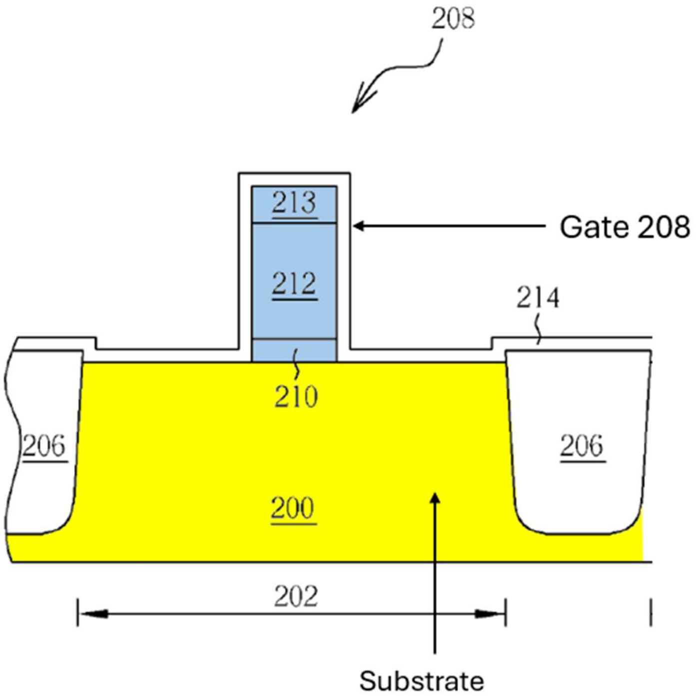
EX2002 at 73.

VI. THE CHALLENGED ’194 PATENT

40. The ’194 patent describes and claims improved FET designs intended to improve the transistor’s performance. The patent discloses a number of ways of improving performance, including combining “raised epitaxial layers” with various other transistor features.

41. An “epitaxial layer” is a high-purity layer of semiconducting material. EX2002 at 18, 380. As the patent describes, these layers may be formed within recesses in the semiconductor substrate and, in addition, “may be grown higher than the surface of the semiconductor substrate 200,” thereby making them “raised epitaxial layers.” *E.g.*, EX1001 at 3:41-54, 6:19-22.

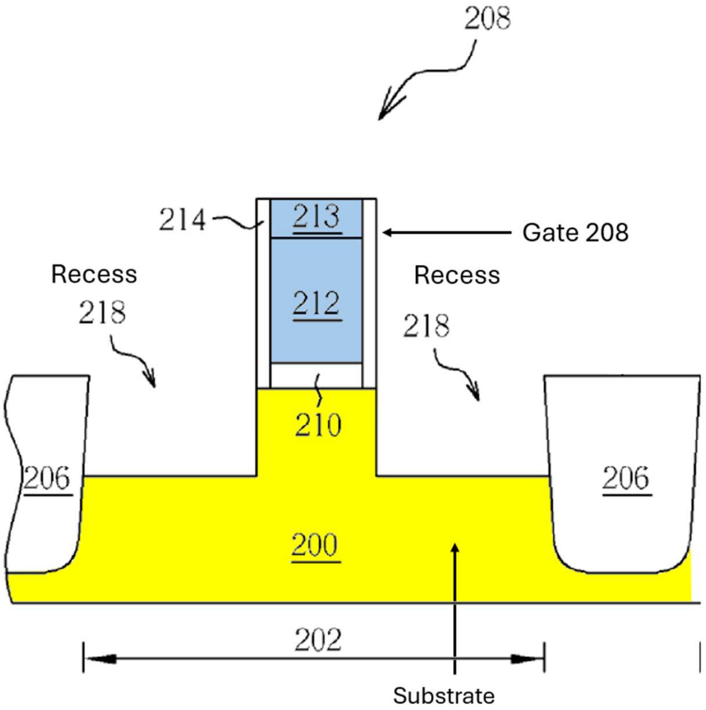
42. The ’194 patent describes a method of fabricating a transistor structure with such raised epitaxial layers. For example, as illustrated below in an annotated portion of Figure 1, the method may start with a gate 208 (annotated in blue and comprising dielectric layer 210, conductive layer 212, and cap layer 213) positioned on substrate 200 (annotated in yellow):



EX1001 at Fig. 1 (annotated), 2:56-3:6.

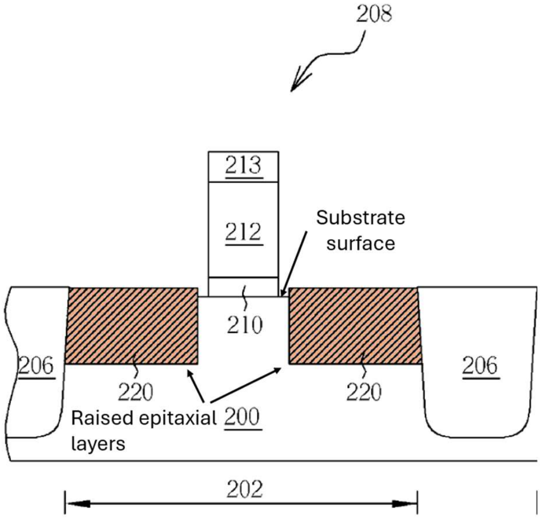
43. As shown, "[s]ubsequently, a protective layer 214 is formed on the semiconductor substrate 200, and the protective layer 214 covers the surface of [the] gate 208." EX1001 at 3:28-30.

44. The substrate is then patterned to form recesses therein. For example, as shown below in an annotated portion of Figure 2, portions of the substrate may be selectively etched away to form recesses 218:



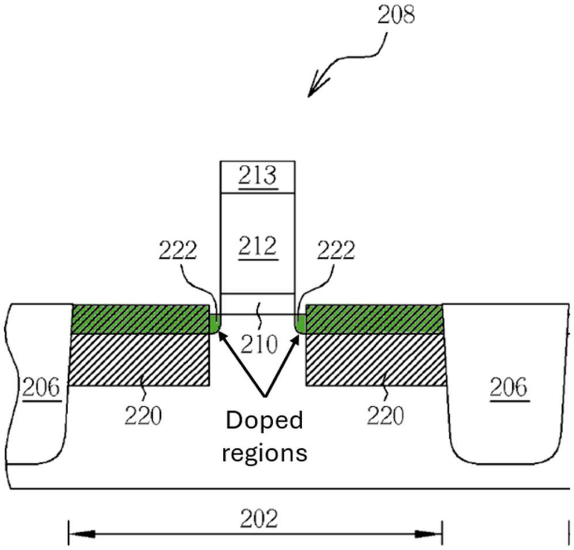
EX1001 at Fig. 2 (annotated), 3:23-28.

45. “Raised epitaxial layers” are then formed in these substrate recesses and next to sides of the gate. For example, “an epitaxial growth process is carried out to form epitaxial layers 220 in the recesses 218.” EX1001 at 3:33-34. As the patent describes, these layers may be formed to a height higher than the surface of that substrate, thereby making them “raised epitaxial layers”: “epitaxial layer 220 is grown in the recess 218 and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” EX1001 at 3:35-38. The illustrative raised epitaxial layers are shown in orange in the following annotated excerpt from Figure 3:



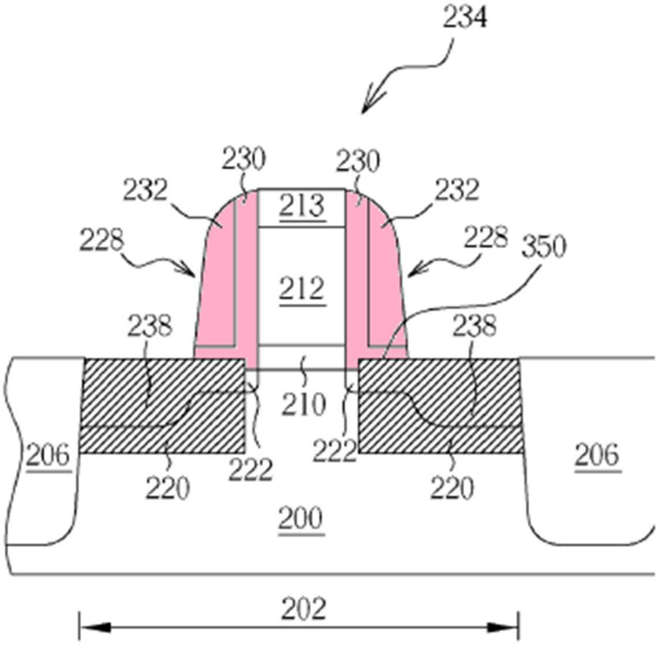
EX1001 at Fig. 3 (annotated), 3:35-38.

46. Selective doping is then performed to form doped regions 222 (annotated in green) in the substrate:



EX1001 at Fig. 4 (annotated), 3:45-48.

47. Spacer 228 (shown below in pink and comprising layers 230 and 232) is subsequently formed on the sidewalls of the gate:



EX1001 at Fig. 5 (annotated).

48. As shown, "[b]ecause each spacer 228 . . . lies over the raised epitaxial layer 220, thus each spacer 228 . . . is tilted upward and a contact surface 350 of the epitaxial layer 220 and the spacer 228 is above the surface of the semiconductor substrate 200." EX1001 at 4:12-17.

49. Significantly, the bottom of the spacer 228 contacts the epitaxial layer 220 above the top of the substrate 200 because the spacer is formed after the epitaxial layer 220 has been formed. A key characteristic of the improved fabrication process

"is to form the epitaxial layer before forming the spacer." *Id.*, 7:15-16. "[T]hus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer." EX1001, 7:16-18. Moreover, "the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the micro-loading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased." *Id.*, 7:18-25.

50. Each of the challenged claims includes the foregoing inventive concepts and combinations, including spacers lying over raised epitaxial layers with a contact surface above the substrate. For example, independent claim 1 recites:

> 1[pre] A method of fabricating a MOS transistor, comprising:
>
> 1[a] providing a semiconductor substrate;
>
> 1[b] forming at least a gate on the semiconductor substrate;
>
> 1[c] forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;
>
> 1[d] forming at least a recess within the semiconductor substrate adjacent to the gate;
>
> 1[e] ***forming an epitaxial layer in the recess, wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate***; and

> 1[f] ***forming a spacer on the sidewall of the gate and on a portion of the epitaxial layer wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate***.

EX1001, claim 1.

51. Similarly, independent claim 10 recites:

> 10[pre] A method of fabricating a CMOS transistor, comprising:
>
> 10[a] providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area;
>
> 10[b] forming a gate on the first conductive transistor area and on the second conductive transistor area respectively;
>
> 10[c] forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate;
>
> 10[d] forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area;
>
> 10[e] ***forming a first epitaxial layer in the first recess, wherein the top surface of the first epitaxial layer is above the surface of the semiconductor substrate***; and

> 10[f] ***forming a spacer on the sidewall of each gate and at least on a portion of the first epitaxial layer, wherein a contact surface of the first epitaxial layer and the spacer is above the surface of the semiconductor substrate***.

EX1001, claim 10.

VII. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

A. Grounds 1A, 1B, And 1C

52. In Grounds 1A and 1B, the Petition alleges that Hoentschel262 anticipates (Ground 1A) and renders obvious (Ground 1B) independent claims 1 and 10 and certain claims depending from claims 1 and 10. Pet., 14. In Ground 1C, the Petition alleges the combination of Hoentschel262 and Wang 407 renders obvious dependent claim 6, which depends from claim 1. Pet., 66. All of these grounds fail because Hoentschel262 does not disclose or render obvious at least elements 1[e], 1[f], 10[e], and 10[f].

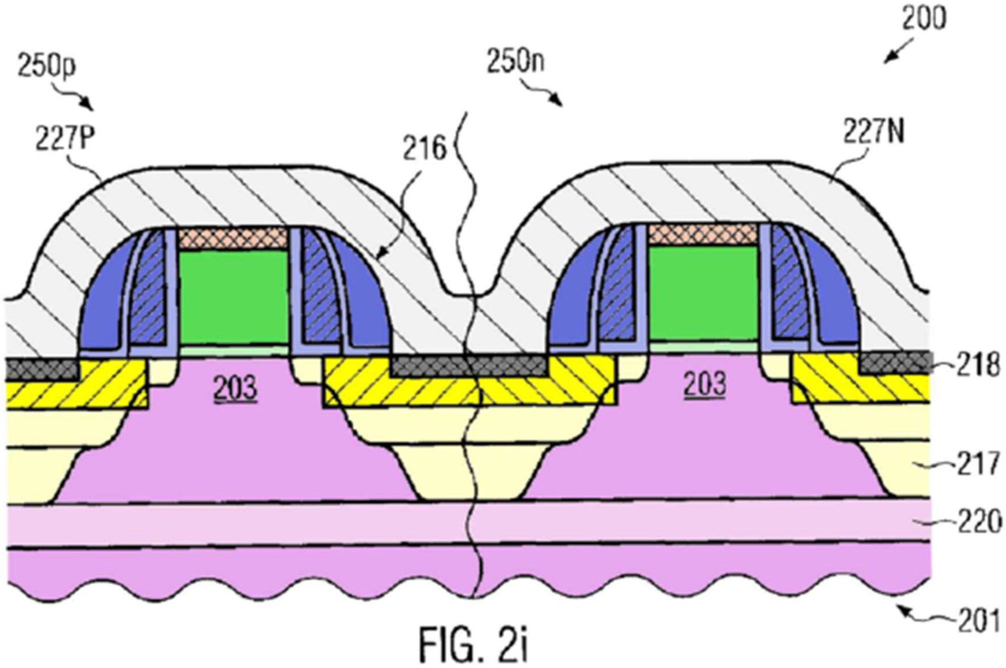
1. Hoentschel262 Does Not Disclose Or Render Obvious "Wherein The Top Surface Of The [First] Epitaxial Layer Is Above The Surface Of The Semiconductor Substrate" (Elements 1[e]/10[e]) And "Wherein A Contact Surface Of the [First] Epitaxial Layer And The Spacer Is Above The Surface Of The Semiconductor Substrate" (Elements 1[f]/10[f])

53. The sole basis for the Petition's allegation that Hoentschel262 discloses or renders obvious "wherein the top surface of the epitaxial layer is above the surface

of the semiconductor substrate" is Hoentschel262's statement that the epitaxial growth process can include "any desired degree of underfilling or overfilling, or a substantially flush configuration." Pet., 28 (citing EX1005-Hoentschel262 at 13:21-26, 9:11-20). According to the Petition, the single word "overfilling" in Hoentschel262 is apparently sufficient to disclose or render obvious elements 1[e] and 10[e]. I disagree. The Petition's mapping of this claim limitation is flatly contrary to the embodiments of Hoentschel226 depicted in the drawings as supported by the specification description. EX1005-Hoentschel262, Figs. 2a-2i. To overcome this actual disclosure, Petitioner relies on a single word from the specification – "overfilling" – but that single word cannot erase the structure shown in the drawings and mandated by the deposition sequence (as explained below) disclosed in Hoentschel226. Indeed, the Petition concedes that Hoentschel262 does not illustrate epitaxial layers above the substrate. Pet., 29. As such, the mere use of the term "overfilling" in Hoentschel262, without more disclosure, is insufficient to disclose or render obvious elements 1[e] and 10[e].

54. Moreover, even if the word "overfilling" was sufficient to suggest "wherein the top surface of the [first] epitaxial layer is above the surface of the semiconductor substrate," Hoentschel262 does not disclose or render obvious "wherein a contact surface of the [first] epitaxial layer and the spacer is above the surface of the semiconductor substrate," as required by all challenged claims. The

Petition alleges that "FIG. 2i shows that Hoentschel262's spacers extend onto the epitaxial layers":



Hoentschel262, FIG. 2i

Pet., 33 (showing annotated EX1005-Hoentschel262, Fig. 2i).

55. However, as shown above, the contact surface between the alleged spacers (in blue in the above figure) and the alleged epitaxial layers (in yellow in the above figure) is not above the alleged surface of the substrate (in pink in the above figure). Despite this, the Petition argues that hypothetically, if the epitaxial layers were above the substrate (which they are not, as illustrated), the contact surface

between the spacers and the epitaxial layer would be above the surface of the substrate, as required by elements 1[f] and 10[f]. Pet., 33-34. I disagree.

56. First, the Hoentschel262 description is inadequate to disclose or render obvious "wherein a contact surface of the epitaxial layer and the spacer is above the surface of the semiconductor substrate," as required by all challenged claims. Moreover, the Petition's argument fails because Hoentschel262's spacers, as depicted in Figure 2i, are incompatible with raised epitaxial layers that are above the substrate. A POSITA would have understood that, if epitaxial layers were raised above the surface of the substrate rather than flush with the substrate, other fabrication steps would need to be altered in order to accommodate this change. As explained above in Section VI, a key characteristic of the '194 patent's improved fabrication process "is to form the epitaxial layer before forming the spacer." EX1001, 7:15-16. This allows the spacers to be formed on top of raised epitaxial layers. In contrast, as explained below, in the embodiment of Hoentschel262 that the Petition relies upon, part of the spacer is formed before the alleged recesses are etched and the alleged epitaxial layers are formed. As such, Hoentschel262's fabrication process is incompatible with raised epitaxial layers.

57. Hoentschel262's Figure 2a through 2i embodiment is the only embodiment relied upon by the Petition. *See* Pet., 14-85. In this embodiment, the fabrication process includes forming a liner 207A (in red below) on the surface of

the substrate 203 and gate 205, followed by forming a conformal spacer layer 206A to provide an offset away from the gate for the formation of a recess, as shown in Hoentschel262's Figs. 2b and 2c:

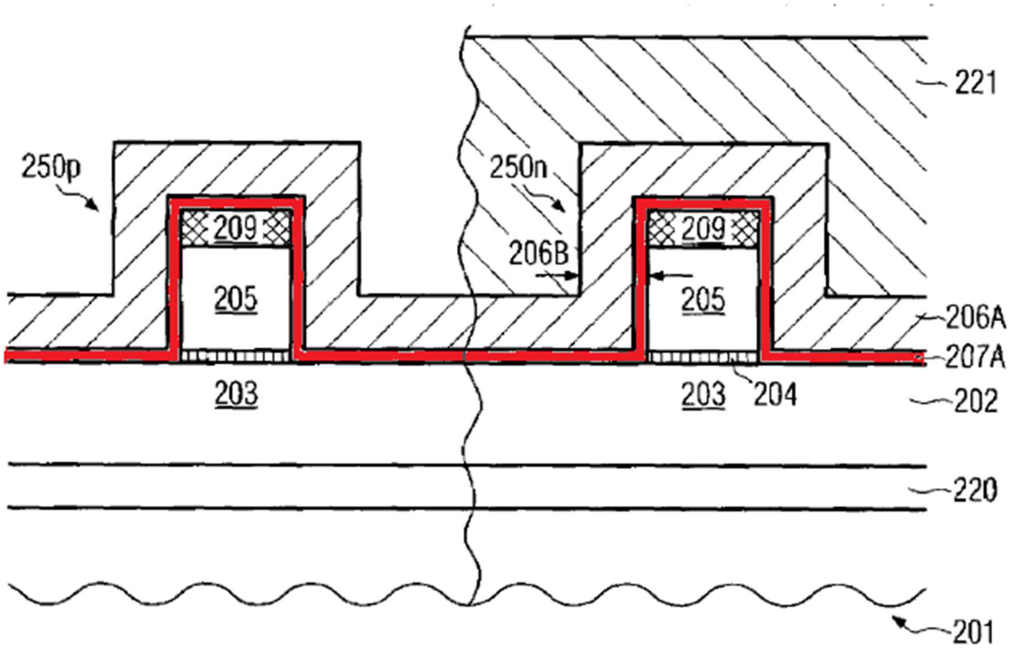


FIG. 2b

EX1005-Hoentschel262, Fig. 2b (annotated).

58. A portion of this liner 207A and spacer layer 206A is removed to form recesses 211p, offset from the gate structure by the residual portions of liner 207A and spacer 206A (labeled as 206) , as shown in Fig. 2c:

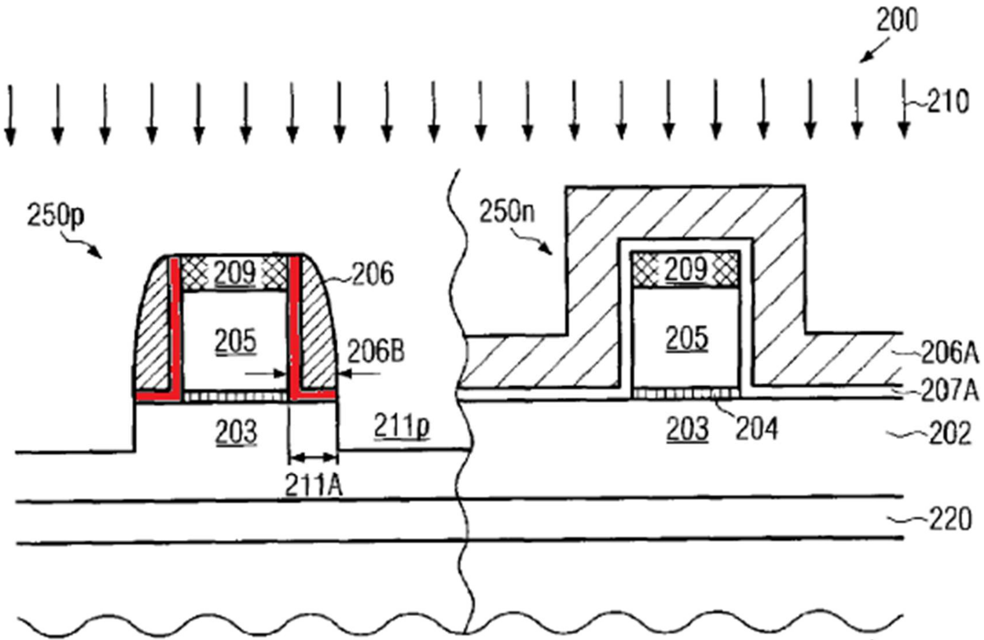


FIG. 2c

EX1005-Hoentschel262, Fig. 2c (annotated).

59. This portion of the liner 207A and spacer 206 persists through the fabrication process (*see*, *e.g.*, *id*., Figs. 2c-2g) and eventually forms part of sidewall spacer structure 216, as shown in Fig. 2i:

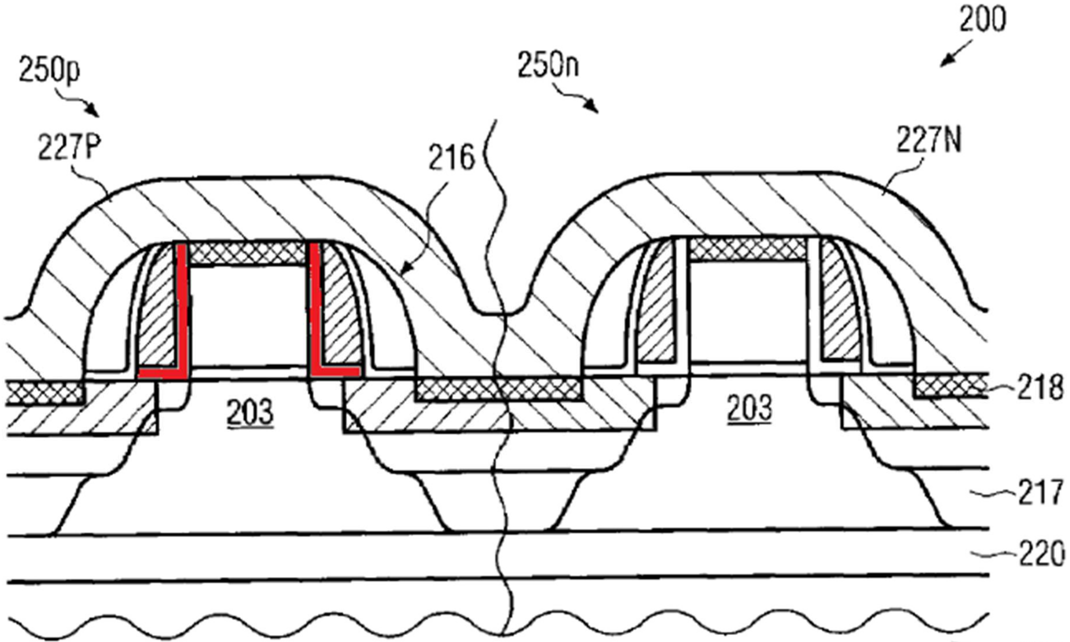


FIG. 2i

EX1005-Hoentschel262, Fig. 2i (annotated).

60. Sidewall spacer structure 216 is the spacer that the Petition identifies as allegedly satisfying elements 1[f] and 10[f]. Pet., 33.

61. Beyond the drawings, the sequence of deposition specified in Hoentschel262 mandates that bottom of the liner 207a is never above the substrate. As discussed above, the liner 207a is deposited on the substrate 201 prior to formation of the recesses 211p and, therefore, prior to the epitaxially grown material 214p. The epitaxial growth, therefore, cannot raise the contact surface of the liner

207a above the top of the substrate, since the liner 207a is in place before the epitaxial growth begins.

62. Petitioner's reliance on Hoentschel262's reference to "overfilling" cannot change the geometry mandated by the deposition sequence. Pet., 33. Even if the epitaxial material were to somehow grow laterally to a position underneath the liner 207A, such growth would not change the vertical position of the liner 207A. Again, the liner 207a is already in position before the epitaxial growth, and lateral "overfilling" cannot change its position vertically. *Id.* Since the bottom of the vertical position of the bottom of the liner 207A is fixed at the top of the substrate, the contact surface between the liner 207A and the epitaxially-grown material 214p cannot be above the top of the substrate.

63. As can be appreciated from Fig. 2i (annotated) above, because the liner 207a is formed along the surface of the substrate and extends onto the epitaxial layer, and because the liner 207a is part of the sidewall spacer 216, Hoentschel262's sidewall spacer 216 is simply incompatible with a raised epitaxial layer with a top surface above the substrate. The Petition fails to address this incompatibility. Pet., 33-34. Nor does the Petition explain how or why a POSITA would have modified Hoentschel262's fabrication process to form its spacers on a raised epitaxial layer. *Id*. And as stated above, Hoentschel262 fails to provide any details to support having a raised epitaxial layer.

64. Accordingly, Hoentschel262 fails to disclose or render obvious elements 1[f] and 1[f].

2. Ground 1C Fails For The Same Reasons As 1A And 1B

65. Ground 1C adds the Wang407 reference to address additional limitations of certain dependent claims, each of which depends from either independent claim 1 or independent claim 10. Pet., 66. Ground 1C does not provide any further analysis regarding claims 1 or 10. Pet., 66-84. Thus, Ground 1C fails for the same reasons as Grounds 1A and 1B.

B. Grounds 2A, 2B, And 2C

66. In Grounds 2A and 2B, the Petition alleges that Wang753 anticipates (Ground 2A) and renders obvious (Ground 2B) independent claims 1 and 10 and certain claims depending from claims 1 and 10. Pet., 84. In Ground 1C, the Petition alleges the combination of Wang753 and Hoentschel262 renders obvious dependent claim 6, which depends from claim 1. Pet., 111. All of these grounds fail because Wang753 does not disclose or render obvious at least elements 1[e] and 10[e].

1. Wang753 Does Not Disclose Or Render Obvious "Wherein The Top Surface Of The [First] Epitaxial Layer Is Above The Surface Of The Semiconductor Substrate" (Elements 1[e]/10[e])

67. Wang753 does not disclose or render obvious "wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate," as required by claims 1 and 10. Indeed, Wang753 never mentions, describes, or

suggests anything regarding the top surface of an epitaxial layer. The Petition does not assert otherwise or even attempt to identify a single mention or description of such epitaxial layers in Wang753. Pet., 92-93.

68. The Petition points to Wang753's "SiGe stressors" as the alleged epitaxial layer. *Id*. But Wang753 simply describes that its stressors 118 are "grown in [substrate] recesses 116," rather than grown out of and above those recesses. *E.g.*, EX1007-Wang753 at 4:10-11, 4:14-17. The Petition admits that Wang753 describes that "[t]he SiGe stressors [are] epitaxially grown ***in*** the recesses 116," and identifies no description of the stressors being further grown out of the recesses and above the substrate. Pet., 92 (emphasis added).

69. In light of the Wang753's complete failure to describe or identify any epitaxial layer with a top surface above the substrate, the Petition resorts to interpreting select figures from Wang753 in an effort to find this missing limitation. Pet., 92-93 (citing EX1007-Wang753, Figs. 5 and 6). But the Petition's attempt to rely on non-scale drawings is inconsistent with and not supported by the accompanying text and the drawings themselves.

a. The Petition Relies On Non-Scale Drawings

70. I understand that the Federal Circuit has repeatedly admonished that invalidity arguments made based solely on drawings not explicitly made to scale are unavailing.

71. Here, Wang753 never states or suggests that its drawings or any elements depicted therein are to scale, and the Petition does not assert otherwise. Nor would any POSITA expect these simplistic drawings to be to scale, because a transistor in 2006 (when Wang753 was filed) was roughly 45 nanometers (where a human hair diameter is 50,000-100,000 nanometers), with a single chip containing hundreds of millions of transistors. Thus, no POSITA would understand Wang753's drawings to be drawn to scale or to represent the actual shapes and proportions of their elements.

72. Because the drawings and their elements are not explicitly to scale, I understand that Petitioners cannot, as they attempt to do here, properly rely on those drawings to establish and prove the "proportions," "sizes," or "quantitative relationship" of any elements in those drawings. I understand that the Federal Circuit has repeatedly made clear that this prohibition on relying on drawings in this manner is well-established.

b. The Petition's Interpretations Of Wang753's Figures Are Unsupported

73. Even if relying on non-scale drawings were not reversible error, Grounds 2A and 2B would still fail because the Petition's interpretations of Wang753's figures are inconsistent with, and not supported by, Wang753's text and the figures themselves. Wang753 expressly describes that its "SiGe stressors" are

grown "***in*** recesses 116," rather than out of the recesses and above the substrate. EX1007-Wang753 at 4:10-11, 4:14-17. Wang753's description is in direct contrast to the challenged '194 patent, which describes that its epitaxial layers are not merely grown "in" the recesses, they are further grown "higher than the surface of the semiconductor substrate:" "epitaxial layer 220 is grown in the recess 218 ***and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.***" EX1001 at 3:51-54 (emphasis added).

74. Indeed, the Petition does not dispute that Wang753 fails to describe the claimed epitaxial layer "wherein the top surface of the epitaxial layer is above the surface of the semiconductor substrate." Instead, the Petition merely asserts that "Wang753 discloses an epitaxial growth process that takes place in the PMS source/drain recesses: 'FIG. 5 illustrates the formation of SiGe stressors 118 and 318 in recesses 116 and 316, respectively. It is preferred that the SiGe stressors be epitaxially grown in the recesses 116 and 316.'" Pet., 92 (quoting EX1007-Wang753, 4:14-17). The Petition does not assert—and could not reasonably assert—that this passage somehow describes epitaxial layers wherein the top surface is above the substrate or otherwise describes that that Wang753's "SiGe stressors" are further grown out from the recess and above the surface of the substrate.

75. Accordingly, Wang753 fails to disclose or render obvious elements 1[e] and 10[e]. Thus, Grounds 2A and 2B fail.

2. Ground 2C Fails For The Same Reasons As Grounds 2A and 2B

76. Ground 2C adds Hoentschel262 to address additional limitations of dependent claims 4 and 13, which depend from independent claims 1 and 10, respectively. Pet., 111. Ground 2C does not provide any further analysis regarding claims 1 or 10. Pet., 111-114. Thus, Ground 2C fails for the same reasons as Grounds 2A and 2B.

Dated: March 12, 2026

Joseph C. McAlexander III
Joseph C. McAlexander III