

No. 2025-1378

**IN THE
UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

SAMSUNG ELECTRONICS CO., LTD.,

Appellant,

v.

NETLIST, INC.,

Appellee.

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in No. IPR2023-00847

APPELLANT'S REPLY BRIEF

September 15, 2025

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**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

CERTIFICATE OF INTEREST

Case Number 2025-1378

Short Case Caption Samsung Electronics Co., Ltd. v. Netlist, Inc.

Filing Party/Entity Samsung Electronics Co., Ltd.

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Samsung Electronics Co., Ltd.	Samsung Semiconductor, Inc.	

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ARGUMENT

I. The Board’s Narrow Reading of the “Data Path” Requirement Cannot Be Sustained

Netlist does not deny that the Board adopted a construction of “*data path*” and applied that construction in its final written decision. BB34-35; RB31. Because that construction is improperly narrow, “the appropriate course in this case, as in so many others involving a reversal of a Board claim construction, is to vacate the Board’s decision and remand the matter.” *Kaken Pharm. Co. v. Iancu*, 952 F.3d 1346, 1355 (Fed. Cir. 2020).

Perhaps not fully confident in the Board’s construction, Netlist leads instead with a new argument that misstates Samsung’s position as to the prior art’s disclosure of the “*data path*” limitation. RB25-31. The sections below first address the Board’s construction of “*data path*” before turning to Netlist’s new argument.

A. The Board Erred in Departing from the Ordinary Meaning

1. Netlist Cannot Rely on the Board’s Error to Substitute a New Construction

While Netlist purports to defend the Board’s construction—i.e., that the data path “is in” the data signal line, Appx17—in actuality it does not and cannot. RB31-36. Rather, Netlist effectively proffers a different construction of “corresponds to” under the guise of applying the Board’s “is in” construction “*in context*.”¹ RB39.

¹ Emphasis added and internal quotation marks omitted unless indicated otherwise.

However, Netlist identifies no such context (and ignores the context of limitations 1[e], 1[f], 2[a], 2[e], 10, and 11, *see* BB37-40, 43-46). Rather, Netlist points to instances where the Board purportedly used “corresponds to” in its ordinary meaning. RB39. In so doing, Netlist does not give any reason to disregard the Board’s previous clear definitional statement of using those words to mean “is in.” *Id.* Nor can Netlist overcome this clear definitional statement by misdirecting the Court’s attention to the construction of other claim terms—e.g., “*data path*”—in isolation. *Id.*

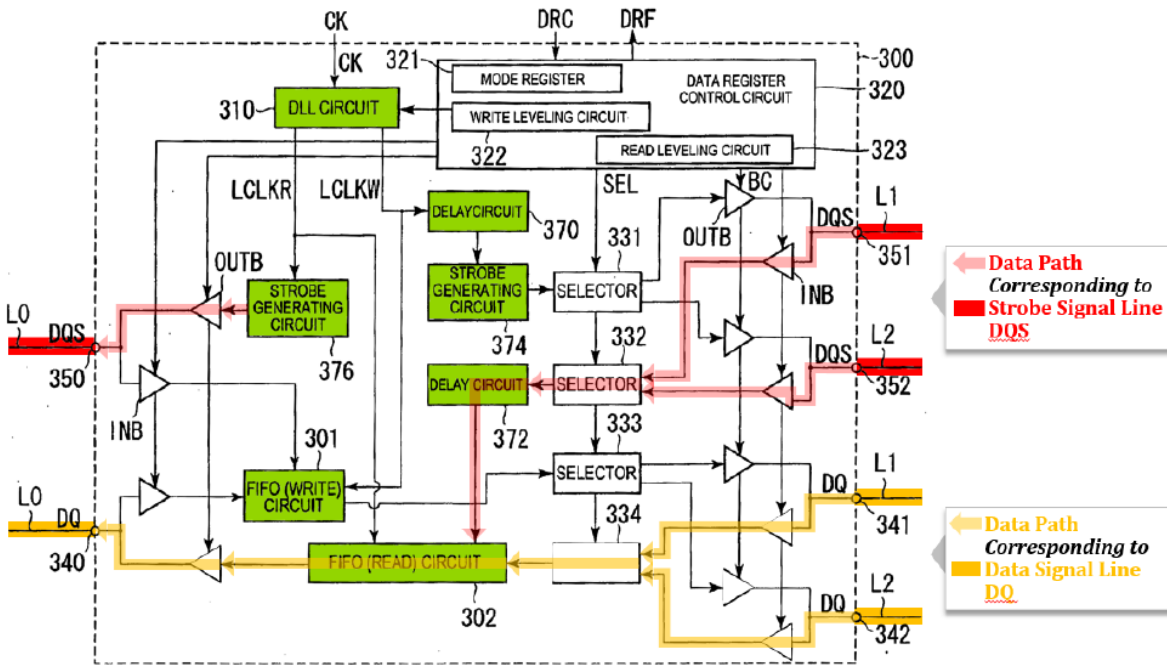
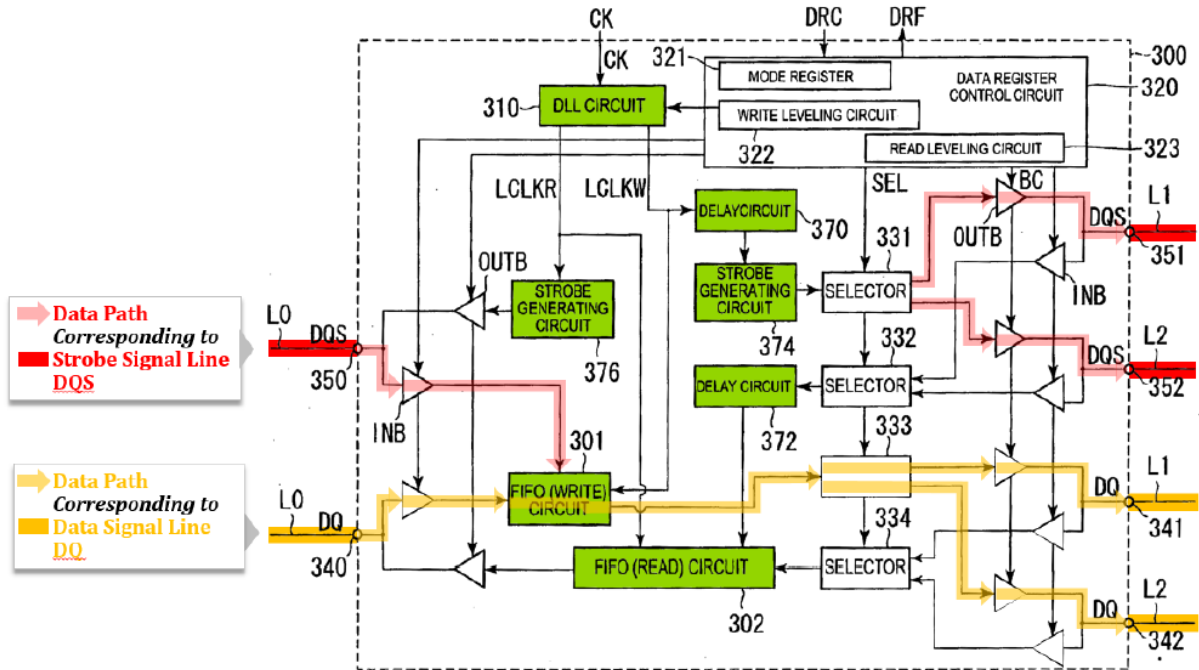
Netlist does not dispute the precedent showing that the Board’s understanding of “corresponding to” as “is in” was too narrow. *Id.* (citing *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013)). Netlist tries to sidestep that precedent by repeating its “in context” argument—namely, that every time the Board repeated the claim language “corresponding to” in its analysis, the Board was actually adopting a broader meaning of that phrase, “exactly as the plain language of claim 1 requires.” RB39-40. But Netlist cannot avoid Samsung’s challenge by rewriting the Board’s opinion to its liking. *HTC Corp. v. Cellular Commc’ns Equip., LLC*, 877 F.3d 1361, 1367 (Fed. Cir. 2017) (“Because [appellant]’s challenge is directed to the Board’s expression of its understanding of the scope of the claim term [], it is properly before us on appeal.”). The appropriate relief for the Board’s

improperly narrow construction is to vacate and remand. *Kaken Pharm.*, 952 F.3d at 1355.

2. Netlist’s New Construction Is Equally Flawed

While Netlist fails to defend the Board’s actual construction, its substitute construction is equally improper. Netlist now argues that “the data path is the path that connects the *data signal lines* [orange below]—not strobe signal lines [red below] or clock signal lines—through the buffer.” RB14 (emphasis in original).² Netlist’s illustration below confirms its extremely narrow construction limiting the “*data path*” to merely the lighter orange lines (to the exclusion of everything else in the buffer circuit 300):

² Netlist restates this exclusionary understanding several times. For example, “i.e., the data path is the route that data signals travel from a data signal line on one side of the buffer to a data signal line on the other side of the buffer. It follows that the claimed data path accommodates *only* data signals, not strobe (or some other) signals.” RB33 (emphasis in original); *see also* RB38 (“the data path of claim 1 ‘corresponds to’ only a *data signal line*”) (emphasis in original).



RB48.

Interpreting “corresponds to” as “connects,” to the exclusion of strobe signals, only defies the term’s ordinary meaning, just like the Board’s flawed approach.

Netlist seeks to impose negative limitations barring other “signals” from using the path, with strobe signals being one example, while acknowledging without rebuttal *Broadcom*’s admonition that correspondence is a “*much broader* concept” than equation. *Broadcom*, 732 F.3d at 1333; RB39; BB36.

Netlist’s attempt to distinguish *Respironics, Inc. v. Invacare Corp.*, 303 F. App’x 865 (Fed. Cir. 2008), and its analysis that “correspondence” encompasses a functional relationship, is unavailing. RB40-41. While Netlist claims that a “conceptual relationship” is different than a “mathematical relationship,” *id.*, *Respironics* contained no “mathematical” formula. The claim language may not be identical; however, the claimed “signal corresponding to” in *Respironics* plays a similar role to the claim language here—“*data path corresponding to*”—given that the claim language here also refers to “*a signal through the data path.*” Compare *Respironics*, 303 F. App’x at 880-81, with Appx117 (19:49-53).

Netlist’s arguments impermissibly assume that claim 1 says “data ***signal line*** path” when in fact the claim language is just “*data path.*” Netlist fails to address the facially broad ordinary meaning of “data” as a modifier. See *Mirror Worlds Techs., LLC v. Meta Platforms, Inc.*, 122 F.4th 860, 871 (Fed. Cir. 2024) (“The phrase ‘data unit’ has a facially broad ordinary meaning that does not exclude a query or a search criterion.”).

The broad meaning of “*data path*” in claim 1 is confirmed by limitation 1[f], which refers to delaying “*a signal through the data path*,” Appx117 (19:49-53), *not* “a *data* signal through the data path” as required by Netlist’s construction, RB33 (“*only data signals*”). Netlist never addresses this key point, which was raised throughout Samsung’s opening brief. BB1, 3, 20-21, 30, 33, 38, 43, 45 n.4. Nor does Netlist contest that limitation 2[e] shows that “*the signal through the data path*” includes *any* “*signal associated with the second memory operation*,” which limitation 10[a] expressly states can be a *strobe* signal (i.e., “*a strobe signal associated with the second memory operation*”), consistent with a POSITA’s knowledge that standard read and write “*memory operation[s]*” transmit *both* data (DQ) and strobe (DQS) signals. BB5-7, 44-45 & n.4; RB6. Netlist’s new construction limiting the “*data path*” to merely the light orange lines above (thus excluding everything else, including strobe signals shown in light red) thus contradicts the express claim language of 1[f], 2[e], and 10[a].

Neither “*data path*” nor “*corresponding to*” justifies Netlist’s new construction offered in place of the Board’s actual construction.

B. The Board Failed to View the Claim as an Artisan of Ordinary Skill

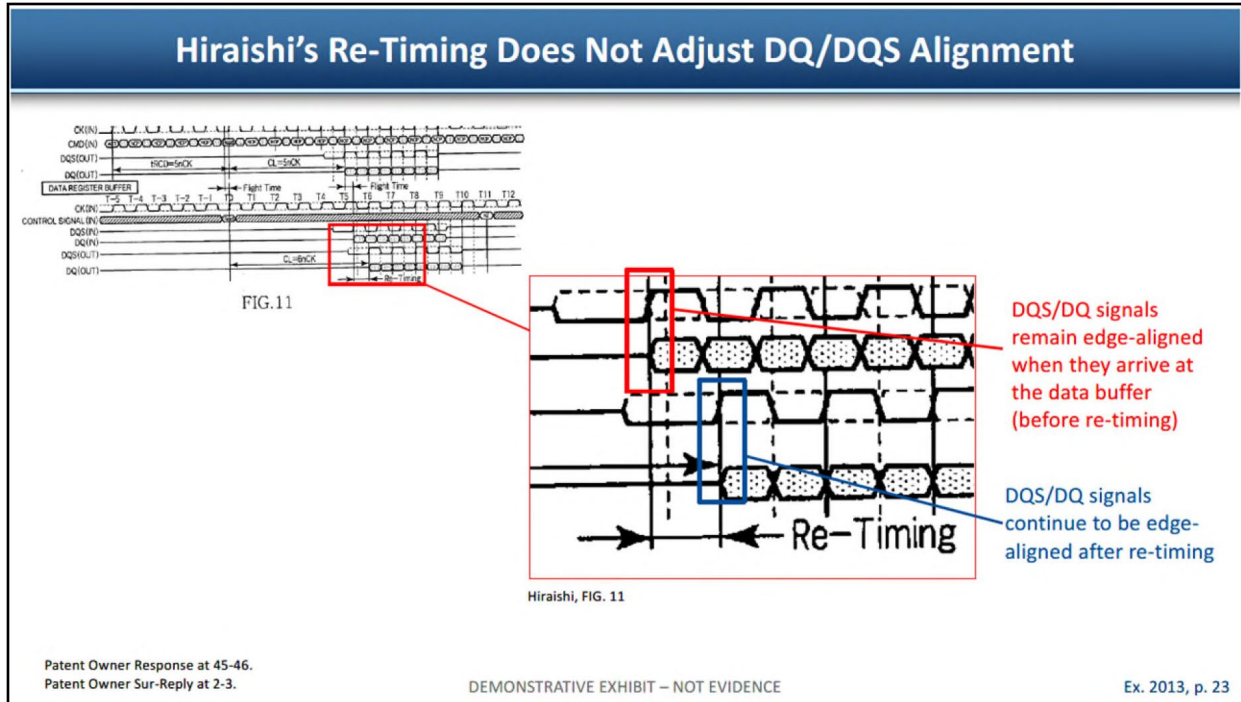
While Netlist treats the knowledge of a person of ordinary skill in the art as “extrinsic evidence” (RB46), it is the starting point for assessing the claim language, *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313-14 (Fed. Cir. 2005) (en banc). And

Netlist itself concedes what a POSITA knew: “[d]ata signals and strobe signals *must be* tightly correlated.” RB6. While Netlist is correct that data and strobe signals “travel on different transmission *lines*,” RB46, those “tightly correlated” signals still *correspond* to each other, which is why the “*data signal line*” *and* the corresponding “*strobe signal line*” *both* correspond to the same “*data path*,” contrary to the Board’s reasoning that only a signal that “is in” the data signal line can “correspond” to that line.

Other than citing to language applying a construction Netlist denies the Board made, and noting that the data/strobe correspondence is temporal, Netlist’s only argument is the nonsensical assertion that a *broader* “data path” construction would “*exclude* embodiments in which [data and strobe] signals travel along *different* paths.” RB47 (emphasis in original). First, this argument again improperly limits the “*data path*” to a single wire (i.e., in orange above, p.4). *See* RB5 (“wire”). Second, claim 1 includes claim 10’s scope, which permits subdividing the “*data path*” of claim 1 into a “*first*” *and* “*second*” “*data path*,” contrary to Netlist’s argument limiting the scope of claim 1 to the path of a *single*, indivisible wire.

Netlist’s argument also ignores that the Board included knowledge of the JEDEC standards as part of ordinary skill, which requires reading the claim with the understanding that data and strobe signals travel together within a tight tolerance. Appx9 (a POSITA “would have been familiar with the JEDEC industry standards”).

Netlist even ignores its own annotations of Hiraishi showing “edge-aligned” data and strobe signals, consistent with a POSITA’s knowledge of JEDEC standards.



BB42; Appx9671-72; Appx10479. Netlist also ignores that Hiraishi’s teachings are the same as the ’608 Patent teachings. Appx106 (step 1880: “Delaying the read strobe signal and the one or more read data signals according to the delay signal”).

The level of ordinary skill here did not involve contested extrinsic evidence, as in the case cited by Netlist. RB46 (citing *Immunex Corp. v. Sanofi-Aventis U.S. LLC*, 977 F.3d 1212, 1221-22 (Fed. Cir. 2020)). The Board’s (and Netlist’s) improper constructions of “corresponding to” cannot be reconciled with the undisputed level of skill. When ordinary artisans’ knowledge is undisputed, the

construction should reflect their understanding. *See Eidos Display, LLC v. AU Optronics Corp.*, 779 F.3d 1360, 1367-68 (Fed. Cir. 2015).

C. Intrinsic Evidence Confirms Samsung’s Construction

The Board failed to read “*a data path corresponding to*” in the full context of claims 1, 2, 10 and the specification. Netlist repeats those errors and mixes two different issues: the meaning of “*data path*” and the meaning of “*corresponding to each data signal line.*” For both terms, the intrinsic evidence supports a reading consistent with the broad terms “*corresponding*” and “*data path.*” Netlist could have drafted a claim to a “data signal line path” or that the “data path is in the data signal line.” But it did not and the intrinsic evidence shows why.

1. Surrounding Limitations of Claim 1

In claim 1, the “*data path corresponding to*” language is part of the “*buffer circuit.*” The claim indicates that the “*buffer circuit*” (and its “*data path*”) is separate from the “*data signal lines*” because it is “*coupled **between***” the “*respective set of data/strobe signal lines*” and the “*respective set of memory devices,*” BB37, as illustrated in Figure 2C, *see* BB47. Netlist concedes this. RB32 (“All agree that a ‘data signal line’ refers to a signal line outside the buffer[.]”). That structure explains why Netlist did not say that the “data path *is in* the data signal line” despite the Board adopting that construction. Furthermore, Netlist concedes that the “*data path*” in the buffer circuit must be large enough to include the entire “*delay circuit,*” RB26,

contrary to the Board’s construction limiting the “*data path*” to being inside a single wire, i.e., “in the data signal line,” Appx17; RB5 (“wire”).

The next portion of claim 1, labeled 1[f], repeats the broad “*corresponding to*” language and then recites that the data path allows “*a signal*”—not just a data signal—to be delayed while traversing it. BB38. This portion of the claim shows why Netlist did not use the claim language “data signal line path,” because the actual claim language allows for different signals, not just data signals, to be delayed through the buffer.

Relatedly, claim 2 uses this “*a signal*” language for antecedent support and confirms this broad adaptability: “*the signal through the data path is a signal associated with the second memory operation.*” BB44-45 & n.4. A POSITA undisputedly would know that *multiple* signals are associated with a memory operation, including “*a strobe signal*” as expressly claimed by limitation 10[a]. BB7, 41, 44-45 & n.4. If “*a signal*” in claim 1 were restricted to a data signal (DQ), as required by the Board’s construction, that would conflict with limitations 2[e] and 10[a].

Contrary to Netlist’s arguments, applying the ordinary meaning of “*corresponding to*” properly applies the limitation and does not “effectively read[] out” claim language. RB37. The “*data path*” inside the buffer has a functional relationship with “*each data signal line in the respective set of data/strobe signal*

lines” outside the buffer, *see* BB38-40, which gives meaning to all of the claim language.

2. “Data Path” in Claim 10

Claim 10’s use of “*data path*” cannot be reconciled with the narrow constructions by Netlist and the Board. BB43-46. Unsurprisingly, Netlist agrees with the Board that “*first data path*” and “*second data path*” **must** be additional data paths different from “*a data path*” in claim 1. RB41-42. First, whether these are additional “data paths” is irrelevant to whether the “*data path*” term, by itself, is limited to data signals. It cannot be, because the “*data path*” can also transmit “*a signal*” that is a “***strobe signal associated with the second memory operation***” as shown by limitations 1[f], 2[e], and 10[a].

In trying to support the “additional data paths” theory of claim 10, Netlist ignores the Board’s citation of *Phillips*, 415 F.3d at 1315 and *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). Appx18-19. Despite Samsung describing why neither case supports the Board’s reasoning, BB43-44, Netlist ignores both.

Netlist also fails to rebut Samsung’s discussion of “first” and “second” in *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). *See* BB46. Nor does Netlist identify any case supporting its “additional data paths” reading. The Court should reject the Board’s assertion that claim 10 must

recite additional data paths unrelated to claim 1's data path, rather than giving additional detail about the initially recited limitation as dependent claims usually do. Claim 1's "a data path" is presumptively read as "one or more data paths," matching claim 10.

Finally, Netlist inaccurately describes Samsung's position as "the 'first' and 'second' data paths in claim 10 do not refer to *additional* paths but rather to a *subset* of the data path of claim 1." RB42 (emphasis in original). Not true. Samsung showed that claim 10 encompassed that *possibility*, but claim 10 is not limited to only that configuration. *See* BB45-46.

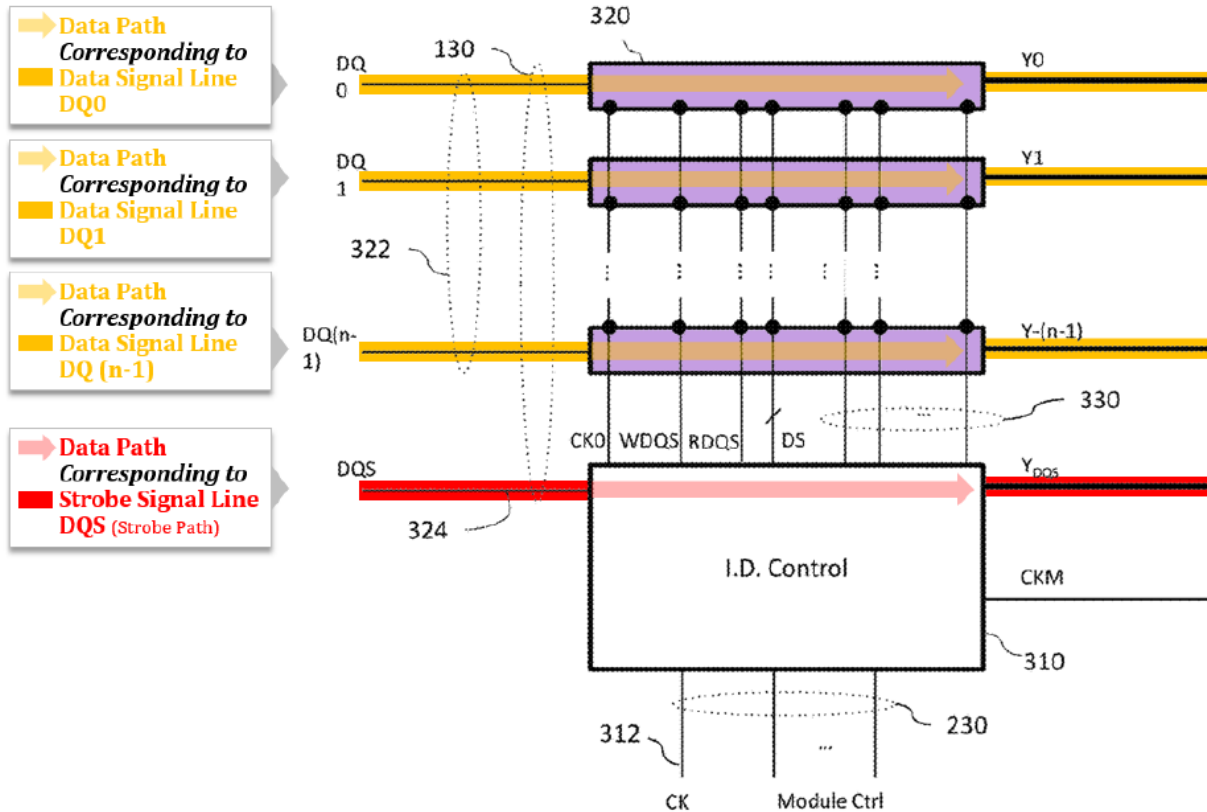
3. Written Description

The Board and Netlist try to limit claim 1 to specific embodiments inconsistent with its language. Read in light of the broad claim language, the written description does not justify those limitations. BB46-51.

Figures 1 and 2C show the data/strobe signal lines 130 outside the buffer circuit, consistent with claim 1's statement that the buffer circuit is coupled between those lines and the memory devices. BB47. Accordingly, the Board's construction of "*corresponding to*" as "is in" conflicts with the written description. Netlist's only response is refusing to acknowledge the Board's construction. RB45.

Figure 3 illustrates the buffer circuit (118) as including circuits and signal lines that receive and output various signals, including data signals (DQ) and a strobe

signal (DQS), traveling horizontally to the right through the buffer. Appx87, Appx112 (10:31-61). Netlist annotates that figure to impose its own construction:



RB34. However, Netlist labels as “data paths” what the ’608 Patent actually calls “signal lines,” thus repeating the Board’s error of equating a signal line with a data path. RB34 (highlighting red and yellow “data paths” over lines that the figure labels collectively as “signal lines 130”); Appx87, Appx110 (6:19-20), Appx112 (10:32). Nor does the text of the specification justify Netlist’s relabeling; “data path” is never mentioned in the context of Figure 3. BB49.

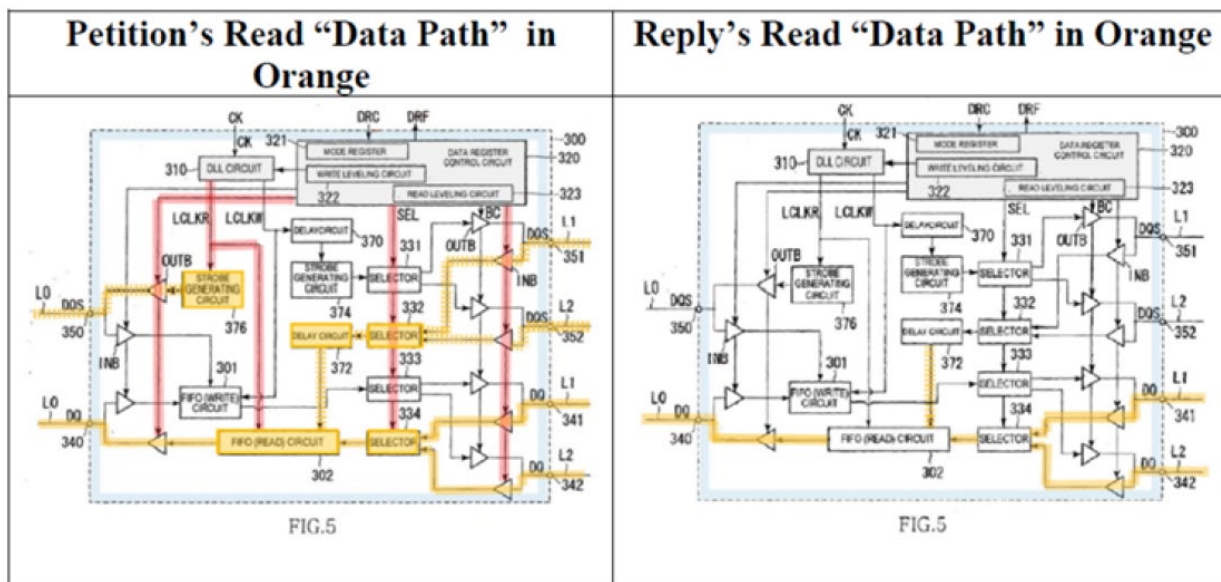
Like the Board, Netlist relies on the Figure 15 and 16 embodiments to limit “data path.” RB35-36. But the broad phrase “data path” (used in claim 1) is not

used in the description of these figures; instead, different, narrower phrases are used, like “read strobe path” and “write data path,” Appx115-16 (16:53-17:60); Appx9593-94, which are not used in the claims. Furthermore, both figures are identified as showing circuitry “in a data buffer.” Appx109 (3:11-15). This use of “*data* buffer” to describe a circuit through which *strobe* signals travel is inconsistent with the Board and Netlist claiming that the word “data” in the phrase “data path” excludes strobe and other non-data signals. RB33. Samsung’s ordinary-meaning construction of data path as including circuitry handling signals functionally related to “*each data signal line*” is consistent. Disclosing a specific embodiment does not limit the claims. BB51. Netlist fails to show any exception to that rule.

D. The Board’s Improper Analysis Requires Vacatur and Remand to Apply the Correct Construction to All Grounds

Rather than meaningfully defend the Board’s construction, Netlist’s brief leads with the argument that Grounds 1 and 2 in the petition did not “disclose the required delay circuit [even] under Samsung’s construction.” RB26. But the Board never made that finding, since the Board relied entirely on its erroneous claim construction, BB52-53 (citing Appx31-43, Appx68-70), and thus it cannot be a basis to affirm the Board’s decision. *See Calcutt v. FDIC*, 598 U.S. 623, 624 (2023) (per curiam) (noting that agency actions may be upheld “only on the same basis articulated in the order by the agency itself”). When the agency has erred, as here, “the proper course, except in rare circumstances, is to remand.” *Id.* at 628-29.

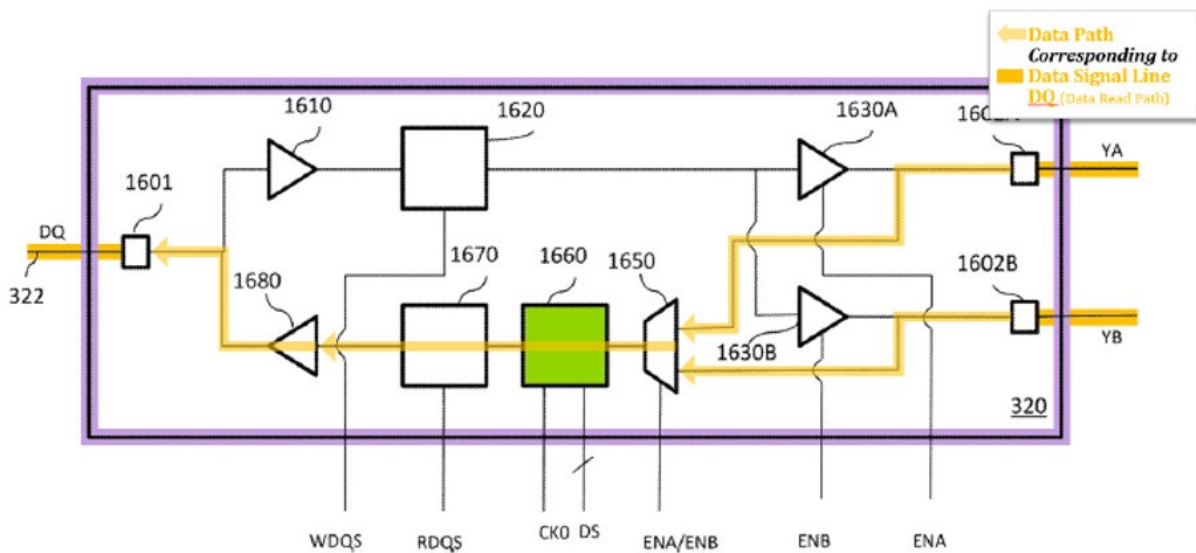
Furthermore, Netlist’s argument misstates Samsung’s position and ignores key portions of the petition. RB16, 25-31. Netlist argues there was a “dramatic shift . . . between petition and reply”:



RB16. To the contrary, both annotated figures above are directly from the petition. Appx190-91 (claim 1), Appx207-10 (dependent claim 10).

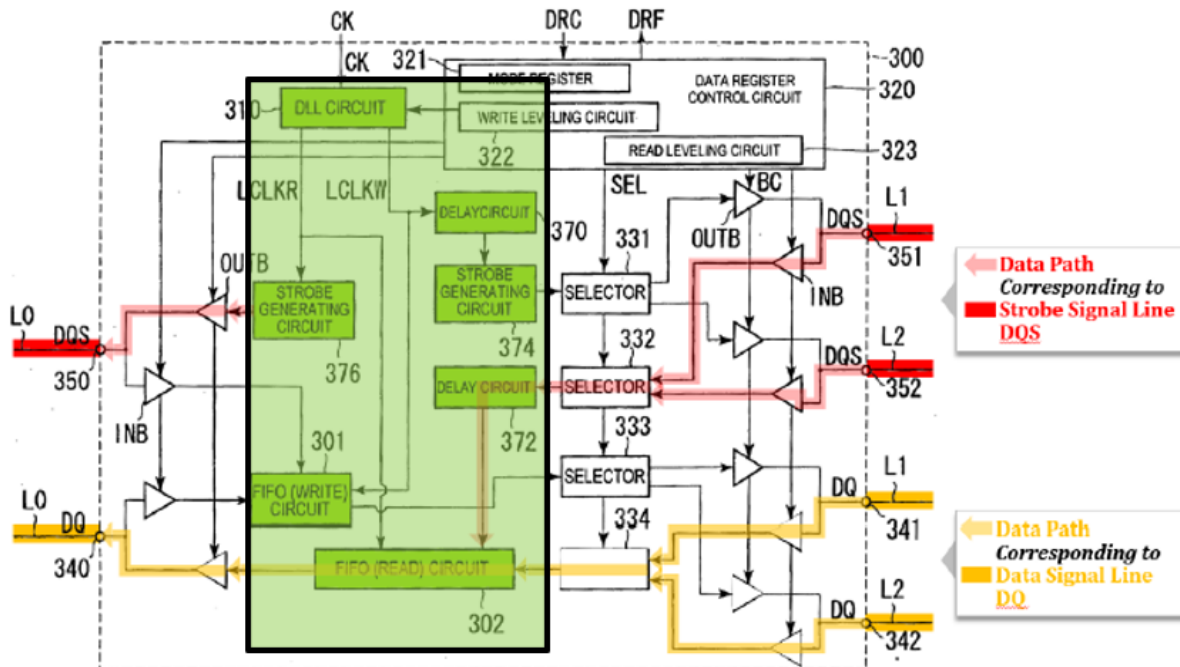
As explained in the petition, claim 1 means what it says: the “*data path*,” and thus the “*delay circuit*,” merely has to “*correspond[]*” to the data signal lines—not be inside them. See, e.g., Appx173-76, Appx187-93; BB33, 36-37. Netlist’s criticism of the petition again depends on construing the “*data path*” as just a single line, RB26-31, rather than something inside the buffer that broadly “*corresponds*” to the data signal lines outside the buffer. Netlist’s construction is so narrow that nothing would ever qualify as the claimed “*delay circuit*,” not even the preferred embodiment, BB71, because there would always be some part of the delay circuit

outside the specific lines traversed by the data and strobe signals. Netlist’s own annotation of the ’608 Patent (below) shows this, because most of the “delay circuit” (green) is either above or below the yellow line that Netlist calls the “data path”—contrary to Netlist’s insistence that “[i]f *any portion* of the delay circuit is not in the data path, the claim is not satisfied.” RB26.



RB73. Of course, the “delay circuit” (green above) “corresponds to” (and touches) the yellow line (delaying signals on that line), but that is also true of the delay

circuitry in Hiraishi, which includes internal detail, even under Netlist's construction:



RB29, 73 (with large green box added).

Netlist's criticism of Samsung's mapping of the "*delay circuit*" also fails because it ignores key portions of Samsung's petition. Samsung's petition followed claim 1 (and the dependent claims) when mapping Hiraishi and Butt to the claim language. Claim 1 starts by identifying the "*data path*" broadly in 1[e] with only the "*corresponding*" language. Appx117 (19:44-45). Moving to 1[f], the claim identifies specific additional components of the "*data path*," including the tri-state buffer and the delay circuit. Appx117 (19:49-53).

The petition followed that structure by first identifying the necessary components of the initial data path (Appx173-76), and then identifying how additional circuitry is included in the data path in the form of the tri-state buffer (Appx182-83) and the delay circuit (Appx183-93). The petition was consistent with Samsung's expert about identifying the components of the "*delay circuit*" for write operations that are included in the data path:

Write FIFO 301 delaying the write data signal, delay circuit 370 delaying the LCLKW signal, the strobe generating circuit 374 generating a delayed strobe signal that is in synch with the delayed write data, and DLL circuit 310 generating the LCLKW signal for timing the output of the delayed data and strobe signals.

Appx187. *Compare id., with* Appx7019-20 (18:18-19:7), Appx7135-38 (134:25-137:22). The petition was also consistent with respect to read operations. *Compare* Appx191, *with* Appx7018 (17:13-17), Appx7135-38 (134:25-137:22).

Netlist incorrectly asserts that "the Board found" certain facts that would not satisfy Samsung's mapping for the "*delay circuit.*" RB28-29 (citing Appx39, Appx40, Appx42). For example, Netlist focuses on "clock signals" like LCLKW (red below), RB28, which Samsung's expert explained "control the data path," Appx7042 (41:7-19):

Appx190. Netlist points to various components of the “*delay circuit*” that the Board found were not in the “*data path*,” RB27-30, but that was under the Board’s erroneous claim construction requiring the “*data path*” (and thus the “*delay circuit*”) to be “in” a single wire (i.e., in the “data signal line”), not under Samsung’s construction, *see* BB53; Appx37 (“[S]everal of [the] elements of Hiraishi alleged to be part of ‘a delay circuit’ are not in a ‘data path’ *as claimed* and do not ‘delay a signal through the data path.’”); Appx40-42. The Board made clear that it was construing “*data path*” to apply in its decision. Appx17 (“The operative issue is the identification of the ‘data path’ that is claimed in claim 1.”). When the Board makes alternative findings using a construction that it rejects, rather than applying the construction it adopted, it identifies what it is doing. *See Celgene Corp. v. Peter*, 931 F.3d 1342, 1351 n.9 (Fed. Cir. 2019) (analyzing obviousness “[e]ven under Celgene’s claim construction” when “the Board held, in the alternative”). Tellingly, Netlist points to no statement that the Board made findings under an alternative construction. There is none.

II. The Board’s Determinations of Prior-Art Teachings Are Collaterally Estopped and Unsupported by Record Evidence

The Board erred in refusing to consider collateral estoppel for subsidiary *factual* findings merely because the obviousness grounds or claim language differed.

As a result, remand is required given the inconsistent factual findings between this IPR and the previous '035 Final Written Decision. BB53-74.³

A. The Board's Collateral-Estoppel Errors Are Independent of the Related Patent's Claim Language

Netlist does not dispute that collateral estoppel applies to underlying *factual* determinations. *Compare* BB53-60, *with* RB56-58. Instead Netlist doubles down on the Board's erroneous collateral-estoppel analysis by focusing on purported "differences between the claims" of the two patents, RB56-57; *see also* Appx20-23 (addressing collateral estoppel only in the context of the differences between the *claims* of the '035 and '608 Patents), despite those claims being found not patentably distinct during prosecution, BB17.

However, Samsung explained that specific factual findings from the '035 Decision resulted in collateral estoppel "*independent* of the claim construction dispute." BB55-56, 62-74. Netlist's arguments about purported differences in claim language are irrelevant to the *factual* issues addressed in both proceedings, discussed in more detail below. *See* RB57-58. Netlist asserts that the "unpatentability" theories in the two IPRs involved different facts, RB58, but that is incorrect: First, the '035 Decision *rejected* the "INB" argument, which was raised by Netlist, not the

³ Netlist complains that certain arguments were "proffered for the first time" in Samsung's Reply. RB55-56. But that is because Netlist dramatically changed its construction for "*data path*" after institution, BB19-21, thus warranting consideration of Samsung's arguments in Reply, as the Board found, Appx45-46.

petitioner, so “INB” cannot justify the inconsistent factual findings in the two IPRs. See BB72-73 (citing Appx6716-22, Appx6724 (“[w]e agree with . . . Petitioner[.]”), Appx6736-37 (“we disagree with [Netlist]”)). Second, Netlist is incorrect that the ’035 Decision “did not involve moving Tokuhiko’s delay element [DR1] into [Hiraishi/Osanai’s] data buffer.” RB58. It did, just like Ground 2 here. BB75-76 (citing Appx6741, Appx10306); Appx6728 (“Tokuhiko’s technique in Osanai/[Hiraishi]’s buffer leveling circuits”).

Netlist seeks to make new law by asserting that “materially different claims, *by definition*, give rise to materially different legal and factual issues of invalidity.” RB61. That assumption is contrary to the Restatement and to cases considering collateral estoppel separately for legal and factual issues. BB58-59 (citing *Papst Licensing GMBH & Co. KG v. Samsung Elecs. Am., Inc.*, 924 F.3d 1243, 1252-53 (Fed. Cir. 2019)). Here, the Board erred by holding that “no estoppel applies” *only* because of differences in claims and differences in legal invalidity issues between the proceedings. Appx20-23. The Board prematurely ended its inquiry and never addressed whether the proceedings had identical *factual* issues, as discussed below. Neither Netlist nor this Court may “supply a reasoned basis for the agency’s action that the agency itself has not given.” *Pfizer Inc. v. Sanofi Pasteur Inc.*, 94 F.4th 1341, 1350 (Fed. Cir. 2024).

Remand, therefore, is required for the Board to consider, in the first instance, whether collateral estoppel applies to these factual issues.

B. The Board Ignored Samsung’s Identification of Specific Factual Issues Resolved by the Previous IPRs of Related Patents

1. The Board Failed to Address Samsung’s Estoppel Arguments Based on Factual Issues

Contrary to Netlist’s arguments, the Board ignored Samsung’s identification of specific factual issues determined by the ’035 Decision. RB58-61. According to Netlist, Samsung identified to the Board only two factual issues for purposes of collateral estoppel, which Netlist labels “(ii)” and “(iii)”: (ii) “the finding that Osanai/Hiraishi teaches controlling timing of data and strobe signals on the data paths” and (iii) “the finding that the DRC signal in Osanai/Hiraishi causes the data buffer to perform read and write leveling.” RB59. As a preliminary matter, Netlist’s framing ignores the other collateral-estoppel arguments that Samsung raised based on the ’035 Decision, including facts with respect to Ground 2. *See* Appx10501-07 (“EX1066”).

More importantly, Netlist cherry-picks the Board’s discussion out of context to suggest that the Board addressed Samsung’s fact-specific estoppel issues. RB58-61. Not so. On issue “(ii),” Netlist points to the Board’s discussion of “input buffers” (“INB”), *see* RB59-60, but as explained above (p.22), the petitioner in the ’035 Decision did not rely on the “INB” to teach any limitation (including

“controlling the timing of the data and strobe signals on the data paths”), so the “INB” cannot justify the inconsistent factual findings in the two IPRs, *see* BB72-73; *see also infra* II.C.3 (pp.33-34).

On issue “(iii),” Netlist argues that the Board “squarely addressed and correctly rejected” that the ’035 Decision found that the DRC signal in Osanai/Hiraishi causes the data buffer to perform read and write leveling. RB60. But Netlist again refers to “INB” (issue “(ii)” directly above), *see* RB60 (citing Appx50-51), which as discussed directly above is incorrect, because neither the petitioner nor the Board in the ’035 Decision relied on the INB for delaying the data and strobe signals. Netlist also refers to selector 334 and the output buffer (“OUTB”), *see* RB60, but the ’035 Decision relied on those to “select[] (or ‘enable[]’) certain paths,” Appx6727, not for “limitation 1[j]” to “control timing of the respective data and strobe signals on the data paths,” Appx6727-37. Netlist does not identify where the Board in this IPR actually addressed Samsung’s argument that the ’035 Decision already found that the DRC signal, which includes a “Mode Register Set” (“MRS”) command, causes Osanai/Hiraishi’s data buffer to perform read and write leveling; nor could it. *See* Appx10485-86 & n.3; *see also* RB59 (acknowledging that Samsung raised this estoppel argument to the Board at Appx10485-86).

2. Samsung Did Not Forfeit Its Estoppel Arguments

Netlist asserts that Samsung forfeited “most” of its estoppel theories by failing to raise them to the Board. RB61-62. That is incorrect. *See* BB53 (providing citations), 62-74.

First, Samsung raised with the Board that the ’035 Decision required finding that the MRS command is used for read and write leveling. Specifically, Samsung argued that the ’035 Decision “already rejected [Netlist’s] argument” and “correctly conclud[ed] that the ‘DRC’ signal identified in the Petition,” which conveys “‘mode register set’ [MRS] commands,” is what “causes Hiraishi’s data buffer to perform read and write leveling.” Appx10485-86 & n.3. Even Netlist acknowledges that Samsung properly raised “the finding that the DRC signal in Osanai/Hiraishi causes the data buffer to perform read and write leveling.” RB59 (citing Appx10485-86).

Second, Samsung pointed out where the ’035 Decision “specifically found that ‘the read and *write leveling* circuits of [Hiraishi] make timing adjustments’ . . . ‘so that [data and strobe] signals between the memory chips and the data register buffers are sent at the appropriate time,’ and ‘these disclosures of [Hiraishi] are sufficient to teach *controlling the timing of data and strobe signals on the data paths* on which those signals travel.’” Appx10470-71 (first emphasis added) (alterations in original) (quoting Appx6736, Appx6737).

Third, Samsung argued that the '035 Decision required the Board to find that Hiraishi's FIFO is a delay circuit for read and write leveling. Samsung argued that "the Board has already ruled against Netlist on this issue [when it] concluded that [Osanai/]Hiraishi teaches '*controlling the timing of data and strobe signals on the data paths*' [L0 to L1/L2, which goes through the *FIFO*] as part of *read and write leveling*." Appx10482-84 (last emphasis added) (citing Appx6736, Appx6737); *see also* Appx10481 ("Even under Netlist's narrower construction, Ground 1 renders obvious a '*delay circuit*' (e.g., the *FIFOs* in Hiraishi and Butt), in the '*data path,*' that delays DQ data signals through that '*data path[.]*'"). Even Netlist acknowledges that Samsung properly raised these arguments about whether Osanai/Hiraishi teach "controlling timing of data and strobe signals on the data paths." RB59 (citing Appx10481-82).

Samsung therefore did not forfeit its estoppel arguments.

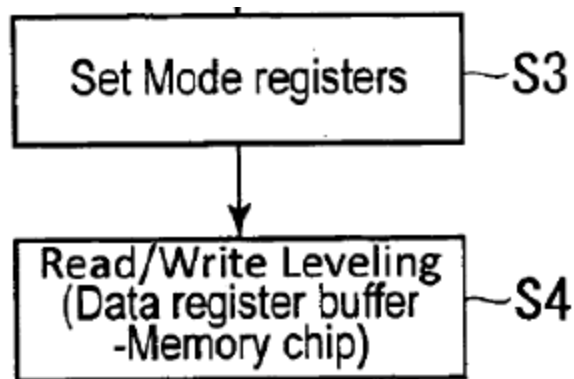
C. The Board's Determinations That Hiraishi's Components Do Not Delay Signals in Response to Standard Commands During Leveling Contradicts its Prior Rulings and the Record

As explained in Samsung's opening brief, the Board made several findings about Hiraishi that conflict with the '035 Decision and lack substantial-evidence support. BB60-74. Because the Board reached these inconsistent findings without any reasoned explanation, remand is warranted. *See Vicor Corp. v. SynQor, Inc.*, 869 F.3d 1309, 1323 (Fed. Cir. 2017).

Netlist argues the Board “credited Netlist’s expert’s testimony,” RB63, but that does not excuse the direct conflict with the ’035 Decision, which the Board ignored. *See Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017) (“We must disregard the testimony of an expert that is plainly inconsistent with the record, or based on an incorrect understanding of the claims.” (cleaned up)). The direct conflict also cannot be justified on the basis that “Samsung submitted *no expert testimony*” in Reply, RB63, which is incorrect: Samsung submitted hundreds of pages of deposition testimony from both experts, which extensively supported its Reply. *See* Appx10470-515 (citing EX1074, EX2012). Netlist is also incorrect that Samsung’s expert declaration cited in the “*petition* is actually *inconsistent* with the reply theory” about the FIFO delaying data signals. RB63. In fact, it is entirely consistent. BB70-71; Appx10227-28.

1. Hiraishi’s Read and Write Leveling Are Performed *in Response to an MRS Command*

Netlist tries to move the goalposts by arguing “[t]he Board correctly found that Hiraishi’s mode register setting (MRS) operation is performed in Step S3 of Figure 13, which is a *separate step* from Step S4 read/write leveling”:



RB63-64 (excerpted); *see also* RB65-66 (similar). But Netlist does not dispute that the MRS command performed in step S3 *causes* the read/write leveling in step S4, thus satisfying the claim language requiring “a delay circuit configured to delay a signal . . . *in response to* at least one of the module control signals,” i.e., the MRS command. Appx117 (19:52-55); BB62-64. The Board therefore erred when it found “an MRS command, as disclosed in the JEDEC standard, is a command signal that one of skill in the art would [not] use in Hiraishi” for read/write leveling. Appx65-67.

That finding directly contradicts the '035 Decision, which Netlist concedes found that Osanai/Hiraishi “perform[s] ‘write leveling’ ‘*in response to* a memory command such as the [MRS] command.”” RB66 (quoting Appx6731-32). Netlist quibbles that the '035 Decision did not “squarely find[] that [Osanai/Hiraishi] performs S4 read/write leveling in response to an MRS command,” RB66, but that distinction makes no sense given that Osanai and Hiraishi share the same Figure 13 that discloses “read/write leveling” at step S4. *See* Appx6227; Appx845.

Netlist's argument that this finding was not "essential" to the '035 Decision (RB66) misstates the law. See BB59 (citing *Mother's Restaurant, Inc. v. Mama's Pizza, Inc.*, 723 F.2d 1566, 1571 (Fed. Cir. 1983)). This finding related to "a central dispute" between the parties, Appx6732-33, and thus was not so "incidental" or "nonessential" that estoppel should not apply, *Mother's Restaurant*, 723 F.2d at 1571.

As a fallback, Netlist asserts that any error was "harmless" because the Board found Hiraishi does not disclose a "*delay circuit*," RB63-64, but the Board's analysis for the "*delay circuit*" applied the wrong claim construction as explained in Section I above (pp.1-14), and also contradicted other parts of the '035 Decision as explained in Section II.C.3 below (pp.33-34). Furthermore, the '035 Decision "regarding MRS commands [was] *relevant*," RB64, because it showed that Hiraishi disclosed claim 1[f] of the '608 Patent exactly as Samsung's petition had asserted based on "mode register set" [MRS] commands, see Appx10485-86 & n.3; Appx184-85; Appx193; Appx10231-33.

Netlist quibbles that Samsung's expert, Dr. Wedig, relied on a command "*similar to the . . . mode register set [MRS]*" to trigger S4 read/write leveling, RB65, but he specifically pointed to the MRS command in the JEDEC standard as an example, Appx714 ("EX1020") (citing Appx3152), consistent with the '035 Decision, Appx6731-32. Netlist brazenly asserts that the "JEDEC standard" "says

nothing” about performing read/write leveling in response to an MRS command, RB65, but that is clearly wrong (and also contrary to the ’035 Decision and Figure 13 of Hiraishi/Osanai above), *see* BB63 (citing Appx10233 (citing and annotating Appx3142 (“MRS”), Appx3128, Appx3135 (“Write leveling”), Appx3140 (“read synchronization”), Appx3151-52, Appx3157, Appx3159-60 (“read timing calibration”))).

Finally, Netlist fails to address the evidence from its own expert that the JEDEC standard requires read and write leveling to be performed in response to the MRS command. *See* BB63 (citing Appx8947-48 (105:12-106:6), Appx8961-70 (119:20-128:22)). The Board ignored this same testimony, uncontested by both parties, which itself warrants remand. *See* Appx65-67; *see also* Appx10486 n.3; *CQV Co. v. Merck Pat. GmbH*, 130 F.4th 1344, 1349-50 (Fed. Cir. 2025) (remanding the Board’s factual finding where the Board “discarded without explanation” “highly material and unrebutted evidence”).

2. Hiraishi’s Write Leveling Accounts for Different Flight-Time Delays Between Data Lines L1 and L2

The Board’s finding that Hiraishi’s write leveling is “not done to determine delays in [DQ] data signal lines to account for different flight time delays for L1/L2” is inconsistent with the ’035 Decision and lacks substantial-evidence support. Appx56; BB64-69.

Netlist asserts there is no inconsistency by citing a portion of the '035 Decision out of context discussing how Hiraishi's S4 write leveling relates to the **DQS strobe** signals. *See* RB71-72 (citing Appx6714). But that ignores that the '035 Decision **also** found that the "read and write leveling circuits of Osanai/[Hiraishi] make timing adjustments [to] **data** and strobe signals." BB65 (quoting Appx6736, and citing Appx6727). Netlist asserts that these "timing adjustments" do not necessarily "delay" a signal as required by claim 1[f] of the '608 Patent, RB72, but that is contrary to the '035 Decision, Appx6727 ("delay"), and makes no sense because data cannot be sent by the buffer before it is received, so the only "timing adjustments" are **delays**, as expressly shown by the "Re-timing" in Figure 12 of Hiraishi that delays **both** DQ data signals and DQS strobe signals by approximately 0.7 clock cycles, BB66 (annotating Appx844); Appx10270-71, Appx10267 (quoting Appx9065-66 (223:20-224:4)).

Netlist argues this finding was not "essential" to the '035 Decision, RB72, when in fact this finding specifically rejected (with several pages of analysis) Netlist's argument that Osanai/Hiraishi does not "Control Timing of **Data** and Strobe Signals on Data Paths" as required by limitation 1[j] of the '035 Patent, Appx6735-37, Appx6707 (1[j]), and thus this finding was not so "incidental" or "nonessential" that estoppel should not apply, *Mother's Restaurant*, 723 F.2d at 1571.

Netlist also fails to show that substantial evidence supports the Board's inconsistent findings here. RB67-71. The "undisputed" fact that write leveling adjusts the DQS strobe signal, RB67-68, does not preclude Hiraishi's write leveling from adjusting the DQ data signals as well. In fact, the opposite is true. Because the DQ data signals *must* remain "tightly correlated" with the DQS strobe signal, as Netlist concedes, RB6, write leveling that delays the DQS strobe signal also delays the DQ data signal, as expressly shown by Figure 12 of Hiraishi, *see* BB65-67; Appx10213-19, Appx10271, and as found by the '035 Decision discussed above.

Netlist argues that its expert, Dr. Mangione-Smith, provided substantial evidence for the Board's decision, but expert testimony that is contradicted by the prior art's express disclosure (as well as a prior Board decision) is not substantial evidence, as shown by the cases cited by Samsung that Netlist completely ignores. *Compare* BB65-68, *with* RB67-71. Netlist also raises the strawman argument that write leveling in Figures 14A-14B is a "separate step" than the "re-timing" shown in Figure 12 of Hiraishi. RB69. But the two steps are linked by LCLKW (ignored by Netlist), which is why the amount of "re-timing" for a write operation in Figure 12 is determined by the write leveling step, *see* BB65-67; Appx10213-14, Appx10275-77, as confirmed by the findings of the '035 Decision discussed above that Osanai/Hiraishi's write leveling results in delays to *both* "data *and* strobe signals *associated with* read and *write operations*," Appx6736.

3. Hiraishi's FIFO Is a Delay Circuit

The Board's findings about Hiraishi's FIFO are inconsistent with the '035 Decision and lack substantial-evidence support. BB69-74.

Netlist argues that the '035 Decision creates no inconsistencies because it purportedly relied on input buffers ("INB") to delay the data signals. RB75 (citing Appx6737). But the petitioner in the '035 Decision *never* relied on INBs. *See* BB72-73 (citing Appx6716-22 (petitioner's contentions, not relying on INBs); Appx6724 ("We agree with and adopt Petitioner's contentions")). And the '035 Decision *rejected* Netlist's arguments about the INBs. *See* BB73 (citing Appx6736-37 ("we disagree with [Netlist's] argument")). As found by the '035 Decision, the INBs simply "act as a gate allowing data and strobe signals to either pass through or not pass through," Appx6737, which is why the INBs must be "activat[ed]" at the correct time, Appx870-71 ¶ 151. But the INBs do not perform the "re-timing" (i.e., delay) of the data signals, which Hiraishi expressly teaches is performed "using the FIFO." Appx869 ¶¶ 130, 135; BB70, 73-74; Appx10277.

Netlist fails to identify substantial evidence supporting the Board's inconsistent finding here that Hiraishi's FIFO does not delay the data signals. RB72-74. Instead Netlist relies on annotated figures never before the Board. *See* RB72-73; *see also* RB28 n.1 ("re-annotat[ing]" the figures). But new evidence provided for the first time on appeal cannot constitute substantial evidence. *See In re*

Gartside, 203 F.3d 1305, 1315 (Fed. Cir. 2000) (“[O]ur review of the Board’s decision is confined to the factual record compiled by the Board[.]”). Moreover, Netlist’s reliance on new figures to argue that “when Hiraishi intended a circuit to be a delay circuit, it said so,” RB74, merely reinforces that Netlist’s argument depends on an incorrect claim construction (discussed above, pp.15-17) rather than what Hiraishi discloses.

Netlist also fails to reconcile the Board’s narrow construction with the preferred embodiment of the ’608 Patent, which relies on structures and a “DS” delay signal that are *not* physically on top of the DQ data line. BB71 (citing Appx8995-96 (153:2-154:5)); *supra* pp.15-17. Netlist’s only response is that the “claims require the ‘delay circuit,’ not a delay signal . . . to be in the data path,” RB74, but that is flatly inconsistent with the Board’s construction, Appx39 (“[T]he LCLKW signal to delay circuit 370 is [not] through the ‘data path’ as claim 1 requires.”).

III. The Board Failed to Address the Use of Tokuhiro’s DR Elements as Delay Circuitry as Samsung Presented in its Petition, Reply, and During the Hearing

The Board erred by ignoring Samsung’s alternative combination under Ground 2 that a “*delay circuit*” in the “*data path*” is disclosed, even under Netlist’s narrow construction. BB74-76. The Board’s finding that Ground 2 only relies on “add[ing]” Tokuhiro’s DR-1 element to Hiraishi is a misreading of Ground 2 and

lacks substantial evidence. Appx68; *SunSpec Alliance v. Tigo Energy, Inc.*, No. 23-1741, 2025 WL 2214160 (Fed. Cir. Aug. 5, 2025) (nonprecedential) (remanding for the Board to consider petitioner’s argument “in the first instance” where the argument was raised in the petition).

Although Netlist argues “underdeveloped” arguments may be forfeited, RB52, a party preserves an issue for appeal if the Board was “fairly put on notice as to the substance of the issue,” *Medtronic, Inc. v. Teleflex Innovations S.À.R.L.*, 68 F.4th 1298, 1304-05 (Fed. Cir. 2023). Samsung did that repeatedly, in the Petition, in the Reply, during the hearing, and by pointing to the nearly identical argument that was successful in the ’035 Decision. BB75-76.

In any event, the Board did not find forfeiture, and none of Netlist’s cases found forfeiture based on that theory. *See Fresenius USA, Inc. v. Baxter Int’l, Inc.*, 582 F.3d 1288, 1296 (Fed. Cir. 2009) (declining to consider “new anticipation argument”); *Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1074 (Fed. Cir. 2017) (finding forfeiture where appellant raised “substantial new arguments”); *Broadcom*, 542 F.3d at 901 (finding waiver where appellant failed to make specific appeal argument below).

Rather than address the Board’s failure, Netlist misrepresents Samsung’s combination, claiming that Tokuhiro’s delay elements must be “in addition” to Hiraishi’s FIFO circuit. RB53. To the contrary, Samsung expressly argued

Tokuhiro's delay elements could be used "instead of" Hiraishi's FIFO circuit (directly on the DQ data line). Appx230; Appx10502; Appx10303; BB75. While the Board has discretion in interpreting petitions, it cannot ignore arguments raised. *See CQV*, 130 F.4th at 1349-50. Moreover, this Court should reject Netlist's supplement to the Board's decision injecting reasoning the Board never gave. *See Pfizer*, 94 F.4th at 1350 ("[W]e may not supply a reasoned basis for the agency's action that the agency itself has not given.").

The Court should remand Ground 2 to the Board to address Samsung's alternative combination.

CONCLUSION

The Board's decision should be vacated and remanded.

Dated: September 15, 2025

Respectfully submitted,

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**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2025-1378

Short Case Caption: Samsung Electronics Co., Ltd. v. Netlist, Inc.

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Name: Michael Hawes