

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-00711

U.S. Patent No. 10,860,506

ZOOM DEPOSITION OF DR. WILLIAM HENRY MANGIONE-SMITH

(Reported Remotely via video & Web videoconference)

Kirkland, Washington (Deponent's location)

Thursday, May 4, 2023

Volume 1

STENOGRAPHICALLY REPORTED BY:
REBECCA L. ROMANO, RPR, CSR, CCR
California CSR No. 12546
Nevada CCR No. 827
Oregon CSR No. 20-0466
Washington CCR No. 3491

JOB NO. J9467698

PAGES 1 - 279



800.211.DEPO (3376)
EsquireSolutions.com

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-00711

U.S. Patent No. 10,860,506

ZOOM DEPOSITION OF DR. WILLIAM HENRY
MANGIONE-SMITH, taken on behalf of the Petitioner,
with the deponent located in Kirkland, Washington,
commencing at 9:01 a.m., Thursday, May 4, 2023,
remotely reported via video & Web videoconference
before REBECCA L. ROMANO, a Registered Professional
Reporter, Certified Shorthand Reporter, Certified
Court Reporter.



800.211.DEPO (3376)
EsquireSolutions.com

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

APPEARANCES OF COUNSEL

(All parties appearing via Web videoconference)

For the Petitioner - Samsung Electronics Co., Ltd.:
BAKER BOTTS L.L.P.
BY: THEODORE W. CHANDLER
Attorney at Law
1801 Century Park East
Suite 2400
Los Angeles, California
(213) 202-5702
ted.chandler@bakerbotts.com

and

BY: FERENC PAZMANDI
Attorney at Law
101 California Street
Suite 3200
San Francisco, California 94111
(415) 291-6255
ferenc.pazmandi@bakerbotts.com

/////



800.211.DEPO (3376)
EsquireSolutions.com

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

APPEARANCES OF COUNSEL(cont'd)
(All parties appearing via Web videoconference)

For the Patent Owner:
IRELL & MANELLA LLP
BY: JONATHAN M. LINDSAY
Attorney at Law
840 Newport Center Drive
Suite 400
Newport Beach, California 92660
(949) 760-0991
jlindsay@irell.com

ALSO PRESENT:
John Reidt, Videographer

/////



800.211.DEPO (3376)
EsquireSolutions.com

I N D E X		
DEPONENT		EXAMINATION
DR. WILLIAM HENRY MANGIONE-SMITH VOLUME 1		PAGE
	BY MR. CHANDLER	10
	BY MR. LINDSAY	260
	BY MR. CHANDLER	270
E X H I B I T S		
NUMBER		PAGE
	(PREMARKED)	
Exhibit 1001	US 10,860,506 B2;	
Exhibit 1003	Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506;	
Exhibit 1005	US Patent Application 2010/0312956 A1;	
Exhibit 1006	US 8,020,022 B2;	
Exhibit 1007	US Patent Application 2006/0277355 A1;	
Exhibit 1008	US 6,184,701 B1;	
Exhibit 1018	Jedec Standard No. 21-C DDR SDRAM Registered Design Specification;	
Exhibit 1020	JEDEC STANDARD DDR3 SDRAM JESD79-3C;	
Exhibit 1029	US Patent Application 2007/0008791 A1;	
/////		



800.211.DEPO (3376)
EsquireSolutions.com

1	E X H I B I T S (cont'd)	
2	NUMBER	PAGE
3	(PREMARKED)	
4	Exhibit 2006	Declaration of Dr. William Henry Mangione-Smith;
5	Exhibit 2007	Joint Claim Construction Chart Pursuant to P.R. 4-4(d);
6	Exhibit 2010	JEDEC STANDARD Double Data Rate (DDR) SDRAM Specification;
7	Exhibit 2011	JEDEC STANDARD DDR SDRAM Specification JESD79-3A;
8	Exhibit 2012	JEDEC STANDARD DDR2 SDRAM SPECIFICATION JESD792;
9	(NEW)	
10	Exhibit 1047	Netlist Technology Tutorial dated May 8, 2017; 55
11	Exhibit 1048	'506 patent (EX1001) Fig. 15 & Fig. 16; 116
12	Exhibit 1049	Data Register Buffer (300) in Hiraishi (EX1005); 179
13	Exhibit 1050	Hiraishi (EX1005) S4 read leveling; 229
14	Exhibit 1051	Hiraishi (EX1005) S4 write leveling; 205
15	Exhibit 1052	Butt (EX1029) Figures 2 and 3; 239
16	Exhibit 1053	JEDEC STANDARD FBDIMM: Advanced Memory Buffer (AMD). 246
17	//////	



800.211.DEPO (3376)
EsquireSolutions.com

1 Kirkland, Washington, Thursday, May 4, 2023

2 9:01 a.m.

3 ---o0o---

4
5 THE VIDEOGRAPHER: Good morning, 09:01:20
6 everybody. We are on the record. The time is
7 9:01 a.m.

8 This marks the beginning of Media Unit
9 No. 1 in the video-recorded deposition of
10 Dr. William Mangione-Smith, in the matter of 09:01:32
11 Samsung Electronics Co., Ltd., et al. versus
12 Netlist, Inc., being heard before the United States
13 Patent and Trademark Office before the Patent Trial
14 and Appeal Board. Case file number is
15 IPR2022-00711, Patent No. 10,860,506 B2. 09:01:52

16 This deposition is being held via Zoom on
17 this 4th day of May 2023.

18 My name is John Reidt. I am the
19 videographer today. The court reporter is
20 Rebecca Romano. And we are representing Esquire 09:02:16
21 Deposition Solutions.

22 Counsel, will you please introduce
23 yourselves and state your affiliations, and the
24 witness will be sworn in.

25 MR. CHANDLER: Good morning. This is 09:02:28



800.211.DEPO (3376)
EsquireSolutions.com

1 Theodore Chandler from Baker Botts on behalf of the 09:02:28
2 Petitioner, Samsung Electronics Co., Ltd.

3 And with me is my colleague,
4 Ferenc Pazmandi.

5 MR. LINDSAY: And this is 09:02:39
6 Jonathan Lindsay with Irell & Manella on behalf of
7 Netlist, Patent Owner, defending Dr. Mangione-Smith
8 today.

9 THE VIDEOGRAPHER: Thank you, Counsel.
10 Will the tran- -- will the court reporter 09:02:54
11 please swear in the witness, and we may proceed.

12 THE COURT REPORTER: At this time, I will
13 ask counsel to agree on the record that there is no
14 objection to this deposition officer administering
15 a binding oath to the deponent via remote 09:02:58
16 videoconference, starting with the noticing
17 attorney, please.

18 MR. CHANDLER: No objection.

19 MR. LINDSAY: No objection here.

20 THE COURT REPORTER: Okay, Doctor. If 09:03:14
21 you could raise your right hand for me, please.

22 THE DEPONENT: (Complies.)

23 THE COURT REPORTER: You do solemnly
24 state, under penalty of perjury, that the testimony
25 you are about to give in this deposition shall be 09:03:14



800.211.DEPO (3376)
EsquireSolutions.com

1 the truth, the whole truth and nothing but the
2 truth?

09:03:14

3 THE DEPONENT: Yes, I do.
4

5

09:03:14

6

7

8

9

10

09:03:14

11

12

13

14

15

09:03:14

16

17

18

19

20

09:03:14

21

22

23

24

25

/////

09:03:29



800.211.DEPO (3376)
EsquireSolutions.com

1 DR. WILLIAM HENRY MANGIONE-SMITH, 09:03:29
2 having been administered an oath, was examined and
3 testified as follows:
4 EXAMINATION
5 BY MR. CHANDLER: 09:03:31
6 Q. Please state your name for the record.
7 A. William Henry Mangione-Smith.
8 Q. What do you do for a living,
9 Dr. Mangione-Smith?
10 A. I am an engineer by profession. 09:03:39
11 Q. And what else do you do?
12 A. I provide engineering consultation. I am
13 an engineer.
14 Q. Were you retained by Netlist to provide
15 opinions in this matter related to Netlist's '506 09:03:51
16 patent?
17 A. I was through Irell & Manella. Yes.
18 Q. And the '506 patent has been marked as
19 Exhibit 1001 and is U.S. Patent No. 10,860,506,
20 correct? 09:04:11
21 A. Yes.
22 Q. And where do you live?
23 A. I live in Kirkland, Washington.
24 Q. And do you have your declaration, marked
25 as Exhibit 2006? 09:04:22



800.211.DEPO (3376)
EsquireSolutions.com

1 A. I do. 09:04:25

2 Q. And if you go to PDF page 109. Let me
3 know when you're there. Actually 106.

4 A. Okay. I don't have the -- yeah. I don't
5 have the PDF. I have the Word. So I -- you may 09:04:47
6 want to send that along as well. Sorry about that.

7 Q. I did. It was the first thing I sent to
8 you.

9 A. You did. Okay. Sorry. Let me find
10 that. 09:04:59

11 Yes, I have it. All right. 109.

12 Q. 109.

13 Does PDF 109 of Exhibit 2006 provide your
14 current contact information --

15 A. Yes. 09:05:23

16 Q. -- at the top?

17 Is that a yes?

18 A. Yes.

19 Q. Given that this is a remote deposition,
20 meaning we are not in the same physical room 09:05:32
21 together, there are a few questions I need to ask,
22 starting with: Where are you physically located
23 right now during this deposition?

24 A. At that address, which is my home
25 address. 09:05:47



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. In Kirkland, Washington? 09:05:47

2 A. Yes, sir.

3 Q. And is there anyone else in the room with
4 you right now?

5 A. There is no one else in the house. 09:05:53

6 Q. And given that I cannot see the room that
7 you are in, would you please let us know if
8 somebody enters the room that you are in at any
9 time before this deposition concludes.

10 A. Yes. 09:06:05

11 Q. And, Dr. Mangione-Smith, what did you
12 bring, if anything, with you to your deposition
13 today?

14 A. I'm not sure how to answer that question.
15 This is my home office. It's full of stuff. 09:06:20

16 Q. What do you have in front of you?

17 A. I've got, on the left, the PDF of my
18 declaration and, to my right, the video Zoom call.

19 Q. Did you bring any printed documents
20 relevant to this matter for your deposition? 09:06:38

21 A. No.

22 Q. And do you have anything besides unmarked
23 PDFs of the documents that have been filed in this
24 IPR?

25 A. I'm sorry. Could you repeat the 09:06:56



800.211.DEPO (3376)
EsquireSolutions.com

1 question. 09:06:58

2 Q. Are all of the PDFs that you have in
3 front of you clean copies of documents that were
4 filed in this IPR, or do you have any PDF files
5 with notes on them? 09:07:09

6 A. I have no notes on any of the PDF files
7 in front of me.

8 Q. And given that I cannot see whether you
9 have anything in front of you, would you please let
10 us know if you or anyone else puts anything in
11 front of you at any time before this deposition
12 concludes. 09:07:18

13 A. Sure.

14 Q. I'll take breaks throughout the
15 deposition, but I want to remind you that during
16 those breaks, under the rules of the PTAB, you
17 should not consult with your counsel about the
18 substance of your testimony. 09:07:30

19 Understood?

20 A. I will happily take your representation. 09:07:43
21 I'm not personally familiar with that rule.

22 Q. And during the deposition, I would ask
23 that you do not look up things on the Internet or
24 do other things on your computer or your phone that
25 we can't see on the camera. 09:07:57



800.211.DEPO (3376)
EsquireSolutions.com

1 Understood? 09:07:59

2 A. Understood.

3 Q. And do you understand that during your
4 deposition, you should not be emailing or texting
5 other people related to the substance of your
6 testimony today? 09:08:06

7 A. Yes, I understand your statement.

8 Q. What did Netlist ask you to do in this
9 matter?

10 A. They asked me to -- excuse me -- consider 09:08:20
11 some documents that were made available as part of
12 the IPR process and to provide expert commentary
13 on -- on them.

14 Q. Including the '506 patent?

15 A. Yes. 09:08:41

16 Q. Did anyone help you with your work?

17 A. Well, the -- my declaration comprises my
18 conclusions, not conclusions from anyone else.

19 Did anyone help me with my work? Sure,
20 in various degrees. For example, the exhibits were 09:08:59
21 made available to me. That certainly was helpful.

22 Q. And who helps you with your work?

23 A. I don't recall who made the exhibits
24 available to me. It would have been somebody at
25 Irell. 09:09:16



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. The law firm, Irell & Manella? 09:09:16

2 A. Yes, sir.

3 Q. Was there anyone else outside of the law
4 firm of Irell & Manella that helped you with your
5 work in this matter? 09:09:29

6 A. No.

7 Q. What did you do to prepare for today's
8 deposition?

9 A. Well, I -- I had a phone call over -- on
10 Saturday, and -- I had a phone call -- or a Zoom 09:09:42
11 call, rather, on Saturday, and a Zoom call
12 yesterday, and I reviewed a number of documents.

13 Q. And who attended those phone calls or
14 Zoom meetings on Saturday and yesterday?

15 A. Mr. Lindsay, and then on Saturday, 09:09:59
16 Ms. Zhong.

17 Q. Annita Zhong? Is that who you're
18 referring to?

19 A. Yes, sir.

20 Q. And how long did -- were those meetings 09:10:13
21 to prepare for the deposition today?

22 A. So the -- the Zoom call on Saturday
23 was -- was scheduled for four hours. I don't
24 remember if we took the full four hours.

25 And then there were actually two calls 09:10:32



800.211.DEPO (3376)
EsquireSolutions.com

1 yesterday, which were probably another five hours. 09:10:34

2 Q. And then you also prepared on your own
3 time for today's deposition; is that correct?

4 A. Yes, sir, that's correct.

5 Q. And approximately how long did you 09:10:45
6 prepare in your own time for today's deposition?

7 A. I couldn't possible answer that. In some
8 sense, from the very first day when I took up this
9 matter was preparation for this testimony.

10 Q. Within the past week, how long did you 09:11:01
11 prepare on your own for today's deposition?

12 A. In addition to those last Zoom calls, I
13 would estimate another maybe ten hours.

14 Q. And in preparation for today's
15 deposition, did you read your expert declaration 09:11:19
16 marked as Exhibit 2006?

17 A. Yes, I reviewed it.

18 Q. Approximately how many hours in total
19 have you spent working on this matter?

20 A. On the IPR specifically? 09:11:41

21 Q. Yes, on this IPR.

22 A. I couldn't answer, in part because --
23 well, I don't keep estimates that closely. And I
24 haven't separated out time from the IPR versus
25 district court litigation time. 09:11:58



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Have you also been consulting for Netlist 09:12:04
2 with respect to the '506 patent in related district
3 court litigation?

4 A. I'd have to go back and double-check if 09:12:20
5 this was one of the patents that was asserted. I
6 think I was asserted early on and then taken off.

7 But I have consulted with them outside of
8 the IPR process in the '506, yeah.

9 Q. In the past year, approximately how many 09:12:33
10 hours have you spent consulting for Netlist?

11 A. In all matters, I assume you are asking
12 about?

13 Q. Yes.

14 A. Yeah, I -- I don't know. Certainly more 09:12:47
15 than the 20 or so that I did immediately preparing
16 for this deposition and, you know, less than a
17 thousand. I don't know. I don't have a good
18 estimate.

19 Q. Would a few hundred hours be a good 09:13:03
20 estimate?

21 A. It might be.

22 Q. How much are you charging Netlist per
23 hour for your time spent on this matter?

24 A. I am charging them at what is my current 09:13:19
25 regular hourly rate, which is \$750 an hour.



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. So would it be fair to say over the past 09:13:28
2 year, you have charged Netlist in excess of
3 \$100,000?

4 A. I would certainly be comfortable with
5 saying that. 750 times the 20 hours that I said 09:13:37
6 I -- I am confident I immediately used to prepare
7 for this is the amount that I've charged them. I
8 don't know about higher estimate. I could review
9 my billing information, should you wish, and get
10 you the accurate number. 09:13:56

11 Q. All right. You have that available in
12 your home office?

13 A. Yes, in my files somewhere.

14 Q. Okay. Maybe at one of the breaks you
15 could take a quick look. 09:14:05

16 Is that possible?

17 A. It is possible.

18 Q. Okay. Approximately how many times have
19 you been deposed before?

20 A. Oh, I don't know. More than ten times. 09:14:16
21 Probably more than 15 days. So I would -- some of
22 the matters have involved multiple days.

23 Q. And have you been qualified as an expert
24 witness before?

25 A. Yes. 09:14:29



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. In any of the previous cases where you 09:14:32
2 have appeared as an expert witness, has a judge
3 ever stricken parts of your expert report or
4 excluded any opinions that were contained in your
5 expert reports, as far as you know? 09:14:48

6 A. As far as I know, I'm not sure. There
7 were some portions for the recent Netlist/Samsung
8 district court case of my report that were removed.
9 I don't know if the judge did that or if it was
10 agreement of the two parties or what. 09:15:12

11 Q. And have you testified at trial as an
12 expert before?

13 A. Yes, I have.

14 Q. And how many times?

15 A. I don't know. Mostly at the ITC in 09:15:24
16 district court. In front of juries, I think three
17 times.

18 Q. You have Exhibit 2006 in front of you,
19 and then if you could go to PDF page 112.

20 And let me know when you're there. 09:15:50

21 A. Okay.

22 Q. Do PDF pages 112 through 131 of
23 Exhibit 2006 list all of your expert depositions
24 and trial testimony?

25 A. As of the date when I submitted this CV 09:16:17



800.211.DEPO (3376)
EsquireSolutions.com

1 to Irell & Manella as part of this process, it was 09:16:20
2 my endeavor to list all of my testimony in my --
3 yes, in this document. I don't know of any errors
4 there.

5 Q. And if you look on the first page of 09:16:35
6 Exhibit 2006, the document was submitted to
7 Irell & Manella on January 31st, 2023; is that
8 correct?

9 A. Sure. But I assume you mean this
10 document, not the CV that was included in the 09:17:04
11 appendix. I don't know what date I provided that
12 CV to them.

13 Q. Well, to be clear, there was -- we only
14 got one document, which is Exhibit 2006, which is
15 what you have, the declaration with the CV at the 09:17:15
16 end.

17 So when do you think this CV is accurate
18 as of?

19 A. I believe it was accurate as of the date
20 when I submitted it to Irell. They packaged -- 09:17:29
21 they packaged it up. I did not produce this final
22 PDF.

23 Q. And approximately when do you believe you
24 submitted your CV to Irell?

25 A. I don't have an approximate date. I 09:17:41



800.211.DEPO (3376)
EsquireSolutions.com

1 would be happy with submitting one that's current 09:17:47
2 as of today if counsel allows and that would be
3 helpful. But I don't remember exactly when I sent
4 that CV out.

5 Q. Yeah. I mean, if you have a current CV, 09:17:56
6 we'll take it.

7 Is that something you have on your
8 computer?

9 A. Yes, I do.

10 Q. Okay. Maybe at a break. We don't have 09:18:08
11 to do it right this second. But at the next break,
12 we can get your billing record information and your
13 CV.

14 Fair enough?

15 MR. LINDSAY: Objection. This is 09:18:21
16 producing new evidence in the case outside of the
17 normal procedure.

18 Q. (By Mr. Chandler) Dr. Mangione-Smith,
19 when did you start your work for Netlist in this
20 matter? 09:18:34

21 A. Assuming "in this matter" means the IPR,
22 I don't know exactly. It was sometime after I
23 started my engagement with them related to Netlist,
24 Netlist and the district court case. This was part
25 of what came out of that work. 09:18:54



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. And that was in 2022 according to PDF 09:18:57
2 page 112 of your expert declaration marked as
3 Exhibit 2006, correct?

4 A. That seems right.

5 Q. Is your expert declaration marked as 09:19:14
6 Exhibit 2006 complete, meaning does it provide a
7 complete statement of all the opinions you intend
8 to express in this matter along with the basis and
9 reasons for those opinions?

10 A. I mean, it holds a complete list of the 09:19:28
11 opinions that I had stated in the declaration. I
12 have no intention of stating any particular opinion
13 going forward. I'll just do my best to answer
14 questions as they come up.

15 Q. Is your expert declaration marked as 09:19:52
16 Exhibit 2006 accurate as far as you know, meaning
17 it does not have any mistakes?

18 A. No.

19 Q. No, it's not accurate; or yes, it is
20 accurate? 09:20:06

21 A. No, it's not accurate.

22 Q. So what is inaccurate about your expert
23 declaration marked as Exhibit 2006? Or did you
24 mishear the question?

25 A. No, I heard the question. There was at 09:20:23



800.211.DEPO (3376)
EsquireSolutions.com

1 least -- well, there was -- there was one section 09:20:27
2 where I believe that we -- that I saw in the review
3 yesterday where the declaration says -- it's
4 talking about a patent, and it misidentifies who
5 owns the patent. 09:20:45

6 I think it said something like Netlist
7 has a patent that does X, Y and Z. And it really
8 should have been the Petitioner.

9 Q. And do you know where that mistake is?

10 A. Not off the top of my head. I could look 09:21:08
11 for it though.

12 Q. Okay. Please do that and let me know.

13 And while you're doing that, was there a
14 second mistake, or is that the only one?

15 A. That's the only one that I'm familiar 09:21:16
16 with.

17 Q. Is it paragraph 11 on page 4 or something
18 else?

19 A. Let me check. I'm pretty sure it was
20 much later than that, but... 09:22:39

21 Yes, that -- you found a second one
22 where -- where I say that I have relied on
23 Petitioner's attorneys for these legal standards.

24 I assume the correct legal term would have been
25 Respondents or Patent Owner. 09:23:07



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Yes. 09:23:11

2 A. But that's -- that's not the one that I
3 was thinking of. And I've done a couple of likely
4 search terms and not found it. So I know roughly
5 on the page where it appeared. I believe there was 09:23:25
6 a footnote on that page as well, if I'm remembering
7 correctly.

8 Q. Okay. If you find it during the
9 deposition, will you point it out?

10 A. Yes. I will be happy to. And I'll just 09:23:46
11 add the commentary that I -- I do think in the
12 context, the -- the proper intention was clear.
13 But if I run across it, I will let you know exactly
14 what I was thinking of.

15 Q. And to be clear, the mistake that you're 09:24:03
16 referring to is that you identified the wrong owner
17 of a patent number, but you identified the correct
18 patent number?

19 A. Yes. Yeah.

20 Q. Okay. And do you have any -- 09:24:15

21 A. Oh, I was just going to say, it wasn't --
22 I am not talking about a patent that's been cited
23 in this matter. It's not part of the prior art.
24 It's just a comment on elements of patents and what
25 people have -- what different entities have done 09:24:32



800.211.DEPO (3376)
EsquireSolutions.com

1 with patents and how they have claimed things in 09:24:35
2 the past.

3 Q. Okay. Do you have any present plans to
4 correct or supplement your expert declaration
5 marked as Exhibit 2006? 09:24:46

6 A. I don't know whether that's possible or
7 not. And I have not discussed it with counsel at
8 Irell & Manella.

9 Q. If you look at the bottom of page 43, top
10 of 44, is that the mistake you're referring to? 09:25:04

11 A. I believe so, although it is one of the
12 exhibits. Yeah, I assume that that's one of the
13 Samsung's patents. I'd have to -- I don't recall
14 the exhibit number, but that seems right. I
15 identify that as Patent Owner's DDR patents. 09:25:35

16 Q. Right, but it's not Netlist's patent;
17 it's Samsung's patent. So that's a mistake at the
18 bottom of the page 43, correct?

19 A. Yes. Yeah, I believe the exhibit and the
20 patent number are correctly identified. The 09:25:49
21 reference to the patent, to who owns it, was
22 incorrect.

23 Q. And, in fact, the exhibit number is, I
24 think, incorrect as well. It's Exhibit 2009, not
25 2008? 09:26:03



800.211.DEPO (3376)
EsquireSolutions.com

1 A. I wouldn't know. I -- that could be the 09:26:03
2 case as well. I certainly endeavored to get it
3 correct at the time.

4 Q. Dr. Mangione-Smith, have you carefully
5 read Netlist's '506 patent marked as Exhibit 1001? 09:26:15

6 A. Yes, I have.

7 Q. And do you believe you understand the
8 '506 patent marked as Exhibit 1001?

9 A. I have an understanding of it. Yes.

10 Q. Do you recall you understand the figures 09:26:32
11 of the '506 patent marked as Exhibit 1001?

12 A. Yes, I have an understanding of the
13 figures.

14 Q. And do you believe you understand the
15 claims at the end of the '506 patent marked as 09:26:44
16 Exhibit 1001?

17 A. I have an understanding of the claims.

18 Q. Have you carefully read the Hiraishi
19 prior art reference marked as Exhibit 1005?

20 A. Yes, I have. 09:27:03

21 Q. Do you believe you understand the
22 Hiraishi prior art reference marked as
23 Exhibit 1005?

24 A. Yes, I believe so.

25 Q. Have you carefully read the Tokuhiko 09:27:13



800.211.DEPO (3376)
EsquireSolutions.com

1 prior art reference marked as Exhibit 1006? 09:27:16

2 A. Yes.

3 Q. And do you believe you understand the
4 Tokuhiro prior art reference marked as
5 Exhibit 1006? 09:27:28

6 A. I have an understanding of that, yes.

7 Q. Have you carefully read the Butt
8 reference marked as Exhibit 1029?

9 A. Yes, I would say so. Although with
10 regards to the art reference, for example, by -- by 09:27:41
11 the Petitioners, I focused on the arguments that
12 they made. But yes, I have an understanding of it.

13 Q. And do you believe you understand the
14 Butt reference marked as Exhibit 1029?

15 A. Yes, I do. 09:27:59

16 Q. Have you carefully read the Ellsberry
17 reference marked as Exhibit 1007?

18 A. Yes, I have.

19 Q. And do you believe you understand the
20 Ellsberry reference marked as Exhibit 1007? 09:28:11

21 A. I believe I have an understanding
22 necessary for forming the opinions that I was asked
23 to consider, yes.

24 Q. Have you carefully read the Kim reference
25 marked as Exhibit 1008? 09:28:25



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes, although unless -- my recollection 09:28:34
2 of Kim is a little bit less. But yes.

3 Q. Do you believe you -- I'm sorry.
4 Say it again?

5 A. But yes, I have reviewed it. 09:28:42

6 Q. And do you believe you understand the Kim
7 reference marked as Exhibit 1008?

8 A. I have an understanding of it, yeah.

9 Q. Have you carefully read the JEDEC
10 Standard JESD79-3C marked as Exhibit 1020? 09:28:54

11 A. Yes, I have reviewed it.

12 Q. And do you believe you understand the
13 JEDEC Standard JESD79-3C marked as Exhibit 1020?

14 A. I have an understanding of it with
15 regards to the issues that I was asked to consider. 09:29:26

16 Q. And in your declaration, you also cited
17 to some other JEDEC standards as well, correct?

18 A. Likely.

19 Q. And do you believe you understood the
20 JEDEC standards that you cited in your expert 09:29:46
21 declaration marked as Exhibit 2006?

22 A. I believe I have an understanding to the
23 extent needed for me to consider the materials I
24 was asked to consider.

25 Q. Could you please turn to page 37 of your 09:30:02



800.211.DEPO (3376)
EsquireSolutions.com

1 expert declaration marked as Exhibit 2006. 09:30:06

2 And let me know when you're there.

3 A. All right. Yeah, I'm there.

4 Q. In your expert declaration, did you use
5 July 2012 as the date for a person of ordinary
6 skill in the art with respect to the '506 patent? 09:30:45

7 A. Yes, I believe so.

8 Q. Unless stated otherwise today, can you
9 please answer my questions from the perspective of
10 a person of ordinary skill in the art as of
11 July 2012. 09:31:11

12 A. I will do my best to do that as
13 appropriate, sure.

14 Q. And can you also answer my questions
15 today in a way that you believe is consistent with
16 the ordinary and accustomed meaning of words to a
17 person of ordinary skill in the art as of
18 July 2012. 09:31:29

19 A. Yes, I will endeavor to do that as it
20 makes sense in the context of the question. 09:31:48

21 Q. Before this matter, had you done work for
22 Netlist previously?

23 A. Yes, I have.

24 Q. When did you first do any work for
25 Netlist? 09:32:08



800.211.DEPO (3376)
EsquireSolutions.com

1 A. I believe that's listed on my CV. That 09:32:09
2 would have been a few years ago in a matter at the
3 ITC.

4 Q. If you go to PDF page 116 of your expert
5 declaration marked as Exhibit 2006. Are you 09:32:28
6 referring to the ITC case Netlist versus SK hynix,
7 Case No. 337-TA-1023?

8 A. Yes, although there were two. I am not
9 sure if that's the first one or the second one.
10 But that is one of them. 09:32:53

11 Q. And then the second one is above that on
12 the same page, ITC Case No. 337-TA-1089 in 2018; is
13 that correct?

14 A. Yeah, I see that. Yes, that's -- that's
15 correct. 09:33:10

16 Q. So were the first two matters that you
17 worked on for Netlist starting in 2017 and 2018?

18 A. Yes.

19 Q. And besides those cases and this series
20 of related cases, is there any other work that 09:33:31
21 you've done for Netlist?

22 A. There was a matter in the -- there was a
23 previous matter in district court, is my
24 recollection, that was involving the law firm
25 Mintz Levin, not Irell. And I did some work for 09:33:54



800.211.DEPO (3376)
EsquireSolutions.com

1 that. I don't think I testified or provided any
2 reports, but I did a small amount of work for that.

09:33:58

3 Q. And you're referring to what's shown on
4 page 114 of your expert declaration marked as 2006,
5 a matter in the year 2020, Netlist versus SK hynix
6 in the Western District of Texas; is that correct?

09:34:10

7 A. Yes.

8 Q. Before you were first engaged by Netlist
9 in 2017, did you know any of the named inventors on
10 the '506 patent identified as Hyun Lee and
11 Jayesh Bhakta?

09:34:29

12 A. Possibly. Not that I recall however.

13 Q. When was the first time that you'd heard
14 of the Hyun Lee and Jayesh Bhakta, the named
15 inventors of the '506 patent?

09:34:48

16 A. I -- I wouldn't know. To be honest with
17 you, I don't usually pay attention to the inventor
18 names. So if you had asked me if I knew those
19 people today before identifying them as the
20 inventors, I probably wouldn't have recalled it. I
21 focus on the -- try to focus more on the technical
22 details.

09:35:02

23 Q. Do you own any Netlist stock or stock
24 options?

25 A. No, I do not.

09:35:11



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. And is your compensation in this case 09:35:12
2 contingent in any way on the outcome?

3 A. No, it is not.

4 Q. In your expert declaration marked as
5 Exhibit 2006, could you please go to paragraph 10 09:35:24
6 on page 4.

7 Let me know when you're there.

8 A. Okay.

9 Q. You reviewed the declaration submitted in
10 this matter by Dr. Khatri, correct? 09:35:48

11 A. Yes, that's correct.

12 Q. Do you disagree with any of Dr. Khatri's
13 opinions?

14 A. I wasn't asked to consider whether I
15 agreed with every opinion he stated in that 09:36:12
16 declaration. So there may be ones that I disagree
17 with. I don't recall as I sit here.

18 Q. Do you identify any disagreement with
19 Dr. Khatri in your declaration?

20 A. I don't believe so. 09:36:28

21 No, that's the only reference to him.

22 Q. And so to be clear, if you want to
23 double-check, his declaration was marked as
24 Exhibit 2005.

25 A. I -- I don't know. I am searching for 09:37:23



800.211.DEPO (3376)
EsquireSolutions.com

1 2005. I don't see a reference to that in mine. 09:37:25

2 MR. LINDSAY: Counsel, could I ask, if
3 you'd like the witness to consider a document,
4 please introduce it.

5 MR. CHANDLER: Well, I am trying to ask 09:37:39
6 him if he expressed any disagreement with
7 Dr. Khatri.

8 Q. (By Mr. Chandler) And,
9 Dr. Mangione-Smith, now that you've had an
10 opportunity to search through your declaration 09:37:56
11 marked as Exhibit 2006, are you aware of any
12 instance where you disagree with any opinions by
13 Dr. Khatri?

14 A. Not that I am aware of, no.

15 Q. Could you go to paragraph 38 of your 09:38:13
16 declaration marked as Exhibit 2006.

17 And let me know when you're there.

18 A. All right. I'm at paragraph 38.

19 Q. Am I correct you adopted the Petitioner's
20 statement with respect to the level of ordinary 09:38:51
21 skill in the art for a person of ordinary skill in
22 the art; is that fair?

23 A. Yes.

24 Q. Let me give you, if you don't have it
25 already, Exhibit 1003, which is Dr. Wedig's 09:39:16



800.211.DEPO (3376)
EsquireSolutions.com

1 declaration. I'll just send it through the chat, 09:39:21
2 or you can pull it up if you have it locally,
3 whatever is easiest for you.

4 And go to Dr. Wedig's statement about the
5 person of ordinary skill in the art, which appears 09:39:35
6 on page 12 of Exhibit 1003, starting at
7 paragraph 37.

8 And let me know when you're there.

9 A. All right. I see it.

10 Q. All right. For purposes of this 09:40:13
11 proceeding, do you agree that a person of ordinary
12 skill in the art would have been someone with an
13 advanced degree in electrical or computer
14 engineering; and at least two years of work
15 experience in the field of memory module design and 09:40:25
16 operation, or a bachelor's degree in such
17 engineering disciplines; and at least three years
18 of work experience in the field?

19 A. If that matches my representation of my
20 understanding of the Petitioner's definition on 09:40:44
21 paragraph 37 of my declaration, yes.

22 Q. It's a little unclear to me. Were you --
23 so you're indicating that you were looking at the
24 petition. So let's go ahead and look at the
25 petition then. 09:41:10



800.211.DEPO (3376)
EsquireSolutions.com

1 Do you have the petition, or do you want 09:41:13
2 me to send it to you?

3 A. I do not have it handy.

4 Q. All right.

5 A. And I will let you know once I have it 09:41:39
6 opened.

7 Q. All right. Do you see at the bottom of
8 page 2 of the petition marked as Paper 1, there is
9 a heading "Person of Ordinary Skill in the Art"?

10 A. Yes, I see that. 09:42:14

11 Q. And you see that the petition marked as
12 Paper 1 cites to Dr. Wedig's declaration marked as
13 Exhibit 1003, specifically to paragraph 37, in
14 support of the definition of a person of ordinary
15 skill in the art? 09:42:34

16 A. I see that there is a -- a citation to
17 that.

18 Q. And for purposes of this proceeding, do
19 you agree that a person of ordinary skill in the
20 art would have been someone with an advanced degree 09:42:46
21 in electrical or computer engineering; and at least
22 two years of work experience in the field of memory
23 module design and operation, or a bachelor's degree
24 in such engineering disciplines; and at least three
25 years of work experience in the field? 09:43:02



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes. I was following along. That's what 09:43:09
2 I say at paragraph 37 of my declaration.

3 Q. And do you believe that you personally
4 are at least a person of ordinary skill in the art?

5 A. Yes. 09:43:19

6 Q. Do you agree a person of ordinary skill
7 in the art would have been familiar with the JEDEC
8 industry standards?

9 A. They may have been.

10 Q. Do you agree a person of ordinary skill 09:43:32
11 in the art would have been knowledgeable about the
12 design and operation of computer memories,
13 including DRAM and SDRAM devices that were
14 compliant with various standards and how they
15 interact with other components of a computer 09:43:45
16 system, such as memory controllers?

17 A. They may have been. There are many
18 different types of memory systems. The JEDEC
19 specifications refer to, you know, one of the most
20 commercially common types in use today. 09:44:02

21 Q. And when you say "one of the most
22 commercially types in use today," what are you
23 referring to?

24 A. The various JEDEC standards. It's an
25 industrial consortium, as I understand it. So 09:44:16



800.211.DEPO (3376)
EsquireSolutions.com

1 they're trying to develop standards and 09:44:18
2 specifications in order to sell products.

3 Q. With respect to memory devices and memory
4 modules?

5 A. Yes. 09:44:30

6 Q. Do you agree a person of ordinary skill
7 in the art would have been familiar with the
8 structure and operation of circuitry used to access
9 and control computer memories and other components
10 of the memory system? 09:44:43

11 A. They likely would have been -- have some
12 familiarity with some of those types of circuits,
13 yes.

14 Q. Do you agree a person of ordinary skill
15 in the art would have been familiar with circuits 09:44:55
16 such as ASICs and CPLDs, as well as low-level
17 circuits such as data buffers, tri-state buffers,
18 flip-flops and registers?

19 A. I would not say that, no.

20 Q. Why not? 09:45:17

21 A. Well, some of those that you referred to
22 are literally circuits. Others are largely devices
23 that are used to implement other circuits. So it's
24 a circuit design technology, I guess I would say,
25 rather than being circuits of any particular type 09:45:42



800.211.DEPO (3376)
EsquireSolutions.com

1 of interest in this matter.

09:45:46

2 Q. Do you agree a person of ordinary skill
3 in the art would be familiar with what's known as
4 ASICs and CPLDs?

5 A. They would probably have some familiarity
6 with that.

09:46:00

7 Q. And what is an ASIC?

8 A. ASIC stands for application-specific
9 integrated circuit.

10 Q. And what's a CPLD?

09:46:14

11 A. That stands for complex programmable
12 logic device. Sometimes it's used to refer to
13 elements that are also called FPGAs. The -- the
14 precise boundary between the two is, in my opinion
15 and experience, a little bit blurry.

09:46:34

16 Q. And at a high level, how would you
17 explain to a layperson what an ASIC is and what a
18 CPLD is?

19 A. Well, certainly at -- at a very high
20 level outside of the -- the particular context of
21 this matter, I would say an ASIC is a physical,
22 what we call, chip that somebody designed to serve
23 a specific purpose.

09:46:53

24 So, for example, Intel makes CPUs that
25 are called general purpose that -- that would not

09:47:18



800.211.DEPO (3376)
EsquireSolutions.com

1 be an ASIC. 09:47:20

2 When I was at Motorola, I was involved in
3 the design of a memory interface chip that was an
4 ASIC, because that particular design was intended
5 to work with one particular product. 09:47:37

6 Q. And what about a CPLD? How would you
7 explain that at a high level to a layperson?

8 A. Well, so one type of circuitry that we
9 design is called digital logic. And a CPLD is one
10 way to implement digital logic. So I could come up 09:47:58
11 with a digital logic circuit that served a
12 particular task that I needed implemented and then
13 decide to put that -- the -- actually instantiate
14 it, create it, in the form of an ASIC; or, in many
15 cases, I could use -- I could choose to implement 09:48:19
16 it using a CPLD or an FPGA.

17 Those are oftentimes engineering or
18 economic design choices, just alternatives.

19 Q. So if I understand what you just said,
20 digital logic could be implemented in an ASIC, or 09:48:38
21 alternatively in a CPLD, or alternatively in an
22 FPGA; is that fair?

23 A. Yes, although it depends on the
24 particular digital circuit. Some of them -- if
25 it's relatively small and relatively low speed, 09:48:56



800.211.DEPO (3376)
EsquireSolutions.com

1 that is in general the case that you could use any 09:48:59
2 of those three alternatives.

3 But ASIC designs tend to provide much
4 greater speed. So if speed is a dramatic concern,
5 one implementation technology would be more 09:49:14
6 attractive over another. And some may just not be
7 practical at all.

8 Q. You referred to some design choices or
9 alternatives between an ASIC, CPLD and FPGA.

10 At a high level, how would characterize 09:49:32
11 the design choices that would lead a person of
12 ordinary skill in the art to either an ASIC or a
13 CPLD or an FPGA?

14 MR. LINDSAY: Objection. Form.

15 THE DEPONENT: Oftentimes those sorts of 09:49:49
16 decisions are made -- they are -- they are
17 significant economic consequences in terms of
18 marketing and development cost. So those decisions
19 are made by people -- not by what we're discussing
20 as a person of ordinary skill in the art here, 09:50:09
21 although a person who makes those kinds of
22 decisions could also be a person of ordinary skill
23 in the art in the context of the '506 patent.

24 Q. (By Mr. Chandler) So when you say
25 "significant economic decisions," do you mean that 09:50:23



800.211.DEPO (3376)
EsquireSolutions.com

1 there's a -- more of a business reason to choose an 09:50:26
2 ASIC, CPLD or FPGA as opposed to a technical
3 reason? Or were you referring to something else?

4 MR. LINDSAY: Objection. Form.

5 THE DEPONENT: I am referring to that 09:50:39
6 there almost always are significant business
7 reasons on top of the technical reasons that we
8 talked about previously.

9 Q. (By Mr. Chandler) And at a high level,
10 what would be the sort of business reasons in favor 09:50:50
11 of an ASIC or a CPLD or an FPGA compared to the
12 other alternatives?

13 MR. LINDSAY: Objection. Form.

14 THE DEPONENT: Well, for the most part,
15 an ASIC is going to provide what we would refer to 09:51:06
16 as the greatest density. So the -- the literal
17 resources in terms of silicon required for
18 implementing a particular circuit will be smaller
19 with an ASIC, the power consumption will tend to be
20 much lower, and the speed will -- the ASIC will 09:51:25
21 give the opportunity to achieve increased
22 performance.

23 One big problem with an ASIC -- or
24 rather, the downside is that some elements of the
25 engineering design process are much more 09:51:41



800.211.DEPO (3376)
EsquireSolutions.com

1 significant, and there's much greater -- up-front 09:51:44
2 manufacturing costs, often referred to as NREs,
3 nonrecov- -- nonrecurring engineering costs.

4 Whereas an FPGA or a CPLD, there are
5 no -- essentially no NREs costs. Those are 09:52:04
6 commodity parts that are produced by a third party.
7 Someone could go out and just buy those, and then
8 they have to do the design time process to figure
9 out how to implement the circuit in them.

10 CLPDs have historically been smaller and 09:52:22
11 slower and cheaper. FPGAs have historically been
12 larger, more complex, more capable, more expensive.
13 But as I suggested, the line between them is a
14 little bit blurry.

15 It's easy -- it's oftentimes easy for me 09:52:42
16 to look at something and say, "Oh, yeah that's a
17 FPGA"; and an alternative, "Oh, no, that's --
18 that's a CPLD," you know. But as they get closer
19 together, different people might disagree.

20 Q. (By Mr. Chandler) You mentioned an ASIC 09:52:57
21 has a larger up-front cost. Does the ASIC have a
22 lower marginal cost if you are producing a high
23 volume of the ASICs?

24 MR. LINDSAY: Objection. Form.

25 Q. (By Mr. Chandler) Compared to a CPLD or 09:53:10



800.211.DEPO (3376)
EsquireSolutions.com

1 FPGA? 09:53:12

2 MR. LINDSAY: Objection. Form.

3 THE DEPONENT: I really don't know. I

4 mean, I would -- I would assume so. As products go

5 into higher volume, they tend to move to ASICs if 09:53:20

6 they didn't use one to begin with.

7 But that's really not my area of

8 expertise.

9 Q. (By Mr. Chandler) Do you believe a

10 person of ordinary skill in the art would be 09:53:31

11 familiar with circuits such as data buffers,

12 tri-state buffers, flip-flops and registers?

13 A. Certainly tri-state buffers, flip-flops,

14 and I think the last one you said was registers.

15 Data buffers have a particular meaning, I 09:53:54

16 believe, in the context of much of the art that

17 we're looking at. So a person of ordinary skill in

18 the art would have an understanding of the general

19 concept of a data buffer. They wouldn't

20 necessarily have an understanding of the specific 09:54:14

21 way that term is used in the context, for example,

22 of the -- the JEDEC standards.

23 Q. What's a register, and how would you

24 explain it to a layperson?

25 A. Well, I haven't taught in quite a few 09:54:32



800.211.DEPO (3376)
EsquireSolutions.com

1 years. But at a very high level, off the top of my 09:54:34
2 head, I would say a register is a piece of hardware
3 that's able to store, over a period of time, a
4 piece of digital information. Typically, that
5 information can be updated over time and accessed 09:54:55
6 at a later point in time.

7 Q. And how would you explain what a
8 flip-flop is to a layperson?

9 A. A flip-flop a little bit more complicated
10 because there are many different types of 09:55:14
11 flip-flops. One of the most common would be called
12 a D flip-flop which, in many ways, people often --
13 I believe people often would consider that to be a
14 1-bit register.

15 Q. And how does a D flip-flop or a 1-bit 09:55:30
16 register work at a high level?

17 A. There is a piece of information that's
18 coming in. And there's a 1-bit input, there's a
19 1-bit output, there's a clock signal, and then
20 typically there's a signal that says "write" or 09:55:50
21 "update."

22 And so the output signal produces --
23 makes available whatever 1 bit of information is
24 stored in the D flip-flop continuously.

25 And then the update signal, or sometimes 09:56:07



800.211.DEPO (3376)
EsquireSolutions.com

1 it's called a write-enable signal, causes the D 09:56:10
2 flip-flop to change the value. Well, to -- to make
3 sure that the value it contains reflects the value
4 on its input line.

5 Q. And what gets output of the flip-flop? 09:56:29

6 A. Whatever -- well, in the case of the --
7 the D flip-flop, whatever 1 bit of information it
8 had been told to maintain over time.

9 Q. And you may have explained it a moment
10 ago, but I just didn't understand it. 09:56:58

11 What does the clock do in a D flip-flop?

12 A. A clock is used generally to make sure
13 that the whole system maintains a sense of
14 synchronization. Most digital logic is called
15 "synchronous," which means that all of the state 09:57:15
16 information for the digital circuitry changes on
17 a -- on a regular sort of heartbeat. And that's
18 the clock I was referring to.

19 Q. How would you explain what a tri-state
20 buffer is to a layperson? 09:57:34

21 A. Well, at a high level, I'd be inclined to
22 say that a tri-state buffer is like a gate. So
23 there's an input and there's an output. And then
24 there's a control signal, which says "make sure the
25 output reflects what the input is." 09:57:57



800.211.DEPO (3376)
EsquireSolutions.com

1 It's a little bit tricky in the sense 09:58:04
2 that if that control is turned off, the output of
3 the tri-state buffer is something such that it
4 doesn't reflect any particular value. And the
5 outputs of two tri-state buffers can be wired 09:58:18
6 together, and as long as only one of them is
7 activated at a time, they won't run into electrical
8 problems.

9 Q. And is there a name for that state you
10 were just referring to? 09:58:32

11 A. Broken.

12 Q. "Broken," like broken wire?

13 A. No, no. I mean, if -- if you have two
14 tri-state buffers outputs connected together, and
15 they are both turned on, you've got -- you've got a 09:58:45
16 broken design. It's wrong. It's prone to failure.

17 Q. And what I was trying to refer to is when
18 the two tri-state buffers are not turned on and
19 your system is not broken, what is the name of that
20 state -- 09:59:09

21 A. Okay.

22 Q. -- when the tri-state buffer is not
23 turned on?

24 A. The output is oftentimes referred to as a
25 Z state. 09:59:21



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. The letter Z? 09:59:22

2 A. Yes, sir.

3 Q. And what does the letter Z stand for or
4 mean?

5 A. To be honest with you, I don't recall. 09:59:33

6 Yeah. It just means that the -- the buffer is --
7 is not driving any signal. So if somebody else is
8 trying to drive a signal that's connected to the
9 output of the buffer, that it will be okay. The
10 buffer won't interfere with it. 09:59:54

11 Otherwise, the problem is if you have two
12 buffers turned on, and one of them is trying to
13 drive an output of 0 volts, and the other one is
14 trying to drive an output of 5 volts, that's a
15 logical error. And it's difficult to describe, to
16 be sure, exactly what the actual value on that
17 combined output wire would be. 10:00:09

18 Q. Why is it called a tri-state buffer?
19 What are the three states?

20 A. Well, we're talking about digital logic. 10:00:29
21 So the three states would be either 0, 1 and Z; or
22 high, low and Z, with 0 and 1 being the same as --
23 I guess I said that, and I reversed the order.

24 0 is typically called low, and 1 is
25 typically called high. But they're referring to 10:00:49



800.211.DEPO (3376)
EsquireSolutions.com

1 the same two states. 10:00:52

2 Q. And how would you explain to a layperson
3 what the Z state of a tri-state buffer is?

4 A. It's a Z -- it's a state where the buffer
5 has no -- I might be inclined to say it's a state 10:01:08
6 where the buffer has no impact on the wire on the
7 circuit to which it is connected.

8 Q. If I understand correctly, would it be
9 fair to say when a tri-state buffer is in a Z
10 state, it's as if that tri-state buffer were 10:01:32
11 disconnected from the rest of the circuit?

12 A. That is certainly the logical intent. Of
13 course, it is still connected. There are still
14 some electrical properties. But that is the
15 intention for the tri-state buffer. 10:01:50

16 Q. Okay.

17 MR. CHANDLER: Why don't we take a quick
18 break. And during the break, if you could do two
19 things for me.

20 One, quickly look at your billing records 10:02:02
21 with respect to how much you have billed Netlist in
22 the last year.

23 And, second, quickly look at your current
24 CV and let me know if the CV that's attached to the
25 back of Exhibit 2006 is out of date, or if the CV 10:02:14



800.211.DEPO (3376)
EsquireSolutions.com

1 at the back of 2006 is essentially more or less 10:02:19
2 current.
3 Fair enough?
4 THE DEPONENT: I will talk to
5 Mr. Lindsay. 10:02:27
6 MR. LINDSAY: I object.
7 Okay. Just because he's sitting in his
8 office doesn't mean you get to take additional
9 discovery of everything he has in his desk and on
10 his computer. 10:02:35
11 You can ask him questions, and he's going
12 to answer to the best of his knowledge, and that's
13 it.
14 MR. CHANDLER: All right. Let's go off
15 the record, and we'll come back. 10:02:44
16 THE VIDEOGRAPHER: We're going off the
17 record. The time is 10:02.
18 (Recess taken.)
19 THE VIDEOGRAPHER: We're going back on
20 the record. The time is 10:13. 10:13:19
21 Q. (By Mr. Chandler) Dr. Mangione-Smith, as
22 a reminder, did you talk with your counsel or
23 anyone else during the break?
24 A. No, I did not.
25 Q. Do you believe the CV at the end of your 10:13:36



800.211.DEPO (3376)
EsquireSolutions.com

1 declaration marked as Exhibit 2006 is up to date? 10:13:39

2 A. Let me review that.

3 No. I can identify at least one matter
4 that I have worked on that is not there, which
5 related to -- which was on behalf of DivX in a 10:14:30
6 disagreement they had with Harman.

7 Q. Do you want to spell it, for the benefit
8 of the court reporter, DivX and Harman.

9 A. DivX is D-I-V-X. And Harman, I guess, is
10 H-A-R-M-A-N. 10:14:49

11 Q. Other than the DivX versus Harman matter,
12 are you aware of anything else that is missing from
13 your CV at the end of Exhibit 2006?

14 A. Not that occurs to me as I sit here.

15 Q. All right. And, approximately, how much 10:15:11
16 do you believe that you have billed to Netlist over
17 the past year?

18 MR. LINDSAY: Objection. Asked and
19 answered.

20 THE DEPONENT: Yeah, I -- I don't really 10:15:21
21 have any more information to provide above and
22 beyond what we discussed prior to the first break.

23 Q. (By Mr. Chandler) Were you familiar with
24 the JEDEC standards at the time of the claimed
25 invention in the '506 patent, which is to say 10:15:41



800.211.DEPO (3376)
EsquireSolutions.com

1 around July of 2012? 10:15:44

2 A. I was familiar -- I had a familiarity
3 with JEDEC, the organization.

4 Q. Had you ever taught any of the JEDEC
5 standards to any of your students? 10:15:57

6 A. I have taught, certainly, many aspects of
7 interfacing to memory devices, some of which are
8 key elements of various JEDEC standards. But I
9 wouldn't say that I ever stepped back and said,
10 "Okay, now we are going to learn specifically about 10:16:22
11 this JEDEC standard."

12 Q. When you taught students, do you recall
13 ever showing any of them any specific JEDEC
14 standards?

15 A. No, it was largely focused in when I 10:16:43
16 taught on technology, not industrial consortiums.

17 Q. Have you ever attended a JEDEC meeting
18 yourself?

19 A. No, I have not.

20 Q. Could you turn to your CV at the back of 10:17:10
21 Exhibit 2006, which I believe starts on page 109 of
22 the PDF file.

23 A. Okay. I am there.

24 Q. And your CV runs from PDF pages 109
25 through 136 of Exhibit 2006, correct? 10:17:33



800.211.DEPO (3376)
EsquireSolutions.com

1 while -- while the term "memory module" can have a 10:19:45
2 much broader meaning in general.

3 Q. Can you explain that last answer a little
4 bit more, what -- the point you are trying to make?

5 MR. LINDSAY: Objection. Form. 10:20:02

6 THE DEPONENT: Well, if I -- I could
7 build a memory system with separate DRAM chips and
8 own my custom controller or an ASIC that are -- or
9 even simpler. I could take the components of --
10 literally of a DDR DIMM and put them on a 10:20:19
11 motherboard, so that there was no separate PC board
12 or no inserting something into a socket.

13 From an engineering point of view, I
14 would say that nothing has changed, while certainly
15 things have changed from a business and 10:20:43
16 manufacturing point of view.

17 So one could say, "Well, that's still a
18 memory module," if it was one.

19 Or one could say, "No, that's not a
20 memory module. A memory module means something 10:20:54
21 that can be inserted into a -- or coupled to a
22 motherboard," for example.

23 Q. (By Mr. Chandler) And how do you believe
24 that a person of ordinary skill in the art would
25 understand the phrase "memory module"? 10:21:10



800.211.DEPO (3376)
EsquireSolutions.com

1 MR. LINDSAY: Objection. Form. 10:21:13

2 THE DEPONENT: I think it depends on the
3 context. I think in the context of the '506 and
4 what we are talking about, largely, absent some
5 other illuminating language, a person would 10:21:24
6 generally understand it to at least cover things
7 like various DDR DIMMs.

8 Q. (By Mr. Chandler) And for the benefit of
9 the court reporter, could you spell DIMM and
10 explain what that is. 10:21:39

11 A. Yeah. DIMM is D-I-M-M. And that stands
12 for dual in-line memory module.

13 And D-D-R stands for double data rate.

14 Q. So can you search your CV for "memory
15 module" and confirm that the only hits are for the 10:22:02
16 consulting work you did for Netlist.

17 A. The phrase "memory modules" appears to
18 only appear under the -- in my CV under headings
19 for work that I've done for Netlist.

20 MR. CHANDLER: I'd like to introduce a 10:22:50
21 new exhibit, which I'll mark as Exhibit 1047. And
22 I'll send it through the chat to everyone.

23 (Exhibit 1047 was marked for
24 identification by the Court Reporter and is
25 attached hereto.) 10:22:58



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) Let me know when you 10:23:00
2 have it on your screen, Dr. Mangione-Smith.

3 A. Yes, I see that.

4 Q. Exhibit 1047 is Netlist's "Technology 10:23:24
5 Tutorial" in the ITC case where you were providing
6 expert testimony about memory modules, correct?

7 A. I'll take your representation that that
8 number is the ITC -- is one of the ITC cases. I
9 don't recall for sure.

10 Q. And do you recall this technology 10:23:43
11 tutorial marked as Exhibit 1047?

12 A. No, not really.

13 Q. But you were at trial in the ITC Case
14 337-TA-1023 when the "Technology Tutorial" marked
15 as Exhibit 1047 was presented to the judge, 10:24:03
16 correct?

17 A. I may have been. Oftentimes I am not --
18 even when I'm in town to testify, I am not in trial
19 the full time.

20 And furthermore, particularly at the ITC, 10:24:18
21 I've seen technology tutorials that were done well
22 in advance of trial and without me present. I
23 don't recall if that was the case here or not.

24 Q. Do you recall any errors or misstatement
25 in Netlist's "Technology Tutorial" marked as 10:24:33



800.211.DEPO (3376)
EsquireSolutions.com

1 Exhibit 1047? 10:24:37

2 A. Given that I don't recall the "Technology
3 Tutorial," I would say that I don't recall any
4 errors or misstatements within it.

5 Q. Could you turn to page 2 of Exhibit 1047. 10:24:48

6 And let me know when you're there.

7 A. Yes, I'm there.

8 Q. Does page 2 of Exhibit 1047 show a
9 picture of a DIMM, which I believe you said is a
10 dual in-line memory module? 10:25:04

11 A. Yes, it does.

12 Q. Could you turn to page 3 of Exhibit 1047.

13 Let me know when you're there.

14 A. Okay. I'm there.

15 Q. Do you agree that SDRAM memory devices 10:25:22
16 "emerged in the 1990s and have been standardized by
17 JEDEC" [as read]?

18 A. That may be the case. I don't have that
19 particular opinion. I haven't -- like I said, I
20 don't recall seeing this document or reviewing 10:25:45
21 them. It's not clearly wrong as to my recollection
22 as I sit here today.

23 Q. Do you agree that "SDRAM has evolved in
24 several generations, including DDR, DDR 2, DDR 3
25 and currently DDR 4"? 10:26:01



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Those are examples of SDRAM technology. 10:26:06
2 There are many other examples of SDRAM technology
3 as well.

4 Q. But I believe you said earlier that's one
5 of the common examples of SDRAM technology: DDR1, 10:26:16
6 DDR2, DDR3 and currently DDR4; is that fair?

7 A. I don't -- I don't recall testifying to
8 that.

9 Q. Do you believe that's correct?

10 A. It is certainly a common form of SDRAM. 10:26:34
11 But SDRAM is used in many contexts that are not DDR
12 of any sort.

13 Q. Please turn to page 4 of Exhibit 1047.
14 Let me know when you're there.

15 A. Okay. 10:26:55

16 Q. Do you agree that "SDRAM contains several
17 sections called banks"?

18 A. It might. It depends on the particular
19 SDRAM.

20 Q. Do you agree that each bank within an 10:27:15
21 SDRAM "consists of rows and columns of memory"?

22 A. It might. That's a common design. It
23 depends on the details of the particular design.

24 Q. So would it be fair to say that a common
25 design of SDRAM is that it "contains several 10:27:34



800.211.DEPO (3376)
EsquireSolutions.com

1 sections called banks" and "each bank consists of 10:27:37
2 rows and columns of memory"?

3 Would that be a common design?

4 A. Outside of the context of any particular
5 patent, that might be a common design. Although, 10:27:45
6 as I said, we're examining a document that I
7 certainly don't recall and I'm not sure I ever
8 seen.

9 Q. Could you turn to page 5 of Exhibit 1047.
10 And let me know when you're there. 10:28:01

11 A. Okay. I'm there.

12 Q. Do you agree that "a rank is a set of
13 DRAMs that are written to or read from together"?

14 A. In -- in this context, in this example,
15 that's how the term "rank" is typically used for 10:28:17
16 DDR DIMMs, multi-rank DDR DIMMs. Many DIMMs only
17 have one rank.

18 Q. And what does "DQ" stand for?

19 A. Oftentimes, that's used to refer to the
20 data which is moved between a memory controller, 10:28:45
21 which is typically -- in the context of a system
22 that uses DDR DIMMs is going to be on a
23 motherboard, and the DIMM itself.

24 Q. And do you agree that this page 5 of
25 Exhibit 1047 illustrates the concept of two ranks, 10:29:05



800.211.DEPO (3376)
EsquireSolutions.com

1 highlighted in green and red, where each rank 10:29:11
2 comprises eight DRAM memory devices, each DRAM
3 memory device is 8 bits wide, resulting in each
4 rank of memory devices having a total bit width of
5 64 bits? 10:29:32

6 A. Some aspects of what you just said I
7 think are clearly illustrated here. Some aspects
8 of it are much less clear.

9 Q. And what's less clear to you?

10 A. Well, for example, it's not clear that 10:29:53
11 the devices marked DRAM1, 2, 3, 4 and 5 are
12 physical devices.

13 Most DRAM chips that I'm familiar with,
14 at least currently, are 4 bits, not 8 bits.

15 But you can design a physical chip like 10:30:11
16 that to have various widths, usually in terms of a
17 power of two.

18 Q. All right. And so are memory modules
19 limited to a 64-bit width, or are other bit widths
20 possible? 10:30:37

21 MR. LINDSAY: Objection. Form.

22 THE DEPONENT: Other bit widths are
23 possible. In fact, I believe that we've seen some
24 examples where other bit widths are used. Yeah.

25 Q. (By Mr. Chandler) So, for example, the 10:30:52



800.211.DEPO (3376)
EsquireSolutions.com

1 memory module could be 32 bits or 16 bits; is that 10:30:53
2 fair?

3 MR. LINDSAY: Objection. Form.

4 THE DEPONENT: They -- they could be. I
5 don't know that that would then satisfy what's 10:31:00
6 colloquially referred to as a DDR or a DDR DIMM in
7 general, let alone any particular JEDEC standard.
8 A more common example would be 72 bits, which
9 certainly falls within various JEDEC standards.

10 Q. (By Mr. Chandler) In the example on 10:31:26
11 page 5 of Exhibit 1047, you see at the bottom it
12 says "x8," which is referred to in the middle of as
13 "by eight"?

14 A. Yes, I see that.

15 Q. And what's "by eight" mean? 10:31:43

16 A. Well, it says -- in the middle there, it
17 says it "writes 8DQ bits," and then that's referred
18 to as "by eight."

19 So it means there's -- it's representing
20 that each one of those arrows conveys 8 bits of 10:31:57
21 data, which almost always means it's got eight
22 physical signal lines, although it might have --
23 easily have 16 or some control signals as well.

24 Q. So in the example on page 5 of
25 Exhibit 1047, would each DRAM be 8 bits wide or 10:32:18



800.211.DEPO (3376)
EsquireSolutions.com

1 referred to as by-eight DRAM? 10:32:24

2 MR. LINDSAY: Objection. Form.

3 THE DEPONENT: That seems to be what
4 they're indicating here, yes.

5 Q. (By Mr. Chandler) And -- 10:32:38

6 A. In this -- in this particular example,
7 yeah.

8 Q. And did you state previously that DIMM
9 memory modules can also have DRAMs of other widths,
10 such as by-four, which would be 4 bits wide? 10:32:50

11 MR. LINDSAY: Objection. Form.

12 THE DEPONENT: Yes. I believe -- well,
13 yes. I'll just leave it at that.

14 Q. (By Mr. Chandler) What are the most
15 common bit widths for DRAMs on a memory module? 10:33:06

16 A. I was just about to comment on that. But
17 then I caught myself because the fact of the matter
18 is, I -- I don't sell products in that marketplace.
19 I don't know what's the most common.

20 I believe that by-four is not at all 10:33:22
21 uncommon. But -- and it may very well be the most
22 common. But the fact of the matter is, I really
23 don't know.

24 Q. But at least by-four and by-eight would
25 be well-known widths of DRAM memory devices for a 10:33:38



800.211.DEPO (3376)
EsquireSolutions.com

1 DIMM memory module; is that fair? 10:33:45

2 MR. LINDSAY: Objection. Form.

3 THE DEPONENT: I -- I would think so,
4 although I'm only cautious to the extent I'm really
5 not sure how common by-eight is. As a concept, 10:33:54

6 it's -- it's certainly not surprising. I just
7 don't know. Even less than the by-four, I don't
8 know what sort of market penetration it has.

9 Q. (By Mr. Chandler) Right.

10 So your instinct is that by-four would be 10:34:08
11 more common than by-eight as far as a bit width for
12 a DRAM memory device on a memory module?

13 MR. LINDSAY: Objection. Form.

14 THE DEPONENT: I would say that that
15 sounds like my instincts as I sit here today for 10:34:21
16 the current market. But that may just be a
17 consequence of the particular devices that I have
18 reviewed over the last few years.

19 Q. (By Mr. Chandler) And do you agree that
20 the data lines on a standard DIMM are 10:34:36
21 bidirectional, meaning that the same data line
22 that's used for a write operation can also be used
23 at a later time for a read operation and vice
24 versa?

25 MR. LINDSAY: Objection. Form. Also 10:34:52



800.211.DEPO (3376)
EsquireSolutions.com

1 beyond the scope of direct. 10:34:53

2 THE DEPONENT: Yes. Most memory modules
3 of this sort are intended to both -- for the memory
4 controller to write data into it and to read data
5 from it. And it's not uncommon for the read and 10:35:10
6 write data to go over the same set of physical
7 wires.

8 Q. (By Mr. Chandler) And you talk about
9 bidirectional in your expert declaration marked as
10 Exhibit 2006, right? 10:35:22

11 B-I, hyphen, directional.

12 A. Likely. It wouldn't surprise me, yeah.

13 Q. Can you turn to page 6 of Exhibit 1047.
14 Let me know when you're there.

15 A. Okay. 10:35:41

16 Q. Do you agree that DQS refers to the data
17 strobe signal?

18 A. So I would say that DQS and what an
19 engineer would refer to -- would speak as a DQS
20 bar -- and it's shown here as DQS with a line over 10:36:08
21 the top of it in this example -- together form a
22 data strobe signal.

23 Although in -- in other contexts, outside
24 of a DDR DIMM and the JEDEC standard, oftentimes
25 you would only have one strobe, not two. Or one 10:36:28



800.211.DEPO (3376)
EsquireSolutions.com

1 wire for that purpose, rather. 10:36:31

2 Q. And can you explain that a little bit
3 more, what you're referring to by "DQS" and "DQS
4 bar" and how they work together to create the data
5 strobe signal. 10:36:43

6 MR. LINDSAY: Objection. Form.

7 THE DEPONENT: Yeah. So this mechanism
8 of sending a piece of information like a strobe
9 signal over two wires that are complementary is
10 often used in -- as the speed of digital circuits 10:37:02

11 gets faster. And so by "complementary" here, all I
12 mean is that when one of the physical wires, the --
13 the electrical signal on it -- as opposed to the
14 logical signal -- when the electrical signal goes
15 high, the complementary wire, the electrical signal 10:37:18
16 will go low.

17 And so a receiver can watch both of those
18 signals, electrical signals, and more reliably
19 determine when the logical signal, like the actual
20 strobe signal that -- that someone wants to send, 10:37:34
21 has made a transition.

22 Q. (By Mr. Chandler) And is that concept
23 shown on page 6 of Exhibit 1047, what you were just
24 describing?

25 A. Yeah, as -- yes, I would -- I would say 10:37:51



800.211.DEPO (3376)
EsquireSolutions.com

1 it is. You'll see there's a -- an arrow towards 10:37:54
2 the left of the page that's marked "tDS." Like I
3 said, I haven't reviewed this, but there's a
4 concept called data setup or setup time. I assume
5 that stands for time for data setup or time for, 10:38:15
6 you know, the -- the D signal to be set up.

7 And then immediately to the right of
8 that, there's something called "tDH." And that, I
9 think, stands for time data hold.

10 So these are specifications that say, if 10:38:35
11 you want to send that information, you to have
12 adhere to whatever the setup and hold time
13 specifications are.

14 Q. And do you agree that DQ can refer to the
15 data signal? 10:38:52

16 A. It -- sure, it can. Yeah.

17 Q. And do you agree that the DQS data strobe
18 clocks the DQ data signal into and out of the DRAM
19 memory device?

20 MR. LINDSAY: Objection. Form. 10:39:11

21 THE DEPONENT: I don't know that I would
22 say that. It -- it's used to control when the --
23 whatever is receiving this, the data, samples it.
24 But ultimately, there will be some delay due to
25 what we call propagation delay, and it's not -- 10:39:33



800.211.DEPO (3376)
EsquireSolutions.com

1 it's not a clock signal. 10:39:38

2 Q. (By Mr. Chandler) When you say "it's not
3 a clock signal," what is not a clock signal?

4 A. Neither the DQS nor the DQS bar nor the
5 DQ data signals are clock signals. None of those 10:39:50
6 are clock signals. That's why -- I wouldn't
7 generally be inclined to say they are clocking the
8 data into whatever the receiver is.

9 Q. And what would you be inclined to say
10 instead? 10:40:05

11 A. They control when the receiver captures
12 the data, when it samples it. When it latches it,
13 is a term that's also used, or when it registers
14 it.

15 Q. And what about when data goes out of the 10:40:20
16 DRAM? How would you characterize that term for
17 when the DQS strobe signal clocks the DQ data out
18 of the DRAM? How would you describe that?

19 MR. LINDSAY: Objection. Form.

20 THE DEPONENT: Well, again, I -- I 10:40:42
21 wouldn't characterize it as clocking. And this is
22 in the specific context of -- of DDR DIMM standard
23 devices.

24 But, again, the strobe signals in
25 general, and certainly in this case, are used to 10:40:58



800.211.DEPO (3376)
EsquireSolutions.com

1 indicate that a particular time has arrived when 10:41:01
2 data carried on some other signal wires should be
3 sampled.

4 Q. (By Mr. Chandler) Does the DQS strobe
5 signal -- is it used for when DQ data goes out of 10:41:20
6 the DRAM or only when it goes into the DRAM?

7 A. Well, again, it -- it depends on the
8 particular context. In the context of a JEDEC
9 standard DDR DIMM, all of the ones that I'm

10 familiar with, the -- the DQS signal -- and from 10:41:45
11 now on, hopefully it's clear when I say "DQS," I
12 mean the two complementary wires. But the DQS

13 signal will go from a controller to the memory
14 chip, telling it to sample when -- when a write is
15 being done, and will generally come from the memory 10:42:09
16 chip to a controller when a read is being done.

17 Q. Do you agree that "one nanosecond is
18 one billionth of a second"?

19 A. Now you've -- you've hit one of my
20 professional weaknesses. It says that here. I -- 10:42:30
21 I don't recall. I have no reason to think it's

22 wrong. I trust that whoever put that on there
23 checked it.

24 I do know that it's about 18 inches of a
25 copper wire, but that's... 10:42:48



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. That was my next question. 10:42:49

2 Do you agree that a signal travels
3 roughly 6 inches in one nanosecond in a memory
4 module, not accounting for load?

5 A. It may. It -- well, first of all, you 10:43:02
6 have to account for load. And it depends an awful
7 lot on the impedance of what it's traveling over.

8 Q. What is load?

9 A. Load generally refers to other electrical
10 circuits that have an impact on the propagation 10:43:23
11 delay of a signal.

12 Q. Your recollection was that a signal would
13 travel, I think you said, about 18 inches in
14 1 nanosecond on copper wire?

15 A. I think that's -- that's about right. 10:43:40
16 There's a famous story by Admiral Grace Murray
17 Hopper who would go around and give talks. She was
18 an engineer and a Navy admiral who was behind a lot
19 of supercomputing development. And this was back
20 when 1 nanosecond was incredibly short. 10:43:56

21 And she would give talks and hold up a
22 piece of wire and say, "You've got to think about
23 this. If you're talking about 1 nanosecond, you
24 can't have a wire go more than..."

25 And so I'm guessing it was probably about 10:44:09



800.211.DEPO (3376)
EsquireSolutions.com

1 18 inches, because she would hold it up in her 10:44:12
2 hand.

3 Q. And for the benefit of the court
4 reporter, can you spell her last name, if you
5 recall. 10:44:19

6 A. Yeah. Hopper, H-O-P-P-E-R.

7 Q. Do you agree that DDR2 memory devices use
8 a clock speed that's approximately twice as fast as
9 the clock speed for DDR1 memory devices?

10 A. I don't have an opinion on that. It 10:44:39
11 indicates that on this slide, but I don't have any
12 particular recollection. I haven't looked at
13 comparing DDR2 to DDR1 with any degree of rigor, as
14 far as I can recall.

15 Q. Do you agree that DDR3 memory devices use 10:44:56
16 a clock speed that's approximately twice as fast as
17 the clock speed for DDR2 memory devices?

18 A. I would be inclined to give the same
19 answer. I -- I don't -- you know, that's what's
20 represented here. I have no reason to think either 10:45:12
21 that it's incorrect or that it's correct.

22 Q. Do you agree that with each generation of
23 the DDR standard that the clock speeds generally
24 got faster?

25 A. Yes, I would -- I would agree with that. 10:45:27



800.211.DEPO (3376)
EsquireSolutions.com

1 I can't point to any one off the top of my head 10:45:29
2 where that was not the case. Or rather, I would
3 say that, generally, the -- the peak speed that's
4 possible, because these modules can run at multiple
5 speeds. 10:45:45

6 Q. This may refresh your recollection a
7 little bit. If you go to your expert declaration
8 and look at -- around paragraph 110, 111.

9 At the end of the paragraph 110, it's
10 fair to say "DDR2 memory operated at effectively 10:46:30
11 twice the speed of DDR1 memory," correct?

12 A. That's what it says. As I -- yes,
13 that -- that's what it says. Although as I was
14 suggesting, I could have been more precise and say
15 that its peak speed is effectively twice the peak 10:47:04
16 speed of the earlier technology.

17 Q. And then if you go to page 101 of your
18 expert declaration marked as Exhibit 2006, on the
19 third line from the top, you indicate that the
20 clock period for a DDR3 memory device is 1.25 10:47:20
21 nanoseconds, correct?

22 A. It indicates that that's the clock speed
23 for the fastest DDR3 when operating at that fastest
24 rate.

25 Q. And that's consistent with page 6 of 10:47:42



800.211.DEPO (3376)
EsquireSolutions.com

1 Exhibit 1047 for DDR3, correct? 1.25 nanoseconds 10:47:47
2 for DDR3?

3 A. Yes, that's what it says.

4 Q. Here's another difficult question for
5 you: Is 1.25 nanoseconds 1,250 picoseconds? 10:48:02

6 A. I believe so, yeah.

7 Q. Please turn to page 7, Exhibit 1047.
8 Let me know when you're there.

9 A. I'm there.

10 Q. Do you agree page 7 of Exhibit 1047 10:48:23
11 illustrates an unbuffered DIMM, also known as a
12 UDIMM?

13 A. That is how it's labeled, and it
14 certainly illustrates aspects of a UDIMM, yes.

15 Q. In your opinion, did a person of ordinary 10:48:40
16 skill in the art know about UDIMM memory modules?

17 A. They very well might. They might not.

18 Q. How would you explain to a layperson what
19 a UDIMM is using the illustration on page 7 of
20 Exhibit 1047? 10:48:59

21 MR. LINDSAY: Objection. Beyond the
22 scope of direct.

23 THE DEPONENT: So I would largely say
24 that over time, initially, memory systems of this
25 sort did not have additional buffers beyond what's 10:49:13



800.211.DEPO (3376)
EsquireSolutions.com

1 shown in this figure. And then some important core 10:49:20
2 technology was introduced, some of which we've --
3 well, we're likely to see, that introduced data
4 buffers into these designs.

5 And so at -- at some point, the industry 10:49:37
6 decided it was useful to distinguish between ones
7 that still did not have data buffers and those that
8 do by using the term "unbuffered," or U in front of
9 DIMM.

10 Q. (By Mr. Chandler) Can you turn to page 8 10:49:55
11 of Exhibit 1047.

12 Let me know when you're there.

13 A. Okay. I'm there.

14 Q. Do you agree that page 8 of Exhibit 1047
15 illustrates a registered DIMM, also known as an 10:50:05
16 RDIMM?

17 A. That is how the figure is labeled, and I
18 believe that they are intending to represent some
19 of the -- some of the main aspects of an RDIMM,
20 yes. 10:50:20

21 Q. In your opinion, did a person of ordinary
22 skill in the art know about RDIMM memory modules?

23 A. As the term for "a person of ordinary
24 skill in the art" is defined that we've been
25 talking about, I think such a person might very 10:50:33



800.211.DEPO (3376)
EsquireSolutions.com

1 well be familiar with RDIMMs. But they might not 10:50:36
2 be.

3 Q. JEDEC had standardized RDIMM memory
4 modules by July of 2012, right?

5 A. I don't recall. I believe it's likely, 10:50:50
6 but to be honest with you, I don't recall.

7 Q. Using page 8 of Exhibit 1047, how would
8 you explain to a layperson what an RDIMM is?

9 MR. LINDSAY: Objection. Beyond the
10 scope of direct. 10:51:05

11 THE DEPONENT: I would say that an
12 addition is made by adding a bit of circuitry,
13 called a register in this figure, which sits
14 between the memory controller and -- and an
15 interface from the register to the various 10:51:26
16 individual DRAM components.

17 Q. (By Mr. Chandler) And what signals does
18 the register of an RDIMM register?

19 A. At a very high level, in a JEDEC RDIMM,
20 the register will register control and -- and 10:51:44
21 address signals.

22 Q. And the clock signal?

23 A. It does register a clock signal as well,
24 but I wouldn't generally characterize that. It
25 does have a clock signal come in and a clock signal 10:52:06



800.211.DEPO (3376)
EsquireSolutions.com

1 that goes out. 10:52:09

2 Q. In an RDIMM, the register does not
3 register the DQ data signals or the DQS strobe,
4 correct?

5 A. In a JEDEC standard RDIMM, the register 10:52:26
6 as shown here does not register the data either
7 being read or written between the module and the
8 memory controller.

9 Q. Please turn to page 9 of Exhibit 1047.
10 Let me know when you're there. 10:52:48

11 A. Okay. I'm there.

12 Q. Do you agree page 9 of Exhibit 1047
13 illustrates a fully-buffered DIMM, also known as a
14 FBDIMM?

15 A. Yes, it is labeled "FBDIMM." 10:53:04

16 Q. In your opinion, did a person of ordinary
17 skill in the art know about FBDIMM memory modules?

18 A. I would give the same answer I gave
19 before: They may have; they may not have.

20 In my experience, I think FBDIMMs are 10:53:22
21 much less common in the marketplace. So even if a
22 person worked with JEDEC DIMMs of various forms,
23 they may not have run across this.

24 But, you know, as I suggested before, I
25 don't -- that's just my intuition. I really don't 10:53:40



800.211.DEPO (3376)
EsquireSolutions.com

1 know what sort of volumes each different kind of 10:53:44
2 DIMM sold in.

3 Q. But JEDEC had standardized FBDIMM memory
4 modules by July of 2012, correct?

5 A. I don't -- I don't know. They may have. 10:53:53

6 Q. Using page 9 of Exhibit 1047, how would
7 you explain to a layperson what an FBDIMM is?

8 MR. LINDSAY: Objection. Beyond the
9 scope of direct.

10 THE DEPONENT: I would say that in this 10:54:09
11 figure, it shows the data signals and the data
12 strobe signals going into a block called AMB, and
13 then signals with data and address and command and
14 clock going out of that to the DRAMs.

15 Q. (By Mr. Chandler) And what does AMB 10:54:32
16 stand for?

17 A. I don't recall as I sit here. I think
18 it's advanced memory buffer.

19 Q. All right. Does the advanced memory
20 buffer, abbreviated AMB, on an FBDIMM buffer all of 10:54:45
21 the signals to and from the memory controller,
22 including data, address, command and clock?

23 MR. LINDSAY: Objection. Beyond the
24 scope of direct.

25 THE DEPONENT: Not that I know of, no. 10:55:04



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) Why do you say that? 10:55:07

2 A. I haven't endeavored to check to see if
3 all the signals between the memory controller and
4 the DIMM go through -- go through the AMB. Many of
5 them do. We've talked about many of them. There 10:55:20
6 are other signals in use in such systems, some of
7 which may not go through the AMB.

8 Q. In an FBDIMM, at least the address
9 command, DQ data and DQS strobe signals are
10 buffered by the AMB before going to the DRAM memory 10:55:39
11 devices and vice versa, correct?

12 MR. LINDSAY: Objection. Beyond the
13 scope of direct.

14 THE DEPONENT: That is what's shown here.

15 Q. (By Mr. Chandler) And is that your 10:55:55
16 understanding and recollection of how an FBDIMM
17 works at a high level?

18 MR. LINDSAY: Objection. Beyond the
19 scope of direct. Also form.

20 THE DEPONENT: Yeah, it might be. I 10:56:08
21 haven't reviewed FBDIMM technology in any great
22 detail in -- in a while. But it's not inconsistent
23 with my understanding.

24 Q. (By Mr. Chandler) What's the benefit of
25 buffering data lines on a memory module? 10:56:21



800.211.DEPO (3376)
EsquireSolutions.com

1 MR. LINDSAY: Objection. Form. 10:56:25

2 THE DEPONENT: It depends on the
3 particular system. There are benefits and there
4 are costs.

5 Q. (By Mr. Chandler) Can you elaborate. 10:56:41

6 A. Sure. What would you like to know about?

7 Q. What are some of the primary benefits of
8 buffering data lines on a memory module?

9 A. So oftentimes, data buffers are added in
10 order to reduce the load seen by the memory 10:56:59

11 controller. That's -- can be particularly
12 important in the context where a DIMM has more than
13 one rank, as we've seen previously; or when the
14 memory controller sees multiple -- meaning it can
15 immediately communicate to multiple -- DIMMs. 10:57:21

16 So that is a common benefit.

17 Q. And why does reducing the load seen by
18 the memory controller create a benefit? How would
19 you explain that to a layperson?

20 MR. LINDSAY: Objection. Form. 10:57:44

21 THE DEPONENT: So the memory controller
22 needs to be able to reliably send information to
23 the DIMM, whether that's commands or an address of
24 where to store data or the data to be stored. And
25 the higher the load is, I would say, the more 10:58:03



800.211.DEPO (3376)
EsquireSolutions.com

1 effort the memory controller needs to put into 10:58:07
2 sending those commands; as well as the higher the
3 load is, the more time it takes for those commands
4 to be reliably received.

5 Q. (By Mr. Chandler) If I understand your 10:58:25
6 last answer, are you saying that buffering the data
7 lines can permit the memory controller to send data
8 signals at higher speeds?

9 MR. LINDSAY: Objection. Misstates prior
10 testimony. 10:58:41

11 THE DEPONENT: In certain use -- usage
12 scenarios, that can be an important element to
13 achieving greater speed of transactions, yes.

14 Q. (By Mr. Chandler) Can you turn to
15 page 10 of Exhibit 1047. 10:59:00

16 And let me know when you're there.

17 A. Okay.

18 Q. Do you agree that page 10 of Exhibit 1047
19 illustrates a DDR3 LRDIMM memory module?

20 A. Yes, I see that it's labeled that way. 10:59:20

21 Q. In your opinion, did a person of ordinary
22 skill in the art know about DDR3 LRDIMM memory
23 modules?

24 A. I would say they may or they may not.
25 And in particular, this is what they refer to as a 10:59:35



800.211.DEPO (3376)
EsquireSolutions.com

1 Gen1 LRDIMM. In my experience, that seems to be 10:59:42
2 much less common, but with the usual caveats of me
3 not having anything beyond my intuition with
4 regards to market sales.

5 Q. But by July of 2012, JEDEC had 10:59:56
6 standardized DDR3 LRDIMM memory modules, correct?

7 A. I don't recall. They may have.

8 Q. Using page 10 of Exhibit 1047, how would
9 you explain to a layperson what a DDR3 LRDIMM
10 memory module is? 11:00:21

11 A. Well, as shown here, the significant
12 difference between, seems to me -- that's a good
13 question.

14 So it combines the aspects of a circuit
15 that does registering along the lines of what we 11:00:50
16 talked about previously, registering and then
17 forwarding the address, command, control and -- and
18 clock signals, as well as registering the data
19 signals flowing into and off of the LRDIMM module.

20 Q. Does the DDR3 LRDIMM have a fly-by 11:01:18
21 arrangement for the command, address and clock
22 signals going to the DRAM memory devices?

23 A. That depends on the particular context,
24 what one means by "fly-by."

25 In this case, the command and control 11:01:37



800.211.DEPO (3376)
EsquireSolutions.com

1 signals, for example, as well as the data signals 11:01:40
2 as illustrated here are sent on a single central
3 set of wires that then pass out to the left and to
4 the right. And those wires are not registered
5 along the way. 11:01:57

6 They do have propagation delay. So a
7 signal will, for example, appear at DRAM5, the
8 block labeled "DRAM5" on this image, prior to the
9 same signal arriving at DRAM8.

10 Q. And similarly, the signal from the memory 11:02:20
11 controller would arrive at DRAM4 prior to arriving
12 at DRAM1, as shown as page 10 of Exhibit 1047; is
13 that fair.

14 MR. LINDSAY: Objection. Form.

15 THE DEPONENT: There is this propagation 11:02:37
16 and delay issue as you move away from that central
17 set of wires, whether it's left to right or right
18 to left. And both are -- both directions are
19 illustrated here.

20 Q. (By Mr. Chandler) Can you turn to page 11:02:56
21 11 of Exhibit 1047.

22 And let me know when you're there.

23 A. Yes, I'm there.

24 Q. Do you agree that page 11 of Exhibit 1047
25 illustrates a memory module that today is known as 11:03:07



800.211.DEPO (3376)
EsquireSolutions.com

1 a DDR4 LRDIMM memory module? 11:03:12

2 A. That -- that is what it's labeled, and I
3 don't know of any particular error there.

4 Q. And using page 11 of Exhibit 1047, how
5 would you explain to a layperson at a high level 11:03:33
6 what a DDR4 LRDIMM memory module is?

7 A. I would say that as this figure
8 illustrates, it's similar to the DDR3 LRDIMMs
9 except that the buffering of data signals is shown
10 to take place in multiple locations, distributed 11:03:57
11 from left to right along the -- the DIMM module.

12 Q. And you're referring to the boxes labeled
13 "DB"; is that correct?

14 A. Yes. DB stands for, in this context,
15 data buffer. 11:04:17

16 Q. And a DDR4 LRDIMM memory module also has
17 a fly-by arrangement for the command, address and
18 clock signals; is that fair?

19 A. Yes.

20 Q. And DDR4 LRDIMM also has a fly-by 11:04:47
21 arrangement for the control signals to the DB data
22 buffers, correct?

23 A. Well, we're not showing any control
24 signals to the DB data buffers. I don't recall if
25 those have a fly-by or more of what we would refer 11:05:11



800.211.DEPO (3376)
EsquireSolutions.com

1 to as a daisy-chained structure. 11:05:14

2 Q. Could you look at Exhibit 1020.

3 Let me know when you have it in front of
4 you.

5 A. Okay. 11:05:36

6 Q. And do you have your exhibits, such as
7 Exhibit 2010, 2011, 2012?

8 A. Not that I can easily put my hands on.

9 Q. Let me try to help you.

10 Do you have them now? 11:06:23

11 A. I have 2010, and the others will be here
12 any second. Did you want me to turn to one of them
13 in particular?

14 Q. Sure. Let's start with 2010.

15 Let me know when you have it. 11:06:33

16 And I'll -- since we're at it, I'll send
17 you one more.

18 A. Okay. I have it open.

19 Q. In your opinion, would a person of
20 ordinary skill in the art have known about the 11:06:51

21 JEDEC standard for DDR memory devices marked as
22 Exhibit 2010 to your declaration?

23 MR. LINDSAY: Objection.

24 THE DEPONENT: They may have; they may
25 not have. 11:07:09



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) Dated June 2000, that 11:07:10
2 standard.

3 A. Yes, the same answer. They -- they may
4 very well have; they may not have.

5 Q. And to be clear, I'm referring to a 11:07:17
6 hypothetical person of ordinary skill in the art,
7 which you understand, hypothetically, knows of all
8 of the art in the field.

9 Do you understand that?

10 MR. LINDSAY: Objection. Form. 11:07:35

11 THE DEPONENT: I guess I -- I would say
12 no, I didn't necessarily understand that. I don't
13 know anybody who knows of all the art, but likely
14 could get access to it.

15 But as well, in this context, the way 11:07:56
16 that we've agreed that a person of ordinary skill
17 in the art is defined, I don't think that that
18 requires them to actually have been working with
19 JEDEC DDR DIMMs or DDR memory chips of any sort.

20 But also, even if they are, oftentimes 11:08:19
21 engineers are using that technology without going
22 to a particular specification. That -- some of
23 them have to, people who build memory modules. But
24 a person of ordinary skill in the art may simply
25 work with memory modules of the sort. 11:08:38



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) For purposes of 11:08:45
2 forming your opinions in this matter, did you treat
3 the JEDEC standard marked as Exhibit 2010, which is
4 the DDR standard from June 2000, as something that
5 was available to and known by the hypothetical 11:08:58
6 person of ordinary skill in the art?

7 A. I believe that it's available to such a
8 person. Although, to be honest with you, the
9 standards have always been made available to me, so
10 I don't know if there's some payment that -- I 11:09:21
11 don't know if they're just publicly available on
12 the Internet, for example. But certainly under
13 some situation, they would be available to a person
14 of ordinary skill in the art.

15 Q. Okay. So would a person of ordinary 11:09:40
16 skill in the art have known about the JEDEC
17 standard for DDR memory devices marked as
18 Exhibit 2010?

19 A. They -- they may have, particularly if
20 they were working with those particular SDRAM 11:10:01
21 chips. But a lot of people in -- in the art -- a
22 lot of -- a person of ordinary skill in the art, as
23 I said, wouldn't be working with those chips
24 directly, or they wouldn't -- even if they were
25 being used in a system. 11:10:22



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. In forming your nonobviousness opinions 11:10:23
2 in this matter, did you treat the JEDEC standard
3 for DDR1 memory devices, marked as Exhibit 2010, as
4 within the knowledge of a person of ordinary skill
5 in the art or not? 11:10:41

6 MR. LINDSAY: Objection. Asked and
7 answered.

8 THE DEPONENT: Well, I think to the
9 extent that certainly -- well, give me a moment to
10 review. 11:10:57

11 Yeah, I don't have -- I don't believe I
12 necessarily formed an opinion on that.

13 But Mr. Wedig says that Tokuhiro notes
14 that the JEDEC standard -- I'm sorry. That's not
15 the reference I was thinking of. 11:11:26

16 He says a person of ordinary skill in the
17 art would have been familiar with the industry
18 standard -- with the JEDEC industry standards. And
19 so in my task of analyzing his arguments, I took
20 into the context his belief in that statement. 11:11:44

21 Q. (By Mr. Chandler) So analyzing
22 Dr. Wedig's arguments, did you assume that a person
23 of ordinary skill in the art would have known about
24 the JEDEC standard for DDR memory devices marked as
25 Exhibit 2010? 11:12:04



800.211.DEPO (3376)
EsquireSolutions.com

1 the cover. 11:14:00

2 A. Yeah, I need to find it because there are
3 multiple windows open. Yes, the cover says
4 June 2010 -- June 2000 rather.

5 Q. And the JESD79-2 standard for DDR2 memory 11:14:12
6 devices is dated September of 2003, as shown in
7 Exhibit 2012, correct?

8 A. I didn't open 2012 yet. I -- I will
9 double-check, but I assume that that's the case,
10 2003. 11:14:42

11 Yes, it says September 2003.

12 Q. And then Exhibit 2011 is the JEDEC
13 standard JESD79-3A for DDR3 memory devices dated
14 September 2007 that you cited, correct?

15 A. Yes. 11:15:10

16 Q. And then Exhibit 1020 is the JEDEC
17 JESD79-3C standard for DDR3 memory devices dated
18 April of 2008, correct?

19 A. No, I believe it's -- that was the
20 underlying document, and this is a revision from 11:15:38
21 November of 2008.

22 Q. My mistake.

23 To be clear, Exhibit 1020 is the JESD79-3
24 standard for DDR3 memory devices dated November
25 2008, correct? 11:15:56



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yeah, and it says "-3C" to indicate the 11:16:00
2 different revisions, to make that a little clearer.

3 Q. Okay.

4 THE DEPONENT: Would now be a good time
5 to take a brief break? 11:16:20

6 MR. CHANDLER: Of course. Five minutes.

7 THE VIDEOGRAPHER: We're going off the
8 record. The time is 11:16.

9 (Recess taken.)

10 THE VIDEOGRAPHER: We're going back on 11:26:09
11 the record. The time is 11:26.

12 Q. (By Mr. Chandler) Dr. Mangione-Smith,
13 could you please turn to your expert declaration
14 marked as Exhibit 2006, and go to the top of
15 page 17. 11:26:23

16 Let me know when you're there.

17 A. The PDF page or the numbered page at the
18 bottom?

19 Q. Numbered page. Numbered page.

20 A. I'm there. 11:26:41

21 Q. All right. I want to get from you a
22 high-level explanation of how the '506 patent works
23 as a preface to some more detailed questions. But
24 with that goal in mind, can you answer my next few
25 questions? 11:27:04



800.211.DEPO (3376)
EsquireSolutions.com

1 Fair enough? 11:27:06

2 MR. LINDSAY: Objection. Form.

3 THE DEPONENT: Yeah, I'll try with the
4 usual caveat that I don't typically characterize
5 patents. The -- the patent claims are what's 11:27:15

6 important generally, and so I focus on exactly what
7 the patent claims say.

8 But the '506 relates to data buffers of
9 the sort that we've been talking about.

10 Q. (By Mr. Chandler) Let me ask -- let me 11:27:34
11 ask the question. I didn't mean for you to try to
12 explain something in the abstract.

13 Just to give you background, so what I
14 want to talk about is some of the figures and some
15 of the text in the '506 patent that describe some 11:27:47
16 of the exemplary embodiments of the claimed
17 invention.

18 Fair enough?

19 A. Got it.

20 Q. And so at the top of page 17 of your 11:28:01
21 expert declaration marked as Exhibit 2006, you cite
22 to Claim 1 of the '506 patent on the fourth line,
23 correct?

24 Where you say "see id., cl. 1," right?

25 A. Yeah. 11:28:25



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. And then you cite to column 15, lines 23 11:28:25
2 through 26, correct?

3 A. Yes.

4 Q. All right. And would it be fair to say 11:28:35
5 that column 15, lines 23 to 26, of the '506 patent
6 relates to an exemplary embodiment of the claimed
7 inventions of the '506 patent?

8 A. I would -- I believe that's the case,
9 yeah.

10 Q. And then if you look at the '506 patent 11:28:55
11 marked as Exhibit 1001, could you go to Figures 12A
12 and 12B.

13 And let me know when you're there.

14 A. Sure. I'm there.

15 Q. Good. 11:29:32

16 And you understand Figures 12A and 12B of
17 the '506 patent?

18 A. I have an understanding of them, yes.

19 Q. And it would be fair to say that
20 Figures 12A and 12B of the '506 patent illustrate 11:29:42
21 an exemplary embodiment of the claimed inventions
22 of the '506 patent?

23 A. That wouldn't surprise me. I don't
24 recall for sure exactly how they are characterized.

25 Q. Can you explain to a layperson what 11:29:58



800.211.DEPO (3376)
EsquireSolutions.com

1 Figures 12A and 12B of the '506 patent are teaching 11:30:05
2 and how that relates to the claimed inventions?

3 MR. LINDSAY: Objection. Form.

4 THE DEPONENT: Sure. In the column 3, it
5 says that 12A to 12B are timing diagrams, which is 11:30:30
6 grammatically problematic. But there are timing
7 diagrams illustrating a write operation and a read
8 operation respectively, performed by a memory
9 module according to one embodiment.

10 Q. (By Mr. Chandler) And so I am looking at 11:30:52
11 Figure 12A, and I've got your 12B. Can you explain
12 to me as a layperson what these figures are
13 teaching with respect to the claimed invention.

14 A. I, in general, wouldn't endeavor to do
15 that. These are not intended to be informative for 11:31:19
16 a layperson. It's fairly -- there's an awful lot
17 of technical detail here.

18 Q. How would you explain to a person of
19 ordinary skill in the art what Figures 12A and 12B
20 are teaching with respect to the claimed invention? 11:31:33

21 A. I would point them to what the patent
22 literally says, which I -- where I read the summary
23 of how they characterize 12A and 12B, as well as
24 further discussion throughout the specification.

25 Q. And can you explain it to me as an expert 11:31:52



800.211.DEPO (3376)
EsquireSolutions.com

1 without just reading to me from the patent. 11:31:53

2 A. Yeah, I could, but I'm -- I'm not really
3 inclined to do that. I will point out that one key
4 element, which is illustrated in 12B, is that it
5 shows a delay of the -- of a data strobe, which is 11:32:07
6 one element or relevant to an awful lot of the
7 claims. Perhaps all the claims. I don't recall if
8 it's relevant to all of the claims.

9 Q. All right. Could you explain that a
10 little bit more. 11:32:24

11 A. Yeah. If you look at 12B, it shows at
12 time t8, there is a -- well, it's -- it's shown
13 in -- there's a signal called DQS which is shown in
14 dotted lines, with an arrow in dotted lines above
15 that going to another box labeled "DQS" that is in 11:32:48
16 solid lines, and it's marked "delay," which to me
17 indicates that 12B is saying that that signal
18 should be delayed in this context from t8 to t9.

19 Q. And do Figures 12A and 12B indicate how
20 to calculate the amount of delay for the DQS strobe 11:33:12
21 signal shown in Figure 12B?

22 A. I don't see any calculation there, other
23 than they're indicating specifically to delay it
24 from what looks to be one time unit, t8 to t9.

25 Q. So in your opinion, Figure 12A and 12B 11:33:39



800.211.DEPO (3376)
EsquireSolutions.com

1 don't disclose how to determine the delay. They 11:33:43
2 only show in Figure 12B that there's some delay
3 that is applying to the DQS strobe signal; is that
4 fair?

5 MR. LINDSAY: Objection. Form. 11:34:01
6 Misstates prior testimony.

7 THE DEPONENT: There's no equation, for
8 example, shown in 12A or 12B to show how to
9 calculate that delay. I don't recall if the
10 discussion of 12A or 12B says, for example, "Well, 11:34:15
11 look at these three factors illustrated here."

12 The delay would be calculated in some
13 particular way, in which case one might say, "Yeah,
14 12A and 12B shows to calculate that delay."

15 I -- I don't recall. I haven't reviewed 11:34:32
16 it for that aspect.

17 Q. (By Mr. Chandler) I mean, but you did
18 review the '506 patent carefully in preparation for
19 your deposition today, correct?

20 A. I believe I -- I testified to that 11:34:48
21 previously. Mostly for my preparation -- specific
22 preparation over the last week or so, I focused on
23 what Dr. Wedig said and what I said to refresh
24 myself of the -- myself of the issues at hand, and
25 then, as needed, went back to the '506. 11:35:08



800.211.DEPO (3376)
EsquireSolutions.com

1 But I certainly did not sit down and do a 11:35:12
2 from-the-fresh, complete review of the '506.

3 Q. At the top of page 17 of your declaration
4 marked as Exhibit 2006, you cited to column 15,
5 lines 23 to 26, correct? 11:35:31

6 A. Yes.

7 Q. Are those relevant -- are those lines of
8 column 15 relevant to understanding Figures 12A and
9 12B of the '506 patent?

10 A. I did cite them here, sure. I tend not 11:36:01
11 to cite material that I think is irrelevant.

12 Q. So can you explain to me and to the board
13 what Figures 12A and 12B are teaching to a person
14 of ordinary skill in the art with respect to the
15 claimed inventions of the '506 patent. 11:36:28

16 MR. LINDSAY: Objection. Asked and
17 answered.

18 Q. (By Mr. Chandler) And if you can't,
19 that's fine, and we'll move on. But I just want
20 to, you know, make sure I've got your testimony 11:36:40
21 here.

22 A. Yeah, it certainly is illustrating a
23 delay of the DQS strobe. I haven't looked at any
24 particular figure and said, well, you know, what
25 exactly is the full breadth of what it's teaching 11:36:52



800.211.DEPO (3376)
EsquireSolutions.com

1 here given the context where it's discussed. 11:36:56

2 So I -- you know, I don't feel prepared
3 to answer that in greater detail without further
4 review beyond what we've been discussing with
5 regards to the delay that's illustrated in 12B. 11:37:09

6 Q. And I believe you said you spent
7 approximately 20 hours preparing for your
8 deposition today over the last week; is that fair?

9 A. That seems about right.

10 Q. Are you able to explain, using 11:37:31
11 Figures 12A and 12B, how the delay in Figure 12B
12 would be determined as taught by the '506 patent?

13 A. Not as I sit here. I -- I haven't
14 reviewed that.

15 The determination of the specific delay, 11:37:55
16 the claims require that there be a predetermined
17 delay. I don't -- I'd have to review all of them.
18 Maybe some of the independent claims further narrow
19 it down, but I don't think that they required there
20 to be a predetermined delay with an exact 11:38:14
21 particular value or calculation.

22 Q. And to be clear, I didn't say
23 "predetermined." I said "determined." So in other
24 words, it could be determined on the fly as opposed
25 to just picking some predetermined delay. 11:38:30



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yeah. Understood. Yeah. 11:38:34

2 Q. Does the '506 patent teach how to
3 determine a delay that is then later used to delay
4 the DQS strobe signal as shown in Figures 12B?

5 MR. LINDSAY: Objection. Form. 11:39:01

6 THE DEPONENT: I -- sure. In 12B, it
7 teaches that it can be one time period.

8 Q. (By Mr. Chandler) And how does the '506
9 patent teach that you would determine that the
10 delay should be one time period rather than another 11:39:21
11 amount, such as two or three time periods?

12 A. It shows it right there. So it -- it
13 teaches that, in this case, it has determined that
14 the delay should be one time period.

15 Q. And what was the basis, according to the 11:39:39
16 '506 patent, for determining that the delay should
17 be one time period? Not that the delay that's
18 actually applied as shown in Figure 12B is one time
19 period, but that beforehand you've determined,
20 okay, I want to delay the strobe period, and I've 11:39:56
21 determined that the proper amount is one time
22 period. How is that taught by the '506 patent?

23 MR. LINDSAY: Objection. Form.

24 THE DEPONENT: To be honest with you, as
25 we sit here, I -- I don't recall. I don't recall 11:40:10



800.211.DEPO (3376)
EsquireSolutions.com

1 that being an issue that Mr. Wedig specifically was 11:40:14
2 addressing.

3 He did bring up a calculation for the
4 delay in the context of some of the prior art, and
5 I did respond to that. But I -- I don't recall 11:40:26
6 commenting on it or specifically searching out what
7 does it talk about for how the delay can be
8 calculated.

9 Q. (By Mr. Chandler) You have Dr. Wedig's
10 declaration marked as Exhibit 1003 in front of you, 11:40:46
11 correct?

12 A. I can bring it up, yes.

13 Q. And on pages 17, 18 and 19 of Dr. Wedig's
14 declaration marked as Exhibit 1003, he discussed
15 Figures 12A and 12B of the '506 patent, correct? 11:41:05

16 A. Yes, I see that.

17 Q. And you reviewed Dr. Wedig's declaration
18 in preparation for today's deposition, correct?

19 A. I did.

20 Q. Does that refresh your recollection as to 11:41:22
21 how the '506 patent teaches determining how to
22 delay the strobe signal DQS in Figure 12B?

23 A. Yes, he appears to be completely
24 consistent with what I just testified.

25 Q. All right. So explain to me, how does 11:41:43



800.211.DEPO (3376)
EsquireSolutions.com

1 Figure 12A and 12B together teach how much of a 11:41:46
2 delay should be applied to the DQS strobe signal in
3 Figure 12B?

4 MR. LINDSAY: Objection. Asked and
5 answered. 11:42:03

6 THE DEPONENT: It teaches that it should
7 be one clock cycle. As Dr. Wedig says, Figure 12A,
8 shows that the data buffer determines a time
9 interval based on reception of the signals. So
10 the -- the figures for 12A are teaching that. 11:42:18

11 Q. (By Mr. Chandler) Okay. And the
12 one-clock-cycle time interval is between where and
13 where in Figure 12A?

14 A. It's between t8 and t9.

15 Q. No. In Figure 12A, is what we are 11:42:38
16 talking about.

17 A. Oh, yes, but the delay is shown in 12B.

18 Q. Yes.

19 But I thought you just said that
20 Dr. Wedig indicated a delay is determined in 11:42:46
21 Figure 12A.

22 A. I -- I meant to say Figure 12. I thought
23 that's what I said, but -- which covers 12A and
24 12B.

25 I think he said Figure 12 as well. Oh, 11:43:01



800.211.DEPO (3376)
EsquireSolutions.com

1 no, he says 12A. Okay. Yeah. Yeah. 11:43:06

2 So I said Figure 12. I was referring to
3 both of them.

4 Q. So I'm still a little confused.

5 What's your testimony as to how 11:43:20

6 Figures 12A and 12B teach coming up with the --
7 with the one-clock-cycle delay for the DQS strobe
8 shown in Figure 12B?

9 MR. LINDSAY: Objection. Form. Asked
10 and answered. 11:43:38

11 THE DEPONENT: Yeah, as I said before,
12 Figure 12B teaches that, in this example, the delay
13 should be one clock period, the period from t8 to
14 t9.

15 Q. (By Mr. Chandler) So it's only the t8 to 11:43:54
16 t9 that's relevant to determining the delay
17 according to the '506 patent; is that correct?

18 A. I -- I wouldn't say that. We're focusing
19 on the two figures, but you have to take the
20 discussion around the figures, the context, into 11:44:17
21 account.

22 I haven't memorized it. I don't recall
23 if there's a greater explanation of why, in this
24 particular case, that particular time is the delay
25 that should be used above and beyond it being shown 11:44:32



800.211.DEPO (3376)
EsquireSolutions.com

1 in the figure itself. 11:44:35

2 Q. Do you disagree with any part of
3 Dr. Wedig's summary of Figures 12A and 12B on
4 pages 17, 18 and 19 of this declaration marked as
5 Exhibit 1003? 11:44:48

6 A. Perhaps. If I thought -- if I saw a
7 disagreement, and I thought a disagreement was
8 relevant and worth commenting on, I likely would
9 have said that in my declaration. But, you know,
10 as I sit here, I haven't -- I certainly haven't 11:45:04
11 memorized those pages of exactly what he said and
12 where the particular points that I had disagreed
13 with occur in his declaration.

14 Q. And to be clear, I didn't see any
15 disagreement in your declaration with Dr. Wedig's 11:45:17
16 discussion of Figures 12A and 12B. So sitting here
17 today, do you recall any disagreement that you have
18 or had with Dr. Wedig's analysis of Figures 12A and
19 12B?

20 A. No, I don't recall any particular 11:45:33
21 disagreement. But it's slightly over 100 pages, my
22 declaration. And if it's in there, I simply don't
23 recall it at the moment and would be happy to
24 review if there was a particular section you wanted
25 to point me to. 11:45:47



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Could you look at Figures 14 through 16 11:45:53
2 of the '506 patent marked as Exhibit 1001.

3 And just let me know when you have those
4 in front of you.

5 A. Yes, I'm there. 11:46:12

6 Q. Do you Figures 14 through 16 in the '506
7 patent illustrate an exemplary embodiment of the
8 claimed inventions of the '506 patent, in your
9 opinion?

10 A. I would have to go back and review how 11:46:23
11 they are discussed, but I would certainly expect
12 that they do.

13 Q. All right. And do you understand
14 Figures 14 through 16 of the '506 patent?

15 A. I have an understanding of them, yes. It 11:46:35
16 may simply be the case that these are illustrating
17 parts of an embodiment without illustrating other
18 aspects. I don't recall.

19 Q. What's the relationship between Figure 14
20 and Figure 15 of the '506 patent? 11:46:50

21 So Figure 14 in the bottom right is
22 numbered 320/620; and then Figure 15 is numbered
23 620 in the bottom right.

24 Do you see that?

25 A. Yes, I see that. 11:47:06



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. All right. So what's your understanding 11:47:09
2 of the relationship between Figures 14 and 15 of
3 the '506 patent?

4 A. So Figure 14 is a diagram illustrating a 11:47:32
5 DQ or DQS routing circuit in a data buffer
6 according to an embodiment, whereas 15 is a diagram
7 illustrating a DQS routing circuit having a delay
8 circuit in a data buffer according to an
9 embodiment. That's how they describe the
10 relationship between them. 11:47:51

11 Q. And what is the relationship between
12 Figure 14, which is numbered 320/620 in the bottom
13 right, and Figure 16, which is numbered 320 in the
14 bottom right?

15 A. Well, the inventors say Figure 16 is a 11:48:04
16 diagram illustrating a DQ routing circuit having a
17 delay circuit in a data buffer according to an
18 embodiment.

19 Q. In Figure 15 of '506 patent, do you see
20 that on the right side, there is a line labeled "YB 11:48:23
21 DQS"?

22 A. Yes, I see that.

23 Q. Using Figure 15 of the '506 patent, can
24 you explain to me the path taken by DQS strobe
25 signal in the read direction starting at YB DQS, 11:48:49



800.211.DEPO (3376)
EsquireSolutions.com

1 and can you sort of briefly explain what happens at 11:48:57
2 each step of the way.

3 MR. LINDSAY: Objection to form.

4 THE DEPONENT: Yeah, I -- I can talk
5 through the path. There are a number of elements 11:49:08
6 here whose function are not clearly labeled. But I
7 will do my best to explain what is visible on
8 Figure 15 and that I recall.

9 So YB DQS comes into 620. It's received
10 on the right-hand side. It passes through this 11:49:24
11 block, which is labeled "1502B." I don't recall
12 exactly what that does.

13 That line then goes down, and it's
14 connected to the output of a tri-state buffer as
15 well as the input to what's called a multiplexor, 11:49:45
16 or a MUX, that's labeled "1550." And that
17 multiplexer is used to select either YB DQS or YA
18 DQS.

19 That's then fed into Figure 1560 -- or
20 element 1560, which also takes in a data strobe 11:50:11
21 signal and a clock.

22 Then it's forwarded on to 1570. And the
23 output of 1570 goes through, again, another
24 tri-state buffer, 1580, and is sent through 1501
25 and then produced as DQS. 11:50:35



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) And the output of 1570 11:50:42
2 also goes up to RDQS, correct?

3 A. It does also do that, yes.

4 Q. And I think you said DS -- the line at
5 the bottom of the Figure 15 is a data strobe. I am 11:51:01
6 not sure that's correct.

7 A. It is labeled "DS." Hopefully what I
8 said is I believe that's a data strobe, but I'm not
9 sure. Like I said, I haven't gone back and
10 reviewed the specific figures that closely. 11:51:17

11 Q. All right. What does 1502B do?

12 A. Figure 15 -- just a moment.

13 So the patent says in the read strobe
14 path, a select circuit 1550, which is the
15 multiplexer we talked about, selects either a read 11:52:55
16 strobe signal via DQS pin 1502A, or a read strobe
17 signal based on DQS pin 1502B.

18 So they are indicating that those are
19 pins on a package.

20 Q. Okay. And I think you said 1550 is the 11:53:18
21 multiplexer, correct?

22 A. Yes.

23 Q. And if you look at the top of column 11,
24 line 1, I think it says "DS" is a delay signal; is
25 that fair? 11:53:36



800.211.DEPO (3376)
EsquireSolutions.com

1 In other words, not a -- not a strobe, 11:53:39
2 but it calls it "a delay signal DS."

3 A. Yeah, I assume so. Yep, it's --

4 Q. It's line --

5 A. It says "a delay signal DS." That's 11:53:50
6 correct. Thank you for reorienting me there.

7 Q. All right. So what does 1560 in
8 Figures 15 do?

9 A. So what it -- so the selected read strobe
10 is delayed by a delay circuit 1560. So that is the 11:54:15
11 circuit that delays that signal, the -- the read
12 strobe signal that was selected between the A and
13 the B path.

14 Q. And what is this vertical line CK0?

15 A. Sorry. I need to go back to that page. 11:54:47
16 So that appears to be being used to clock
17 element 1520.

18 Q. I'm referring to CK0 that goes into 1560,
19 along with DS that goes into 1560.

20 Do you see that? 11:55:23

21 A. Did I read off the wrong part? Let me
22 see.

23 I see. Thank you.

24 Yeah, vertically it goes 1520. It does
25 also go into 1560, yeah. 11:55:38



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Okay. So what is CK0? 11:55:40

2 A. CK0 is a signal that's being used to
3 clock those two, those two box. It's a
4 reconstructed clock -- or regenerated clock.

5 Q. All right. So what are the signals CK0 11:56:01
6 and DS going into 1560 doing?

7 A. They're being used to clock those
8 elements, to control those elements.

9 Q. And which element are you referring to?

10 A. The -- the two elements it goes into, the 11:56:46
11 two buffers. It only goes into two elements.

12 Q. I think I may have confused you. So I'm
13 focusing on 1560 in Figures 15.

14 Do you see that?

15 A. Yep. 11:57:00

16 Q. And then coming into 1560, there are, I
17 guess, two signals, labeled "CK0" and the other is
18 labeled "DS," for delay signal, correct?

19 A. Yes.

20 Q. How do the signals CK0, the clock signal, 11:57:18
21 and the DS, the delay signal, affect 1560?

22 A. Well, the delay signal indicates a -- an
23 amount for delay that should be applied. And the
24 clock signal, I believe, indicates when to clock
25 that device 1560. 11:57:46



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. And what do you mean by "clock that 11:57:51
2 device 1560"?

3 A. Well, as we talked about before, most
4 digital circuits are called "synchronous," so their
5 state or their registers only get updated on a 11:58:04
6 clock edge. And that's typically what clocks are
7 used for. So it's updating the state of 1560.

8 Q. Okay. And what's the label for 1560?
9 How does the patent describe it?

10 A. Just a moment. They call it a delay 11:58:43
11 circuit.

12 MR. CHANDLER: Do you need to take your
13 phone call?

14 THE DEPONENT: I do. Thank you very
15 much. I completely lost time. And you warned me 11:58:52
16 that you might, but thank you for not.

17 MR. CHANDLER: But to be clear, I mean,
18 should we stop now, or are you waiting for someone
19 to call you such that we should keep going?

20 THE DEPONENT: No, I need to get onto -- 11:59:02
21 I need to jump onto a Zoom call.

22 MR. CHANDLER: And how long will that be?

23 THE DEPONENT: Probably half an hour.
24 Yeah, I don't think it's going to go any longer. I
25 won't go any longer. Let's put it that way. 11:59:12



800.211.DEPO (3376)
EsquireSolutions.com

1 MR. CHANDLER: Okay. Well, let's take a 11:59:15
2 break then and -- until 12:45. And we can -- is
3 that enough time for you to do your call and get
4 lunch?

5 MR. LINDSAY: Well, yeah, we can go off 11:59:24
6 the record and talk about that off --

7 MR. CHANDLER: Yeah.

8 THE VIDEOGRAPHER: We're going off the
9 record. The time is 11:59.

10 (Recess taken.) 11:59:37

11 THE VIDEOGRAPHER: We're going back on
12 the record. The time is 1:04.

13 Q. (By Mr. Chandler) Welcome back,
14 Dr. Mangione-Smith.

15 Do you have any corrections or 01:04:16
16 clarifications that you would like to make to your
17 testimony from before lunch, or are you ready to
18 proceed?

19 A. I am ready to proceed.

20 Q. So we were discussing Figure 15 of the 01:04:31
21 '506 patent. Do you still have that up in front of
22 you?

23 A. In just a moment. Okay. Yep.

24 Q. And we were discussing the path that the
25 DQS strobe signal takes in the redirection from 01:04:49



800.211.DEPO (3376)
EsquireSolutions.com

1 right to left. And in Figure 15, I think we left 01:04:51
2 off at box 1560. And I wanted to pick up from
3 there.

4 Is that all right?

5 A. Sure. 01:05:11

6 Q. Okay. So what happens after box 1560?

7 A. So then it enters box 1570, which is
8 described as a sampler circuit.

9 Q. Okay. And what does the sampler circuit
10 1570 in Figure 15 of the '506 patent do? 01:05:29

11 A. It samples that input.

12 Q. And "that input" being the -- the DQS --
13 (Simultaneously speaking.)

14 THE DEPONENT: Yeah. The delayed DQS.

15 Q. (By Mr. Chandler) All right. And what 01:05:51
16 does the clock signal CK0 going into the sampler
17 circuit 1570 do?

18 MR. LINDSAY: Objection --

19 THE DEPONENT: Well --

20 MR. LINDSAY: Objection. Form. 01:06:04

21 THE DEPONENT: Well, in column 15, it
22 says that the sampler circuit 1570 samples
23 according to the buffered module clock signal CK0.

24 Q. (By Mr. Chandler) So does the clock
25 signal CK0 cause sampler circuit 1570 to sample the 01:06:26



800.211.DEPO (3376)
EsquireSolutions.com

1 stroke signal? 01:06:32

2 A. That appears to be what it's indicating,
3 yes.

4 Q. And how does it -- that work?

5 A. When the buffered clock signal is 01:06:47
6 transitioned, 1570 samples its -- its input.

7 Q. And then what happens?

8 MR. LINDSAY: Objection. Form.

9 THE DEPONENT: So then it gets -- then
10 the output of 1570 gets passed to 1580, which is a 01:07:13
11 tri-state buffer.

12 Q. (By Mr. Chandler) And as I think we
13 discussed, I guess it also goes up to RDQS,
14 correct?

15 A. That's correct. 01:07:28

16 Q. And at 11, column 11, line 1, RDQS is the
17 read DQS strobe; is that the way it's described?

18 A. Yes, that's the label it's given.

19 Q. And is that a delayed strobe?

20 A. I believe it's delayed with the value of 01:08:01
21 DS.

22 Q. Okay. And then after tri-state buffer
23 1580, what happens next in Figure 15 of the '506
24 patent?

25 A. So next, it goes to element 1501, which I 01:08:16



800.211.DEPO (3376)
EsquireSolutions.com

1 believe is just, again, another pin output. But -- 01:08:19
2 but I will check for sure.

3 Yes, it's a pin.

4 Q. Okay. Could you turn to Figure 16 of the 01:08:39
5 '506 patent.

6 And let me know when you're there.

7 A. Okay.

8 Q. Using Figure 16 of the '506 patent, can
9 you explain the path taken by DQ data signal in the
10 read direction starting at the YB line on the right 01:08:59
11 side. And briefly explain what happens at each
12 step of the way, and -- and also pause at each step
13 of the way because I may have questions.

14 A. Sure. So the YB signal is input -- is
15 provided to pin 1602B. 01:09:26

16 Q. And to be clear, that's a DQ data signal;
17 is that fair?

18 A. Let me go back -- I -- I haven't reviewed
19 this in quite some time -- and see.

20 So Figure 16 is a diagram illustrating a 01:09:58
21 DQ routing circuit having a delay circuit in a data
22 buffer according to an embodiment. So yes, it
23 should be a DQ data signal.

24 Q. Okay. So after the data signal comes in
25 on line YB into 1602B, the pin, what happens next? 01:10:14



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Then it's connected to the output of the 01:10:22
2 tri-state buffer 1630B as well as input to a
3 multiplexer 1650.

4 Q. Okay. What does the multiplexer 1650 do
5 in Figure 16? 01:10:40

6 A. It multiplexes between the two input --
7 possible input signals YA and YB.

8 Q. Okay. So we're assuming YB gets selected
9 in this example. So what happens next after
10 multiplexer 1650 selects the DQ data signal from 01:11:03
11 YB?

12 A. Then it gets passed to element 1660.

13 Q. And what does 1660 do with the DQ data
14 signal?

15 A. 1660 is a delay circuit that includes a 01:11:26
16 set of delay stages.

17 Q. And what does the CK0 clock signal and DS
18 delay signal going into 1660 do?

19 A. Well, as best I recall, the DS, the delay
20 signal, delays the input, the YB values. And then 01:12:02
21 once they pass through that delay, they are clocked
22 when CK0 is asserted.

23 Q. All right. And what happens next in
24 Figure 16 of the '506 patent after the DQ data
25 signal comes out of 1660? 01:12:22



800.211.DEPO (3376)
EsquireSolutions.com

1 A. So after that, it goes to element 1670. 01:12:42

2 Q. And what is element 1670?

3 A. So that's characterized in column 17 as a
4 receiver circuit.

5 Q. And when I searched for it, I actually 01:13:18
6 came up with a different description. Is there
7 another description of 1670 in the '506 patent?

8 A. I don't see one.

9 Q. The first hit that comes up when I
10 searched is, I guess, column 18, line 4. 01:13:50

11 A. Sure. It's referenced there, yeah.

12 Q. So is 1670 a sampler circuit, or a
13 receiver circuit, or both or neither?

14 MR. LINDSAY: Objection. Form.

15 THE DEPONENT: So it is referred to 01:14:20
16 clearly as a receiver circuit, column 18. And it
17 says that it refers to the sampler circuit 1570 or
18 1670. So 1570 is a sampler circuit. 1670, as I
19 read this, is a receiver circuit.

20 Q. (By Mr. Chandler) Okay. What does the 01:14:40
21 receiver circuit 1670 do?

22 A. It receives the input and samples it.

23 Q. And what does the delay read strobe
24 signal RDQS going into 1670 do?

25 A. It controls when that -- when those 01:15:06



800.211.DEPO (3376)
EsquireSolutions.com

1 signals are sampled. 01:15:12

2 Q. And how does that work?

3 MR. LINDSAY: Objection. Form.

4 THE DEPONENT: I am not following you.

5 In principal, it could work in a number of 01:15:26

6 different ways. It's used to strobe, presumably,

7 those values.

8 Q. (By Mr. Chandler) And what do you mean
9 by the RDQS is used to strobe those values? What
10 values are you referring to, and what do you mean
11 by the verb "strobe"? 01:15:48

12 MR. LINDSAY: Objection. Form.

13 THE DEPONENT: The values are the input
14 values that proceeded from the far right where we
15 started the conversation. And I believe it's YB, 01:16:03

16 but I'm looking at the figure right now. And

17 "strobe" is the action generally taken as a

18 consequence of receiving a strobe signal. It

19 causes a sampling to happen.

20 Q. (By Mr. Chandler) Now, the RDQS signal 01:16:30
21 coming into Figure 16 was delayed by Figure 15,
22 right?

23 MR. LINDSAY: Objection. Form.

24 THE DEPONENT: They do both refer to

25 RDQS. It could be the case that's what is delayed 01:16:45



800.211.DEPO (3376)
EsquireSolutions.com

1 from Figure 15. I haven't put the two of them 01:16:49
2 together in quite sometime.

3 Q. (By Mr. Chandler) Does the delay to the
4 RDQS strobe signal delay the DQ data signal in
5 Figure 16? 01:17:15

6 A. Well, the -- the RDQS signal does cause
7 1670 to sample the -- the delayed input values,
8 yeah.

9 Q. And then what does 1670 do after that?

10 A. So after that, let's go back to 01:17:55
11 Figure 16. After that, the output goes to a
12 tri-state buffer 1680. And then the output of that
13 buffer, if it's activated, goes to 1601, which is a
14 pin.

15 Q. And what causes 1670 to output the data? 01:18:23

16 MR. LINDSAY: Objection. Form.

17 THE DEPONENT: I -- I guess I don't know
18 for sure. It indicates that the -- that there is
19 an output that flows to 1680. I don't recall that
20 there was much discussion beyond it samples the 01:18:50
21 input. Yeah.

22 MR. CHANDLER: Let me mark an exhibit.

23 (Exhibit 1048 was marked for
24 identification by the Court Reporter and is
25 attached hereto.) 01:19:09



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) All right. You should 01:19:14
2 be getting Exhibit 1048.

3 And once you open that up, let me know
4 when you have it.

5 A. Okay. I have it. 01:19:38

6 Q. All right. So Exhibit 1048 is Figures 15
7 and 16 of the '506 patent marked as Exhibit 1001,
8 annotated with some color arrows. There's a dashed
9 orange arrow at the bottom for DQS. There's a
10 solid orange arrow at the top for DQ going through 01:19:58
11 Figure 16. And then there's the blue arrow for
12 RDQS going up from Figure 15 into Figure 16.

13 Do you see all that?

14 A. Yes.

15 MR. LINDSAY: Objection. Foundation. 01:20:20
16 Beyond the scope of direct.

17 Q. (By Mr. Chandler) When the DQ data
18 signal comes out of the left side of Figure 16 on
19 line 322, is it edge-aligned with the DQS strobe
20 signal coming out of the left side of Figure 15 on 01:20:39
21 line 324?

22 MR. LINDSAY: Objection. Foundation.
23 Beyond the scope of direct.

24 Q. (By Mr. Chandler) And this is also --
25 and you can also look at Figure 14. I don't want 01:20:55



800.211.DEPO (3376)
EsquireSolutions.com

1 to limit you to Exhibit 1048. Feel free to, 01:20:59
2 you know, look at Figure 14 or other figures as
3 well, if it's helpful.

4 A. Yeah. So it might be; it might not be.

5 Q. And why do you say that? 01:21:17

6 A. Because when -- when we started talking
7 about RDQS, I said that I hadn't reviewed how 15
8 and 16 go together. They both do say RDQS. I
9 don't know that that's -- I don't recall that
10 that's the same signal. It might be. 01:21:39

11 Then there's also the issue of, in my
12 mind, what does "edge-aligned" mean. There has to
13 be some degree of closeness for something to be
14 aligned or not. They're never going to be
15 perfectly aligned, I guess is what I'm trying to -- 01:22:00
16 trying to speak to.

17 Q. Okay. So it would be fair to say that,
18 in your opinion, DQ data signal and DQS strobe
19 signal will not always be aligned with each other?

20 MR. LINDSAY: Objection. Foundation. 01:22:18
21 Beyond the scope of direct.

22 THE DEPONENT: It depends on the -- on
23 the situation. I think that depending on how it's
24 implemented and what the -- what's the word I'm
25 looking for -- the -- the -- how tight the timing 01:22:34



800.211.DEPO (3376)
EsquireSolutions.com

1 parameters are, if these are implemented 01:22:38
2 together -- if -- one could determine that they are
3 aligned or that they are not aligned.

4 Q. (By Mr. Chandler) And what do you
5 believe the '506 patent teaches, after your -- 01:22:48
6 after your --

7 MR. LINDSAY: Objection.

8 Q. (By Mr. Chandler) -- review?

9 MR. LINDSAY: Form.

10 THE DEPONENT: I think the '506 patent 01:23:00
11 teaches the inventions in the claims.

12 Q. (By Mr. Chandler) A little different --
13 that wasn't quite my question.

14 My question was, what do you believe the
15 '506 patent teaches with respect to whether the DQ 01:23:14
16 data signal coming out of Figure 16 and also
17 Figure 14 -- whether or not it's aligned with the
18 DQS strobe signal coming out of Figure 15, also
19 shown as coming out of Figure 14?

20 MR. LINDSAY: Objection. Form. 01:23:37

21 THE DEPONENT: I -- I don't recall. If
22 there's something in particular in the '506 you
23 want to point me to. I don't recall if they said
24 that it's intended to be edge-aligned or not.

25 Q. (By Mr. Chandler) So I'm a little 01:23:55



800.211.DEPO (3376)
EsquireSolutions.com

1 confused by your testimony in your declaration. At 01:23:56
2 some points, you and your declaration seem to
3 insist that DQ and DQS will always be edge-aligned.
4 At other times, you say, as you just said now,
5 "Well, it depends. They may not be edge-aligned." 01:24:12
6 So I'm trying to get your best testimony
7 on this issue.
8 MR. LINDSAY: Objection. Form.
9 THE DEPONENT: Would you like to point me
10 to where in my report I discuss that? I'd be happy 01:24:24
11 to refresh my memory.
12 Q. (By Mr. Chandler) Well, I think it's
13 referred to probably over 20 times.
14 A. Pardon me?
15 Q. I think it's referred to in your report 01:24:39
16 over probably 20 times.
17 So I'm a little confused about what your
18 testimony is.
19 MR. LINDSAY: Is there a question
20 pending, Counsel? 01:25:09
21 MR. CHANDLER: It's the same question
22 I've been asking a few times about --
23 THE DEPONENT: I'm not seeing any
24 reference to Figure 16 in my report.
25 Q. (By Mr. Chandler) Correct. 01:25:25



800.211.DEPO (3376)
EsquireSolutions.com

1 You refer to DQ and DQS in your report, 01:25:25
2 which is shown in Figure 15 and Figure 16. So
3 that's what I'm trying to understand is, how would
4 a person of ordinary skill in the art reading the
5 '506 patent, in your opinion, understand whether or 01:25:44
6 not the DQ data signal and the DQS strobe signal
7 shown in Figures 15 and 16, as well as Figure 14,
8 whether or not those two signals are in line with
9 each other.

10 MR. LINDSAY: Objection. Form. 01:26:04

11 THE DEPONENT: One would read the patent
12 in detail and see if it specifies that. These are,
13 I think we've agreed -- I think the phrase you used
14 "exemplary embodiments." These are embodiments of
15 at least aspects of the claim. 01:26:27

16 As I said, I don't recall if the patent
17 specifically said 15 and 16 go together. They very
18 well might. I'm not seeing a reference to
19 Figure 16 either.

20 So you're asking me details about a 01:26:44
21 figure -- two figures that may go together or may
22 not, may be embodiments that go together.
23 Oftentimes, embodiments or parts of embodiments
24 don't go together. That, as far as I can tell,
25 didn't come up in my declaration or Wedig's, which 01:27:04



800.211.DEPO (3376)
EsquireSolutions.com

1 is what I focused on.

01:27:08

2 And -- and in some cases, the signals
3 are -- the DQ and DQS are intended to be
4 edge-aligned; and in some cases, they are not
5 intended to be edge-aligned.

01:27:23

6 Q. (By Mr. Chandler) And in other cases,
7 they could become misaligned, correct?

8 A. If -- if by "misaligned" you mean out of
9 alignment to such a degree that the system fails to
10 work, sure. Any -- any electrical system has
11 operating limitations, yeah.

01:27:37

12 Q. And including Figure 15 and 16 in the
13 '506 patent; is that fair enough?

14 MR. LINDSAY: Objection. Form.

15 THE DEPONENT: That's underspecified. I
16 mean, presumably, if one were to build those
17 circuits, they would have some maximal clock speed
18 that they could operate at. And if you tried to
19 operate them at twice that clock speed, they would
20 fail. Or they'd have some maximal voltage that
21 they could operate at. If you tried to operate
22 them at twice that voltage, they would likely fail.

01:27:57

01:28:13

23 Q. (By Mr. Chandler) Turn to Figure 10A in
24 the '506 patent.

25 Let me know when you're there.

01:28:33



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Okay. I'm there. 01:28:35
2 Q. And you see in upper left, there's 910?
3 A. You said Figure 10. You meant -- you
4 said 10A or...
5 Q. Yes. 01:29:04
6 A. Okay. I was on 10D. Yes, I see 910.
7 Q. All right. What is 910 in the '506
8 patent?
9 A. 910 is illustrating this circuit,
10 Figure 10A. 01:29:22
11 Q. And how does the '506 patent describe
12 what 910 is?
13 A. It says, "In an embodiment, a receiver
14 circuit includes a metastability detection circuit
15 (MDC)" [as read], labeled "910." 01:29:49
16 Q. Okay. And what is 1042 in Figure 10A?
17 A. It says that "MDC910 includes a sampler
18 circuit 1042." [as read]
19 Q. And what does the sampler circuit 1042
20 take as its inputs? 01:30:27
21 A. It says it "samples MCS1 according to CK0
22 and outputs a sampled result A."
23 Q. And what is MSC1 and what is CK0?
24 A. Well, MCS1 is the output from multiplexer
25 1071 and CK0 is the output from multiplexor 1072. 01:31:25



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. But what is MCS1? What kind of signal is 01:31:31
2 that?
3 A. It's the output of the multiplexor 1071.
4 Q. Is MCS1 a module control signal?
5 A. I don't recall. I haven't -- yeah, it 01:31:57
6 could be.
7 Q. You read the patent carefully, right?
8 A. Yes, that's correct.
9 Q. Column 12, line 13.
10 A. Yes, I see it. 01:32:34
11 Q. So what is MCS1 going into 1042?
12 A. 1042 is a sampler circuit "that samples
13 MCS1 according to CK0."
14 I thought we just talked about that,
15 but -- but that's how it's characterized. 01:33:09
16 Q. All right. So what happens when the
17 clock signal CK0 goes to the sampler circuit 1042?
18 A. It's used as an input to 1042 in order to
19 control sampling of MCS1.
20 Q. And what does sampler circuit 1042 do 01:33:41
21 next?
22 A. It "outputs a sampled result A to sampler
23 circuit 1044." [as read]
24 Oh, no. Hold on a second.
25 Yeah, it "outputs a sampled result A." 01:34:12



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Not to 1044 but to 1050, right? 01:34:16

2 A. Give me a moment.

3 Yes, that's correct.

4 Q. And so what is "metastability," and what
5 is this metastability detection circuit 910 01:34:40
6 accomplishing?

7 MR. LINDSAY: Objection. Outside the
8 scope of direct. Form.

9 THE DEPONENT: Metastability is a problem
10 that occurs within latches or flip-flops of digital 01:34:51
11 circuits that can cause a value to be -- well, it
12 causes misoperation, malfunction of the latch of
13 the register of the flip-flop.

14 Q. (By Mr. Chandler) And why? Why is there
15 a misoperation? 01:35:18

16 MR. LINDSAY: Objection. Form. Outside
17 the scope of direct.

18 THE DEPONENT: Metastability happens when
19 an input value changes at an unfortunate point in
20 time such that its value cannot be reliably 01:35:34
21 sampled.

22 Q. (By Mr. Chandler) Could you look at
23 Figure 7 of the '506 patent marked as Exhibit 1001.

24 Let me know when you're there.

25 A. Sure. I'm there. 01:35:53



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Figure 7 shows module control circuit 116 01:35:54
2 on the left side, correct?

3 A. Yes.

4 Q. And then coming out of the module control
5 circuit are two signals labeled "MCS" for module 01:36:10
6 control signal and "CK" for clock, correct?

7 MR. LINDSAY: Objection. Form.

8 THE DEPONENT: Yes, MCS, and then a
9 complementary clock, CK and CK bar.

10 Q. (By Mr. Chandler) All right. And take a 01:36:30
11 look at column 12 of the '506 patent marked as
12 Exhibit 1001, lines 51 through 62.

13 Does the '506 patent indicate that the
14 MCS signal and the CK clock signal can become
15 misaligned? As shown, for example, in Figure 8. 01:37:03

16 A. I'm still reading that longish passage.
17 So they -- they suggest that the
18 alignment can change and they cannot be perfectly
19 aligned. I'm not sure if they're -- I don't think
20 they are using the -- I didn't see the phrase 01:37:48
21 "misaligned," and I sort of talked about that
22 before.

23 I would be inclined to think "misaligned"
24 means so much out of alignment that things won't
25 work. 01:38:03



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Figure 8 shows that the module control 01:38:06
2 signal MCS and the clock signal CK can become
3 misaligned such that the result is metastability,
4 correct?

5 MR. LINDSAY: Objection. Outside the 01:38:31
6 scope of direct.

7 THE DEPONENT: I wouldn't say that, and
8 I -- I don't recall either me or Dr. Wedig
9 commenting on this. I haven't looked at this in
10 quite some time. 01:38:43

11 Q. (By Mr. Chandler) Column 12, lines 51
12 through 62, teach that the alignment of the CK
13 clock signal and the MCS module control signal can
14 be shifted to such an extent that the result, as
15 shown at the bottom of Figure 8, can be 01:39:08
16 metastability, correct?

17 MR. LINDSAY: Objection. Outside the
18 scope of direct.

19 THE DEPONENT: You said you were back at
20 column 12, right, 51 through 60-something? 01:39:35

21 Q. (By Mr. Chandler) 62. I mean, it -- you
22 can carry it over to the top of column 13 if you
23 want.

24 A. Yes, I see that. It says "that the
25 sampled results could be metastable." 01:40:16



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. And the reason the sampled results would 01:40:20
2 be metastable is because the CK clock signal and
3 the MCS module control signal are so far out of
4 alignment that the result is metastability?

5 MR. LINDSAY: Objection. Form. 01:40:40

6 THE DEPONENT: Yeah. If the necessary
7 setup and hold times are not adhered to,
8 metastability can be a result.

9 Q. (By Mr. Chandler) And in Figure 8, how
10 far off is the alignment between the clock signal 01:40:53
11 CK and the module control signal as shown at 840,
12 approximately?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE DEPONENT: It's hard to say, because 01:41:31
16 it's not clear if they're -- if the alignment is
17 supposed to be going to the left or to the right.
18 They're -- they do not -- the transition of those
19 signals does not appear to be aligned.

20 Q. (By Mr. Chandler) Well, in Figure 8 at 01:41:53
21 row 810, the clock signal and the module control
22 signal is perfectly aligned, correct?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct. Form.

25 THE DEPONENT: I think they're trying to 01:42:07



800.211.DEPO (3376)
EsquireSolutions.com

1 illustrate that, sure. I mean, nothing is ever 01:42:09
2 perfectly aligned, but I think that's the principle
3 they are trying to illustrate.

4 Q. (By Mr. Chandler) But, I mean, that's
5 the phrase they use, correct, is "perfectly 01:42:18
6 aligned," at line 52 of column 12?

7 MR. LINDSAY: Objection. Outside the
8 scope.

9 THE DEPONENT: I thought -- I thought you
10 asked me if they were perfectly aligned, not if 01:42:30
11 they used the phrase "perfectly aligned."

12 Q. (By Mr. Chandler) The '506 patent
13 teaches in Figure 8 that the clock signal and the
14 module control signal are "perfectly aligned" at
15 row 810, correct? 01:42:47

16 MR. LINDSAY: Objection. Outside the
17 scope.

18 THE DEPONENT: I -- I believe it uses
19 that phrase, sure.

20 Q. (By Mr. Chandler) And then down at 840, 01:42:55
21 how far out of alignment in terms of clock cycles
22 is the CK signal and the module control signal MCS,
23 approximately?

24 MR. LINDSAY: Objection. Outside the
25 scope. Form. 01:43:14



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: I think we answered that 01:43:19
2 before. I answered that. You asked it before we
3 moved onto 1 -- to 810. Looking at that figure, I
4 think it's impossible to say.

5 Q. (By Mr. Chandler) And why do you say 01:43:34
6 "it's impossible to say"?

7 MR. LINDSAY: Objection. Outside the
8 scope.

9 THE DEPONENT: There's not enough
10 information on there to say how far out of 01:43:40
11 alignment they are.

12 Q. (By Mr. Chandler) But it's so far out of
13 alignment that it causes metastability, correct?

14 MR. LINDSAY: Objection. Outside the
15 scope. Form. 01:43:52

16 THE DEPONENT: The discussion says that
17 they're -- yes, the clock is rising in a
18 metastability region.

19 Q. (By Mr. Chandler) What causes or what
20 can cause the clock signal to become not aligned 01:44:10
21 with the module control signal MCS?

22 MR. LINDSAY: Objection. Form. Outside
23 the scope, if it's referring to the same figure.

24 THE DEPONENT: So they're assuming they
25 were effectively aligned at some point. They could 01:44:40



800.211.DEPO (3376)
EsquireSolutions.com

1 then become out of alignment by having either one 01:44:43
2 of them delayed or both of them delayed by an
3 unequal amount.

4 Q. (By Mr. Chandler) And what could cause
5 an unequal delay between those two signals? 01:45:04

6 MR. LINDSAY: Objection. Outside the
7 scope. Form.

8 THE DEPONENT: Presumably a difference in
9 electrical properties along the propagation path
10 for the signals. 01:45:21

11 Q. (By Mr. Chandler) Is it possible for two
12 signals that travel in parallel on a memory module
13 to become not aligned with each other as a result
14 of electrical properties along the propagation path
15 of those two signals? 01:45:58

16 A. Yes, it's possible.

17 Q. Is it possible for a DQ data signal and a
18 DQS strobe signal that travel in parallel on a
19 memory module to become not aligned with each other
20 as a result of electrical properties along the 01:46:26
21 propagation path of those two signals?

22 A. Well, given that I just talked about
23 signals in general and agreed that they could
24 become not aligned, and these are just particular
25 signals, yes. And any two signals following a 01:46:44



800.211.DEPO (3376)
EsquireSolutions.com

1 parallel path could become not -- that were 01:46:49
2 considered aligned at one point could become not
3 aligned at the end point.

4 Q. Could you look at your expert declaration
5 marked as Exhibit 2006. 01:47:09

6 Let me know when you have it in front of
7 you.

8 A. Okay.

9 Q. And go to page 58.

10 Let me know when you've got that in front
11 of you. 01:47:27

12 A. Okay.

13 Q. Okay. In paragraph 109 and 110 and
14 111 -- I think we discussed this briefly before --
15 you refer to the DDR1 standard, the DDR2 standard 01:47:42
16 and the DDR3 standard that came out in 2000, 2003
17 and 2007, respectively; is that right?

18 A. That sounds right.

19 Q. Did either the DDR1 standard or the DDR2
20 standard provide for read or write leveling? 01:48:02

21 A. I'm not sure. I thought the read
22 leveling came in at DDR3. But I -- I don't recall
23 for sure.

24 Q. Did the DDR3 standard provide for read
25 and write leveling? 01:48:25



800.211.DEPO (3376)
EsquireSolutions.com

1 A. I think it did. Yeah, I comment here 01:48:31
2 that it -- DDR3 provides leveling. I just don't
3 recall for sure if it provided both read and write.

4 Q. Why was leveling needed for the DDR3
5 standard? 01:48:58

6 A. Likely for many reasons. To get a
7 complete answer, you would have to ask members of
8 the committee. At least one part of it was the use
9 of what we've been referring to as fly-by
10 communications methods. 01:49:18

11 Q. But to be clear, I mean, fly-by
12 communication methods existed with the DDR1 and
13 DDR2 standard for things like RDIMMs, correct?

14 A. Correct.

15 MR. LINDSAY: Objection. Form. 01:49:33

16 THE DEPONENT: I don't remember that
17 there were RDIMMs for DDR1 and DDR2, and I'm not
18 suggesting that fly-by was something developed as
19 part of DDR3. But the use of that communications
20 pattern is one of the things that was addressed by
21 use of leveling techniques. 01:49:55

22 Q. (By Mr. Chandler) So how does read and
23 write leveling address issues related to fly-by
24 arrangements? What are you trying to get at with
25 that statement? 01:50:22



800.211.DEPO (3376)
EsquireSolutions.com

1 MR. LINDSAY: Objection. Form. 01:50:25

2 THE DEPONENT: So when there's a fly-by
3 communication structure, there's an order as a
4 sequence of components. In this case, SDRAM chips
5 that receive signals over a common communications 01:50:40
6 channel. So there's no register breaking it up.

7 And as we talked about, physical wires
8 have a propagation delay. As a consequence of
9 that, the signals will be received at some chips
10 before they're received at others. 01:51:01

11 And leveling is one technique -- one
12 aspect of leveling is accounting for possible
13 errors as a result of the timing of activation
14 between the nearest and the farthest element.

15 Q. (By Mr. Chandler) And so what does 01:51:26
16 leveling accomplish?

17 A. Well, one thing that it's designed to
18 accomplish in general is to avoid having an error
19 caused by the result of the use of -- pardon me --
20 the use of fly-by communications. 01:51:44

21 Q. And why would fly-by communications
22 result in an error, and how does leveling prevent
23 that error from happening?

24 MR. LINDSAY: Objection. Form.

25 THE DEPONENT: Well, fly-by 01:52:01



800.211.DEPO (3376)
EsquireSolutions.com

1 communications can introduce an error -- it doesn't 01:52:02
2 always -- as a result of different modules getting,
3 receiving, a signal at different points in time.

4 And leveling is a technique to try to undo the
5 problem -- the timing problems introduced by the 01:52:23
6 fly-by communications.

7 Q. (By Mr. Chandler) And so as a result of
8 leveling, what signals in particular get leveled
9 with each other?

10 A. It -- it depends. There's different ways 01:52:40
11 to do read leveling and write leveling in different
12 systems. It's in general an attempt to correct
13 the -- any possible errors or avoid errors that
14 could be because caused by the fly-by
15 communications. 01:52:57

16 Q. Can you look at the DDR3 standard marked
17 as Exhibit 1020. Let me know when you're there.

18 A. Okay. I got it open.

19 Q. Go to page 26 of Exhibit 1020.
20 Let me know when you're there. 01:53:15

21 A. Okay.

22 Q. Are you familiar with the MRS command,
23 the mode register set command, in the JEDEC
24 standard?

25 MR. LINDSAY: Objection. Outside the 01:53:43



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of direct. 01:53:43

2 THE DEPONENT: I -- I don't recall. Have
3 I reviewed this at some point? Likely, but I don't
4 recall "Mode Register 1," for example.

5 Q. (By Mr. Chandler) There is a command 01:54:05
6 JEDEC called the MRS, or mode register set, command
7 that sets various mode registers in the DDR memory
8 device; is that fair?

9 MR. LINDSAY: Objection. Outside the
10 scope of direct. Form. 01:54:23

11 THE DEPONENT: I -- I don't recall. I
12 haven't really looked at this specification in
13 detail with regards to this investigation. I mean,
14 if there's something in particular you want to
15 point me to, I'd be happy to review it. And, yeah, 01:54:41
16 this is presumably just for this specification as
17 opposed to, you know, all JEDEC SDRAM devices.

18 Q. (By Mr. Chandler) Sure.
19 So on page 33 of Exhibit 1020, you see
20 the first row is the command "Mode Register Set", 01:54:59
21 abbreviated "MRS"?

22 MR. LINDSAY: Objection. Outside the
23 scope.

24 THE DEPONENT: Yes, I see those words.

25 Q. (By Mr. Chandler) And then back on 01:55:11



800.211.DEPO (3376)
EsquireSolutions.com

1 page 26 of Exhibit 1020, one of the mode registers 01:55:14
2 set by the MRS command is labeled "A7, Write
3 leveling enable."

4 Do you see that?

5 MR. LINDSAY: Objection. Outside the 01:55:44
6 scope.

7 THE DEPONENT: I wouldn't say it that
8 way. But I do see that it appears that there's a
9 1-bit register, A7, labeled "write leveling
10 enable." 01:55:54

11 Q. (By Mr. Chandler) And the 1-bit
12 register, A7, labeled "write leveling enable" is
13 configured by the mode register set command, MRS,
14 correct?

15 MR. LINDSAY: Objection. Outside the 01:56:17
16 scope. Form.

17 THE DEPONENT: Could be.

18 Q. (By Mr. Chandler) And --

19 A. I haven't reviewed this anytime recently,
20 so... 01:56:28

21 Q. All right. So page 22 of Exhibit 1020 at
22 the top says that the four mode registers provided
23 by the DDR3 SDRAM "must be programmed via a mode
24 register set (MRS) command," correct?

25 MR. LINDSAY: Objection. Outside the 01:56:54



800.211.DEPO (3376)
EsquireSolutions.com

1 scope. 01:56:54

2 THE DEPONENT: I'm sorry. I'm not
3 following. Where exactly on page 22?

4 Q. (By Mr. Chandler) The top, the first
5 line. The "four Mode Registers, provided by the 01:57:13
6 DDR3 SDRAM . . . must be programmed via a Mode
7 Register Set (MRS) command," correct?

8 MR. LINDSAY: Objection. Outside the
9 scope.

10 THE DEPONENT: It says that, yes. 01:57:30

11 Q. (By Mr. Chandler) And it goes on to say
12 the -- at the end of that line, the "contents of
13 the Mode Registers must be fully initialized and/or
14 re-initialized, i.e., written, after power up
15 and/or reset for proper operation," correct? 01:57:45

16 MR. LINDSAY: Objection. Outside the
17 scope.

18 THE DEPONENT: I believe you have read
19 that correctly, yeah.

20 Q. (By Mr. Chandler) So at power-up, one of 01:57:56
21 the mode registers shown on page 26 of Exhibit 1020
22 is whether or not write leveling is enabled,
23 correct?

24 MR. LINDSAY: Objection. Outside the
25 scope. 01:58:14



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: So one of the -- one 01:58:18
2 element of mode register MR1, as we talked about,
3 is this 1-bit A7 field which indicates whether
4 write leveling is enabled.

5 Q. (By Mr. Chandler) And then on the bottom 01:58:35
6 of page 27 of the DDR3 standard marked as
7 Exhibit 1020 is a description of write leveling,
8 correct?

9 MR. LINDSAY: Objection. Outside the
10 scope. 01:58:47

11 THE DEPONENT: There's a section labeled
12 "Write leveling," yeah. And we can read it and
13 discuss what it literally says, but I don't, as I
14 sit here, have an understanding of exactly what
15 it's referring to. 01:59:02

16 Q. (By Mr. Chandler) But you would agree
17 that the DDR3 JEDEC standard marked as
18 Exhibit 1020, dated November 2008, provided for
19 write leveling, fair?

20 A. It discusses what it calls "write
21 leveling," sure. 01:59:23

22 Q. And it teaches, at the bottom of page 27
23 of Exhibit 1020, that "For better signal integrity,
24 DDR3 memory module adopted fly-by topology for the
25 commands, addresses, control signals, and clocks," 01:59:55



800.211.DEPO (3376)
EsquireSolutions.com

1 correct? 01:59:57
2 A. Yes, that's what it says.
3 Q. And that "causes flight time skew between
4 clock and strobe at every DRAM on the DIMM,"
5 according to this DDR3 JEDEC standard, correct? 02:00:11
6 A. Yes, that's roughly what it says there.
7 Yep.
8 Q. And would it be fair to say that write
9 leveling is intended to correct for "flight time
10 skew between the clock and the strobe at every DRAM 02:00:31
11 on the DIMM"?
12 MR. LINDSAY: Objection. Outside the
13 scope.
14 THE DEPONENT: Well, at the bottom of the
15 page, it says that there is "a 'write leveling'
16 feature to allow the controller to compensate for 02:00:45
17 skew."
18 Q. (By Mr. Chandler) And page 42 of the
19 DDR3 DIMM standard marked as Exhibit 1020 provides
20 more detail about write leveling, correct? 02:01:05
21 A. It would appear to go into more detail on
22 what write leveling means in this context, yeah.
23 Q. Now I want to switch to read leveling,
24 all right?
25 A. Sure. 02:01:28



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. The DDR3 standard marked as Exhibit 1020 02:01:29
2 has, on page 31, a reference to a "Multi-Purpose
3 Register (MPR)" at the bottom of page 31, correct?

4 MR. LINDSAY: Objection. Outside the
5 scope. Form. 02:01:49

6 THE DEPONENT: Yes, I see Section 3.4.5.1
7 is titled "Multi-Purpose Register," and then,
8 parenthetically, "(MPR)."

9 Q. (By Mr. Chandler) And the DDR3 standard
10 teaches that the MRS command will set a mode 02:02:08
11 register bit A0 and bit A1 which will affect the
12 MPR location, correct?

13 MR. LINDSAY: Objection. Outside the
14 scope. Form.

15 THE DEPONENT: You're paraphrasing a lot 02:02:34
16 of words there, so let me try to -- from different
17 sentences.

18 I'm sorry. I'm having trouble following.
19 Could you repeat the question.

20 Q. (By Mr. Chandler) Let me ask a slightly 02:03:07
21 different question.

22 In the DDR3 standard marked as
23 Exhibit 1020, on page 31, the mode register set
24 command will set various bits in mode register MR3,
25 including bit A2, titled MPR. 02:03:26



800.211.DEPO (3376)
EsquireSolutions.com

1 And I will stop there; is that correct? 02:03:42

2 MR. LINDSAY: Objection. Outside the
3 scope of direct.

4 THE DEPONENT: Yeah, the second sentence
5 says, "To enable the MPR, a MODE Register Set 02:03:49
6 command must be issued to MR3 Register with bit A2
7 equal to 1." [as read]

8 Q. (By Mr. Chandler) And if bit A2 equals
9 1, then the multi-purpose register, abbreviated
10 "MPR," is enabled, correct? 02:04:08

11 MR. LINDSAY: Objection. Outside the
12 scope of direct.

13 THE DEPONENT: I think it's -- I think
14 it's enabled regardless, it looks to me.

15 Q. (By Mr. Chandler) "To enable the MPR" -- 02:04:40
16 the multi-purpose register -- "a MODE Register Set
17 command must be issued to MR3 Register with bit A2
18 equal to 1" [as read], correct?

19 MR. LINDSAY: Objection. Outside the
20 scope of direct. 02:04:54

21 THE DEPONENT: That's -- that's what it
22 says. It's a little bit confusing, but that's what
23 it says.

24 I don't know how that register is
25 disabled. It's got a value or 1 or 0 in it. 02:05:21



800.211.DEPO (3376)
EsquireSolutions.com

1 It's -- the register itself is going to be enabled. 02:05:26

2 Q. (By Mr. Chandler) To disable the mode --
3 the multi-purpose register, MPR, the bit A2 would
4 be set to zero, correct?

5 MR. LINDSAY: Objection. Foundation. 02:05:55
6 Outside the scope of direct.

7 THE DEPONENT: It says if MR3 bit A2 is
8 set to zero, then the MPR is disabled.

9 Q. (By Mr. Chandler) All right. And then
10 look at page 48 of the DDR3 standard marked as 02:06:28
11 Exhibit 1020.

12 Let me know when you're there.

13 A. Sure.

14 Q. Page 48 of the DDR3 standard marked as
15 Exhibit 1020 provides some additional detail about 02:06:47
16 the multi-purpose register, abbreviated "MPR,"
17 correct?

18 MR. LINDSAY: Objection. Outside the
19 scope.

20 THE DEPONENT: It's got a section titled 02:07:00
21 "Multi Purpose Register" and a figure that's
22 labeled "MPR Block Diagram."

23 Q. (By Mr. Chandler) And in Figure 20 of
24 the "MPR Block Diagram," on the right-hand side, it
25 says "Multipurpose register Pre-defined data for 02:07:13



800.211.DEPO (3376)
EsquireSolutions.com

1 Reads," correct? 02:07:18

2 MR. LINDSAY: Objection. Outside the

3 scope.

4 THE DEPONENT: That's what it says. Is

5 it saying that's the multi-purpose register? 02:07:26

6 Q. (By Mr. Chandler) The DDR3 standard

7 teaches using the multi-purpose register for

8 calibrating reads "until the read data capture at

9 the memory controller is optimized" [as read], as

10 stated on page 51, correct? 02:07:58

11 MR. LINDSAY: Objection.

12 THE DEPONENT: I don't have --

13 MR. LINDSAY: Outside the scope of

14 direct.

15 THE DEPONENT: Yeah, if it says -- it 02:08:04

16 says what it says. We were looking -- yeah, this

17 is -- based on the line of questions you -- well,

18 let me see.

19 Q. (By Mr. Chandler) So page 51, second

20 line from the top of Exhibit 1020, the "memory 02:08:22

21 controller repeats these calibration reads until

22 read data capture at memory controller is

23 optimized," correct?

24 A. Yes, that's what it says.

25 MR. LINDSAY: Objection. Outside the 02:08:38



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of the direct. 02:08:38

2 Q. (By Mr. Chandler) And that's using the
3 MPR multipurpose register shown in Figure 21,
4 correct?

5 MR. LINDSAY: Objection. Outside the 02:08:45
6 scope of direct. Foundation.

7 THE DEPONENT: There is no register shown
8 in 21, Figure 21. Furthermore, what you pointed me
9 to as the MPR is that 1-bit register. And now
10 there's a whole bunch of functions which are 02:09:01
11 labeled "MPR" which can't possibly be accomplished
12 with a 1-bit register, so...

13 Q. (By Mr. Chandler) I think -- I think
14 perhaps you've become a little confused.

15 So there is a register for enabling the 02:09:17
16 MPR functionality that we discussed with respect to
17 the mode register set command. But then separate
18 from that, there is this multi-purpose register
19 which can be used to read out predefined data
20 patterns, as taught on page 51 of Exhibit 1020, 02:09:40
21 correct?

22 MR. LINDSAY: Objection. Outside the
23 scope. Form.

24 THE DEPONENT: So they -- they work close
25 together, and they're both labeled "MPR." They're 02:09:50



800.211.DEPO (3376)
EsquireSolutions.com

1 both multipurpose registers. 02:09:52

2 Yeah, it's -- I -- I likely do
3 misunderstand. It's very confusing.

4 Q. (By Mr. Chandler) Top of page 48 of
5 Exhibit 1020 states, "The Multi Purpose Register 02:10:14
6 (MPR) function is used to Read out a predefined
7 system timing calibration bit sequence," correct?

8 MR. LINDSAY: Objection. Outside the
9 scope.

10 THE DEPONENT: That's what it says. 02:10:30

11 Q. (By Mr. Chandler) And then page 51 of
12 Exhibit 1020 shows, in Figure 21, the "MPR Readout
13 of predefined pattern," correct?

14 MR. LINDSAY: Objection. Outside the
15 scope. 02:10:45

16 THE DEPONENT: Where is that?

17 Q. (By Mr. Chandler) The title of Figure 21
18 at the bottom of page 51.

19 A. No, I mean where does it show that?

20 Q. It shows the DQ data coming out in a 02:11:00
21 predefined pattern, correct?

22 MR. LINDSAY: Objection. Assumes facts
23 not in evidence. Outside the scope of direct.

24 THE DEPONENT: I don't know. I haven't
25 reviewed this in quite a long time. 02:11:12



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) By the time of the 02:11:18
2 DDR3 standard, was read leveling known?

3 A. Maybe. I'm not sure. I don't know when
4 the -- you know, at what point the concept was
5 introduced. 02:11:52

6 Q. By the time of the '506 patent in July of
7 2012, was read leveling and write leveling known?

8 A. Well, again, I don't know what date the
9 concept of read leveling in particular was
10 introduced into the community, so I can't answer 02:12:12
11 that.

12 Q. Well, but you know that Hiraishi is prior
13 art and refers to read leveling and write leveling,
14 correct?

15 MR. LINDSAY: Objection. Form. 02:12:23

16 THE DEPONENT: He does refer to read
17 leveling. It's not clear what he means by read
18 leveling. How it's implemented is pretty sparse.
19 But that is prior art, yeah.

20 Q. (By Mr. Chandler) And the '506 patent 02:12:34
21 refers to read leveling and write leveling as a
22 prior art technique, correct?

23 A. I -- I don't recall. I haven't memorized
24 it. If it does, it does. It wouldn't surprise me
25 at all. 02:12:47



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. In paragraph 114 of your expert 02:13:04
2 declaration marked as 2006, you talk about Butt; is
3 that correct?

4 A. Yes. Pardon me. Yes.

5 Q. And that discussion of Butt actually 02:13:28
6 begins on paragraph 109 and carries over to
7 paragraph 114; is that fair?

8 A. Yes, that's the -- 109 is the start of
9 the section discussing Butt and Hiraishi.

10 Q. And you characterize Butt as having "old 02:13:47
11 DDR teachings," correct, in paragraph 109 of your
12 declaration marked as Exhibit 2006?

13 A. Yes, that's the heading of that Section C
14 is --

15 Q. And so your -- 02:14:07

16 A. -- is "Old DDR Technology," that phrase.
17 Yeah.

18 Q. So your opinion is a person of ordinary
19 skill in the art would not have looked at Butt's,
20 quote, old DDR teachings, end quote, to modify or 02:14:15
21 provide details about Hiraishi's DDR memory
22 modules, correct?

23 A. Yeah, I think I say pretty clearly that
24 they would not have looked to Butt to modify
25 Hiraishi. 02:14:32



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. In forming your opinions, you believe 02:14:32
2 that Butt's teachings were limited to the old DDR1
3 standard published in 2000, correct?

4 A. I don't believe I said that. I'd be
5 happy to review something if you wanted me to. 02:14:50

6 Q. Is that not what you said in paragraph
7 110?

8 A. Yeah, but I thought your question was
9 it -- it only relates to that. Maybe I misheard.
10 It does relate -- it does relate to the older 02:15:11
11 technology, but that doesn't mean it doesn't relate
12 to newer technology as well.

13 Q. That was my next question.

14 So Butt's teachings are not limited to
15 the DDR1 technology but are also relevant to the 02:15:23
16 DDR2 and DDR3 technology, correct?

17 A. I don't know. Perhaps. I mean, yeah,
18 I -- it's -- maybe; maybe not. I don't recall if
19 Dr. Wedig commented on that and if I replied to it,
20 I don't think that that was really one of the 02:15:50
21 material elements that was -- yeah, I guess I'll
22 leave it at that.

23 Q. In forming your nonobviousness opinions,
24 did you consider whether or not Butt's teachings
25 were relevant to the DDR3 memory modules? 02:16:08



800.211.DEPO (3376)
EsquireSolutions.com

1 A. In forming my opinions, I reviewed the 02:16:16
2 arguments that Dr. Wedig put forth and evaluated
3 them.

4 Q. And Dr. Wedig relied on Butt, correct?

5 A. Yes. 02:16:31

6 Q. And in forming your nonobviousness
7 opinions, did you believe that Butt's teachings
8 were relevant to DDR3 memory modules or not?

9 A. That's not an exercise that anybody I'm
10 familiar with would conduct. I -- I wasn't asked 02:16:53
11 to look at art not owned by my client and consider
12 whether it applies to products not sold by my
13 client. That's -- that would be something new,
14 you know.

15 Dr. Wedig made some arguments. I was 02:17:12
16 asked to consider the arguments, analyze them, and
17 comment on them. And that's what I endeavored to
18 do.

19 Q. All right. So just to be sure I
20 understand, you did not consider whether Butt's 02:17:26
21 teachings are relevant to DDR3 memory modules?

22 MR. LINDSAY: Objection. Misstates
23 testimony. Form.

24 THE DEPONENT: Not in the abstract
25 outside of my analysis of Dr. Wedig's opinions and 02:17:43



800.211.DEPO (3376)
EsquireSolutions.com

1 arguments. 02:17:50

2 Q. (By Mr. Chandler) In forming your
3 nonobviousness opinions, did you consider whether
4 Butt's teachings were relevant to read leveling?

5 A. Only to the extent that Dr. Wedig relied 02:18:16
6 upon -- relied upon that concept.

7 Q. But what about your opinions? I'm trying
8 to understand your opinions, not Dr. Wedig.

9 A. Yeah, my opinions are focused in the
10 context of his arguments. That's what I was asked 02:18:36
11 to address.

12 So there -- there's certainly -- for
13 example, there's a lot of technology that Butt
14 refers to which absolutely is used in DDR2 and DDR3
15 and 4 and 5 and will be used in 6. 02:18:54

16 I'm not saying it's, you know, Butt's
17 claimed inventions or anything in particular, or
18 how significant Butt is as -- as an origin, a
19 seminal piece of work, in any of those particular
20 areas. 02:19:14

21 Q. Butt teaches centering the DQS strobe
22 relative to the DQ data signal, correct?

23 A. Butt talks about a way to accomplish
24 that, yes.

25 Q. And that teaching is relevant to DDR2 and 02:19:34



800.211.DEPO (3376)
EsquireSolutions.com

1 DDR3 technology, right? 02:19:38

2 MR. LINDSAY: Objection. Form.

3 THE DEPONENT: Could be.

4 Q. (By Mr. Chandler) You haven't formed the
5 opinion that it's not relevant, right? 02:19:54

6 MR. LINDSAY: Objection. Form.

7 THE DEPONENT: I have charged my client
8 only for the time that they asked me and the task
9 they asked me to look at, which was evaluating
10 Dr. Wedig's arguments. Not whether some of the art 02:20:11
11 was related to other specs -- specifications on
12 products that my clients, as far as I know, don't
13 make.

14 Q. (By Mr. Chandler) Butt's teachings on
15 centering the DQS strobe signal with the DQ data 02:20:35
16 signal are relevant to DDR2 memory modules, DDR3
17 memory modules, DDR4 memory modules being sold
18 today, and the latest standard, DDR5 memory
19 modules, correct?

20 MR. LINDSAY: Objection. Form. 02:21:03

21 THE DEPONENT: Maybe. You'll have to
22 refresh my memory if I took a stand on that.

23 Q. (By Mr. Chandler) Do you have any
24 opinion now on that question?

25 MR. LINDSAY: Same objection. 02:21:18



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: Well, Butt talks about a 02:21:25
2 particular way to accomplish -- to determine how to
3 do that centering. There are other ways to do it.
4 So, you know, whether Butt is relevant to some --
5 to the data centering technique in a specific 02:21:40
6 specification or not, I -- I don't know. I don't
7 have an opinion as I sit here.

8 Q. (By Mr. Chandler) Is centering the
9 strobe signal relative to the DQ data signal, is
10 that important to DDR3 and later technologies? 02:21:57

11 MR. LINDSAY: Objection. Form.

12 THE DEPONENT: In many situations. In
13 some situations, it -- it might not be. In fact,
14 in some situations you may want to have them not
15 centered. 02:22:19

16 Q. (By Mr. Chandler) But in many
17 situations, you would want them centered, because
18 otherwise you could get problems such as
19 metastability or, in the worst case, the circuit
20 just doesn't work, right? 02:22:38

21 If the DQ and -- data signal and DQS
22 strobe signal becomes misaligned, you get some
23 problems?

24 A. Well, that assumes --

25 MR. LINDSAY: Objection. Form. 02:22:49



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: Yeah, that assumes that 02:22:50
2 the setup in all times are equal. They don't have
3 to be equal.

4 Q. (By Mr. Chandler) In your opinion, are
5 the teachings of Butt relevant to DDR3 memory 02:23:16
6 modules such as Hiraishi? Or do you not know?

7 A. No, it's -- it's not relevant.

8 Q. So in forming your nonobviousness
9 opinions, you believe that Butt's teachings were
10 not relevant to DDR3 memory modules like Hiraishi, 02:23:48
11 correct?

12 A. What I'm saying is they're not relevant
13 to Hiraishi. Hiraishi has circuitry for centering
14 the signals. It does the 90 percent delay. That's
15 the delay. 02:24:12

16 Butt is -- is trying to figure what the
17 delay should be. Hiraishi doesn't need Butt.
18 Hiraishi knows what the delay should be.

19 Q. In a DDR3 memory module, the DQ data
20 signal and the DQS strobe signal can become out of 02:24:32
21 alignment, as taught by Butt, correct?

22 A. Sure. Yeah.

23 Q. And when that happens, Butt's technique
24 can solve that problem of the DQ data signal and
25 the DQS strobe signal being out of alignment; is 02:24:57



800.211.DEPO (3376)
EsquireSolutions.com

1 that fair? 02:25:01
2 MR. LINDSAY: Objection. Form.
3 THE DEPONENT: I think that that
4 accurately paraphrases some of what Butt claims to
5 teach, sure. 02:25:13
6 Q. (By Mr. Chandler) And when a memory
7 module tries to capture the read data, having the
8 DQS strobe signal properly centered is important,
9 right?
10 MR. LINDSAY: Objection. Form. 02:25:31
11 THE DEPONENT: It might be, but as I
12 mentioned, that assumes that the setup and hold
13 times are -- are equal.
14 Q. (By Mr. Chandler) Butt teaches that when
15 capturing the read data, centering the DQS strobe
16 signal is important, correct? 02:25:52
17 A. Yeah, I believe -- I believe that's
18 accurate.
19 Q. Can you look at the DDR3 JEDEC standard
20 marked as Exhibit 1020 and go to page 58. 02:26:18
21 Let me know when you're there.
22 A. Okay.
23 Q. What is the difference between a clock
24 signal and a strobe signal?
25 A. As a starting point, a clock signal is 02:26:39



800.211.DEPO (3376)
EsquireSolutions.com

1 periodic. 02:26:41

2 Q. And in slightly less technical terms,
3 what do you mean by "a clock signal is periodic"?

4 A. Yeah, it goes up and down at a regular
5 rate. So it can be used to time how long an event 02:26:56
6 takes.

7 Q. But a strobe signal also goes up and down
8 at a regular rate, doesn't it?

9 A. No.

10 Q. And why do you say that? 02:27:12

11 A. Because it doesn't. I mean, it -- it
12 just doesn't.

13 Q. So what does a strobe signal do?

14 MR. LINDSAY: Objection. Form.

15 THE DEPONENT: A strobe signal goes up 02:27:23
16 and down when it needs to indicate to something
17 that we might call a sampler that it should sample
18 its inputs.

19 Q. (By Mr. Chandler) But when the strobe
20 signal is going up and down, it's going up and down 02:27:37
21 at a regular rate until it stops going up and down;
22 is that fair?

23 A. No.

24 Q. Why do you say that?

25 A. Because it -- it doesn't. It -- if -- 02:27:49



800.211.DEPO (3376)
EsquireSolutions.com

1 if -- you -- you could have a strobe signal that, 02:27:53
2 in a certain context, in a certain piece of
3 hardware, actually went up and down for some period
4 of time at a regular rate. That is not at all the
5 property of strobe signals in general. It's not at 02:28:08
6 all the property of strobe signals in the context
7 that we are talking about.

8 Q. Okay. So how would you explain to a
9 layperson what a clock signal is versus what a
10 strobe signal is. 02:28:28

11 MR. LINDSAY: Objection. Form.

12 THE DEPONENT: A clock signal, in
13 general, is used to measure a time. And a strobe
14 signal is used to indicate that some data should be
15 sampled. It's -- it's known to be in a good state, 02:28:47
16 so it can be accurately read when the strobe signal
17 is asserted.

18 Q. (By Mr. Chandler) And when you say "when
19 the strobe signal is asserted," is -- I think
20 previously you used the word "transition"; is 02:29:04
21 that --

22 A. Yeah, although usually it's just on one
23 edge as a concept. So if you had one strobe
24 signal, typically you'd say when it goes from
25 zero -- from low to high, that's the transition 02:29:17



800.211.DEPO (3376)
EsquireSolutions.com

1 that causes the sampling to happen. 02:29:20

2 But, you know, we've seen complementary
3 strobe signals, and DDR uses both edges. But,
4 yeah, in -- in general, when it transitions from
5 one state to another, there will be a direction of 02:29:35
6 transition that is known to be indicating that
7 sampling should occur.

8 Q. Okay. And so page 58 of Exhibit 1020
9 shows a clock signal at the top of Figure 28; is
10 that fair? 02:29:50

11 A. Yes, it shows a clock signal.

12 Q. And then the next row of Figure 28 on
13 page 58 of Exhibit 1020 shows a DQS strobe signal;
14 is that fair?

15 A. Yes. 02:30:07

16 Q. And the JEDEC standard shows the DQS
17 strobe signal going low for a clock cycle and then
18 transitioning from low to high; is that correct?

19 A. Sort of. It's showing both DQS
20 complementary signals transitioning. So one goes 02:30:34
21 low to high, the other one goes high to low.

22 Q. Okay. For simplicity, let's just focus
23 on the DQS strobe with the understanding that there
24 would be a complementary strobe as well.

25 Is that okay? 02:30:52



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes, fair enough. 02:30:54

2 Q. So the JEDEC standard shows the DQS
3 strobe signal going low for a clock cycle and, then
4 it transitions high, correct?

5 A. Yes, some portions of this figure show 02:31:11
6 that sequence.

7 Q. Okay. Why does the strobe do that?

8 A. Because it's indicating to the receiver
9 that it should sample its inputs.

10 Q. Why does it have to go low before it 02:31:29
11 goes -- for a clock cycle before it goes high?

12 A. Because it's the transition that triggers
13 the sampling, not the value. So it's not when the
14 thing is high it samples or when it's low it
15 samples. It's when it goes low to high. 02:31:47

16 Q. Why does the JEDEC standard have the DQS
17 strobe signal go low for a clock period before it
18 goes high?

19 A. You would have to ask them.

20 Q. Is that common in the JEDEC standard for 02:32:02
21 the strobe signal to go low, for a clock signal
22 then to go high, and then alternate between low and
23 high every half clock cycle?

24 MR. LINDSAY: Objection. Form.

25 THE DEPONENT: Well, it's -- even on this 02:32:22



800.211.DEPO (3376)
EsquireSolutions.com

1 figure, it's not always doing that. I'll point 02:32:23
2 out, at the beginning, it's low for longer than a
3 clock cycle.

4 So, yeah, I mean, in this specification,
5 it's showing it going low to high one, two, three, 02:32:36
6 I think four times.

7 Q. (By Mr. Chandler) And then it goes low?

8 A. Then it goes low, and then it goes to
9 high Z.

10 Q. And is high Z what you were discussing 02:32:53
11 earlier as the Z state, the --

12 A. Yes. Yeah, it's -- it's considered a
13 high-impedance state. So sometimes it's just
14 called Z; sometimes it's high Z.

15 Q. Does the clock signal ever go to a high Z 02:33:09
16 state?

17 A. If it does, you've got a real problem. I
18 don't see it here. And it shouldn't. If a clock
19 signal does that, then any synchronous digital
20 circuit that it drives will, at least for that time 02:33:25
21 period, stop changing at all, stop working.

22 Q. The JEDEC standard refers to something
23 called the preamble of the DQS strobe; is that
24 correct?

25 A. Likely. Preambles are used quite often. 02:33:42



800.211.DEPO (3376)
EsquireSolutions.com

1 I don't recall reading about the preamble in this 02:33:46
2 context and -- and how it's used.

3 Q. So footnote 4 on page 58 of Exhibit 1020
4 refers to the preamble, correct?

5 A. It says, "The minimum pulse width of read 02:34:06
6 preamble is defined by tRPE (min)." [as read]

7 Q. "tRPRE (min)"?

8 A. Yes, that's right.

9 Q. And that's shown on the DQS line,
10 correct? 02:34:31

11 A. Yes, both the middle line and on the
12 bottom line.

13 Q. So the JEDEC standard teaches the DQS
14 strobe signal as a preamble of tRPRE, which is
15 longer than one clock cycle before the strobe 02:34:53
16 transitions from low to high; is that right?

17 A. I don't know. I haven't reviewed this
18 any time recently. It's a dense document.

19 The figure here is showing tRPRE as being
20 bigger than one clock cycle. It could certainly be 02:35:14
21 the case that -- it almost certainly is a variable.
22 Otherwise, it would have said exactly what it was.
23 It could be multiple clock cycles; it could be less
24 than a clock cycle. It's not --

25 Q. Yeah, I guess -- 02:35:30



800.211.DEPO (3376)
EsquireSolutions.com

1 A. It's not clear from here what -- exactly 02:35:31
2 how long it is.

3 Q. But it would be defined in the JEDEC
4 standard if we looked for it, I assume?

5 A. It -- it would be defined. It may not be 02:35:40
6 statically defined. It may be defined based on
7 values that change at run time. I would be
8 surprised if tRPRE min was not defined somewhere
9 else. Otherwise, somebody trying to implement this
10 would -- would say, "How do I know how long that 02:35:59
11 is? You haven't told me."

12 Q. So it looks like it's defined on page 164
13 of Exhibit 1020; is that fair?

14 THE VIDEOGRAPHER: Counsel, we've been on
15 the record for a hour and 30 minutes. Can we go 02:36:18
16 off the record for one second?

17 MR. CHANDLER: Let me get an answer to
18 the question, and then we'll --

19 THE VIDEOGRAPHER: Sure.

20 THE DEPONENT: I'm almost there. 02:36:32

21 No, it's not defined. It's characterized
22 as -- as a range. It's not clear what exactly it
23 is.

24 Q. (By Mr. Chandler) It's got to be a
25 minimum of 0.9 times the clock cycle tCK, correct? 02:37:23



800.211.DEPO (3376)
EsquireSolutions.com

1 A. That appears to be what it's saying, 02:37:28
2 yeah.

3 MR. CHANDLER: All right. Let's go off
4 the record for about five minutes for the
5 videographer, and then we'll resume. 02:37:40

6 THE DEPONENT: Great.

7 THE VIDEOGRAPHER: Thank you, Counsel.
8 We're going off the record. The time is 2:37.

9 (Recess taken.)

10 THE VIDEOGRAPHER: We're going back on 02:47:56
11 the record. The time is 2:47.

12 Q. (By Mr. Chandler) Dr. Mangione-Smith, do
13 you still have page 164 of Exhibit 1020, the JEDEC
14 DDR3 standard, in front of you?

15 A. Yes, I do. 02:48:11

16 Q. And you discussed this very page of this
17 very document in your declaration, right?

18 A. I may have. It wouldn't surprise me. I
19 don't recall. I'd be happy to refresh my memory if
20 you want to point me to something. 02:48:27

21 Q. Page 65 of your declaration marked as
22 Exhibit 2006 cites to this very table appearing on
23 page 164 of the DDR3 standard marked as
24 Exhibit 1020, correct?

25 A. Yes. 02:48:48



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. So you've looked at this table, and you 02:48:48
2 understand it, right?

3 A. I -- I understand the elements that I
4 commented on, yeah. At least those.

5 Q. Look at page 100 of your declaration 02:49:09
6 marked as Exhibit 2006.

7 Let me know when you're there.

8 A. I'm there.

9 Q. Table 50 of the JEDEC DDR3 standard, top
10 row, shows that for a DDR3-800 memory device, the 02:49:28
11 minimum clock cycle is 2.5 nanoseconds, correct?

12 A. Yeah, that appears to be the case.

13 Q. So that's 2,500 picoseconds?

14 A. Sure.

15 Q. And then if you go to page 65 of your 02:49:48
16 declaration marked as Exhibit 2006, you cite to
17 Table 65 of the DDR3 standard, which shows that
18 there can be a skew between the DQS strobe signal
19 and the DQ data signal when leaving the memory
20 device that is up to 200 picoseconds, correct? 02:50:15

21 A. Yeah, I mean, I -- it probably should
22 have said something like the maximum tolerable skew
23 according to spec is 200 picoseconds.

24 Q. So under the DDR3 standard, a DQS-to-DQ
25 skew of up to 200 picoseconds is permitted for the 02:50:49



800.211.DEPO (3376)
EsquireSolutions.com

1 signals coming out of the DDR3 memory device, 02:50:59
2 correct?

3 A. Yeah, it says that -- well, specifically
4 for DDR3-800, that is the maximum tolerable skew.
5 Yeah. 02:51:24

6 Q. And so a math question for you: If the
7 skew is 200 picoseconds, and the clock period is
8 2,500 picoseconds, as we discussed a moment ago,
9 how many degrees can the DQS strobe be skewed
10 relative to the DQ data signal? 02:51:48

11 A. I don't know. I'm not going to do the
12 math in my head while being videotaped.

13 Q. Would it be 200 divided by 2,500 times
14 360 degrees?

15 A. Could be. 02:52:08

16 Q. Well, can you tell me. You can pull up a
17 calculator if you want, or you can ask me to --

18 A. No, I just -- you know, it's -- it is a
19 mathematical equation. It is whatever it is. I
20 don't want to use a calculator. I don't really 02:52:20
21 want to calculate it. I haven't -- I don't usually
22 deal with delays in terms of degrees. If you
23 represent that that's what it is, I have no reason
24 to disbelieve you.

25 Q. Well, I mean, you refer a lot to a 02:52:33



800.211.DEPO (3376)
EsquireSolutions.com

1 90-degree delay, right? 02:52:35

2 A. Yes.

3 Q. And that's one-quarter of a clock cycle?

4 A. Yes.

5 Q. In this page, 65 of your declaration, 02:52:49

6 you're referring to 200 picoseconds relative to a

7 clock cycle of 2,500 picoseconds. And so I'm

8 trying to understand, to make an apples-to-apples

9 comparison, how many degrees that is.

10 A. Sure. I understand, yeah. 02:53:09

11 Q. So I'll perform the calculation for you,

12 but I want to make sure that the equation is

13 correct in your mind to calculate --

14 A. It -- it might be a little easier, at

15 least for me, to go the other way, if you'll buy 02:53:26

16 this: That if it's 2,500 picoseconds, figuring out

17 what a quarter of that is, that's easier math for

18 me to do on the spot, and then comparing that to

19 the 200.

20 Q. Sure. 02:53:45

21 So a quarter of 2,500 is 625?

22 A. That sounds right to me. And I apologize

23 for cutting you off there. I just -- I didn't want

24 to stall, but I didn't want to --

25 Q. I got it. 02:54:04



800.211.DEPO (3376)
EsquireSolutions.com

1 A. -- do the other equation wrong on the 02:54:05
2 spot and feel silly.

3 Q. So if the skew were 625 picoseconds, that
4 would be a 90-degree skew. Here it's about a third
5 of that. It's 200 picoseconds. And by my 02:54:17
6 calculation, that's 28.8 degrees.

7 Does that sound reasonable?

8 A. Sure. That's about a third of the
9 90 degrees. That sounds reasonable. Although, I
10 mean, this is not -- this is not the skew you're 02:54:32
11 seeing. This is the -- the worst-case skew you
12 could have to operate under the specification.

13 Q. So the maximum skew permitted for the
14 DDR3-800 is, in terms of degrees, 200 picoseconds
15 divided by 2,500 picoseconds, which is the clock 02:54:54
16 cycle, times 360 degrees equals 28.8 degrees.

17 Does that sound reasonable?

18 A. Yes.

19 Q. And to be clear, this 28.8-degree skew
20 permitted by the DDR3 standard, that's at the 02:55:13
21 moment the DQS and DQ signals are leaving the
22 memory device, correct?

23 In other words, JEDEC can't guarantee
24 that as the DQ and DQS travels along the wire that
25 they won't become further skewed. 02:55:43



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes, that -- that's correct. And towards 02:55:49
2 the bottom of paragraph 124, I say that it's only
3 complying if the DQS signal were activated; and
4 then, up to 200 picoseconds later, the DQ signal
5 was activated. 02:56:06

6 Q. And so that's referring to coming out of
7 the memory device?

8 A. Indeed.

9 Q. All right. And so it's possible -- I'm
10 not saying it's necessary -- but it's possible the 02:56:21
11 skew of up to 28.8 degrees could get worse as the
12 signals travel along the wire and the memory module
13 to their destination; is that fair?

14 A. Sure. I think that spec we were looking
15 at was just for the DRAM chip, not for the DIMMs. 02:56:41
16 So it would make sense that it would only be
17 talking the -- the chip performance.

18 Q. So at various points you referred to
19 taking a DQS strobe signal and delaying it by
20 90 degrees, correct? 02:57:11

21 A. Yes.

22 Q. But to be clear, under the DDR3 standard,
23 that DQS strobe signal could end up anywhere from
24 less than 61.2 degrees to more than 118.8 degrees
25 relative to the DQ data signal, correct, given that 02:57:36



800.211.DEPO (3376)
EsquireSolutions.com

1 skew that we just discussed at 28.8 degrees? 02:57:42

2 A. I -- to be honest with you, I'm not sure.
3 Reading this, it's only talking about the skew to
4 one side, not both, right, with the DQS signal
5 being activated first, and then subsequently the DQ 02:58:04
6 signals being activated.

7 It may be that -- that the skew coming
8 out is symmetric. I don't recall for sure.

9 Q. The standard doesn't limit the direction
10 in which the skew exists, right? It could be a 02:58:25
11 skew in one direction or it could be a skew in the
12 other direction, right?

13 A. It certainly could be. I just don't
14 recall if this skew that it will tolerate can go in
15 either direction. It may be symmetric; it may be 02:58:45
16 asymmetric.

17 Q. Now, in forming your -- I apologize. I
18 lost something where I was.

19 Bear with me one moment.

20 Look at page 57 of the JEDEC standard 03:00:03
21 marked as Exhibit 1020.

22 Are you there?

23 A. No. Almost. Okay.

24 Q. So the bottom of page 57 of the JEDEC
25 standard marked as Exhibit 1020 shows that the 200 03:00:39



800.211.DEPO (3376)
EsquireSolutions.com

1 picosecond skew that we were discussing, labeled 03:00:44
2 "tDQSQ," can be either to the left of the eye or to
3 the right of the eye, correct?

4 A. It's showing tDQSQ can be either to the
5 left or to the right. 03:01:17

6 Q. Okay. Can you turn to paragraph 114 of
7 your declaration marked as Exhibit 2006.

8 A. Or actually, is that -- I'm sorry.
9 I'm -- I'm trying to read this again.

10 It looks -- it looks to me like it's only 03:01:36
11 to the left. But maybe I'm reading the chart
12 wrong. So the -- the -- there's a red circle with
13 a line going to the left for tDQSQ, and it goes to
14 the left in both cases.

15 Q. Up above, it indicates tDQSQ describes 03:02:07
16 the latest valid transition for the rising data
17 strobe.

18 A. I was looking at the bottom figure.
19 Where are you pointing me to?

20 Q. The same page, but at the top. There's 03:02:22
21 some text.

22 A. Okay.

23 Q. "tDQSQ."

24 A. Yeah, I see that.

25 Q. And then it also, for the following 03:02:32



800.211.DEPO (3376)
EsquireSolutions.com

1 strobe, it says "tDQSQ describes the latest valid 03:02:34
2 transition"?

3 A. Sure. Yeah.

4 Q. And so do you think the skew is only to
5 one side or to both sides, the permitted skew? Or 03:03:00
6 are you not sure?

7 A. No, this -- this seems to show only to
8 the one side. It's double data rate. So there's a
9 transition on the rising transition and the falling
10 edge. 03:03:16

11 But as -- as I've said, it's been a long
12 time since I've looked at this, and there's huge
13 parts I did not rely upon.

14 Q. Well, I mean, you refer to the 200
15 picosecond skew, which is why I was bringing this 03:03:38
16 up. I mean, that is something you talked about,
17 right?

18 A. Yes, out of the 211 pages, that -- that
19 is a piece that I brought out. Yeah.

20 Q. So look at your declaration in 03:03:58
21 paragraph 114.

22 A. You said paragraph or page? You must
23 have meant paragraph, yeah.

24 Q. Page 60, paragraph 114.

25 A. Okay. I'm there. 03:04:17



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. At the end of that paragraph, you assert 03:04:18
2 the data centering for purposes of
3 capturing/sampling data is not read leveling,
4 correct?

5 A. Yes. 03:04:26

6 Q. In forming your nonobviousness opinions,
7 you believe that read leveling does not include the
8 step of aligning the DQS strobe signal with the DQ
9 data signal; is that correct?

10 MR. LINDSAY: Objection. Misstates prior 03:04:54
11 testimony.

12 THE DEPONENT: I -- I wouldn't say that,
13 no.

14 Q. (By Mr. Chandler) In your opinion, does 03:05:00
15 read leveling include the step of aligning the DQS
16 strobe signal with the DQ data signal?

17 A. No.

18 Q. Okay. So in forming your opinion, you
19 believe that read leveling does not include the
20 step of aligning the DQS strobe signal with the DQ 03:05:21
21 data signal; is that correct?

22 A. Unless when you say "aligning" you -- you
23 include relative aligning. They're -- they're not
24 aligned. They're -- well, for example, delayed by
25 90 degrees is a delay between them. 03:05:37



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. I was trying to exclude relative 03:05:52
2 alignment.

3 A. Okay.

4 Q. Because -- so let me be more clear with
5 that caveat in mind. 03:06:00

6 Do you believe that read leveling
7 includes the step of centering the DQS strobe
8 signal with the DQ data signal?

9 A. I would expect so. I think it depends on
10 the specific situation in any case, certainly in 03:06:19
11 read leveling, but in other situations where
12 there's some circuit that's sampling its input.

13 You want to have a relationship between
14 the -- when the sample data is valid and when the
15 strobe signal is asserted that gives you confidence 03:06:39
16 you'll be within the eye, within the
17 greater-than-the-whole time and less -- I'm
18 sorry -- greater than the setup time and less than
19 the hold time.

20 But in some situations, that's so easy to 03:06:54
21 accomplish, you don't really need to think about
22 much of anything. It's just that the DDR systems,
23 the timing is so aggressive, it becomes a very
24 complicated problem.

25 Q. So with at least the DDR systems, do you 03:07:10



800.211.DEPO (3376)
EsquireSolutions.com

1 think it would be normal for the read leveling 03:07:16
2 process to include the step of centering the DQS
3 strobe signal with the DQ data signal?

4 A. Yeah, because if my recollection is
5 right, they're -- they're coming out edge-aligned, 03:07:35
6 and they have to not be edge-aligned for the
7 sampling.

8 Q. And are you referring to simply delaying
9 the strobe signal by precisely 90 degrees? Or are
10 you referring to actually aligning the strobe 03:08:16
11 signal with the data signal even if that requires a
12 delay more than 90 degrees or less than 90 degrees
13 to get it centered?

14 A. I'm just talking about the delaying it
15 such that the designer has confidence that the data 03:08:37
16 will be reliably sampled, would be within the eye.

17 Q. And sometimes that delay might be more
18 than 90 degrees to get it in the center of the eye,
19 and other times it might be less than 90 degrees to
20 get it in the center of the eye; is that fair? 03:08:56

21 A. Well, it doesn't have to get it in the
22 center of the eye. In some cases, the delay might
23 be more than 90 degrees or less than 90 degrees
24 because there are limitations in precision. Maybe
25 I'm trying to make it exactly 90 degrees, and it's 03:09:14



800.211.DEPO (3376)
EsquireSolutions.com

1 as close as I can get it. That's good enough. 03:09:17

2 There could also be situations where
3 for -- perhaps I accounted for the 28, et cetera,
4 degrees of difference that we were just talking
5 about and set the delay to something other than 03:09:29
6 approximately 90 degrees.

7 Q. And I'm trying to look at what you just
8 said.

9 You referred to 28 degrees, et cetera.
10 You're referring there to the 28.8 degree skew 03:10:08
11 permitted by the DDR3 standard that we discussed a
12 moment ago?

13 A. Yes.

14 Q. And then as we discussed, the skew,
15 though, can sometimes be more than 28.8 degrees 03:10:29
16 given what happens along the wires in the memory
17 module, correct?

18 A. Yeah. It's a specification for the DRAM
19 chip, not the memory module.

20 I'm sorry. Not -- not the DIMM. 03:10:47

21 Q. Can you look at the Hiraishi marked as
22 2006.

23 A. I'm assuming that's the same Hiraishi
24 we --

25 Q. I'm sorry. 1006. 03:11:19



800.211.DEPO (3376)
EsquireSolutions.com

1 reduce the load capacitance to permit a high data 03:13:10
2 transfer rate, as you indicate at the beginning of
3 paragraph 42; is that fair?

4 A. Yes, that's the intent of -- that's one
5 of the intents of those data buffers. 03:13:23

6 Q. And Hiraishi's data buffers are
7 distributed along the memory module. There's not a
8 single central data buffer, but instead there's
9 multiple distributed data buffers on Hiraishi's
10 memory module, correct? 03:13:42

11 A. I don't recall for sure. I think that's
12 the case. Yeah. Yeah, that appears to be the
13 case.

14 Q. That's shown, for example, on Figure 1 of
15 Hiraishi marked as Exhibit 1005? 03:13:52

16 A. Yes.

17 Q. Turn to page 45 of your expert
18 declaration marked as Exhibit 2006.

19 Let me know when you're there.

20 A. I'm sorry. You said page 45? 03:14:21

21 Q. Yes.

22 A. Okay. I'm almost there.

23 Okay.

24 Q. Figure 5 of Hiraishi shows some buffers
25 labeled "INB" and "OUTB," correct? 03:14:42



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes. 03:14:48

2 Q. Would you pronounce that "INB" or "OUTB,"
3 or how would you say?

4 A. Yeah, I think that's -- it's input buffer
5 and output buffer. Yeah, "INB" and "OUTB." 03:14:58

6 Q. And the upper right of Figure 5 shows a
7 buffer control signal BC that goes to the INB and
8 the OUTB buffers, correct?

9 A. Yes, although it's -- it's two signals.
10 I don't recall if they call BC in or BC out or 03:15:17
11 BC1 or BC2. But they have to be two signals since
12 if they're both asserted, you've got a problem.

13 Q. All right. What does the control signal
14 do to the INB buffer and the OUTB buffer?

15 A. So those signals coming in from the -- 03:15:37
16 the sides of the triangles control whether the
17 buffer is activated or whether its output state is
18 in the Z state.

19 Q. So are INB and OUTB buffers in Figure 5
20 of Hiraishi tri-state buffers? 03:15:57

21 A. Yes.

22 Q. And the control signal coming either to
23 the -- I guess it always comes to the top of the
24 triangle -- would either put the tri-state buffer
25 in a high Z state, or it would enable the buffer to 03:16:18



800.211.DEPO (3376)
EsquireSolutions.com

1 pass the input to the output. 03:16:27
2 Is that a fair summary?
3 A. Yes, I think that's accurate.
4 Q. Could you turn to page 24 of your expert
5 declaration marked as Exhibit 2006. 03:16:50
6 Let me know when you're there.
7 A. Okay.
8 Q. In paragraph 52 of your expert
9 declaration marked as Exhibit 2006, you indicate
10 that Hiraishi has both S4 leveling and S5 leveling, 03:17:05
11 correct?
12 A. Yes.
13 Q. In Hiraishi, S4 leveling is performed by
14 write leveling circuit 322 and read leveling
15 circuit 323 in data register control circuit 320 of 03:17:24
16 the data register buffer 300 shown in Figure 5?
17 A. Yes.
18 Q. S5 leveling, in contrast, is performed by
19 circuitry inside the system memory controller,
20 correct? 03:17:52
21 A. In part, yeah.
22 Q. What do you mean by that, "in part"?
23 A. Well, we -- we've really only been
24 talking about S4. I thought S4 was read and write
25 leveling from the buffer to the memory. 03:18:12



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Okay. Look at paragraph 53, the next 03:18:16
2 page.

3 A. Okay.

4 Q. That's what I was getting at.

5 So -- 03:18:23

6 A. Okay. Yeah. Yeah.

7 Q. And so S5 leveling is performed by the
8 system memory controller and the host computer
9 outside --

10 A. That's -- 03:18:40

11 Q. -- the memory module, correct?

12 A. That's right.

13 Q. And since you seemed to have a momentary
14 confusion between S4 and S5 made me feel better,
15 because I had the same confusion. 03:18:55

16 MR. CHANDLER: And to that end, let me
17 introduce Exhibit 1049.

18 (Exhibit 1049 was marked for
19 identification by the Court Reporter and is
20 attached hereto.) 03:19:02

21 Q. (By Mr. Chandler) And let me know when
22 you have it up.

23 A. Okay.

24 Q. So Exhibit 1049 is something I created
25 simply to try to allow us all to remember the 03:19:24



800.211.DEPO (3376)
EsquireSolutions.com

1 difference between S4 leveling and S5 leveling. 03:19:28

2 A. Yeah. I had -- I had the relationship
3 right in my head, just a question of where the
4 control function resided.

5 But yeah, S4 is from the buffer to the 03:19:42
6 memory, and S5 is from the buffer to the memory
7 controller.

8 Q. Okay. So as shown in Exhibit 1049,
9 Hiraishi discloses both S4 read and write leveling
10 between the data register buffer 300 and the memory 03:19:59
11 chip, which is shown on the right side as green.

12 Plus, Hiraishi also discloses S5 read and write
13 leveling between the memory controller in the host
14 computer and the data register buffer 300; is that
15 fair? 03:20:25

16 A. Yeah. I guess I would just say that
17 it -- it discloses that S5 leveling is done. It
18 may not be disclosing exactly how it's done, if
19 it's being done in the host memory controller. But
20 it is disclosing S4 and S5 for read and write. 03:20:41

21 Q. And S5 read and write leveling, it's not
22 performed by the data register buffer 300, correct?

23 That's what you stated in --

24 A. Yeah, that's -- that's correct.

25 Q. -- paragraph -- okay. 03:21:01



800.211.DEPO (3376)
EsquireSolutions.com

1 Whereas S4 read and write leveling is 03:21:03
2 performed by the circuitry in the data register
3 buffer 300 of Figure 5 of Hiraishi, correct?

4 A. Yes, that's correct.

5 Q. Okay. And that's really all that this 03:21:19
6 exhibit was intended to memorialize. Feel free to
7 keep it or put it aside.

8 A. Okay.

9 Q. So I want to focus for a moment on S4.
10 Okay? 03:21:52

11 A. Yes, sir.

12 Q. What does S4 read leveling in Hiraishi
13 accomplish?

14 A. It's -- it's an attempt to control the
15 system such the buffers distributed across the DIMM 03:22:10
16 can reliably sample the -- the data values being
17 read from the DRAM chips.

18 Q. And what is being leveled relative to
19 what in Hiraishi's S4 read leveling?

20 A. I mean, I can tell you what it does. I 03:22:40
21 don't -- it's always struck me as a weird term, so
22 I don't -- "what is being leveled."

23 I mean, it's -- it's responding to the
24 fact that as the control signals propagate from the
25 middle of the DIMM out to the edges, there's a 03:22:52



800.211.DEPO (3376)
EsquireSolutions.com

1 propagation delay. And as a consequence of that, 03:22:54
2 the data out and the data strobes from the DRAMs
3 will be sent at different times. Across, you know,
4 one chip will be different from the next chip from
5 the next chip. 03:23:11

6 Q. During Hiraishi's S4 read leveling, does
7 the memory device change the timing of the data
8 that is being output, or does the timing of the
9 memory device stay the same during read leveling?

10 A. Well, the memory -- if I understand the 03:23:37
11 question right, the memory device, in principle, I
12 don't think it knows -- I don't think it has to
13 know anything about read leveling. A chip could be
14 used on its own or with a different mechanism for
15 distributing the control signals such that they -- 03:23:53
16 if the control signals were fully aligned, then
17 there wouldn't be this fly-by problem.

18 So, yeah, I think the read leveling issue
19 only comes up at the data buffers, not at the
20 memory chip itself. 03:24:13

21 Q. Okay. So in Hiraishi's S4 read leveling,
22 the data register buffer 300 shown in Figure 5 is
23 what performs the read leveling; is that fair?

24 A. Yes, that's my understanding.

25 Q. During S4 read leveling in Hiraishi, does 03:24:32



800.211.DEPO (3376)
EsquireSolutions.com

1 the data register buffer 300 change the timing of 03:24:37
2 either the DQS strobe signal or the DQ data signal?

3 A. No, that's -- that's completely
4 controlled by the -- by the SDRAM chip.

5 Q. So in your opinion, as we -- I think you 03:25:04
6 said a moment ago, the SDRAM chip doesn't change
7 its timing, correct, during read leveling?

8 A. Correct.

9 Q. And furthermore, if I understand you
10 correctly, your opinion is that Hiraishi's data 03:25:23
11 register buffer 300, during S4 read leveling, also
12 does not change the timing of either the DQS strobe
13 signal or the DQ data signal, correct?

14 A. Not as they come out of the DRAM. They
15 just yeah, come out of the DRAM as they come out. 03:25:41

16 Now, I want to be a little bit careful.
17 There's -- there's really -- there's typically two
18 parts to something like read or write leveling.
19 There's a training and setup period, and then
20 there's a regular operation. During regular 03:25:57
21 operation, it is doing read leveling, but it's not
22 being trained. It's not considering any other
23 values in any way.

24 Q. As a result of Hiraishi's S4 read
25 leveling, does the data register buffer 300 change 03:26:16



800.211.DEPO (3376)
EsquireSolutions.com

1 the timing of either the DQS strobe signal or the
2 DQ data signal as it goes through the data register
3 buffer 300?

03:26:22

4 A. Sure. It probably shouldn't, but it
5 could, yeah.

03:26:49

6 Q. Why do you say "it probably shouldn't"?

7 A. Well, what the read leveling circuit is
8 doing is it's generating these BC signals. And so
9 if a -- the timing -- there is -- from a point of
10 view of physics, there will be a time delay to go
11 through each of those tri-state buffers, but we
12 want them to be essentially instantaneous. So
13 let's assume that they're exactly the same. I'm
14 sorry. That there is no effective time delay.

03:27:17

15 So the only way I could think that it
16 could change the timing of the DQ or the DQS is if
17 it turned on the buffer later than it should have,
18 in which case the system would just fail.

03:27:32

19 Q. Okay. But assuming the system doesn't
20 fail, in your opinion, S4 read leveling in
21 Hiraishi, based on your understanding, should not
22 change the timing of either the DQS strobe signal
23 or the DQ data signal as it passes through the data
24 register buffer 300, correct?

03:27:51

25 A. I think that that's right. I mean,

03:28:18



800.211.DEPO (3376)
EsquireSolutions.com

1 the -- these data buffers are presumed to all be 03:28:19
2 identical. There's, you know, eight or nine of
3 them on a -- on a distributed data buffer design.
4 They have the same delay through that circuitry for
5 the DQ and DQS. So, yeah, it shouldn't be changing 03:28:36
6 the -- the delay within the buffer itself.

7 Q. And that's the understanding of Hiraishi
8 that you used in forming your nonobviousness
9 opinions, correct?

10 A. Yeah. There's -- there's no -- there's 03:29:00
11 no variable delay path in there that I see. I
12 mean, there is -- there is a fixed delay for the
13 DQS in the delay circuit 372, so I guess that was a
14 little bit inaccurate. It was inaccurate.

15 But other than that, that's a fixed 03:29:19
16 delay. It -- you know, everything else is
17 anticipated to not have any delay.

18 Q. So in your opinion, in S4 read leveling
19 in Hiraishi, the data register buffer is not
20 supposed to create any variable delay for either 03:29:42
21 the DQS strobe signal or the DQ data signal in your
22 opinion, correct?

23 MR. LINDSAY: Objection. Misstates prior
24 testimony. Form.

25 THE DEPONENT: Well, it's not supposed to 03:29:58



800.211.DEPO (3376)
EsquireSolutions.com

1 create any delay for the -- for the DQ signals. 03:29:59

2 And then it -- it introduces this fixed delay for
3 the DQS signal.

4 Q. (By Mr. Chandler) But not any sort of
5 variable delay that depends on the fly-by delay, 03:30:18
6 correct?

7 A. That's right. The fly-by delay causes
8 the signals coming out the DRAM chip to have delays
9 relative to each other but not within one of the
10 DRAM chips. 03:30:39

11 Q. And in your opinion, Hiraishi's S4 read
12 leveling does not remove any of the fly-by delays,
13 correct?

14 A. No, I wouldn't -- I wouldn't say that.

15 Q. Why not? 03:31:03

16 A. Well, the fly-by delays are still there.
17 It -- it does change the timing of the INB path,
18 but the signals come out of the chips as they -- as
19 they come out. That -- that is affected by the
20 fly-by time. And it goes through Hiraishi's data 03:31:25
21 buffer in a -- in a fixed delay. Well, no delay --
22 essentially no delay, with the exception of the
23 FIFO and then the delay circuitry 372.

24 Q. In your opinion, after S4 read leveling,
25 Hiraishi's data buffer will send the DQS strobe 03:31:48



800.211.DEPO (3376)
EsquireSolutions.com

1 signal and the DQ data signal to the system memory 03:31:53
2 controller without any changes to the timing of
3 those signals, other than the fixed 90-degree
4 adjustment of the strobe signal, correct?

5 A. I -- I don't think so. But maybe I 03:32:15
6 misheard the question.

7 Could you repeat it.

8 Q. In your opinion, after S4 read leveling,
9 Hiraishi's data register buffer 300, shown in
10 Figure 5, will send the DQS strobe signal and the 03:32:30
11 DQ data signal to the system memory controller
12 without any changes to the timing of those signals
13 other than the fixed 90-degree delay to the DQS
14 strobe signal, correct?

15 A. No. 03:32:55

16 Q. Okay. Explain it to me, then.

17 A. Well, the DQS signal is not sent through
18 the memory controller. That's -- that's one issue.

19 The second issue is that there's a FIFO
20 302 which introduces some clock-period-based delay. 03:33:14

21 Q. Why do you say that the DQS strobe signal
22 is not sent to the system memory controller?

23 A. Because it's not.

24 Q. Where does it go?

25 A. It goes into -- well, it goes through the 03:33:43



800.211.DEPO (3376)
EsquireSolutions.com

1 tri-state buffers first, and then it goes into a 03:33:50
2 selector, and then it goes into a delay circuit,
3 and then it goes into the FIFO 302.

4 Q. But then the data register buffer 300
5 outputs a DQS strobe signal, right, at 350? 03:34:09

6 A. Not the DQS strobe signal that we've been
7 talking about. You were talking about it going
8 from one side and passing through and asking about
9 delays. It -- there is no such signal.

10 Q. I want to focus on the timing of the DQS 03:34:30
11 strobe signal that comes into the data register
12 buffer 300 and the DQS strobe signal that goes out
13 of the register data buffer 300 in Hiraishi.

14 Understood?

15 A. Okay. Sure. 03:34:47

16 Q. And Hiraishi calls it "DQS" in both
17 instances, right?

18 A. It is labeled "DQS." It's a signal used
19 to strobe data.

20 Q. In your opinion, does Hiraishi's data 03:34:59
21 buffer 300, after S4 read leveling, introduce a
22 variable delay to the DQS strobe signal that's sent
23 to the system memory controller?

24 A. Possibly. I mean, the emphasis of the
25 analysis has been on the read side, but I would 03:35:45



800.211.DEPO (3376)
EsquireSolutions.com

1 have to review. I think 376, the -- well, no. 03:35:48

2 I guess I'd have to say the answer to
3 that is no.

4 Q. So in forming your nonobviousness
5 opinions, you believe that Hiraishi's data register 03:36:03
6 buffer 300, after S4 read leveling, does not
7 introduce a variable delay in the DQS strobe signal
8 that's sent to the system memory controller,
9 correct?

10 A. That's right. It gets generated. It 03:36:27
11 goes through a tri-state buffer. It goes out the
12 pin.

13 Q. So in your opinion, the fly-by delays
14 that exist on the memory module will be present
15 both at the input to Hiraishi's data register 03:37:17
16 buffer 300 for the DQS strobe signal as well as the
17 output of the DQS strobe signal that goes to the
18 system memory controller; is that fair?

19 A. I don't know that I would say that.
20 That's not really something I've discussed. 03:37:43

21 Q. I'm just trying to understand what you
22 believe the S4 read leveling accomplishes, if
23 anything, relative to the DQS strobe signal that's
24 coming into the data register buffer 300 in
25 comparison to the DQS strobe signal that's going 03:38:01



800.211.DEPO (3376)
EsquireSolutions.com

1 out the data register buffer 300. 03:38:05

2 A. Read leveling is about accounting for
3 timing differences caused by the fly-by
4 communications path in the buffer for reading that
5 data. 03:38:20

6 So that's why one of things that it does
7 is it turns on the -- the inbound, the INB path,
8 but only turns it on when it needs to be turned on.
9 That's part of read leveling, knowing when to turn
10 that on. 03:38:38

11 But ultimately, you know, if -- if
12 everything works according to plan, the data gets
13 put into a FIFO circuit, which is labeled "302."
14 And then at some point after that, it gets clocked
15 out, and the system generates a value of DQS to 03:38:54
16 coincide with that.

17 Q. Could you look at paragraph 12 of
18 Hiraishi marked as Exhibit 1005.

19 Let me know when you're there.

20 Do you see the heading "Brief Description 03:39:45
21 of the Drawings" in --

22 A. Yes, I -- yes, I do.

23 Q. And then do you see in paragraph 13,
24 there is a reference to a schematic diagram; and
25 then in paragraph 14, there's a reference to a 03:39:56



800.211.DEPO (3376)
EsquireSolutions.com

1 block diagram? 03:39:56

2 A. Yes.

3 Q. What's the difference between a schematic
4 diagram and a block diagram?

5 A. I don't know what they mean by the 03:40:06
6 difference here. Let me go back and see if I can
7 identify what I would consider a difference.

8 One view is that schematics often are
9 illustrating electrical components, like resistors
10 and transistors. 03:40:24

11 Oh, okay, yeah. This is -- so Figure 1
12 is more of a component, a physical component,
13 organization. It shows some nonfunctional blocks,
14 for example, nonfunctional elements. Whereas
15 Figure 2 is just focusing on major functional 03:40:41
16 element and the communications between them.

17 Q. And outside of Hiraishi, is it common to
18 distinguish between a schematic diagram and a block
19 diagram? Is that a distinction that you're
20 familiar with? 03:41:05

21 A. It's -- it's not uncommon. It's -- I
22 would say it's not unheard of, either, to use the
23 term to describe both. You know, here's a -- I
24 would feel fine if somebody turned to Figure 2 and
25 said, "Here's a schematic of, you know, the -- the 03:41:22



800.211.DEPO (3376)
EsquireSolutions.com

1 major components." 03:41:25
2 You know, Figure 1 is much less a block
3 diagram because it doesn't show just blocks. But
4 Figure 2 I could say is a schematic or a block
5 diagram. 03:41:40
6 Q. All right. But the way Hiraishi
7 describes it is Figure 1 is a schematic diagram,
8 and Figure 2 is a block diagram.
9 A. Yes, sir.
10 Q. Figure 5 is a block diagram, correct, in 03:41:51
11 Hiraishi?
12 A. If he describes it -- yeah, if he
13 describes it that way. He probably would.
14 It's sort of, I would say, halfway
15 between, because it does show blocks, but it also 03:42:07
16 does show what I would consider to be literal
17 circuits, like the tri-state buffers.
18 Q. But paragraph 17 of Hiraishi describes
19 Figure 5 as a block diagram, correct?
20 A. Let me see. Yes. 03:42:24
21 Q. Hiraishi does not describe Figure 5 as a
22 schematic diagram, correct?
23 A. Not in paragraph -- not in paragraph 17.
24 Q. And not elsewhere either, right?
25 A. I -- I don't recall. Like I said, to me, 03:42:47



800.211.DEPO (3376)
EsquireSolutions.com

1 in many cases the terms are interchangeable, 03:42:51
2 although there are situations where they're not.

3 Q. But Hiraishi doesn't use them
4 interchangeably, right? He either describes the
5 figure as a block diagram or a schematic diagram? 03:43:03

6 MR. LINDSAY: Objection. Form.

7 THE DEPONENT: Yeah, I don't know.
8 Hiraishi is -- describes it as -- as he describes
9 it.

10 In these paragraphs 12 through 17, he 03:43:12
11 appears to not be using them interchangeably.

12 Q. (By Mr. Chandler) So Figure 1, according
13 to Hiraishi, is a schematic diagram; Figure 2 is a
14 block diagram; Figure 5 is a block diagram;
15 Figure 6 is a block diagram; Figures 8A and 8B are 03:43:31
16 schematic diagram; Figures 9A and 9B are a
17 schematic diagram, according to Hiraishi.

18 Is that correct?

19 A. I'm going to trust that you repeated it
20 accurately. 03:43:48

21 I was going back and looking at Figure 4,
22 which he doesn't characterize as either. It's not
23 clear to me why he calls that a perspective view.
24 Figure 4 has got functional blocks, and it shows
25 communications paths between them. 03:44:02



800.211.DEPO (3376)
EsquireSolutions.com

1 So again, he describes them the way he 03:44:13
2 does. It's not clear to me in each of these cases
3 why he chooses those terms or, you know, what
4 significance there would be between one or the
5 other. 03:44:24

6 I would say Figure 4 is a block diagram
7 and it's a schematic.

8 Q. But that's not what Hiraishi says, right?

9 A. No, no. That's what I would say. Yeah.
10 I don't think his -- 03:44:36

11 Q. Right.

12 A. I don't think his terminology there is --
13 at least in those passages we've -- we've looked at
14 just now, his terminology is not clear, why -- why
15 he calls one -- one thing versus the other. 03:44:49

16 Q. But he clearly uses a different
17 description for different figures, right? Some are
18 schematic diagrams in his view, and some are block
19 diagrams in his view; is that fair?

20 MR. LINDSAY: Objection. Asked and 03:45:09
21 answered.

22 THE DEPONENT: Yeah, and some are
23 perspective views. And, you know, it could be the
24 case that, you know, he's calling one -- one as
25 being subsumed in his view by another. I don't 03:45:22



800.211.DEPO (3376)
EsquireSolutions.com

1 know exactly what -- what he means and what the 03:45:25

2 bounds are for what he means when he calls

3 something a schematic versus a block diagram.

4 Maybe block diagrams are all -- also schematics, or

5 vice versa. 03:45:39

6 Q. (By Mr. Chandler) Could you turn to

7 page 45 of your expert declaration marked as

8 Exhibit 2006.

9 Let me know when you're there.

10 A. Sure. 03:45:59

11 Q. You've annotated Figure 5 of Hiraishi on

12 page 45 of your declaration marked as Exhibit 2006,

13 correct?

14 A. Yes. I've added coloring. I don't think

15 there's any changes other than highlighting certain 03:46:12

16 paths and elements.

17 Q. In the upper right of Figure 5 of

18 Hiraishi, you've highlighted the data register

19 control circuit 320 in red, correct?

20 A. Yes, that's correct. 03:46:27

21 Q. The data register control circuit 320 in

22 Figure 5 of Hiraishi receives an input signal

23 labeled "DRC" at the top of the figure, correct?

24 A. Yes, I see that.

25 Q. And DRC is a signal coming from the 03:46:44



800.211.DEPO (3376)
EsquireSolutions.com

1 module controller on Hiraishi's memory module, 03:46:52
2 correct, as shown, for example, in Figure 7?

3 A. Yes.

4 Q. Does Figure 5 of Hiraishi show any other
5 input signals to block 320 besides the DRC signal 03:47:21
6 coming from the module controller?

7 A. Any other input -- input signals?

8 Q. That was my question.

9 A. Yeah, it's -- it's showing quite a few.

10 Oh, I'm sorry. Let me take a step back. 03:47:42
11 Could you repeat the question. I want to make sure
12 I'm oriented.

13 Q. Does Figure 5 of Hiraishi show any other
14 input signals to block 320 besides the DRC signal
15 from the module controller? 03:47:56

16 A. No, it does not.

17 Q. For example, does Figure 5 of Hiraishi
18 show block 320 receiving the DQS strobe signals
19 from lines 351 and 352?

20 A. No, it does not. 03:48:21

21 Q. Does Figure 5 of Hiraishi show block 320
22 receiving the DQ data signals from lines 341 and
23 342?

24 A. No, it does not.

25 Q. In forming your opinions about Hiraishi, 03:48:36



800.211.DEPO (3376)
EsquireSolutions.com

1 did you believe that the read leveling circuit 03:48:40
2 inside block 320 of Figure 5 does not receive any
3 information about the DQS strobe signals from line
4 351 and 352 or the DQ data signals from lines 341
5 and 342? 03:48:58

6 A. No, I wouldn't say that.

7 Q. Can you explain why not.

8 A. Sure. The DRC signal is configuring the
9 delay or configuring, for example, the -- the read
10 leveling, which is information about the DQS and DQ 03:49:19
11 signals.

12 Q. The DQS and DQ signals don't go to the
13 module controller though, right?

14 A. That's correct.

15 Q. And in your opinion, the DQS and DQ 03:49:38
16 signals don't go to block 320 of Figure 5 of
17 Hiraishi either, correct?

18 A. This doesn't show that. I don't know why
19 they would.

20 Q. So in forming your opinions about 03:49:53
21 Hiraishi, is it fair to say you believe that the
22 read leveling circuit inside block 320 of Figure 5
23 does not receive information about the DQS strobe
24 signals from lines 351 and 352 going to the memory
25 chip or from the DQ data signals, lines 341 and 03:50:21



800.211.DEPO (3376)
EsquireSolutions.com

1 342, going to the memory chip? 03:50:26

2 A. I think --

3 MR. LINDSAY: Objection. Form.

4 THE DEPONENT: Yeah. I think you said
5 information about those. And if that's -- if I 03:50:33
6 heard correctly. Again, like I said before, I
7 would disagree with that characterization.

8 Q. (By Mr. Chandler) So what information
9 about the DQS strobe signal and the DQ data signal,
10 in your opinion, goes to the read leveling circuit 03:50:48
11 inside block 320?

12 A. Information that comes over the DRC
13 signals.

14 Q. And how does the DRC signal know anything
15 about the DQS strobe signal or the DQ data signal? 03:51:04

16 A. Well, I can talk about how that's often
17 done. I haven't really focused on that with
18 regards to Hiraishi, how Hiraishi does it. But the
19 whole intent is to account for the skew that fly-by
20 introduces. 03:51:28

21 Q. Okay.

22 A. So during S4 training, it accounts for
23 the skew the fly-by introduces, and that skew
24 particular to each DRAM chip is directly related --
25 is information that's directly related to when the 03:51:43



800.211.DEPO (3376)
EsquireSolutions.com

1 DQ and DQ strobe signals will be generated. 03:51:47

2 Q. So in your opinion, the read leveling
3 circuit inside block 320 of Figure 5 of Hiraishi
4 will receive information about the DQS strobe
5 signals and the DQ data signals, correct? 03:52:05

6 A. Yes. It needs that in order, at least in
7 part, to know when to turn on the input buffers.

8 Q. But in your opinion, the read leveling
9 circuit inside block 320 of Figure 5 of Hiraishi
10 does not receive the DQS strobe signal itself from 03:52:33
11 lines 351 and 352 and does not receive the DQ data
12 signal from lines 341 and 342, correct?

13 MR. LINDSAY: Objection. Form.

14 THE DEPONENT: Yeah, Figure 5 does not
15 show it receiving either of those signals. I'm not 03:52:53
16 relying on the notion that it receives either one
17 of those signals. I don't know why it would need
18 to receive either one of those signals.

19 So I would agree with you, barring
20 there's some weird part of Hiraishi that neither I 03:53:08
21 nor Dr. Wedig have discussed, where they discuss,
22 "Oh, we could do something interesting with -- with
23 those signals." But I don't think that it's
24 receiving them, no.

25 Q. (By Mr. Chandler) And that's the 03:53:22



800.211.DEPO (3376)
EsquireSolutions.com

1 understanding that you've used in forming your 03:53:22
2 nonobviousness opinions, correct?

3 A. Yes, that's correct.

4 Q. And the module controller does not
5 receive the DQS strobe signals or the DQ data 03:53:36
6 signals from any of the memory chips, correct?

7 A. That's correct.

8 Q. So the module controller doesn't know
9 about any of the timing of the DQS strobe signals
10 or the DQ data signals coming out of the memory 03:53:56
11 chips on the memory module, correct?

12 A. It might. That information is generally
13 presented to it, but simply to pass along. I don't
14 know why it would retain that information or what
15 use it would make out of it. 03:54:14

16 Q. Why do you say -- so I'm a little
17 confused, because a moment ago you told me that the
18 DQS strobe signal and the DQ data signal, it
19 doesn't go to the module controller and it doesn't
20 go to the read leveling circuit. 03:54:26

21 So how would either the read leveling
22 circuit or the module controller know anything
23 about these DQS strobe signals and DQ data signals
24 that go directly from memory chip to the data
25 buffer? 03:54:42



800.211.DEPO (3376)
EsquireSolutions.com

1 A. My son's name is Ryan. Have you ever met 03:54:47
2 Ryan? No. But I just told you something about
3 him. The -- the data buffer knows to do read
4 leveling by virtue of knowing something about the
5 DQ and DQS signals. That doesn't mean it has to 03:55:04
6 get them.

7 It's -- you, I think, have consistently,
8 at least several times, said "any information about
9 them." That's different from knowing them.

10 So both the module controller receives 03:55:18
11 information about the timing of DQS and DQ, as does
12 the -- the data buffer, but -- as does the element
13 320 of the data buffer. But doesn't require that
14 they actually receive those signals directly or
15 even indirectly. 03:55:41

16 Q. If it doesn't receive it directly or
17 indirectly, how does it receive?

18 A. It doesn't have to receive it. It has to
19 receive -- you asked me information about it, not
20 it. That -- it receives information about it. It 03:55:57
21 knows the data buffer that's closest to the -- the
22 midline on the DIMM has its read leveling
23 programmed such that it knows that the fly-by
24 delays for that DRAM chip will be relatively small.
25 And the one that's all the way far on the left has 03:56:21



800.211.DEPO (3376)
EsquireSolutions.com

1 different read leveling levels programmed into it 03:56:24
2 that indicate a different delay value for the
3 RDRAMs, and those values get programmed through the
4 module controller.

5 So the -- the information about the 03:56:35
6 delays per column of the DRAMs goes through the
7 module controller and goes to the data buffers.

8 Q. And that's done before -- that's done
9 regardless of the actual DQS and DQ signals coming
10 out. That's based on the physical layout of the 03:57:04
11 memory module, correct?

12 MR. LINDSAY: Objection. Form.

13 THE DEPONENT: Yeah. It's -- it's
14 largely based on the -- on the physical layout as
15 well as some dynamic issues. As these things get 03:57:16
16 hot, their performance changes. But the
17 fundamental issue that's trying to be addressed
18 here is the physical layout.

19 Q. (By Mr. Chandler) Okay. So during the
20 S4 read leveling itself, you believe that the read 03:57:29
21 leveling circuit inside block 320 does not receive
22 the DQS strobe signals from lines 351 and 352 and
23 does not receive the DQ data signals from lines 341
24 and 342, correct?

25 MR. LINDSAY: Objection. Asked and 03:57:52



800.211.DEPO (3376)
EsquireSolutions.com

1 answered. Form. 03:57:52

2 THE DEPONENT: Yes. As far as I know,
3 element 320 does not receive the DQ or DQS signals
4 either during the S4 read level training or during
5 what I would characterize as normal operations. 03:58:09

6 Q. (By Mr. Chandler) And that's the
7 understanding that you used when forming your
8 nonobviousness opinions?

9 A. I would -- I would say so. But it really
10 didn't enter into the analysis at all, where they 03:58:25
11 draw a box -- to label this. I mean, Dr. Wedig, I
12 don't think, relied on whether that was the case or
13 not. I -- I believe it's the case that those
14 signals are not received, but it's not really
15 something that occurred to me. It's not shown 03:58:45
16 here. I don't know why it would happen, but I
17 guess it could.

18 Q. In forming your opinions about Hiraishi
19 with respect to S4 write leveling, you believe that
20 the write leveling circuit inside block 320 of 03:59:02
21 Figure 5 does not receive the DQS strobe signals
22 from lines 351 and 352 or the DQ data signals from
23 lines 341 and 342, correct?

24 MR. LINDSAY: Objection. Beyond the
25 scope of direct. Form. 03:59:20



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: Yeah. I -- I -- really, 03:59:25
2 we've been talking about the read path, not the
3 write path. I -- I don't have a complete
4 characterization of everything that Hiraishi does,
5 but -- DQ, DQS... 03:59:39

6 Again, I don't -- I don't see any path
7 that goes from DQS 350 and DQ 340 into block 320.
8 I haven't relied on it either being present or not,
9 such -- such communications either being present or
10 not present. I'm not aware of why those signals 04:00:20
11 would need go in there.

12 Q. (By Mr. Chandler) Turn to page 27 of
13 your expert declaration marked as Exhibit 2006.

14 Let me know when you're there?

15 A. Will do. 04:00:34

16 Q. In paragraph 55 of your expert
17 declaration, you discuss S4 write leveling in
18 Hiraishi, and you've annotated Figures 14A and 14B
19 as part of that discussion, correct?

20 A. Yes. 04:00:51

21 Q. So I want to introduce an exhibit just
22 for sort of easy of reference.

23 MR. CHANDLER: This will be Exhibit 1051.

24 (Exhibit 1051 was marked for
25 identification by the Court Reporter and is 04:01:05



800.211.DEPO (3376)
EsquireSolutions.com

1 attached hereto.) 04:01:05
2 Q. (By Mr. Chandler) Let me know when you
3 have it.
4 A. Will do. Okay.
5 Q. So Exhibit 1051 shows Figure 5 of 04:01:22
6 Hiraishi in the upper left; Figures 14A and 14B of
7 Hiraishi in the upper right, as annotated by you;
8 and then paragraphs 142 through 146 of Hiraishi
9 along the bottom.
10 Understood? 04:01:39
11 A. Yes.
12 Q. And Figures 14A and 14B of Hiraishi
13 explain the S4 write leveling operation that takes
14 place in Hiraishi's data register buffer 300 in
15 Figure 5, correct? 04:01:57
16 A. Yes.
17 Q. And Figure 14A shows before write
18 leveling, and Figure 14B shows after write
19 leveling, correct?
20 A. Yes. 04:02:26
21 Q. What's the goal of Hiraishi's S4 write
22 leveling? What are you trying to accomplish?
23 A. The goal is to allow the -- in essence,
24 it's the same goal as with read leveling. It's to
25 allow the receiver of the data to reliably sample 04:02:45



800.211.DEPO (3376)
EsquireSolutions.com

1 it. 04:02:50

2 Q. And what signal is being leveled
3 according to Figures 14A and 14B in Hiraishi's S4
4 write leveling?

5 A. I don't -- I don't know. I don't think 04:03:05
6 of it as a signal being leveled.

7 Could you rephrase the question.

8 Q. What signal is being delayed in
9 Hiraishi's S4 write leveling to permit reliable
10 sampling of the data, as you stated a moment ago? 04:03:30

11 MR. LINDSAY: Objection. Form.

12 THE DEPONENT: Yeah. Hold on a second.

13 "What signal is being delayed"? So no
14 signal is being delayed.

15 Q. (By Mr. Chandler) So after S4 write 04:04:18
16 leveling in Hiraishi, your opinion is that no
17 signal coming out of the data buffer is delayed in
18 comparison to before the write leveling operation
19 was performed; is that correct?

20 A. Well, we've been only talking about two 04:04:39
21 signals. Yeah, let me take a step back.

22 We've been talking about two signals,
23 the -- the DQ signal and the DQS. So, again, I
24 tripped myself up. There -- there is a plurality
25 of clock cycle delay for the DQ signal based on 04:04:55



800.211.DEPO (3376)
EsquireSolutions.com

1 FIFO 301. But then the DQS signal terminates at 04:05:02
2 301.

3 Q. Figure 14A, in comparison to Figure 14B,
4 shows that there's been a change in the timing of
5 at least one of the signals, right? 04:05:27

6 A. No, I -- I don't think so. What are
7 you -- what are you pointing to?

8 Q. I'm pointing to what you're pointing to,
9 which is, your annotations show that given the
10 change in the timing, when DQS(IN) transitions, in 04:05:42
11 one instance, DQ(OUT) is high; in the other
12 instance, DQ(OUT) is low, right?

13 A. When DQ in -- when DQS transitions, you
14 said?

15 Q. Yes. 04:06:17

16 A. Okay.

17 Q. In paragraph 145 of Hiraishi teaches that
18 the write leveling circuit 322 of the data register
19 buffer 300 changes an output timing of the data
20 strobe signal DQS, correct? 04:06:40

21 A. Yeah, but that's not delaying it. It
22 generates the output timing.

23 Q. And it changes it. It delays the signal
24 in the sense that it's changing its relative phase
25 compared to the clock signal, right? 04:07:03



800.211.DEPO (3376)
EsquireSolutions.com

1 MR. LINDSAY: Objection. Asked and 04:07:06
2 answered.

3 THE DEPONENT: No. Absolutely not. No.
4 That is not how it works. It's not changing it.
5 It didn't exist before. It's creating it. And so 04:07:16
6 it's not delaying it relative to something else.
7 It's just determining when it should be sent.

8 Q. (By Mr. Chandler) It's changing the
9 output timing, right?

10 A. No. There was no output timing until it 04:07:29
11 created it. It's not changing it from anything.

12 Q. It's changing --

13 A. It's not delaying it from anything. It's
14 just determining it.

15 Q. It's changing it from Figure 14A to 04:07:39
16 Figure 14B, right?

17 A. Maybe we are looking at two different
18 things.

19 Okay. So we're looking at DQS(OUT).
20 Well, yeah, but -- but even if it is, these -- 04:08:00
21 these are two different time periods. It's --
22 it's -- there is no DQS(OUT) signal that then is
23 delayed or that has timing which is then changed.

24 Q. During write leveling, during Hiraishi's
25 S4 write leveling -- 04:08:26



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yeah. 04:08:30
2 Q. -- what signal is Hiraishi's data buffer
3 sending to the memory chip?
4 A. So it's sending to the -- the data buffer
5 is sending to the memory chips DQ and DQS. 04:08:45
6 Q. Are you sure about that?
7 A. During -- during the S4 write level
8 training period? Sure. It's -- it's trying to do
9 a write with its current configuration, and then
10 the -- whether the write actually succeeded is 04:09:03
11 going to be checked.
12 Q. And that's on -- in Figure 14A, you see
13 there's DQS(OUT) for the data register buffer?
14 A. Yes.
15 Q. So Figure 14A shows that Hiraishi's data 04:09:26
16 buffer is sending to the memory chip the DQS(OUT)
17 signal, correct?
18 A. Yes.
19 Q. During S4 write leveling, Hiraishi's data
20 buffer does not send a DQ data signal to the memory 04:09:48
21 chip. The DQ data signal is an incoming data
22 signal from the memory chip, right? Or do you not
23 know?
24 A. During -- during write leveling, what has
25 to happen is you have to check and see if the 04:10:06



800.211.DEPO (3376)
EsquireSolutions.com

1 current configuration can reliably write data to 04:10:10
2 the memory. So you -- you write -- you write data.
3 You send DQ data to the memory, and then you turn
4 it around and you read it back, and you see if what
5 you got back is what you wrote. And if you don't, 04:10:24
6 if it's not, you indicate an error, and somebody
7 adjust the timing.

8 At least that's the only way I know write
9 leveling can work. But -- the training part, yeah.

10 Q. During S4 write leveling, the memory chip 04:10:43
11 sends back to Hiraishi's data buffer a signal on
12 the DQS(IN) line, correct?

13 A. Unless I'm reading this --

14 Q. I'm sorry. I apologize.

15 During Hiraishi's S4 write leveling, the 04:11:14
16 memory chip sends a signal back to the data
17 register buffer on the DQ line. And so when that
18 signal comes out of the memory chip, it's described
19 as DQ(OUT); and when it goes into the data register
20 buffer, it's described as DQ(IN), correct? 04:11:36

21 A. Maybe I'm just reading this wrong. I --
22 I don't think so. I believe this is saying -- I
23 thought this was saying DQS(IN) is the signal
24 coming in from memory controller to data buffer,
25 and DQS(OUT) is the signal going out of the data 04:11:59



800.211.DEPO (3376)
EsquireSolutions.com

1 buffer to the memories. 04:12:02

2 Q. Now you've confused me, because you
3 started introducing the memory controller.

4 There's --

5 A. Yeah. 04:12:08

6 Q. There's no memory controller in S4 write
7 leveling. It's just between the data register
8 buffer and the memory chip, correct?

9 A. There's -- there's a memory controller
10 that's intimately involved in it. 04:12:17

11 Q. You told me previously that in S4 write
12 leveling, that's performed by the data register
13 buffer, and then separately, there's S5 write
14 leveling that's performed by the system memory
15 controller, correct? 04:12:34

16 A. No.

17 Q. Figure 14 --

18 A. The -- S4 is doing read and write
19 leveling between the data buffer and -- and the
20 DRAMs. That doesn't mean that those are the only 04:12:47

21 two components involved. It's -- it's accounting
22 for the fly-by errors introduced there. Similarly,
23 S5 is between the memory controller and the -- and
24 the data buffers. But that doesn't that mean that
25 the DRAMs aren't involved there. They are. 04:13:02



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Figure 14A only shows the data register 04:13:05
2 buffer and the memory chip, correct?

3 A. It has labels for those two components,
4 yes.

5 Q. And same with Figure 14B? 04:13:19

6 A. Yes. Yes, that's true as well.

7 Q. Figures 14A and 14B, which are describing
8 Hiraishi's S4 write leveling, only show that the
9 memory chip is sending a signal on the DQ line back
10 to the data register buffer, correct? 04:13:58

11 MR. LINDSAY: Objection. Asked and
12 answered.

13 THE DEPONENT: So it's my understanding
14 that this is talking about how the write leveling
15 is used. This is how operations happen. 04:14:16

16 Hiraishi doesn't really talk about --
17 much at all that I can recall about how read or
18 write leveling, the training, is actually
19 accomplished, which is why I said I think the
20 DQ(IN) is coming in from the memory controller and 04:14:36
21 going -- and the DQ(OUT) is going the other way.

22 But like I said, maybe I'm just reading
23 it wrong.

24 Q. (By Mr. Chandler) I think you're reading
25 it wrong. I mean, paragraphs 142, 143, et cetera, 04:14:45



800.211.DEPO (3376)
EsquireSolutions.com

1 are describing what you characterize as the 04:14:48
2 training for write leveling. They're not
3 describing a normal write operation. They're
4 describing what happens during S4 write leveling
5 to, as you describe it, train the data register 04:15:06
6 buffer to change the output timing that's described
7 in paragraph 145 of the data strobe signal DQS,
8 correct?

9 A. No, I don't -- I mean, it just says --
10 and this is one of my frustrations. I think I 04:15:36
11 understand it. But, you know, I would have
12 preferred if he had said something like "read/write
13 leveling training." Because during regular
14 operations, when you do a read, you do read
15 leveling. You're not training. You're using the 04:15:53
16 read leveling training.

17 So this is -- I think the way he's using
18 "write leveling" here is just talking about doing a
19 regular write operation. Because there's -- I
20 don't think there's any discussion of detecting an 04:16:11
21 error and sending a signal back. Maybe there is
22 and I just missed it.

23 Q. Okay. So when forming your opinions, you
24 understood Figures 14A and 14B and the associated
25 discussion in Hiraishi to be describing a regular 04:16:29



800.211.DEPO (3376)
EsquireSolutions.com

1 write operation as opposed to the training involved 04:16:33
2 for write leveling; is that fair?

3 A. I -- I think this is doing write leveling
4 based on the results of the training, yeah.

5 Q. So in forming your opinions, you did not 04:17:01
6 understand Figures 14A and 14B as doing the
7 training needed for write leveling. Instead, you
8 understood Figures 14A and 14B as write operations
9 later on that take advantage of the results of that
10 training; is that correct? 04:17:32

11 A. Yeah, because if it was a training, you
12 would be showing the memory chip having DQ
13 inputting data and outputting data.

14 Q. And in your opinion, Figures 14A and 14B
15 don't show inputting data and outputting data? 04:18:09

16 A. Well, there's only DQ(OUT) labeled, so I
17 think that they're just focusing on one signal
18 called DQ(OUT), or one set of logical signal as
19 DQ(OUT).

20 Q. But there's also DQ(IN), right? 04:18:30

21 A. To the memory chip?

22 Q. On the data register buffer, there's a
23 signal going out called DQS, and there's a signal
24 coming in called DQ. In the memory chip, there's a
25 signal coming in called DQS, and there's a signal 04:18:45



800.211.DEPO (3376)
EsquireSolutions.com

1 going out called DQ, right? 04:18:48

2 A. Yeah. The data buffer generates the
3 DQS(OUT), and it -- it receives, during a -- during
4 a regular write operation, DQ(IN) from the memory
5 controller. 04:19:05

6 Q. Okay. But to be clear, your
7 understanding of Figures 14A and 14B is that those
8 show a regular write operation; they're not showing
9 the training that would take place during
10 initialization of the memory module. 04:19:18

11 A. Give me -- give me just one moment to
12 finish refreshing my memory.

13 Yeah, I'm sorry. No. This is describing
14 the training. You're right.

15 Q. Okay. During Hiraishi's S4 write
16 leveling, the data buffer sends a strobe signal on
17 what's labeled DQS(OUT) to the memory chip,
18 correct? 04:20:08

19 A. Yes.

20 Q. And then during Hiraishi's S4 write
21 leveling, the memory chip sends back to the data
22 register buffer 300 a signal on the line DQ,
23 correct? 04:20:28

24 A. Yes.

25 Q. And when that signal leaves the memory 04:21:00



800.211.DEPO (3376)
EsquireSolutions.com

1 chip, it's labeled DQ(OUT), and when that same 04:21:02
2 signal arrives at the data register buffer, it's
3 labeled DQ(IN) in Figures 14A and 14B of Hiraishi,
4 correct?

5 A. Yes. 04:21:18

6 Q. And in your opinion, Hiraishi's write
7 leveling circuit in block 320 does not receive the
8 signal that comes back from the memory chip on the
9 DQ line, correct?

10 A. Yeah, let me see. 04:21:38

11 Yeah, I don't think it receives the DQ
12 signal. 320 doesn't receive the DQ signal. But
13 let me -- having my recollection be wrong once, let
14 me read a little more carefully.

15 Yeah. So the end of paragraph 146 says 04:22:17
16 as "a result of the write leveling" -- "a result of
17 the write leveling operation is stored in the data
18 register control unit 320." [as read]

19 So there does have to be -- well, yeah,
20 it says that. It doesn't say it's receiving the DQ 04:22:36
21 directly or indirectly.

22 Q. In your opinion, does Hiraishi's write
23 leveling circuit in block 320 receive the signal on
24 DQ from the memory chip during S4 write leveling?

25 A. I think we've talked about this a couple 04:23:23



800.211.DEPO (3376)
EsquireSolutions.com

1 of times. But having been wrong once, let me 04:23:24
2 restate my opinion.

3 320, there's no signal paths shown here
4 for 320 to receive the -- the DQ values, the DQ
5 signals. I don't know why it would. I don't 04:23:46
6 recall Hiraishi discussing that. But, you know, it
7 doesn't change my opinion one way or another
8 whether it does or not.

9 Q. Is it possible, in your opinion, that
10 Figure 5 does not show every connection and that, 04:24:11
11 in fact, the DQ signal that comes from the memory
12 chip does go to block 320 and is used by the write
13 leveling circuit 322? Is that a possible
14 understanding of Hiraishi, in your opinion?

15 MR. LINDSAY: Objection. Form. 04:24:39

16 THE DEPONENT: No, Hiraishi doesn't
17 disclose anything that would require that, explain
18 how it would -- would be used. No. I can't
19 imagine that. I -- I don't know what it would
20 possibly do with that information. 04:24:55

21 Q. (By Mr. Chandler) That's why I wanted to
22 be clear.

23 So your opinion is that it's not
24 possible, and it wouldn't -- not make any sense, in
25 your view, for the signal from the memory chip sent 04:25:04



800.211.DEPO (3376)
EsquireSolutions.com

1 over DQ during S4 write leveling to go to the write 04:25:11
2 leveling circuit in block 320 of the data register
3 buffer 300, correct?

4 MR. LINDSAY: Objection. Form.

5 THE DEPONENT: It is absolutely possible. 04:25:29
6 I could design this any way I wanted. I don't see
7 any purpose. And in context of Hiraishi, I don't
8 think it's possible, because I think if it was
9 done, they would have discussed it.

10 I think what's -- what's not discussed is 04:25:43
11 always possible, but, you know, when I'm looking at
12 this art, I consider it in the context of what it
13 discloses and what a person of ordinary skill in
14 the art would understand.

15 Is it possible that that's done? Yes. 04:25:56
16 For what reason? I have no idea. Is there any way
17 to -- to suspect they would do it? Not that I'm
18 aware of.

19 Q. (By Mr. Chandler) Would it be obvious
20 for a write leveling circuit to use the signal 04:26:07
21 coming back from the memory chip on the DQ line as
22 part of write leveling, in your opinion?

23 A. The way Hiraishi is constructed, it would
24 not be obvious for 320 to use either DQ or DQS.
25 There is no rational explanation for any use that 04:26:34



800.211.DEPO (3376)
EsquireSolutions.com

1 it would make -- that I -- that I have -- that I 04:26:39
2 could imagine or that I've heard anybody talk
3 about.

4 So not only is it not obvious. I have no
5 idea why anybody, even with hindsight, would do 04:26:46
6 that.

7 Q. And that's the understanding that you
8 used in forming your nonobviousness opinions,
9 correct?

10 A. That is my understanding. That was my 04:26:59
11 understanding when I formed those opinions.

12 But as I said, Dr. Wedig, as far as I
13 recall, didn't introduce that. So I -- this is not
14 something I sat down, "Okay, I need to get this
15 issue straight in my mind." 04:27:15

16 I've got an understanding of Hiraishi, I
17 looked at the arguments he made, and I responded to
18 them.

19 MR. LINDSAY: I just want to see -- we've
20 been going awhile -- if there was a breaking point 04:27:31
21 coming up?

22 MR. CHANDLER: Soon.

23 Q. (By Mr. Chandler) The last sentence in
24 paragraph 144 of Hiraishi states that "the signal
25 DQ is input to the data register buffer 300, by 04:27:44



800.211.DEPO (3376)
EsquireSolutions.com

1 which the data register buffer 300 can find a 04:27:51
2 direction of phase shift of the clock signal CK and
3 the data strobe signal DQS," correct?

4 And this is all in the context of S4
5 write leveling. 04:28:09

6 A. That's -- that is literally what it says,
7 yeah.

8 Q. And, in your opinion, that is done
9 without the DQ signal going into block 320 of
10 Hiraishi's data register buffer 300, shown in 04:28:29
11 Figure 5?

12 A. Yeah. I mean, even if it went into
13 there, it couldn't determine the direction of the
14 phase shift.

15 MR. CHANDLER: Okay. Why don't we take a 04:28:49
16 short break.

17 MR. LINDSAY: Sounds good.

18 THE VIDEOGRAPHER: We are going off the
19 record. The time is 4:29.

20 (Recess taken.) 04:28:58

21 THE VIDEOGRAPHER: We going back on the
22 record. The time is 4:41.

23 Q. (By Mr. Chandler) Dr. Mangione-Smith,
24 could you look at Exhibit 2007, which I put in the
25 chat in case you don't have it handy. 04:41:40



800.211.DEPO (3376)
EsquireSolutions.com

1 A. I will let you know once I have it open. 04:41:48
2 Yes, I see it.
3 Q. Exhibit 2007 is the "Joint Claim
4 Construction Chart" that was filed in the
5 Eastern District of Texas on September 30th, 2022, 04:42:14
6 correct?
7 A. Yes.
8 Q. And if you go to page 10 of Exhibit 2007.
9 Let me know when you're there.
10 A. PDF or numbered page 10? 04:42:42
11 Q. Numbered in the bot- --
12 A. Sorry.
13 Q. Numbered in the bottom right corner. So
14 "Netlist Exhibit 2007, p.10." [as read]
15 A. Got it. Yes, I'm there. 04:42:57
16 Q. And do you see that in district court,
17 the parties agreed that the proper construction for
18 the phrase "one or more or previous operations" in
19 the '506 patent should be "one or more previous
20 memory operations"? 04:43:09
21 A. Yes, I see that.
22 Q. Okay. Do you agree with that claim
23 construction?
24 MR. LINDSAY: Objection. Outside the
25 scope of direct. 04:43:20



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: I haven't really 04:43:23
2 considered it. I haven't read any arguments behind
3 it or -- yeah.

4 Q. (By Mr. Chandler) Do you disagree with
5 it? 04:43:32

6 MR. LINDSAY: Objection. Outside the
7 scope of direct.

8 THE DEPONENT: I -- I don't have an
9 opinion as I sit here. Claim construction, I -- I
10 don't recall looking at that claim construction 04:43:40
11 term previously. Maybe I did.

12 Let me see.

13 Q. (By Mr. Chandler) And to be clear, I
14 don't see a section in your declaration on claim
15 construction. But I just want to make sure whether 04:44:08
16 or not you're offering any opinions on claim
17 construction, including specifically for this
18 phrase, "one or more previous operations."

19 A. No, I'm not.

20 Q. All right. Do you have any opinion on 04:44:23
21 whether or not the claim limitation "one or more
22 previous operations" can include or must exclude
23 operations related to read leveling and write
24 leveling?

25 MR. LINDSAY: Objection. Outside the 04:44:44



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of direct. 04:44:44
2 Q. (By Mr. Chandler) Do you have any
3 opinion on that?
4 A. No, I haven't considered it.
5 Q. Okay. So as a claim construction matter, 04:44:50
6 you don't have any opinion on that issue?
7 A. To the best of my recollection, yeah.
8 Q. Could you turn to page 69 of your expert
9 declaration marked as Exhibit 2006.
10 And do you see that you've annotated 04:45:21
11 Figure 5 of Hiraishi at the top of page 69 of
12 Exhibit 2006?
13 A. Yes, I see that. Yes. That's right.
14 Yeah.
15 Q. Toward the left side of Figure 5 of 04:45:34
16 Hiraishi, do you see there's a strobe generating
17 circuit 376?
18 A. Yes.
19 Q. Figure 5 of Hiraishi only shows one input
20 to the strobe generating circuit 376, and that's 04:45:45
21 the clock signal "LCLKR," correct?
22 A. Yes, that's what it shows.
23 Q. How would you pronounce "LCLKR"?
24 A. I guess it's local clock read. But I --
25 I don't know that I would -- I try to not pronounce 04:46:10



800.211.DEPO (3376)
EsquireSolutions.com

1 it, I guess. 04:46:12

2 Q. The clock signal LCKLR [sic] is a
3 periodic signal, as we discussed previously,
4 correct?

5 MR. LINDSAY: Objection. Misstates prior 04:46:27
6 testimony.

7 THE DEPONENT: Yeah, I think we talked
8 about clocks being periodic. I assume that signal
9 is an ordinary clock and that it is also periodic.

10 Q. (By Mr. Chandler) In your opinion, does 04:46:40
11 the strobe generating circuit 376 need any other
12 inputs besides the clock signal LCKLR to function
13 properly.

14 A. Hiraishi doesn't appear to think that
15 there's anything significant worth mentioning. 04:47:02
16 There's nothing that I'm aware of.

17 The output buffer shown to the left of it
18 can be used effectively to turn it on or off,
19 although alternatively, you could have incorporated
20 that as an input to the strobe generating circuit 04:47:19
21 and thought of it that way.

22 Q. But the way that Figure 5 of Hiraishi is
23 set up, the LCKLR signal would cause the strobe
24 generating circuit 376 to always output a strobe
25 signal, and then it's up to the output buffer to 04:47:56



800.211.DEPO (3376)
EsquireSolutions.com

1 either permit that signal to pass through or to 04:47:59
2 essentially block that signal; is that fair?

3 MR. LINDSAY: Objection. Form.

4 THE DEPONENT: Let me go back and review
5 exactly what it says about 376 and the rest of the 04:48:10
6 disclosure. That seems to be the case, but going
7 simply off of my recollection.

8 Yeah. It doesn't seem to identify any
9 other input. It's -- it's not equating it. I'm --
10 I'm looking at paragraph 84 where it says that the 04:49:07
11 "strobe generating circuit 376 generates a data
12 strobe signal DQS to be supplied to the data
13 connector 120, in synchronization with an internal
14 clock that is generated by a DLL circuit."

15 [as read] 04:49:31

16 So it is synchronized. It says it's a
17 strobe signal, which suggests that it's not the
18 local clock, but it doesn't say exactly how it
19 would be modified. Or at least it suggests to me
20 that it's some -- it's not just the local clock. 04:49:46

21 Q. (By Mr. Chandler) I'm sorry. When you
22 say "it's not just the local clock," what do you
23 mean by "it"? So what is not just the local clock?

24 A. The output. The strobe that it
25 generates. 04:50:00



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Can you state affirmatively your 04:50:05
2 understanding of what Figure 5 shows in Hiraishi
3 with the respect to the strobe generating circuit
4 376, how it works.

5 A. Sure. It -- the strobe generating 04:50:20
6 circuit gener- -- well, it says it generates an
7 output strobe. I think that that's not quite
8 accurate as far as I can tell, because in which
9 case you might not need the output buffer. But the
10 combination of the strobe generating circuit and 04:50:41
11 the output buffer forms a DQS.

12 Q. And what's the relevance of the LCLKR
13 clock signal to the strobe generating circuit 376?

14 A. Well, that's used to allow the DQ and the 04:51:09
15 DQS signals leaving to the left of the Figure 5 to
16 be edge-aligned.

17 Q. From the perspective of the strobe
18 generating circuit 376, can the clock signal LCLKR
19 be delayed by more than one clock cycle? Or does
20 that not make sense because the rising edge of the 04:51:47
21 clock cycle will look the same either way?

22 A. Well, it's -- it's not delayed at all.
23 It's just generated.

24 Q. But the DLL circuit can essentially shift
25 the clock circuit LCLKR, correct? 04:52:30



800.211.DEPO (3376)
EsquireSolutions.com

1 A. No. 04:54:56

2 Q. So in your opinion, strobe generating
3 circuit 376 does not ever receive a delayed clock
4 cycle L -- sorry -- clock signal LCLKR, correct?

5 A. I'm sorry. I think you -- could you 04:55:32
6 repeat that. I think you might have mispronounced,
7 or maybe I misheard, which one of the clocks you
8 were thinking of.

9 Q. I'm going to focus back on the left clock
10 in the read direction, 376. 04:55:44

11 A. Got it.

12 Q. So in your opinion, the clock signal
13 LCLKR is not delayed, period, correct?

14 A. No, it is delayed. From the point of
15 view of the strobe generating circuit 376, it's not 04:56:05
16 delayed.

17 Q. How much is the clock signal LCLKR
18 delayed by?

19 A. However much, presumably, 310 is
20 configured to implement. And it -- it's phase 04:56:30
21 delayed typically from CK, although the -- it could
22 be a multiple in which case it's not just delayed.

23 Q. But if 310 delays the clock signal LCLKR
24 by more than one clock cycle, the strobe generating
25 circuit 376 won't know that because every rising 04:57:01



800.211.DEPO (3376)
EsquireSolutions.com

1 edge looks the same, correct?

04:57:10

2 A. If it delays it by half of a clock cycle,
3 376 won't know it for exactly the same reason. It
4 doesn't know that the signal was delayed at all.

5 Q. DLL circuit 310 cannot delay clock cycle
6 LCLKR by a phase of more than 360 degrees, correct?

04:57:24

7 A. Yeah, I guess -- I guess that's accurate.
8 It could delay it for a greater period of time, but
9 it's -- the multiples will disappear out.

10 (Exhibit 1050 was marked for
11 identification by the Court Reporter and is
12 attached hereto.)

04:57:58

13 MR. CHANDLER: Let me introduce a new
14 exhibit, which will be 1050. I will put it in the
15 chat.

04:58:32

16 Q. (By Mr. Chandler) Let me know when you
17 have it.

18 A. All right. I have it.

19 Q. Exhibit 1050 shows, for convenience,
20 several figures from Hiraishi as well as several
21 paragraphs for easy of reference.

04:59:00

22 In particular, in the upper left, there's
23 Figure 5 of Hiraishi. In the upper right, there's
24 Figure 15 of Hiraishi. Towards the bottom right,
25 there's Figure 11 of Hiraishi. And then on the

04:59:15



800.211.DEPO (3376)
EsquireSolutions.com

1 bottom left and the bottom, there's paragraphs 147,
2 150, 151, 123 and 130 of Hiraishi. 04:59:20

3 Understood?

4 A. Yes.

5 Q. Figure 15 of Hiraishi explains the 04:59:32
6 S4 read leveling operation that takes place in
7 Hiraishi's data register buffer 300 in Figure 5,
8 correct?

9 A. Yes, it says it's a timing chart for
10 explaining the read leveling operation between the 05:00:04
11 data register buffer 300 and the memory chip 200.

12 Q. And the timing operation for S4 read
13 leveling is performed by the read leveling circuit
14 323 shown in Figure 5, according to paragraph 147
15 of Hiraishi, correct? 05:00:27

16 A. That's what it says.

17 Q. If Figure 15 of Hiraishi, each data
18 register buffer receives a read command at time
19 zero, which I've sort of highlighted in a red box
20 in Exhibit 1050, correct? 05:00:46

21 A. I'm sorry. Could you reorient me again
22 or repeat the question.

23 Q. Yeah, sure. First let me just sort of
24 get you looking at it. And then let me know when
25 you're looking, and then I'll ask the question. 05:00:54



800.211.DEPO (3376)
EsquireSolutions.com

1 So I'm sort of focused on Figure 15, 05:00:55
2 which is kind of the upper right of Exhibit 1050.
3 And I'm focused on the date of register buffer,
4 which is sort of the bottom half of Figure 15.
5 I've highlighted in blue where it says "data 05:01:07
6 register buffer," as opposed to the top half of
7 Figure 15, it says "memory chip" highlighted in
8 green.
9 Are you with me?
10 A. Yep, I'm with you. 05:01:16
11 Q. In Figure 15 of Hiraishi, each data
12 register buffer receives a read command at time T0
13 as shown in the red box that I've added to
14 Exhibit 1050, correct?
15 A. Yes. 05:01:37
16 Q. In Figure 15 of Hiraishi, there is a
17 time "A," which I have highlighted with a blue box
18 in Exhibit 1050, correct?
19 A. Yes, I see that.
20 Q. According to Figure 15 of Hiraishi, data 05:01:54
21 buffer 300-0 will receive the DQ data signal from
22 memory shift 200-0 in a shorter amount of time than
23 data buffer 300-4 will receive its DQ data signal
24 from memory chip 200-19.
25 Correct? 05:02:18



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes, I see. 05:02:18

2 Q. So, for example, data buffer 300-0
3 receives the DQ data signal from its memory chip at
4 around time T5 plus about one-quarter; whereas data
5 buffer 300-4 receives the DQ signal from its memory 05:02:37
6 chip at around time T5 plus about three-quarters.

7 Is that a reasonable description of
8 what's shown in Figure 15?

9 A. Now I think you lost -- oh, I see. Yeah,
10 that doesn't -- sure. That doesn't seem wrong to 05:03:08
11 me.

12 Q. So Figure 15 of Hiraishi shows that
13 different data buffers can receive the DQ data
14 signal from the memory chip at different times,
15 correct? 05:03:21

16 A. Yeah, different data buffers will receive
17 the DQ data signals from different SDRAMs at
18 different times.

19 Q. Paragraph 151 of Hiraishi teaches that
20 during S4 read leveling, the data register buffer 05:03:39
21 measures time A, which is related to when the DQ
22 data signal arrives from the memory chip. And then
23 the data register buffer stores that information in
24 the data register control circuit 320, correct?

25 A. Sure, I see that. 05:04:02



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. Figure 11 of Hiraishi shows the timing 05:04:30
2 for a read operation after S4 read leveling has
3 taken place, correct? So in other words, a normal
4 read operation?

5 A. I believe that's the case, yeah. 05:04:58

6 Q. At the bottom of Figure 11 in Hiraishi,
7 do you see the line DQS(OUT) and DQ(OUT) at the
8 very bottom of Figure 11?

9 A. Yes.

10 Q. Those are signals that the data register 05:05:18
11 buffer is sending to the system memory controller,
12 correct? As part of a read operation?

13 A. Yes, that's my understanding.

14 Q. For example, Figure 11 of Hiraishi shows
15 that around time T5, the data register buffer, 05:06:00
16 starts to send the preamble for the DQS strobe
17 signal to the system memory controller on the line
18 DQS(OUT), correct?

19 A. T5? It looks like that might be the end
20 of the preamble. 05:06:33

21 Q. Around T5 to T6 would be the preamble
22 that the data register buffer sends to the system
23 memory controller in DQS(OUT); is that fair?

24 A. It -- it may say that. I -- I don't
25 recall. My recollection just looking at this is 05:06:53



800.211.DEPO (3376)
EsquireSolutions.com

1 that the preamble was not necessarily in multiples 05:06:55
2 of a clock, and it -- it just looks like the time
3 from T4 to T5 matches what we were looking at
4 previously for the preamble.

5 Q. Well, I want to make sure we're looking 05:07:11
6 at the same thing. So in Figure 11, I'm looking at
7 the, you know, second line from the bottom that's
8 labeled DQS(OUT), and --

9 A. I was looking -- I was looking at the one
10 above. Sorry. Okay. 05:07:25

11 Q. So let me ask the question again. And,
12 you know, feel free to zoom in on the exhibit.

13 A. I have it.

14 Q. Figure 11 of Hiraishi shows that around
15 T5, the data register buffer starts to send the 05:07:42
16 preamble for the DQS strobe signal to the system
17 memory controller on the line DQS(OUT), correct?

18 A. Yes, I'm with you there.

19 Q. And Figure 11 of Hiraishi shows that the
20 preamble for the strobe signal DQS(OUT) is low for 05:07:58
21 an entire clock cycle from T5 to T6, approximately;
22 and then the strobe signal transitions every half
23 clock cycle until approximately time T10, correct?

24 A. Yes, I see that.

25 Q. Figure 11 of Hiraishi shows that at 05:08:26



800.211.DEPO (3376)
EsquireSolutions.com

1 precisely T6, which is to say, six clock cycles 05:08:30
2 after the data buffer received the read command,
3 the data buffer sends the DQ data signal to the
4 system memory controller on the line DQ(OUT),
5 correct? 05:08:52

6 A. Yes, I see that.

7 Q. So Figure 15 of Hiraishi shows that each
8 data register buffer can receive the data signal
9 from the memory chip at a different time on line
10 DQ(IN). And Figure 11 of Hiraishi shows that each 05:09:12
11 data register buffer will output the data signal to
12 the system memory controller on line DQ(OUT) at
13 precisely time T6, correct?

14 A. Yes, in this example. Yes, that's right.

15 Q. Dr. Mangione-Smith, would it be fair to 05:09:46
16 say that Netlist did not invent the memory module?
17 In other words, memory modules were known before
18 the '506 patent, right?

19 A. Sure.

20 Q. Netlist did not invent DDR1 memory 05:09:58
21 devices, correct?

22 A. Not as far as I'm aware.

23 Q. Netlist did not invent DDR2 memory
24 devices, correct?

25 A. That's right. Although that isn't really 05:10:09



800.211.DEPO (3376)
EsquireSolutions.com

1 something I was asked to consider, yep. 05:10:12

2 Q. Netlist did not invent DDR3 memory
3 devices either, right?

4 A. Not as far as I know.

5 Q. Netlist did not invent buffered DIMM 05:10:21
6 memory modules, correct? Those existed before the
7 '506 patent?

8 A. As far as I know, they haven't claimed to
9 invent them, no.

10 Q. Netlist did not invent distributed data 05:10:34
11 buffers for a memory module, correct?

12 MR. LINDSAY: Objection. Outside the
13 scope.

14 THE DEPONENT: Yeah, so part of the --
15 I -- actually, getting back to the buffer aspect as 05:10:47
16 well, I mean, in this family of patents, data
17 buffers have a particular meaning, I think. So
18 simply, they -- they didn't invent the concept of a
19 tri-state, for example, or putting a tri-state
20 buffer between a memory controller and -- and an 05:11:06
21 SDRAM chip. However, the -- the partic- -- they
22 invented the inventions that they claim.

23 Q. (By Mr. Chandler) Netlist did not invent
24 the concept of putting a data buffer on the memory
25 module, correct? 05:11:24



800.211.DEPO (3376)
EsquireSolutions.com

1 THE VIDEOGRAPHER: We're going off the 05:12:28
2 record. The time is 5:12.
3 (Recess taken.)
4 THE VIDEOGRAPHER: We're going back on
5 the record. The time is 5:24. 05:24:25
6 Q. (By Mr. Chandler) Please turn to the
7 Tokuhiro reference marked as Exhibit 1006.
8 Let me know when you have it up.
9 A. All right.
10 Q. And could you look at Figure 11 of 05:24:44
11 Tokuhiro, please.
12 A. Yes, I see it.
13 Q. The left side of Figure 11 of Tokuhiro
14 shows an element labeled "DR1," correct?
15 A. Yes. 05:25:10
16 Q. DR1 in Figure 11 of Tokuhiro, marked as
17 Exhibit 1006, is a variable delay element, correct?
18 A. That is my recollection.
19 Q. And Tokuhiro uses the diagonal arrow to
20 indicate a variable delay, correct? 05:25:32
21 A. Yes.
22 Q. Could you turn to Figure 5 of Tokuhiro.
23 A. Okay.
24 Q. And Figure 5 of Tokuhiro shows the
25 variable delay element, DR1, correct? Sort of in 05:25:58



800.211.DEPO (3376)
EsquireSolutions.com

1 the middle. 05:26:06
2 A. Yes, I see it.
3 Q. And Figure 5 also shows the variable
4 delay element DW1, correct?
5 A. Yes. 05:26:17
6 Q. And there's also, I guess, a variable
7 delay element DW0, correct?
8 Towards the top. Sorry.
9 A. Thank you. Yes, I see it.
10 Q. And further toward the right, under FF0, 05:26:44
11 there's a different variable delay element that's
12 not labeled.
13 A. Yes, I see that.
14 Q. With the diagonal arrow, correct?
15 A. Yes. 05:27:03
16 Q. And then at the bottom of Figure 5,
17 there's more variable delay element to DR1, DR2,
18 DW1 and DW2, correct?
19 A. That's right.
20 (Exhibit 1052 was marked for 05:27:18
21 identification by the Court Reporter and is
22 attached hereto.)
23 MR. CHANDLER: All right. I'm going to
24 mark a new Exhibit 1052, coming through to you.
25 THE DEPONENT: Okay. 05:27:46



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. (By Mr. Chandler) So Exhibit 1052 is, 05:27:47
2 again, more for convenience really. But just to be
3 clear, what I've done is I've reprinted Figure 2 to
4 have Butt reference, marked as Exhibit 1029, on the
5 left side; and I've reprinted Figure 3A from the 05:28:06
6 Butt reference on the right side. And I've just
7 added an arrow showing the relationship between
8 Figure 3A and Figure 2, which is the -- Figure 3A
9 provides some more detail about element 114 that is
10 highlighted in red in Figure 2 on Exhibit 1052. 05:28:29
11 Understood?
12 A. Yes.
13 Q. And in Figure 2 of Butt, at the bottom,
14 do you see a box labeled 118, and it says "GATEON
15 circuit"? 05:28:52
16 A. Yes.
17 Q. And then on the right side of Figure 3A,
18 do you see that there's a GATEON_UN signal going to
19 123a?
20 A. Yes. 05:29:08
21 Q. What does the GATEON signal do in
22 general, and in particular with respect to 123a?
23 A. Well, this is -- so -- so 123a has the
24 signal GATEON, G-A-T-E-O-N, and then _UN. And then
25 that's shown going to a multiplexer which selects 05:29:48



800.211.DEPO (3376)
EsquireSolutions.com

1 between a zero value and an input value of, it 05:29:55
2 says, "DQS/DQS_UN."

3 Q. And what is your understanding of how --
4 Butt, marked as 1029, uses the GATEON signal in his
5 circuitry? 05:30:22

6 A. Well, here, it's shown being driven to
7 this -- I don't recall what the "UN" designation
8 meant. But it's shown being driven to that
9 multiplexer to select between those two input
10 values that I just mentioned. 05:30:39

11 Q. Is it possible that "UN" refers to "upper
12 nibble"?

13 A. Yeah, it could be. Yeah.

14 Q. Okay. So when GATEON is enabled, what
15 does multiplexer 123a do; and then when GATEON is
16 disabled, what does multiplexer 123a do? 05:31:05

17 A. Well, it looks to me like when it's on,
18 the multiplexer outputs whatever is on DQS/DQS, as
19 you suggested, upper nibble. And when it's off,
20 it's connected to ground or logical zero low value
21 logic. 05:31:30

22 Q. So using Exhibit 1052, I want to sort of
23 walk through with you how a DQS strobe signal
24 travels from the DDR memory chip on the right of
25 Figure 2 of Butt to the left side of Figure 2 to 05:32:06



800.211.DEPO (3376)
EsquireSolutions.com

1 the memory controller. 05:32:12

2 Understood? What our...

3 A. I do, with the caveat that I wasn't
4 endeavoring to understand Butt any more than to be
5 able to evaluate the arguments made by Dr. Wedig. 05:32:25

6 Q. But you did review Figures 2 and 3A of
7 Butt, right?

8 A. I did.

9 Q. And you also read Butt, marked as
10 Exhibit 1029, correct? 05:32:42

11 A. Yes, but I'll have a greater recollection
12 and fluidity with the elements that Dr. Wedig
13 relied upon.

14 Q. So Figure 2 of Butt shows a DQS strobe
15 signal going from the DDR memory device 106, which
16 I've highlighted in green in Exhibit 1052, going to
17 an IO buffer 108, correct? As shown in Figure 2. 05:33:00

18 A. Yes. Yeah, I see it.

19 Q. And then after, that the DQS strobe
20 signal goes to selector 123a in box 114, which is
21 shown in Figure 3A of Butt, correct? 05:33:29

22 A. Yes.

23 Q. And as you indicated a moment ago, when
24 the GATEON_UN signal is enabled, the DQS signal
25 will pass through selector 123a and will go in a 05:33:55



800.211.DEPO (3376)
EsquireSolutions.com

1 couple places, but for now let's go up. It will go 05:34:08
2 up to delay element 124a; is that correct?
3 A. Yes.
4 Q. And delay element 124a will delay the DQS
5 strobe signal by a variable amount indicated by 05:34:25
6 that diagonal arrow, correct?
7 A. Yes.
8 Q. After being delayed by 124a, the DQS
9 strobe signal goes to register 121a, among other
10 places, correct? 05:34:51
11 A. Yes.
12 Q. The delayed DQS strobe signal at register
13 121a causes the DQ read data to be registered and
14 then output towards the left of Figure 3A, correct?
15 A. Yes. 05:35:25
16 Q. And then both the delay DQS strobe
17 signal, which I guess is now being labeled
18 PDQS_OUT_UN, and the DQ data signal, which is now
19 being labeled DR_PDQ_OUT, go to the asynchronous
20 FIFO 112 shown in Figure 2 of Butt, correct? 05:35:56
21 A. Yes.
22 Q. And then finally, the DQS and DQ signal
23 go from the asynchronous FIFO to the memory
24 controller on lines that are labeled -- well, let
25 me ask you. 05:36:37



800.211.DEPO (3376)
EsquireSolutions.com

1 What happens after the asynchronous FIFO 05:36:38
2 112 to -- to the data signal?

3 A. Well, the data signal looks like it's
4 being written out under -- over -- I guess it's
5 P -- I don't know if it's PI or PL_R_PDQ and 05:36:58
6 PI_R_NDQ.

7 Q. Could you turn to paragraph 63 of the
8 Butt reference mark as Exhibit 1029.

9 Let me know when you're there.

10 A. Almost there. Okay. 05:37:37

11 Q. In paragraph 63 of the Butt reference
12 marked as Exhibit 1029, Butt teaches that his
13 invention could be implemented in an
14 application-specific integrated circuit,
15 abbreviated "ASIC," correct? 05:37:56

16 A. Yes.

17 Q. Alternatively, his invention could be
18 implemented in an FPGA, correct?

19 A. That's what he states, yeah.

20 Q. That's what Butt states in paragraph 63 05:38:12
21 of Exhibit 1029?

22 A. Yes.

23 Q. And as we discussed earlier, you believe
24 a person of ordinary skill in the art would know
25 what an FPGA is what an ASIC is, correct? 05:38:24



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes. That doesn't necessarily mean they 05:38:31
2 would know how to work with one or design with
3 them, but they would be familiar with the concept
4 and --

5 Q. They would under what Butt is trying to 05:38:39
6 convey in paragraph 63 of Exhibit 1029?

7 A. I would think so.

8 Q. Can you go to your declaration marked as
9 Exhibit 2006, and go to page 52.

10 And do you see paragraph 95? 05:39:03

11 A. Not yet. Okay.

12 Q. You would agree that the Butt reference
13 marked as Exhibit 1029 teaches how to determine the
14 optimin -- optimum, rather, offset delay values for
15 the DQS strobe signal, correct? 05:39:24

16 A. I would agree that that is what Butt
17 claims, yes.

18 MR. CHANDLER: Why don't we take a quick
19 break, and hopefully we will finish up soon.

20 THE VIDEOGRAPHER: We're going off the 05:39:43
21 record. The time is 5:39.

22 (Recess taken.)

23 THE VIDEOGRAPHER: We're going back on
24 the record. The time is 5:48.

25 Q. (By Mr. Chandler) Dr. Mangione-Smith, 05:48:52



800.211.DEPO (3376)
EsquireSolutions.com

1 are there any corrections or clarifications you'd 05:48:53
2 like to make to any of the testimony that you've
3 given to me so far today?

4 A. Not that occurs to me, no.
5 (Exhibit 1053 was marked for 05:49:03
6 identification by the Court Reporter and is
7 attached hereto.)

8 MR. CHANDLER: All right. Let me mark
9 the next exhibit, 1053, in the chat.

10 Q. (By Mr. Chandler) Let me know when you 05:49:10
11 have it.

12 A. Okay. I have it.

13 Q. Exhibit 1053 is the JEDEC standard
14 JESD82-20, dated March 2007, for the FBDIMM
15 advanced memory buffer, abbreviated "AMB"; is that 05:49:45
16 correct?

17 A. Yes.

18 Q. And earlier today, we were looking at
19 Netlist's technology portfolio marked as
20 Exhibit 1047 which, on page 9, showed an FBDIMM 05:50:04
21 illustration at a high level, correct?

22 A. Yes, I recall discussing that with you.

23 Q. And I think you may have been a little
24 unsure at that point whether or not FBDIMM was
25 prior art to the '506 patent. But now that you 05:50:23



800.211.DEPO (3376)
EsquireSolutions.com

1 have Exhibit 1053, would you agree that FBDIMM had 05:50:27
2 been standardized by JEDEC before the '506 patent
3 came out?

4 A. That appears to be the case.

5 Q. In Exhibit 1053, could you look at 05:50:43
6 page 15 in the bottom right page number. It's
7 labeled as "Figure 1.1 - Advanced Memory Buffer
8 Block Diagram."

9 And let me know when you're --

10 A. Yes. 05:51:03

11 Q. So do you have in front of you the
12 advanced memory buffer block diagram for the JEDEC
13 FBDIMM standard marked as Exhibit 1053?

14 A. Yes, I do.

15 Q. And this is the block diagram for the 05:51:18
16 AMB, which is -- if you look at the tutorial slide
17 1047, page 9, is that central buffer on the memory
18 module that buffers address command DQ data and DQS
19 strobe signals, correct?

20 MR. LINDSAY: Objection. Outside the 05:51:48
21 scope of direct.

22 THE DEPONENT: Yeah. It appears that
23 it's referring to the same AMB.

24 But I'll just mention, just like I
25 commented on at presentation, I don't recall 05:52:00



800.211.DEPO (3376)
EsquireSolutions.com

1 reviewing the JEDEC standard, this JEDEC standard, 05:52:03
2 one way or another. I may have. I simply have no
3 recollection of it as I sit here.

4 Q. (By Mr. Chandler) Okay. The AMB buffer, 05:52:18
5 shown here on page 15 of Exhibit 1053, contains
6 several different blocks, correct? Is that a -- a
7 fair characterization to start?

8 MR. LINDSAY: Objection. Outside the
9 scope of direct.

10 THE DEPONENT: Visually, there are 05:52:44
11 multiple rectangular objects in the figure, yes.

12 Q. (By Mr. Chandler) So, for example,
13 towards the upper left, the AMB includes a command
14 decoder? There's a box for that, right?

15 MR. LINDSAY: Objection. Outside the 05:53:03
16 scope of direct.

17 THE DEPONENT: The upper left, I see the
18 PLL and the reset control.

19 Q. (By Mr. Chandler) A little bit below 05:53:13
20 that to the right.

21 A. Yes. Okay. I see a box labeled "Command
22 Decoder & and CRC Check."

23 Q. The AMB and FBDIMM also includes core
24 control, correct?

25 MR. LINDSAY: Objection. Outside the 05:53:29



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of direct. 05:53:30

2 THE DEPONENT: I only know that it's got
3 a box labeled "Core Control and CRSs." I don't
4 have any other understanding of what that is as I
5 sit here. 05:53:43

6 Q. (By Mr. Chandler) The AMB includes data
7 CRC. And you're familiar with CRC, correct?

8 A. Yes.

9 MR. LINDSAY: Objection. Outside the
10 scope. 05:53:55

11 THE DEPONENT: It has a box labeled "Data
12 CRC Generation & Read FIFO." [as read] But as I've
13 said, I don't have any understanding beyond simply
14 what the labels say.

15 Q. (By Mr. Chandler) You understand what
16 data CRC is? 05:54:12

17 A. Sure.

18 Q. Could you explain that briefly.

19 MR. LINDSAY: Objection. Outside the
20 scope of direct. 05:54:17

21 THE DEPONENT: "CRC" is an abbreviation
22 for "cyclic redundancy check." It's a way to
23 protect against errors in information that's being
24 communicated.

25 Q. (By Mr. Chandler) The AMB in an FBDIMM 05:54:34



800.211.DEPO (3376)
EsquireSolutions.com

1 also has in the middle what is described as 05:54:38
2 "MEMBIST," which stands for "memory built-in self
3 test," correct?

4 MR. LINDSAY: Objection. Assumes facts
5 not in evidence. Outside the scope of direct. 05:54:59
6 Form.

7 THE DEPONENT: It's got a box labeled
8 "External MEMBIST DDR Calibration & DDR IOBIST" --
9 that's I-O-B-I-S-T, slash, D-F-X.

10 And MEMBIST is M-E-M-B-I-S-T. 05:55:18

11 And BIST typically, or often, has a
12 meaning "built-in self test," but I don't know
13 exactly what this block is doing.

14 Q. (By Mr. Chandler) The MEMBIST, built-in
15 self test, in the AMB at the FBDIMM, that's 05:55:37
16 described further on page 38 of Exhibit 1053,
17 correct?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct.

20 THE DEPONENT: I -- I don't believe so, 05:55:48
21 but -- because I -- I haven't -- I don't recall.
22 However, it -- it doesn't say "built-in MEMBIST."
23 It says "external MEMBIST."

24 Q. (By Mr. Chandler) On page 38 of
25 Exhibit 1053, there's a Section 3.8, "DDR MEMBIST," 05:56:06



800.211.DEPO (3376)
EsquireSolutions.com

1 correct? 05:56:13
2 MR. LINDSAY: Objection. Outside the
3 scope of direct.
4 THE DEPONENT: I'm sorry. Can you give
5 me the page number again. 05:56:25
6 Q. (By Mr. Chandler) And again, I'm looking
7 at the -- the bottom right page number.
8 A. Yeah.
9 Q. So Exhibit 1053, page 38, as shown in the
10 bottom right of the -- the exhibit. 05:56:35
11 A. So yes, section 3.8 has the title "DDR
12 MEMBIST."
13 Q. And that's referring to the MEMBIST in
14 the AMB shown on page 15 of the block diagram for
15 the AMB, correct? 05:57:00
16 MR. LINDSAY: Objection. Outside the
17 scope of direct.
18 THE DEPONENT: I have no opinion on that,
19 other than they use -- they both use the word
20 "MEMBIST." 05:57:10
21 Q. (By Mr. Chandler) And you understand
22 what built-in self test is, correct?
23 MR. LINDSAY: Objection. Outside the
24 scope of direct.
25 THE DEPONENT: It's a general concept 05:57:22



800.211.DEPO (3376)
EsquireSolutions.com

1 with a number of different implementations, but 05:57:23
2 yes, I do.

3 Q. (By Mr. Chandler) At a high level, could
4 you explain what MEMBIST built-in self test is.

5 MR. LINDSAY: Objection. Outside the 05:57:34
6 scope of direct.

7 THE DEPONENT: "BIST" stands -- stands
8 for "built-in self test." It's a mechanism for a
9 device to test itself. The term "MEMBIST" isn't
10 confusing to me, but it's also not a common -- 05:57:50
11 memory built-in self test or memory BIST, sure.
12 But I'm just saying the particular phrasing here,
13 "MEMBIST," is not something that I recall seeing
14 before. But it doesn't confuse me.

15 Q. (By Mr. Chandler) All right. And on 05:58:06
16 page 15 of Exhibit 1053, below the MEMBIST box,
17 there's another box for a pattern generator,
18 correct?

19 MR. LINDSAY: Objection. Outside the
20 scope of direct. 05:58:19

21 THE DEPONENT: I see a box labeled "Sync
22 & Idle Pattern Generator." But I have no
23 understanding of it beyond how it's titled.

24 Q. (By Mr. Chandler) In the AMB, on the
25 FBDIMM memory module, there is an SMBus controller 05:58:37



800.211.DEPO (3376)
EsquireSolutions.com

1 shown sort of towards the bottom left of page 15 of 05:58:42
2 Exhibit 1053, correct?

3 MR. LINDSAY: Objection. Outside the
4 scope of direct.

5 THE DEPONENT: Yes, I see a box labeled 05:58:54
6 "SMBus Controller."

7 Q. (By Mr. Chandler) And you understand
8 what the SMBus is, correct?

9 A. Yes. I don't know what it's used for
10 here, however. 05:59:07

11 Q. What's the standard usage for an SMBus on
12 a memory module?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE DEPONENT: It's -- it's used for a 05:59:24
16 number of different purposes. It's -- it's an
17 old-technology, slow, very small -- so it's got
18 advantages and disadvantages -- communications bus
19 between multiple chips.

20 Q. (By Mr. Chandler) And "SMBus" stands for 05:59:38
21 "system management bus"; is that correct?

22 MR. LINDSAY: Objection. Outside the
23 scope of direct.

24 THE DEPONENT: That's correct.

25 Q. (By Mr. Chandler) And, for example, the 05:59:48



800.211.DEPO (3376)
EsquireSolutions.com

1 SMBus can be used during power-on for initial 05:59:49
2 communications between the memory module and the
3 system memory controller. That's one potential use
4 for the SMBus, correct?

5 MR. LINDSAY: Objection. Outside the 06:00:04
6 scope of direct.

7 THE DEPONENT: It makes more sense to me
8 to discuss specific implementations. I've seen
9 that in some context. Not in the AMB context.

10 Q. (By Mr. Chandler) The AMB on an FBDIMM 06:00:21
11 includes a number of different multiplexers,
12 labeled "mux," as shown on page 15 of Exhibit 1053,
13 correct?

14 MR. LINDSAY: Objection. Outside the
15 scope of direct. 06:00:33

16 THE DEPONENT: It seems to show, I think,
17 four different multiplexers: One near the top
18 going into the purple box; two on the right-hand
19 side going to the DDR IOs; one sort of near the
20 bottom, going into a box labeled "failover." 06:01:00

21 But beyond those images and the label, I
22 have no particular understanding of what they're
23 used for here.

24 Q. (By Mr. Chandler) The AMB chip in the
25 FBDIMM includes a DDR state controller, as shown 06:01:22



800.211.DEPO (3376)
EsquireSolutions.com

1 right in the middle of Figure 15 -- I'm sorry -- 06:01:30
2 page 15 of Exhibit 1053, correct?

3 A. I would --

4 MR. LINDSAY: Objection. Outside of the
5 scope of direct. 06:01:41

6 THE DEPONENT: Yeah, I wouldn't know.

7 Q. (By Mr. Chandler) On page 15 of
8 Exhibit 1053, the block diagram for the advanced
9 memory buffer shows that there is a DDR state
10 controller inside that chip, correct? 06:02:00

11 MR. LINDSAY: Objection. Outside the
12 scope of direct.

13 THE DEPONENT: No, I wouldn't say that.
14 We've been talking about this figure. This figure
15 does show a block that says "DDR State Controller
16 and CSRs." 06:02:12

17 Q. (By Mr. Chandler) That's what I was
18 referring to.

19 A. I -- I don't know what's in any
20 particular chip, or on any particular DIMM, or on
21 what -- talking about AMB -- or -- 06:02:23

22 Q. That's what I meant. That's what I
23 meant, the -- what I meant. When I said "chip," I
24 meant the AMB chip.

25 A. Got it. 06:02:41



800.211.DEPO (3376)
EsquireSolutions.com

1 Q. So, for clarity, the AMB chip as a whole 06:02:41
2 would include functionality for a DDR state
3 controller as shown on page 15 of Exhibit 1053,
4 correct?

5 MR. LINDSAY: Objection. Outside the 06:02:53
6 scope of direct.

7 THE DEPONENT: Yeah, I wouldn't -- I
8 wouldn't go that far. I'm comfortable saying
9 Figure 1.1 shows that box. That's what it shows.

10 Q. (By Mr. Chandler) And there are a number 06:03:07
11 of other boxes shown in the block diagram for the
12 advanced memory buffer that would -- that page 15
13 of Exhibit 1053 teaches as being included in the
14 advanced memory buffer. But we just haven't
15 discussed all of those other blocks, correct? 06:03:32

16 MR. LINDSAY: Objection. Outside the
17 scope of direct.

18 THE DEPONENT: I'm sorry. Could you
19 repeat the question.

20 Q. (By Mr. Chandler) We've discussed a 06:03:43
21 number of different blocks shown in the block
22 diagram for the advanced memory buffer on page 15
23 of Exhibit 1053. But there are even more blocks
24 beyond what we've discussed, correct?

25 MR. LINDSAY: Objection. Outside the 06:04:02



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of direct. 06:04:03

2 THE DEPONENT: There are even more labels
3 on boxes that we have not read, yes.

4 Q. (By Mr. Chandler) All right. So there's
5 additional functionality in the AMB buffer even 06:04:10
6 beyond what we've been discussing for the last 10
7 or 15 minutes, right?

8 MR. LINDSAY: Objection. Outside the
9 scope of direct.

10 THE DEPONENT: Well, beyond the -- the 06:04:24
11 multiplexers and an SMBus controller, I don't know
12 that we've been discussing any functionality.
13 We've been reading labels on the boxes.

14 Q. (By Mr. Chandler) And Exhibit 1053 is
15 over 175 pages long, and it provides a description 06:04:44
16 of the advanced memory buffer for an FBDIMM,
17 correct?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct.

20 THE DEPONENT: Based on simply reading 06:05:03
21 the title and the label of Figure 1, it would
22 appear that that's likely the case.

23 Q. (By Mr. Chandler) And so if you look,
24 for example, at the table of contents on page 5 of
25 Exhibit 1053, there's a description of the FBD 06:05:15



800.211.DEPO (3376)
EsquireSolutions.com

1 channel interface, correct? 06:05:25

2 MR. LINDSAY: Objection. Outside the
3 scope of direct.

4 THE DEPONENT: Yes, I see labeled "FBD
5 Channel Interface." 06:05:36

6 Q. (By Mr. Chandler) There's a description
7 for the DDR interface for the AMB, correct?

8 A. I wouldn't say that. There's a section
9 that says DDR interface.

10 Q. There's a section starting at page 24,
11 according the table of contents, for DDR
12 calibration, correct? 06:05:51

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE DEPONENT: The table of contents has
16 a listing for DDR calibration and the number 24
17 next to it. 06:06:04

18 Q. (By Mr. Chandler) And I'm running out of
19 time, but there's -- there's a lot. There's a lot
20 in here in Exhibit 1053 about the advanced memory
21 buffer, right? 06:06:24

22 MR. LINDSAY: Objection. Form. Outside
23 the scope of direct.

24 THE DEPONENT: 190 pages is not a
25 particularly long standard, but there appears to be 06:06:36



800.211.DEPO (3376)
EsquireSolutions.com

1 a lot of material in here. 06:06:42

2 Q. (By Mr. Chandler) And there appears to
3 be a lot of blocks in Figure 1.1 on page 15 of
4 Exhibit 1053, the block diagram for the AMB; is
5 that fair? 06:07:00

6 A. There are --
7 MR. LINDSAY: Objection. Outside the
8 scope of direct. Form.

9 THE DEPONENT: There are several
10 additional blocks above and beyond what we've
11 labeled. 06:07:06

12 Q. (By Mr. Chandler) Dr. Mangione-Smith, do
13 you have any clarifications or corrections that you
14 would like to make to your testimony that you gave
15 to me today? 06:07:18

16 THE DEPONENT: No, sir.

17 MR. CHANDLER: All right. I think I'm
18 out of time, so I will pass the witness.

19 MR. LINDSAY: Okay. Let's take five
20 minutes. 06:07:30

21 THE VIDEOGRAPHER: We're going off the
22 record. The time is 6:07.

23 (Recess taken.)

24 THE VIDEOGRAPHER: We are going back on
25 the record. The time is 6:13. 06:13:35



800.211.DEPO (3376)
EsquireSolutions.com

1 EXAMINATION 06:13:37
2 BY MR. LINDSAY:
3 Q. Okay. Dr. Mangione-Smith, I just want to
4 ask a few clarifying questions so that the record's
5 clear. 06:13:46
6 Can you turn to your declaration,
7 Exhibit 2006, paragraph 60, 6-0.
8 A. I will let you know when I'm there.
9 Okay.
10 Q. Okay. In this paragraph, do you say that 06:14:29
11 "Hiraishi describes an approach for read leveling
12 that does not rely on adjusting the timing of the
13 strobe signals themselves, but instead only adjusts
14 the timing of when the input buffers INB are turned
15 so that they are active when data arrives"? 06:14:49
16 MR. CHANDLER: Objection. Outside --
17 THE DEPONENT: Yes.
18 MR. CHANDLER: Sorry, Dr. Mangione-Smith.
19 If you can just wait until I can get my objection
20 so we don't speak over each other. 06:14:57
21 Objection. Outside the scope of cross.
22 And objection. Leading.
23 THE DEPONENT: Yes, that is -- that's
24 what I said. That's my opinion. And hopefully, if
25 I testified throughout this long day on something 06:15:09



800.211.DEPO (3376)
EsquireSolutions.com

1 touching the subject, I didn't suggest something 06:15:13
2 contrary to that.

3 Q. (By Mr. Lindsay) So all of your
4 testimony here today is consistent with what you
5 stated in paragraph 60? 06:15:20

6 A. As far as I know.

7 MR. CHANDLER: Objection. Leading.
8 And your answer, Dr. Mangione-Smith.

9 THE DEPONENT: As far as I know, my
10 testimony is consistent. 06:15:34

11 Q. (By Mr. Lindsay) In the last sentence of
12 paragraph 60, do you say that Hiraishi does
13 describe a separate retiming operation, which you
14 say you will discuss below?

15 MR. CHANDLER: Objection. Outside the 06:15:50
16 scope of cross. And leading.

17 THE DEPONENT: Yes. Yes.

18 Q. (By Mr. Lindsay) Okay. If you can
19 scroll down for to me to paragraph 73, and the last
20 sentence of paragraph -- 06:16:12

21 A. I'm there.

22 Q. -- 73.

23 Could you read that last sentence for me,
24 please.

25 MR. CHANDLER: Objection. Outside the 06:16:19



800.211.DEPO (3376)
EsquireSolutions.com

1 scope of cross. As well as objection to leading. 06:16:19

2 THE DEPONENT: So it says "I also do not
3 agree that Hiraishi's S4 leveling operation adjusts
4 read timing within Hiraishi's data buffer, although
5 Hiraishi does perform a separate retiming operation 06:16:36
6 which I describe below."

7 Q. (By Mr. Lindsay) Is that still your
8 opinion?

9 A. Yes.

10 MR. CHANDLER: Objection. 06:16:46

11 Q. (By Mr. Lindsay) And all of your
12 testimony here today consistent with that opinion?

13 MR. CHANDLER: Objection. We got to back
14 up.

15 So objection. Outside the scope of 06:16:54
16 cross. And objection. Leading.

17 THE DEPONENT: Is my video frozen again?

18 MR. CHANDLER: It is.

19 MR. LINDSAY: Yes.

20 MR. CHANDLER: Even Zoom objects. 06:17:06

21 THE DEPONENT: One could hardly blame it.

22 (Technical difficulties; discussion off
23 the stenographic record.)

24 THE DEPONENT: Okay.

25 Q. (By Mr. Lindsay) Okay. And then if you 06:17:34



800.211.DEPO (3376)
EsquireSolutions.com

1 scroll down to paragraph 115 for me. In your 06:17:35
2 declaration still, of course.

3 A. Okay.

4 Q. Okay. Do you recall earlier today
5 testifying about fly-by delays and whether Hiraishi 06:17:55
6 corrected for those fly-by delays when it receives
7 signals from the memory devices?

8 A. Yes.

9 Q. Do you state here that for those fly-by
10 delays that "Hiraishi uses an entirely different 06:18:18
11 retiming operation which Petitioner does not
12 address and which is also unrelated to
13 strobe-centering"?

14 MR. CHANDLER: Objection. Outside the
15 scope of cross. And objection. Leading. 06:18:31

16 THE DEPONENT: Yes, that's what I say.

17 Q. (By Mr. Lindsay) Does the next sentence
18 go on to say that "this re-timing operation is
19 based on an internal local clock which re-times the
20 read data output from FIFO and generates a new DQS 06:18:49
21 strobe signal using the strobe generating circuit
22 376 that's in synchronization with the internal
23 clock LCLKR"?

24 MR. CHANDLER: Objection. Outside the
25 scope of cross. And objection. Leading. 06:19:06



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: Yes, I see that text. And 06:19:10
2 that is still your opinion.

3 Q. (By Mr. Lindsay) And is that consistent
4 with all of your earlier testimony today?

5 A. I believe so. 06:19:20

6 MR. CHANDLER: Sorry. Objection.
7 Leading.

8 Q. (By Mr. Lindsay) Does Hiraishi apply a
9 fixed delay to the DQS strobe signal that it
10 receives using circuit 372? 06:19:39

11 A. Yes, that's my recollection, assuming 372
12 is the 90-degree delay circuitry.

13 Q. If you look at paragraph 87. Sorry to
14 jump around, but I just wanted to orient your
15 memory there. 06:20:32

16 Paragraph 87 of your declaration, the
17 second --

18 A. Okay. Yes, I'm there.

19 Q. -- sentence from the end.

20 Does it say "delay circuit 372 then 06:20:44
21 applies the fixed delay to the selected DQS"?

22 MR. CHANDLER: Objection. Outside the
23 scope of cross. And objection. Leading.

24 THE DEPONENT: Yes, that's -- that's what
25 it says, that is my understanding, and I believe 06:20:58



800.211.DEPO (3376)
EsquireSolutions.com

1 it's consistent with my testimony throughout the 06:21:01
2 day.

3 Q. (By Mr. Lindsay) In your opinion, why
4 does Hiraishi delay the DQS signal by that fixed
5 amount? 06:21:14

6 A. Because it believes that that is an
7 effective way to get the DQS centered in the eye.

8 Q. Other than delaying the DQS by that fixed
9 amount using circuit 372, does Hiraishi describe
10 any sort of other data centering operations? 06:21:34

11 A. No, not that I can think of.

12 Q. Other than delaying the DQS signal by
13 that fixed amount using circuit 372, does Hiraishi
14 indicate the need to perform any sort of additional
15 data strobe centering such as that described in 06:21:56
16 Butt?

17 MR. CHANDLER: Objection. Leading.

18 THE DEPONENT: No, I don't believe so.
19 Hiraishi seems -- "Hiraishi," rather, seems to
20 believe that it's a complete and effective design 06:22:14
21 and doesn't identify any flaws in that approach of
22 using a 90-degree delay.

23 Q. (By Mr. Lindsay) Other than delaying the
24 DQS signal by that fixed amount using circuit 372,
25 would a person of ordinary skill in the art believe 06:22:31



800.211.DEPO (3376)
EsquireSolutions.com

1 that Hiraishi would benefit from an additional data 06:22:34
2 centering operation such as what Butt describes?

3 MR. LINDSAY: Objection. Form. And
4 objection. Leading.

5 THE DEPONENT: I don't believe so. I 06:22:50
6 think reading Hiraishi, a person would understand
7 how the -- the delay centers the strobe in the eye
8 and wouldn't -- wouldn't identify any particular
9 flaw in that approach. I don't recall Dr. Wedig
10 identifying any particular flaw in that approach. 06:23:13

11 Q. (By Mr. Lindsay) Okay. Can you, if you
12 wouldn't mind, turn to the Butt reference,
13 Exhibit 1029.

14 A. Okay.

15 Q. Okay. Do you recall a short time ago 06:23:37
16 discussing paragraph 63 with Mr. Chandler,
17 particularly the part where it talks about the
18 invention being implemented as an application
19 specific integrated circuit?

20 A. Yes, I recall that discussion. 06:24:02

21 Q. Okay. The paragraph directly above that,
22 could you read the first sentence into the
23 record --

24 MR. LINDSAY: We lost video. Are you
25 still there, Dr. Mangione-Smith? 06:24:17



800.211.DEPO (3376)
EsquireSolutions.com

1 (Technical difficulties; discussion off 06:24:25
2 the stenographic record.)

3 MR. CHANDLER: So objection. Outside the
4 scope of cross. And objection. Leading.

5 THE DEPONENT: So you asked me to read 06:24:31
6 the first sentence of paragraph 62; is that
7 correct?

8 Q. (By Mr. Lindsay) Yes.

9 MR. CHANDLER: Same objection.

10 THE DEPONENT: So it says "the functions 06:24:38
11 performed by the flow diagrams of Figures 5 through
12 7 may be implemented using a conventional general
13 purpose digital computer programmed according to
14 the teachings of the present specification as well
15 be apparent to those skilled in the relevant arts." 06:24:54
16 [as read]

17 Q. (By Mr. Lindsay) Okay. And if you could
18 scroll up to Figure 5. We'll take a look at 5, 6
19 and 7 briefly.

20 MR. CHANDLER: Objection. Outside the 06:25:15
21 scope of cross. And objection. Leading.

22 MR. LINDSAY: I don't think there's
23 actually a question there.

24 Q. (By Mr. Lindsay) What is Figure 5
25 describing? 06:25:28



800.211.DEPO (3376)
EsquireSolutions.com

1 similar approach to determine the minimum value, in 06:27:07
2 that it keeps decreasing the delay value until the
3 test fails, at which point it says the last minimal
4 value that I use shall be -- that passed the test
5 will be registered as the minimum -- minimum value 06:27:25
6 that works.

7 Q. (By Mr. Lindsay) So back to paragraph
8 62. Does paragraph 62 then indicate that the
9 strobe centering technique that Butt describes is
10 implemented using a general purpose digital 06:27:45
11 computer?

12 MR. LINDSAY: Objection. Outside the
13 scope of cross. And objection. Leading.

14 THE DEPONENT: Yes, I believe that it's
15 indicating that. 06:27:58

16 MR. LINDSAY: Okay. I have no more
17 questions.

18 MR. CHANDLER: All right. Let's go off
19 the record briefly.

20 THE VIDEOGRAPHER: Counsel, would you 06:28:18
21 like to take a break for a minute.

22 MR. CHANDLER: Yes, please.

23 THE VIDEOGRAPHER: Yes. Very good.

24 We're going off the record. The time is
25 6:28. 06:28:24



800.211.DEPO (3376)
EsquireSolutions.com

1 (Recess taken.) 06:28:25
2 THE VIDEOGRAPHER: We're going back on
3 the record. The time is 6:31.
4 FURTHER EXAMINATION
5 BY MR. CHANDLER: 06:31:44
6 Q. Dr. Mangione-Smith, could you please turn
7 back to the Butt reference marked as Exhibit 1029,
8 and go to paragraph 62 and 63.
9 And let me know when you're there.
10 A. Yes, I'm there. 06:31:55
11 Q. The Butt reference, in paragraph 62,
12 teaches that certain functionality may be
13 implemented using a conventional general purpose
14 digital computer. But Butt doesn't say that it's
15 required to implement his invention using a 06:32:17
16 conventional general purpose digital computer,
17 correct?
18 A. That's correct.
19 Q. And, in fact, in paragraph 63 of Butt,
20 marked as Exhibit 1029, he teaches that his 06:32:32
21 invention may also be implemented in an ASIC or an
22 FPGA or a few other ways that are described in
23 paragraph 63, correct?
24 A. Well, in 62, he's specifically talking
25 about the flow diagrams of 5 through 7. If the -- 06:33:03



800.211.DEPO (3376)
EsquireSolutions.com

1 assuming the present invention covers those flow 06:33:05
2 diagrams, then sure, he's talking about these other
3 modes of implementation.

4 Q. And if you look, for example, in
5 paragraph 12 of Butt, he indicates that Figure 5 is 06:33:23
6 part of the present invention, correct?

7 A. It's -- it says it's -- it doesn't say it
8 is a preferred embodiment of the invention. It
9 says it's a flow diagram illustrating a turning
10 process in accordance with it. 06:33:53

11 I'm not saying it's not part of the
12 present invention. I'm just pointing out that he's
13 using different words to characterize it there.
14 And I don't recall if -- yeah, I guess I'll leave
15 it at that. 06:34:06

16 Q. Figure 5 is a preferred embodiment of the
17 present invention, correct?

18 A. Well, Figure 5 is a flow diagram
19 illustrating a training process in accordance with
20 a preferred embodiment. 06:34:22

21 Q. Of the present invention, right?

22 A. Yeah.

23 Q. And paragraph 63 of Butt tells us that
24 the present invention may be implemented in an
25 ASIC, correct? 06:34:35



800.211.DEPO (3376)
EsquireSolutions.com

1 A. Yes. 06:34:39

2 Q. Or an FPGA, right?

3 A. Yes, that's correct.

4 Q. And Butt never says that the only way to
5 implement his invention would be using a 06:34:48
6 conventional general purpose digital computer,
7 correct?

8 A. He says that the flow diagrams may be
9 implemented that way, and that the invention may be
10 implemented using an FPGA or an ASIC. 06:35:06

11 Q. So Butt is teaching some alternative ways
12 to implement his invention, correct?

13 MR. LINDSAY: Objection. Asked and
14 answered.

15 THE DEPONENT: Yeah, Butt is at least 06:35:23
16 teaching that his invention can be implemented with
17 an FPGA, an ASIC. I'd have to go back. I think
18 they said a CPLD again or -- I think there was a
19 third technology.

20 Q. (By Mr. Chandler) Butt never says that 06:35:40
21 his invention must be implemented using a
22 conventional general purpose digital computer, only
23 that it may be, correct?

24 MR. LINDSAY: Objection. Asked and
25 answered. 06:35:50



800.211.DEPO (3376)
EsquireSolutions.com

1 THE DEPONENT: We've talked about Butt. 06:35:55

2 We've looked at that sentence saying it may be. I
3 haven't memorized Butt, so I'm not going to say
4 that it doesn't say that it must be. My
5 expectation is that it probably does not say that, 06:36:07
6 but I can't say authoritatively.

7 Q. (By Mr. Chandler) And with respect to,
8 you know, what the present invention is, if you
9 look at Claim 1 of Butt, determining an optimum
10 offset delay value is part of Butt's claimed 06:36:22
11 invention, right?

12 MR. LINDSAY: Objection. Outside the
13 scope of direct or redirect.

14 THE DEPONENT: So Claim 1 does state a
15 method for calibrating a data-valid window, 06:36:50
16 compromising the steps of, and then it moves
17 forward, yeah.

18 Q. (By Mr. Chandler) And part of the
19 claimed invention in Claim 1 is determining an
20 optimum offset delay value, correct? 06:37:04

21 MR. LINDSAY: Objection. Outside the
22 scope of redirect.

23 THE DEPONENT: That is what the language
24 says.

25 Q. (By Mr. Chandler) And Butt teaches that 06:37:14



800.211.DEPO (3376)
EsquireSolutions.com

1 the present invention can be implemented in an ASIC 06:37:15
2 or an FPGA or other methods described in paragraph
3 63, correct?

4 MR. LINDSAY: Objection. Asked and
5 answered. 06:37:30

6 THE DEPONENT: Yeah, I think we've been
7 over that a couple times. It -- he uses the
8 language, the present invention may also be
9 implemented by the preparation of an ASIC, ASSP --
10 that's what he used -- FPGA. 06:37:49

11 Q. (By Mr. Chandler) For example, Butt does
12 not say that the claimed invention in Claim 1 must
13 be implemented using a conventional general purpose
14 digital computer; is that fair?

15 MR. LINDSAY: Objection. Again, asked
16 and answered. 06:38:08

17 THE DEPONENT: Yeah, I think I just
18 answered that a moment ago. I won't take a
19 position on that. I know he says that it may be.
20 I don't know any place off the top of my head where
21 it says it must be. 06:38:22

22 Q. (By Mr. Chandler) And you're not
23 offering the opinion, either in your declaration or
24 right now, that Butt has taken the position that
25 his invention must be implemented in a general 06:38:32



800.211.DEPO (3376)
EsquireSolutions.com

1 purpose digital computer, correct? That's not an 06:38:37
2 opinion that you're offering?

3 A. Not as I sit here, particularly because
4 of what's recited in paragraph 63.

5 MR. CHANDLER: Okay. Thank you, 06:39:15
6 Dr. Mangione-Smith. I have no further questions.

7 That concludes your deposition.

8 THE DEPONENT: All right. Thank you.
9 Have a good evening, everybody.

10 MR. LINDSAY: Okay. 06:39:26

11 THE VIDEOGRAPHER: Thank you, Counsel.

12 Before I go off the record, I just want
13 to make sure you have standing orders for video?

14 MR. CHANDLER: At some point we will
15 order the video, yes. 06:39:39

16 THE VIDEOGRAPHER: No order at this time.
17 Okay. Thank you.

18 Then this concludes the deposition of
19 Dr. William Mangione-Smith. The number of media
20 units used was one, containing ten video clips. 06:39:48

21 We're going off the record. The time is
22 6:39.

23 (Deposition concluded at 6:39 p.m.)

24

25 ---o0o--- 06:39:55



800.211.DEPO (3376)
EsquireSolutions.com

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

I, DR. WILLIAM HENRY MANGIONE-SMITH, do hereby
declare under penalty of perjury that I have read
the foregoing transcript; that I have made any
corrections as appear notes; that my testimony as
contained herein, as corrected, is true and
correct.

Executed this ____ day of _____,
2023, at _____, _____.

DR. WILLIAM HENRY MANGIONE-SMITH



800.211.DEPO (3376)
EsquireSolutions.com

1 I, Rebecca L. Romano, a Registered
2 Professional Reporter, Certified Shorthand
3 Reporter, Certified Court Reporter, do hereby
4 certify:

5 That the foregoing deposition testimony was
6 taken remotely before me at the time and place
7 therein set forth; that any deponent in the
8 foregoing deposition, prior to testifying, was
9 administered an oath; that a record of the
10 deposition was recorded stenographically by me and
11 which was thereafter transcribed under my
12 direction; that the foregoing transcript is a true
13 record of the testimony given.

14 Further, that if the foregoing pertains to the
15 original transcript of a deposition in a Federal
16 Case, before completion of the proceedings, review
17 of the transcript [] was [X] was not requested.

18 I further certify I am neither financially
19 interested in the action nor a relative or employee
20 of any attorney or any party to this action.

21 IN WITNESS WHEREOF, I have subscribed my
22 name this 9th day of May, 2023.

23 

24 Rebecca L. Romano, RPR, CCR
25 CSR. No 12546



800.211.DEPO (3376)
EsquireSolutions.com

1 DEPOSITION ERRATA SHEET

2 Case Name: Samsung Electronics v. Netlist, Inc.
3 Name of Deponent: Dr. William Henry Mangione-Smith
4 Date of Deposition: May 4, 2023
5 Job No.: J9467698

6 Reason Codes: 1. To clarify the record.
7 2. To conform to the facts.
8 3. To correct transcript errors.

9 Page _____ Line _____ Reason _____
10 From _____ to _____

11 Page _____ Line _____ Reason _____
12 From _____ to _____

13 Page _____ Line _____ Reason _____
14 From _____ to _____

15 Page _____ Line _____ Reason _____
16 From _____ to _____

17 Page _____ Line _____ Reason _____
18 From _____ to _____

19 Page _____ Line _____ Reason _____
20 From _____ to _____

21 Page _____ Line _____ Reason _____
22 From _____ to _____

23 Page _____ Line _____ Reason _____
24 From _____ to _____

25 Page _____ Line _____ Reason _____
From _____ to _____



800.211.DEPO (3376)
EsquireSolutions.com

DEPOSITION ERRATA SHEET			
1			
2	Page _____	Line _____	Reason _____
3	From _____	to _____	
4	Page _____	Line _____	Reason _____
5	From _____	to _____	
6	Page _____	Line _____	Reason _____
7	From _____	to _____	
8	Page _____	Line _____	Reason _____
9	From _____	to _____	
10	Page _____	Line _____	Reason _____
11	From _____	to _____	
12	Page _____	Line _____	Reason _____
13	From _____	to _____	
14	Page _____	Line _____	Reason _____
15	From _____	to _____	
16	Page _____	Line _____	Reason _____
17	From _____	to _____	
18	Page _____	Line _____	Reason _____
19	From _____	to _____	
20	Page _____	Line _____	Reason _____
21	From _____	to _____	
22	_____ Subject to the above changes, I certify that the transcript is true and correct		
23	_____ No changes have been made. I certify that the transcript is true and correct.		
24			
25	_____ DR. WILLIAM HENRY MANGIONE-SMITH		



800.211.DEPO (3376)
EsquireSolutions.com

	191:11	125:12	1029	1049
\$	192:2,7	1003	27:8,14	179:17,
	193:12	33:25	240:4	18,24
\$100,000	257:21	34:6	241:4	180:8
18:3	273:9,14,	35:13	242:10	1050
	19 274:12	97:10,14	244:8,12,	124:1
\$750	1,250	100:5	21 245:6,	229:10,
17:25	71:5	1005	13 266:13	14,19
	1-bit	26:19,23	270:7,20	230:20
-	44:14,15,	175:1,8	1042	231:2,14,
	18,19	176:15	122:16,	18
---o0o---	136:9,11	190:18	18,19	1051
7:3	138:3	1006	123:11,	204:23,24
275:25	144:9,12	27:1,5	12,17,18,	205:5
-3C	1.1	174:25	20	1052
88:1	247:7	238:7,17	1044	239:20,24
	256:9	1007	123:23	240:1,10
	259:3	27:17,20	124:1	241:22
0	1.25	1008	1047	242:16
	70:20	27:25	54:21,23	1053
0	71:1,5	28:7	55:4,11,	246:5,9,
47:13,21,	10	101	15 56:1,	13 247:1,
22,24	32:5	70:17	5,8,12	5,13
141:25	78:15,18	1020	57:13	248:5
0.9	79:8	28:10,13	58:9,25	250:16,25
161:25	80:12	82:2	60:11,25	251:9
	122:3	87:16,23	63:13	252:16
	221:8,10	134:17,19	64:23	253:2
1	257:6	135:19	71:1,7,	254:12
	10,860,506	136:1,21	10,20	255:2,8
1	7:15	137:21	72:11,14	256:3,13,
7:9 35:8,	10:19	138:7,18,	73:7	23
12 44:23	100	23 139:19	74:9,12	257:14,25
45:7	100:21	140:1,23	75:6	258:20
47:21,22,	163:5	142:11,15	78:15,18	259:4
24 68:14,	1001	143:20	79:8	106
20,23	10:19	144:20	80:12,21,	11:3
89:22,24	26:5,8,	145:5,12	24 81:4	242:15
104:24	11,16	154:20	246:20	1071
110:16	90:11	157:8,13	247:17	122:25
129:3	101:2	160:3	1048	123:3
135:4	116:7	161:13	115:23	1072
141:7,9,	124:23	162:13,24	116:2,6	122:25
18,25		168:21,25	117:1	
176:14				



800.211.DEPO (3376)
EsquireSolutions.com

108	22:2	230:2	100:3,16,	17 206:3
242:17	243:20	123a	19	207:3
109	244:2	240:19,	13	208:15
11:2,11,	114	22,23	123:9	209:12,15
12,13	31:4	241:15,16	126:22	212:1,7
51:21,24	147:1,7	242:20,25	190:23	213:24
52:4	169:6	124	130	214:6,8,
131:13	170:21,24	167:2	230:2	14 215:7
147:6,8,	240:9	124a	131	216:3
11	242:20	243:2,4,8	19:22	14B
10:02	115	12:45	136	204:18
49:17	263:1	108:2	51:25	205:6,12,
10:13	116	12A	52:5	18 206:3
49:20	30:4	90:11,16,	14	207:3
10A	125:1	20 91:1,	101:1,6,	208:16
121:23	118	5,11,19,	14,19,21	212:5,7
122:4,10,	240:14	23 92:19,	102:2,4,	213:24
16	118.8	25 93:8,	12 116:25	214:6,8,
10D	167:24	10,14	117:2	14 215:7
122:6	11:16	94:8,13	118:17,19	216:3
11	88:8	95:11	120:7	15
23:17	11:26	97:15	190:25	18:21
80:21,24	88:11	98:1,7,	211:17	90:1,5
81:4	11:59	10,13,15,	142	94:4,8
104:23	108:9	21,23	205:8	101:20,22
110:16	12	99:1,6	212:25	102:2,6,
229:25	34:6	100:3,16,	143	19,23
233:1,6,	98:22,25	18	212:25	103:8
8,14	99:2	12B	144	104:5,12
234:6,14,	123:9	90:12,16,	219:24	105:8
19,25	125:11	20 91:1,	145	106:13
235:10	126:11,20	5,11,19,	207:17	108:20
238:10,	128:6	23 92:4,	213:7	109:1,10,
13,16	190:17	11,17,19,	146	21 110:23
110	193:10	21,25	205:8	114:21
70:8,9	271:5	93:2,8,	216:15	115:1
131:13	120	10,14	147	116:6,12,
148:7	225:13	94:9,13	230:1,14	20 117:7
111	121a	95:5,11	14A	118:18
70:8	243:9,13	96:4,6,18	204:18	120:2,7,
131:14	123	97:15,22	205:6,12,	17 121:12
112		98:1,3,		229:24
19:19,22		17,24		230:5,17
		99:6,8,12		231:1,4,
				7,11,16,
				20 232:8,



800.211.DEPO (3376)
EsquireSolutions.com

12 235:7	113:17,18	1680	242:6,14,	11:13
247:6	1580	115:12,19	17 243:20	16:16
248:5	103:24	17	2,500	19:18,23
251:14	110:10,23	88:15	163:13	20:6,14
252:16	16	89:20	164:8,13	22:3,6,
253:1	60:1,23	94:3	165:7,16,	16,23
254:12	101:1,6,	97:13	21 166:15	25:5
255:1,2,7	14	100:4	2.5	28:21
256:3,12,	102:13,15	113:3	163:11	29:1 30:5
22 257:7	111:4,8,	192:18,23	20	31:4 32:5
259:3	20 112:5,	193:10	17:15	33:11,16
150	24 114:21	175	18:5 95:7	48:25
230:2	115:5,11	257:15	119:13,16	49:1
1501	116:7,11,	18	142:23	50:1,13
103:24	12,18	67:24	200	51:21,25
110:25	117:8	68:13	163:20,	63:10
1502A	118:16	69:1	23,25	70:18
104:16	119:24	97:13	164:7,13	88:14
1502B	120:2,7,	100:4	165:6,19	89:21
103:11	17,19	113:10,16	166:5,14	94:4
104:11,17	121:12	19	167:4	131:5
151	1601	97:13	168:25	147:2,12
230:2	115:13	100:4	170:14	162:22
232:19	1602B	175:6	230:11	163:6,16
1520	111:15,25	190	200-0	169:7
105:17,24	1630B	258:24	231:22	174:22
1550	112:2	1990s	200-19	175:4
103:16	164	56:16	231:24	176:18
104:14,20	161:12	1:04	2000	178:5,9
1560	162:13,23	108:12	83:1 84:4	195:8,12
103:19,20	1650	<hr/>	86:25	204:13
105:7,10,	112:3,4,	2	87:4	223:9,12
18,19,25	10	<hr/>	131:16	245:9
106:6,13,	1660	2	148:3	260:7
16,21,25	112:12,	35:8	2003	2007
107:2,7,8	13,15,18,	56:5,8,24	87:6,10,	87:14
109:2,6	25	59:11	11 131:16	131:17
1570	1670	191:15,24	2005	220:24
103:22,23	113:1,2,	192:4,8	32:24	221:3,8,
104:1	7,12,18,	193:13	33:1	14 246:14
109:7,10,	21,24	240:3,8,	2006	2008
17,22,25	115:7,9,	10,13	10:25	25:25
110:6,10	15	241:25	2009	87:18,21,
				25 138:18



800.211.DEPO (3376)
EsquireSolutions.com

25:24	94:5	30	31st	340
2010	24	161:15	20:7	204:7
82:7,11, 14,22	178:4	300	32	341
84:3,18	258:10,16	178:16	60:1	196:22
85:3,25	26	180:10,	320	197:4,25
86:25	90:2,5	14,22	102:13	199:12
87:4	94:5	181:3	178:15	202:23
2011	134:19	182:22	195:19,21	203:23
82:7	136:1	183:1,11,	196:5,14,	342
87:12	137:21	25 184:3,	18,21	196:23
2012	27	24 187:9	197:2,16,	197:5
29:5,11, 18 51:1	138:6,22	188:4,12,	22 198:11	198:1
73:4 75:4	204:12	13,21	199:3,9	199:12
79:5 82:7	28	189:6,16,	201:13	202:24
87:7,8	52:2,6	24 190:1	202:21	203:23
146:7	157:9,12	205:14	203:3,20	350
2017	174:3,9	207:19	204:7	188:5
30:17	28.8	215:22	216:7,12,	204:7
31:9	166:6,16	218:3	18,23	351
2018	167:11	219:25	217:3,4,	196:19
30:12,17	168:1	220:1,10	12 218:2,	197:4,24
2020	174:10,15	230:7,11	24 220:9	199:11
31:5	28.8-degree	300-0	232:24	202:22
2022	166:19	231:21	320/620	203:22
22:1	2:37	232:2	101:22	352
221:5	162:8	300-4	102:12	196:19
2023	2:47	231:23	322	197:4,24
7:1,17	162:11	232:5	116:19	199:11
20:7	3	301	178:14	202:22
21	3	207:1,2	207:18	203:22
144:3,8	56:12,24	302	217:13	360
145:12,17	59:11	187:20	323	164:14
211	91:4	188:3	178:15	166:16
170:18	175:23	190:13	230:14	229:6
22	3.4.5.1	30th	324	37
136:21	140:6	221:5	116:21	28:25
137:3	3.8	31	33	34:7,21
23	250:25	140:2,3,	135:19	35:13
90:1,5	251:11	23	337-TA-1023	36:2
		310	30:7	370
		228:19,23	55:14	227:20
		229:5	337-TA-1089	372
			30:12	185:13



800.211.DEPO (3376)
EsquireSolutions.com

186:23	12 176:3	205:5,15	102:3,19,	5:12
264:10,	43	217:10	23 108:21	238:2
11,20	25:9,18	220:11	109:10	5:24
265:9,13,	44	223:11,	110:23	238:5
24	25:10	15,19	111:5,8	5:39
374	45	224:22	112:24	245:21
227:22	176:17,20	226:2,15	113:7	5:48
376	195:7,12	229:23	116:7	245:24
189:1	48	230:7,14	118:5,10,	
223:17,20	142:10,14	238:22,24	15,22	<hr/>
224:11,24	145:4	239:3,16	120:5	6
225:5,11	4:29	257:24	121:13,24	<hr/>
226:4,13,	220:19	267:11,	122:7,11	6
18 227:7,	4:41	18,24	124:23	63:13
11 228:3,	220:22	268:6	125:11,13	64:23
10,15,25	4th	270:25	128:12	68:3
229:3	7:17	271:5,16,	146:6,20	70:25
263:22	5	18	221:19	150:15
38	<hr/>	50	235:18	193:15
33:15,18	5	163:9	236:7	267:18
250:16,24		506	246:25	268:10
251:9		10:15,18	247:2	
3A	5	14:14	51	6-0
240:5,8,	47:14	17:2,8	125:12	260:7
17 242:6,	58:9,24	26:5,8,	126:11,20	60
21 243:14	59:11	11,15	143:10,19	170:24
<hr/>	60:11,24	29:6	144:20	260:7
4	150:15	31:10,15	145:11,18	261:5,12
<hr/>	176:24	40:23	52	60-
4	177:6,19	50:25	128:6	something
7:1 23:17	178:16	54:3	178:8	126:20
32:6	181:3	88:22	245:9	61.2
56:25	182:22	89:8,15,	53	167:24
57:13	187:10	22 90:5,	179:1	62
59:11,14	192:10,	7,10,17,	55	125:12
61:10	19,21	20,22	204:16	126:12,21
113:10	193:14	91:1	57	267:6
150:15	195:11,	93:18,25	168:20,24	269:8
160:3	17,22	94:2,9,15	58	270:8,11,
193:21,24	196:4,13,	95:12	131:9	24
194:6	17,21	96:2,8,	154:20	620
42	197:2,16,	16,22	157:8,13	101:23
139:18	22 199:3,	97:15,21	160:3	103:9
175:4,6,	9,14	99:17		
	203:21	101:2,6,		
		8,14,20		



800.211.DEPO (3376)
EsquireSolutions.com

625	270:25	74:9,12	141:6,8,	accomplishe
165:21	72	75:6	17 142:3,	d
166:3	60:8	246:20	7	144:11
63	73	247:17	A7	212:19
244:7,11,	261:19,22	90	136:2,9,	accomplishe
20 245:6	750	153:14	12 138:3	s
266:16	18:5	166:9	abbreviated	189:22
270:8,19,	_____	167:20	75:20	accomplishi
23 271:23	8	171:25	135:21	ng
274:3	_____	173:9,12,	141:9	124:6
275:4	_____	18,19,23,	142:16	accordance
64	8	25 174:6	244:15	271:10,19
59:5	59:3,14	90-degree	246:15	account
64-bit	60:20,25	165:1	abbreviatio	68:6
59:19	72:10,14	166:4	n	99:21
65	73:7	187:3,13	249:21	198:19
162:21	125:15	264:12	ability	accounted
163:15,17	126:1,15	265:22	237:19	174:3
165:5	127:9,20	910	absent	accounting
69	128:13	122:2,6,	54:4	68:4
223:8,11	810	7,9,12,15	absolutely	133:12
6:07	127:21	124:5	150:14	190:2
259:22	128:15	95	208:3	211:21
6:13	129:3	245:10	218:5	accounts
259:25	84	9:01	abstract	198:22
6:28	225:10	7:2,7	89:12	accurate
269:25	840	9A	149:24	18:10
6:31	127:11	193:16	accepted	20:17,19
270:3	128:20	9B	86:1,15	22:16,19,
6:39	87	193:16	access	20,21
275:22,23	264:13,16	_____	37:8	154:18
_____	8A	A	83:14	178:3
7	193:15	_____	accessed	226:8
7	8B	a.m.	44:5	229:7
71:7,10,	193:15	7:2,7	accomplish	accurately
19 124:23	8DQ	A0	133:16,18	154:4
125:1	60:17	140:11	150:23	156:16
196:2	_____	A1	152:2	193:20
267:12,19	9	140:11	172:21	accustomed
268:22,25	_____	A2	181:13	29:16
	9	140:25	205:22	achieve
				41:21



800.211.DEPO (3376)
EsquireSolutions.com

achieving	11:24, 25	138:24	63:16	171:8, 15,
78:13	73:21		65:14, 17	20, 22, 23
acronym	75:13, 22	advance	67:17	173:10
52:8	76:8	55:22	68:2	
action	77:23	advanced	69:7, 15,	alignment
114:17	79:17, 21	34:13	22, 25	121:9
	81:17	35:20	71:10	125:18, 24
activated	132:23	75:18, 19	72:14	126:12
46:7	150:11	246:15	74:12	127:4, 10,
115:13	247:18	247:7, 12	78:18	16 128:21
167:3, 5	263:12	255:8	80:24	129:11, 13
168:5, 6	addressed	256:12,	138:16	130:1
177:17	132:20	14, 22	199:19	153:21, 25
activation	202:17	257:16	221:22	172:2
133:13	addresses	258:20	245:12, 16	alternate
active	138:25	advantage	247:1	158:22
260:15	addressing	214:9	262:3	alternative
actual	97:2	advantages	agreed	42:17
47:16	adhere	253:18	32:15	272:11
64:19	65:12	affect	83:16	alternative
202:9	adhered	106:21	120:13	ly
add	127:7	140:11	130:23	39:21
24:11	adjust	affected	221:17	224:19
added	210:7	186:19	agreement	244:17
77:9	adjusting	affiliation	19:10	alternative
195:14	260:12	s	ahead	s
231:13	adjustment	7:23	34:24	39:18
240:7	187:4	affirmative	algorithm	40:2, 9
adding	adjusts	ly	268:7	41:12
73:12	260:13	226:1	aligned	AMB
addition	262:3	aggressive	117:14,	75:12, 15,
16:12	administere	172:23	15, 19	20 76:4,
73:12	d	agree	118:3, 17	7, 10
additional	10:2	8:13	125:19	246:15
49:8	administeri	34:11	127:19, 22	247:16, 23
71:25	ng	35:19	128:2, 6,	248:4, 13,
142:15	8:14	36:6, 10	10, 11, 14	23 249:6,
257:5	admiral	37:6, 14	129:20, 25	25 250:15
259:10	68:16, 18	38:2	130:13,	251:14, 15
265:14	adopted	56:15, 23	19, 24	252:24
266:1	33:19	57:16, 20	131:2, 3	254:9, 10,
address		58:12, 24	171:24	24
		62:19	182:16	255:21, 24
			aligning	256:1
				257:5



800.211.DEPO (3376)
EsquireSolutions.com

258:7	apparent	applying	arrangement	82:20
259:4	267:15	93:3	s	83:6,8,
amount	Appeal	approach	132:24	13,17,24
18:7 31:2	7:14	260:11	arrive	84:6,14,
92:20	appeared	265:21	80:11	16,21,22
96:11,21	19:2 24:5	266:9,10	arrived	85:5,17,
106:23	appearing	268:15	67:1	23 86:7
130:3	162:22	269:1	arrives	91:19
231:22	appears	approximate	216:2	94:14
243:5	34:5	20:25	232:22	97:4
265:5,9,	54:17	approximate	260:15	120:4
13,24	97:23	ly	arriving	146:13,
analysis	105:16	16:5,18	80:9,11	19,22
86:3,16,	110:2	17:9	arrow	147:19
17 100:18	136:8	18:18	65:1	149:11
149:25	162:1	20:23	92:14	151:10
188:25	163:12	50:15	116:9,10,	218:12,14
203:10	176:12	69:8,16	11 238:19	244:24
analyze	193:11	95:7	239:14	246:25
149:16	247:4,22	127:12	240:7	265:25
analyzing	258:25	128:23	243:6	arts
85:19,21	259:2	174:6	arrows	267:15
and/or	appendix	234:21,23	60:20	ASIC
137:13,15	20:11	April	116:8	38:7,8,
Annita	apples-to-	87:18	art	17,21
15:17	apples	area	24:23	39:1,4,
annotated	165:8	43:7	26:19,22	14,20
116:8	application	areas	27:1,4,10	40:3,9,12
195:11	266:18	150:20	29:6,10,	41:2,11,
204:18	application	arguments	17 33:21,	15,19,20,
205:7	-specific	27:11	22 34:5,	23 42:20,
223:10	38:8	85:19,22	12 35:9,	21 53:8
annotations	244:14	149:2,15,	15,20	244:15,25
207:9	applied	16 150:1,	36:4,7,11	270:21
anticipated	96:18	10 151:10	37:7,15	271:25
185:17	98:2	219:17	38:3	272:10,17
anytime	106:23	222:2	40:12,20,	274:1,9
136:19	applies	242:5	23 43:10,	ASICS
apologize	149:12	arrangement	16,18	37:16
165:22	264:21	79:21	53:24	38:4
168:17	apply	81:17,21	71:16	42:23
210:14	264:8	arriving	72:22,24	43:5
		s	74:17	aspect
			78:22	93:16
				133:12



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 287
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 287

236:15	271:1	204:10	212:9	basis
aspects	assumption	218:18	213:21	22:8
51:6	86:2,15	224:16	215:21	96:15
59:6,7	asymmetric	235:22	216:8	BC
71:14	168:16	awful	218:21	177:7,10
72:19	asynchronou	68:6	220:21	184:8
79:14	s	91:16	225:4	BC1
101:18	243:19,23	92:6	228:9	177:11
120:15	244:1	awhile	236:15	BC2
assert	attached	219:20	238:4	177:11
171:1	48:24		245:23	Bear
asserted	54:25	B	259:24	168:19
17:5,6	115:25		262:13	begin
112:22	179:20	B-I	269:7	43:6
156:17,19	205:1	63:11	270:2,7	beginning
172:15	229:12	B2	272:17	7:8 159:2
177:12	239:22	7:15	background	176:2
ASSP	246:7	bachelor's	89:13	begins
274:9	attempt	34:16	Baker	147:6
assume	134:12	35:23	8:1	behalf
17:11	181:14	back	bank	8:1,6
20:9	attended	17:4	57:20	50:5
23:24	15:13	48:25	58:1	belief
25:12	51:17	49:1,15,	57:17	85:20
43:4 65:4	attention	19 51:9,	58:1	believes
85:22	31:17	20 52:14	bar	265:6
87:9	attorney	68:19	63:20	benefit
105:3	8:17	88:10	64:4 66:4	50:7 54:8
161:4	attorneys	93:25	125:9	69:3
184:13	23:23	101:10	barring	76:24
224:8	attractive	104:9	199:19	77:16,18
assumes	40:6	105:15	based	266:1
145:22	authoritati	108:11,13	98:9	benefits
152:24	vely	111:18	104:17	77:3,7
153:1	273:6	115:10	143:17	Bhakta
154:12	avoid	126:19	161:6	31:11,14
250:4	133:18	135:25	184:21	bidirection
assuming	134:13	162:10	202:10,14	al
21:21	aware	191:6	206:25	62:21
112:8	33:11,14	193:21	214:4	63:9
129:24	50:12	196:10	257:20	
174:23		206:21	263:19	
184:19		210:4,5,		
264:11		11,16		



800.211.DEPO (3376)
EsquireSolutions.com

big	60:1, 8,	blue	8:1	13:14, 16
41:23	17, 20, 25	116:11		18:14
bigger	61:10	231:5, 17	boundary	
160:20	140:24		38:14	briefly
billed	blame	blurry	bounds	103:1
48:21	262:21	38:15	195:2	111:11
50:16	block	42:14	box	131:14
billing	75:12	board	92:15	249:18
18:9	80:8	7:14	106:3	267:19
21:12	103:11	53:11	109:2, 6, 7	269:19
48:20	142:22, 24	94:12	203:11	bring
billionth	191:1, 4,	bot-	230:19	12:12, 19
67:18	18 192:2,	221:11	231:13, 17	97:3, 12
binding	4, 8, 10, 19	bottom	240:14	bringing
8:15	193:5, 14,	25:9, 18	242:20	170:15
BIST	15 194:6,	35:7	248:14, 21	broad
250:11	18 195:3,	60:11	249:3, 11	237:3
252:7, 11	4 196:5,	88:18	250:7	broader
bit	14, 18, 21	101:21, 23	252:16,	53:2
28:2	197:2, 16,	102:12, 14	17, 21	broken
38:15	22 198:11	104:5	253:5	46:11, 12,
42:14	199:3, 9	116:9	254:18, 20	16, 19
44:9, 23	202:21	126:15	256:9	brought
45:7 46:1	203:20	138:5, 22	boxes	170:19
53:4	204:7	139:14	81:12	buffer
59:4, 19,	216:7, 23	140:3	256:11	43:19
22, 24	217:12	145:18	257:3, 13	45:20, 22
61:15	218:2	160:12	breadth	46:3, 22
62:11	220:9	167:2	94:25	47:6, 9,
64:2 70:7	225:2	168:24	break	10, 18
73:12	247:8, 12,	169:18	21:10, 11	48:3, 4, 6,
92:10	15 250:13	205:9	48:18	9, 10, 15
140:11, 25	251:14	221:13	49:23	75:18, 20
141:6, 8,	255:8, 15	229:24	50:22	81:15
17, 22	256:11, 21	230:1	88:5	98:8
142:3, 7	259:4	231:4	108:2	102:5, 8,
145:7	blocks	233:6, 8	220:16	17
175:17	191:13	234:7	237:24	103:14, 24
183:16	192:3, 15	239:16	245:19	110:11, 22
185:14	193:24	240:13	269:21	111:22
248:19	248:6	247:6	breaking	112:2
bits	256:15,	251:7, 10	133:6	115:12, 13
59:3, 5, 14	21, 23	253:1	219:20	175:17
	259:3, 10	254:20	breaks	176:8
		Botts		



800.211.DEPO (3376)
EsquireSolutions.com

177:4,5, 7,14,17, 24,25 178:16,25 180:5,6, 10,14,22 181:3 182:22 183:1,11, 25 184:3, 17,24 185:3,6, 19 186:21,25 187:9 188:4,12, 13,21 189:6,11, 16,24 190:1,4 200:25 201:3,12, 13,21 205:14 206:17 207:19 209:2,4, 13,16,20 210:11, 17,20,24 211:1,8, 13,19 212:2,10 213:6 214:22 215:2,16, 22 216:2 218:3 219:25 220:1,10 224:17,25 226:9,11 230:7,11, 18 231:3, 6,12,21, 23 232:2, 5,20,23	233:11, 15,22 234:15 235:2,3, 8,11 236:15, 20,24 237:4 242:17 246:15 247:7,12, 17 248:4 255:9 256:12, 14,22 257:5,16 258:21 262:4 buffered 76:10 109:23 110:5 175:14 236:5 buffering 76:25 77:8 78:6 81:9 buffers 37:17 43:11,12, 13,15 46:5,14, 18 47:12 71:25 72:4,7 77:9 81:22,24 89:8 106:11 175:9,25 176:5,6, 9,24 177:8,19, 20 181:15	182:19 184:11 185:1 188:1 192:17 199:7 202:7 211:24 232:13,16 236:11,17 237:3,4 247:18 260:14 build 53:7 83:23 121:16 built-in 250:2,12, 14,22 251:22 252:4,8, 11 bunch 144:10 bus 253:18,21 business 41:1,6,10 53:15 Butt 27:7,14 147:2,5, 9,10,24 149:4 150:13, 18,21,23 152:1,4 153:5,16, 17,21 154:4,14 240:4,6, 13 241:4, 25 242:4,	7,9,14,21 243:20 244:8,11, 12,20 245:5,12, 16 265:16 266:2,12 268:7 269:9 270:7,11, 14,19 271:5,23 272:4,11, 15,20 273:1,3, 9,25 274:11,24 Butt's 147:19 148:2,14, 24 149:7, 20 150:4, 16 151:14 153:9,23 273:10 buy 42:7 165:15 by-eight 61:1,24 62:5,11 by-four 61:10,20, 24 62:7, 10 <hr/> C <hr/> calculate 92:20 93:9,14 164:21 165:13	calculated 93:12 97:8 calculation 92:22 95:21 97:3 165:11 166:6 calculator 164:17,20 calibrating 143:8 273:15 calibration 143:21 145:7 250:8 258:12,16 call 12:18 15:9,10, 11,22 38:22 65:25 107:10, 13,19,21 108:3 155:17 177:10 called 38:13,25 39:9 44:11 45:1,14 47:18,24, 25 57:17 58:1 65:4,8 73:13 75:12 92:13 103:15 107:4
---	--	---	--	--



800.211.DEPO (3376)
EsquireSolutions.com

135:6	123:7	30:19,20	centers	96:8 97:9
159:14,23	216:14	39:15	266:7	98:11
214:18,	carried	52:3 55:8	central	99:15
23,24,25	67:2	121:2,4,6	80:2,16	104:1
215:1	carries	169:14	176:8	107:12,
calling	147:6	173:22	247:17	17,22
194:24	carry	193:1	cetera	108:1,7,
calls	126:22	194:2	174:3,9	13
15:13,25	case	caught	212:25	109:15,24
16:12	7:14 19:8	61:17	Chandler	110:12
105:2	21:16,24	caused	7:25 8:1,	113:20
138:20	26:2	133:19	18 10:5	114:8,20
188:16	30:6,7,12	134:14	21:18	115:3,22
193:23	32:1 40:1	190:3	33:5,8	116:1,17,
194:15	45:6	cautious	40:24	24 118:4,
195:2	55:5,13,	62:4	41:9	8,12,25
camera	23 56:18	caveat	42:20,25	119:12,
13:25	66:25	89:4	43:9	21,25
capable	70:2	172:5	48:17	121:6,23
42:12	79:25	242:3	49:14,21	124:14,22
capacitance	87:9 90:8	caveats	50:23	125:10
175:18	93:13	79:2	53:23	126:11,21
176:1	96:13	center	54:8,20	127:9,20
capture	99:24	173:18,	55:1	128:4,12,
143:8,22	101:16	20,22	59:25	20 129:5,
154:7	114:25	centered	60:10	12,19
captures	133:4	152:15,17	61:5,14	130:4,11
66:11	152:19	154:8	62:9,19	132:22
capturing	160:21	173:13	63:8	133:15
154:15	163:12	265:7	64:22	134:7
capturing/ sampling	172:10	centering	66:2 67:4	135:5,18,
171:3	176:12,13	150:21	72:10	25
careful	184:18	151:15	73:17	136:11,18
86:23	194:24	152:3,5,8	75:15	137:4,11,
183:16	203:12,13	153:13	76:1,15,	20 138:5,
carefully	220:25	154:15	24 77:5	140:9,20
26:4,18,	225:6	171:2	78:5,14	141:8,15
25 27:7,	226:9	172:7	80:20	142:2,9,
16,24	228:22	173:2	83:1 84:1	23 143:6,
28:9	233:5	265:10,15	85:21	19 144:2,
93:18	247:4	266:2	88:6,12	13 145:4,
	257:22	269:9	89:10	11,17
	cases		91:10	146:1,20
	19:1		93:17	150:2
			94:18	151:4,14,
				23 152:8,



800.211.DEPO (3376)
EsquireSolutions.com

16 153:4	255:7,17	11,12,15	cheaper	235:9
154:6,14	256:10,20	channel	42:11	236:21
155:19	257:4,14,	133:6	check	241:24
156:18	23 258:6,	258:1,5	23:19	254:24
159:7	18 259:2,	characteriz	76:2	255:10,
161:17,24	12,17	ation	111:2	20,23,24
162:3,12	260:16,18	198:7	209:25	256:1
171:14	261:7,15,	204:4	248:22	chips
179:16,21	25	248:7	249:22	53:7
186:4	262:10,	characteriz	checked	59:13
193:12	13,18,20	e	67:23	83:19
195:6	263:14,24	40:10	209:11	84:21,23
198:8	264:6,22	66:16,21	chip	133:4,9
199:25	265:17	73:24	38:22	181:17
202:19	266:16	89:4	39:3	186:10,18
203:6	267:3,9,	91:23	59:15	200:6,11
204:12,23	20 268:4,	147:10	67:14,16	209:5
205:2	12,23	193:22	167:15,17	253:19
206:15	269:18,22	203:5	174:19	choices
208:8	270:5	213:1	180:11	39:18
212:24	272:20	271:13	182:4,5,	40:8,11
217:21	273:7,18,	characteriz	13,20	choose
218:19	25	ed	183:4,6	39:15
219:22,23	274:11,22	90:24	186:8	41:1
220:15,23	275:5,14	113:3	197:25	chooses
222:4,13	change	123:15	198:1,24	194:3
223:2	45:2	161:21	200:24	circle
224:10	125:18	charged	201:24	169:12
225:21	161:7	18:2,7	209:3,16,	circuit
229:13,16	182:7	151:7	21,22	37:24
236:23	183:1,6,	charging	210:10,	38:9
237:11,	12,25	17:22,24	16,18	39:11,24
18,23	184:16,22	chart	211:8	41:18
238:6	186:17	169:11	212:2,9	42:9
239:23	207:4,10	221:4	214:12,	48:7,11
240:1	213:6	230:9	21,24	79:14
245:18,25	217:7	chat	215:17,21	102:5,7,
246:8,10	changed	34:1	216:1,8,	8,16,17
248:4,12,	53:14,15	54:22	24	104:14
19 249:6,	208:23	220:25	217:12,25	105:10,11
15,25	changing	229:15	218:21	107:11
250:14,24	159:21	246:9	230:11	109:8,9,
251:6,21	185:5	cheaper	231:7,24	17,22,25
252:3,15,	207:24	42:11	232:3,6,	111:21
24 253:7,	208:4,8,	channel	14,22	
20,25		133:6		
254:10,24		258:1,5		



800.211.DEPO (3376)
EsquireSolutions.com

112:15	24 266:19	CKO	clarificati	clients
113:4,12,	circuitry	105:14,18	ons	151:12
13,16,17,	37:8 39:8	106:1,2,	108:16	clips
18,19,21	45:16	5,17,20	246:1	275:20
122:9,14,	73:12	109:16,	259:13	clock
18,19	153:13	23,25	clarifying	44:19
123:12,	178:19	112:17,22	260:4	45:11,12,
17,20,23	181:2	122:21,	clarity	18 66:1,
124:5	185:4	23,25	256:1	3,5,6
125:1,5	186:23	123:13,17	clean	69:8,9,
152:19	241:5	cl	13:3	16,17,23
159:20	264:12	89:24	clear	70:20,22
172:12	circuits	claim	20:13	73:22,23,
178:14,15	37:12,15,	89:22	24:12,15	25 75:14,
184:7	17,22,23,	120:15	32:22	22 79:18,
185:13	25 43:11	221:3,22	59:8,9,10	21 81:18
188:2	64:10	222:9,10,	67:11	98:7
190:13	68:10	14,16,21	83:5	99:13
195:19,21	107:4	223:5	87:23	103:21
197:1,22	121:17	236:22	95:22	105:16
198:10	124:11	273:9,14,	100:14	106:3,4,
199:3,9	192:17	19 274:12	107:17	7,20,24
200:20,22	citation	claimed	111:16	107:1,6
202:21	35:16	25:1	127:16	109:16,
203:20	cite	50:24	132:11	23,24
207:18	89:21	89:16	146:17	110:5
216:7,23	90:1	90:6,21	161:1,22	112:17
217:13	94:10,11	91:2,13,	166:19	121:17,19
218:2,20	163:16	20 94:15	167:22	123:17
223:17,20	cited	101:8	172:4	125:6,9,
224:11,	24:22	150:17	193:23	14 126:2,
20,24	28:16,20	236:8	194:2,14	13 127:2,
225:11,14	87:14	237:2	215:6	10,21
226:3,6,	94:4	273:10,19	217:22	128:13,21
10,13,18,	cites	274:12	222:13	129:17,20
24,25	35:12	claims	227:18	139:4,10
227:7,20,	162:22	26:15,17	240:3	154:23,25
22 228:3,	CK	89:5,7	260:5	155:3
15,25	125:6,9,	92:7,8	clearer	156:9,12
229:5	14 126:2,	95:16,18	88:2	157:9,11,
230:13	12 127:2,	118:11	client	17 158:3,
232:24	11 128:22	154:4	149:11,13	11,17,21,
240:15	220:2	245:17	151:7	23 159:3,
244:14	228:21			15,18
244:14				160:15,
263:21				20,23,24
264:10,20				
265:9,13,				



800.211.DEPO (3376)
EsquireSolutions.com

161:25	144:24	combination	247:25	190:4
163:11	174:1	226:10	commenting	191:16
164:7	closely	combined	97:6	193:25
165:3,7	16:23	47:17	100:8	204:9
166:15	104:10	combines	126:9	253:18
206:25		79:14	commerciall	254:2
207:25	closeness	comfortable	y	community
220:2	117:13	18:4	36:20,22	146:10
223:21,24	closer	256:8	committee	compared
224:2,9,12	42:18	command	132:8	41:11
225:14,	closest	75:13,22	commodity	42:25
18,20,22,23	201:21	76:9	42:6	207:25
226:13,	CLPDS	79:17,21,	common	comparing
18,19,21,	42:10	25 81:17	36:20	69:13
25 227:3,	coincide	134:22,23	44:11	165:18
5,7,8,9,	190:16	135:5,6,	57:5,10,	comparison
14,16,19,	colleague	20 136:2,	22,24	165:9
23,24,25	8:3	13,24	58:3,5	189:25
228:3,4,	colloquiall	137:7	60:8	206:18
9,12,17,	y	140:10,24	61:15,19,	207:3
23,24	60:6	141:6,17	22 62:5,	compensate
229:2,5	color	144:17	11 74:21	139:16
234:2,21,	116:8	230:18	77:16	compensatio
23 235:1	coloring	231:12	79:2	n
263:19,23	195:14	235:2	133:5	32:1
clock-	column	247:18	158:20	complementa
period-	90:1,5	248:13,21	191:17	ry
based	91:4	commands	252:10	64:9,11,
187:20	94:4,8	77:23	communicate	15 67:12
clocked	104:23	78:2,3	77:15	125:9
112:21	109:21	138:25	communicate	157:2,20,
190:14	110:16	comment	d	24
clocking	113:3,10,	24:24	249:24	complete
66:7,21	16 123:9	61:16	communicati	22:6,7,10
clocks	125:11	132:1	on	94:2
65:18	126:11,	149:17	132:12	132:7
66:17	20,22	commentary	133:3	204:3
107:6	128:6	14:12	communicati	265:20
138:25	202:6	24:11	ons	completely
224:8	columns	commented	132:10,19	97:23
228:7	57:21	148:19	133:5,20,	107:15
close	58:2	163:4	21 134:1,	183:3
		175:22	6,15	



800.211.DEPO (3376)
EsquireSolutions.com

complex	272:6, 22	confirm	consistent	contained
38:11	274:14	54:15	29:15	19:4
42:12	275:1	confuse	70:25	contents
compliant	concept	252:14	97:24	137:12
36:14	43:19	confused	261:4, 10	257:24
complicated	58:25	99:4	262:12	258:11, 15
44:9	62:5	106:12	264:3	context
172:24	64:22	119:1, 17	265:1	24:12
Complies	65:4	144:14	consistentl	29:20
8:22	146:4, 9	200:17	y	38:20
complying	150:6	211:2	201:7	40:23
167:3	156:23	confusing	consists	43:16, 21
component	236:18, 24	141:22	57:21	54:3
191:12	237:1	145:3	58:1	58:4, 14,
components	245:3	252:10	consortium	21 66:22
36:15	251:25	confusion	36:25	67:8
37:9 53:9	concern	179:14, 15	consortiums	77:12
73:16	40:4	connected	51:16	79:23
133:4	concluded	46:14	constructed	81:14
191:9	275:23	47:8	218:23	83:15
192:1	concludes	48:7, 13	constructio	85:20
211:21	12:9	103:14	n	86:3, 15,
212:3	13:12	112:1	221:4, 17,	17 92:18
comprises	275:7, 18	241:20	23 222:9,	95:1 97:4
14:17	conclusions	connection	10, 15, 17	99:20
59:2	14:18	217:10	223:5	139:22
compromisin	conduct	connector	consult	150:10
g	149:10	225:13	13:17	156:2, 6
273:16	confidence	consequence	consultatio	160:2
computer	172:15	62:17	n	218:7, 12
13:24	173:15	114:18	10:12	220:4
21:8	confident	133:8	consultatio	254:9
34:13	18:6	182:1	n	contexts
35:21	configurati	consequence	n	57:11
36:12, 15	on	s	10:12	63:23
37:9	209:9	40:17	consulted	contingent
49:10	210:1	considered	17:7	32:2
179:8	configured	131:2	17:1, 10	continuousl
180:14	136:13	159:12	52:20	Y
267:13	228:20	222:2	54:16	44:24
268:2	configuring	223:4	consumption	contrary
269:11	197:8, 9	contact	41:19	261:2
270:14, 16		11:14	contrast	contrast
				178:18



800.211.DEPO (3376)
EsquireSolutions.com

control	143:9,21,	conversatio	81:13,22	158:4
37:9	22 178:19	n	86:14,25	159:24
45:24	179:8	114:15	87:7,14,	160:4,10
46:2	180:7,13,	convey	18,25	161:25
60:23	19 187:2,	245:6	89:23	162:24
65:22	11,18,22	conveys	90:2	163:11,20
66:11	188:23	60:20	93:19	164:2
73:20	189:8,18	copies	94:5	165:13
79:17,25	196:1,6,	13:3	97:11,15,	166:22
81:21,23	15 197:13	copper	18 99:17	167:1,20,
106:8	200:4,8,	67:25	104:2,6,	25 169:3
123:4,19	19,22	68:14	21 105:6	171:4,9,
125:1,4,6	201:10	copy	106:18	21 174:17
126:1,13	202:4,7	268:13	110:14,15	175:5,10,
127:3,11,	210:24	core	119:25	14,15,19
21	211:3,6,	72:1	121:7	176:10,25
128:14,22	9,15,23	248:23	123:8	177:8
129:21	212:20	249:3	124:3	178:11,20
138:25	215:5	corner	125:2,6	179:11
177:7,13,	233:11,	221:13	126:4,16	180:22,24
16,22	17,23	correct	127:22	181:3,4
178:15	234:17	10:20	128:5,15	183:7,8,
180:4	235:4,12	16:3,4	129:13	13 184:24
181:14,24	236:20	20:8 22:3	132:13,14	185:9,22
182:15,16	242:1	23:24	134:12	186:6,13
195:19,21	243:24	24:17	136:14,24	187:4,14
216:18	252:25	25:4,18	137:7,15,	189:9
232:24	253:6	26:3	23 138:8	192:10,
248:18,24	254:3,25	28:17	139:1,5,	19,22
249:3	255:10,15	30:13,15	9,20	193:18
controlled	256:3	31:6	140:3,12	195:13,
183:4	257:11	32:10,11	141:1,10,	19,20,23
controller	controllers	33:19	18 142:4,	196:2
53:8	36:16	51:25	17 143:1,	197:14,17
58:20	controls	52:20	10,23	199:5,12
63:4	113:25	55:6,16	144:4,21	200:2,3,
67:13,16	convenience	57:9	145:7,13,	6,7,11
73:14	229:19	69:21	21	202:11,24
74:8	240:2	70:11,21	146:14,22	203:23
75:21	conventiona	71:1 74:4	147:3,11,	204:19
76:3	l	75:4	22 148:3,	205:15,19
77:11,14,	267:12	76:11	16 149:4	206:19
18,21	270:13,16	79:6	150:22	207:20
78:1,7	272:6,22		151:19	209:17
80:11	274:13		153:11,21	210:12,20
139:16			154:16	211:8,15
			157:18	212:2,10



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 296
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 296

213:8	255:2,10	275:11	CPUS	165:23
214:10	256:4,15,		38:24	CV
215:18,23	24 257:17	couple		19:25
216:4,9	258:1,7,	24:3	CRC	20:10,12,
218:3	12 267:7	216:25	248:22	15,17,24
219:9	270:17,	243:1	249:7,12,	21:4,5,13
220:3	18,23	274:7	16,21	30:1
221:6	271:6,17,	coupled	create	48:24,25
223:21	25 272:3,	53:21	39:14	49:25
224:4	7,12,23	court	64:4	50:13
226:25	273:20	7:19	77:18	51:20,24
228:4,13	274:3	8:10,12,	185:20	52:8,13,
229:1,6	275:1	20,23	186:1	15,17,19,
230:8,15,	corrected	16:25	created	22 54:14,
20	263:6	17:3	179:24	18
231:14,	correcting	19:8,16	208:11	cycle
18,25	86:22	21:24	creating	98:7
232:15,24	corrections	30:23	208:5	157:17
233:3,12,	108:15	50:8	cross	158:3,11,
18	246:1	54:9,24	260:21	23 159:3
234:17,23	259:13	69:3	261:16	160:15,
235:5,13,	correctly	115:24	262:1,16	20,24
21,24	24:7	179:19	263:15,25	161:25
236:6,11,	25:20	204:25	264:23	163:11
25 237:7,	48:8	221:16	267:4,21	165:3,7
12,19	137:19	229:11	268:5,13,	166:16
238:14,	183:10	239:21	24 269:13	206:25
17,20,25	198:6	246:6	CRSS	226:19,21
239:4,7,	cost	cover	249:3	227:8,14,
14,18	40:18	54:6	CSRS	16,19,23,
242:10,	42:21,22	87:1,3	255:16	24,25
17,21	costs	covers	current	228:4,24
243:2,6,	77:4	98:23	11:14	229:2,5
10,14,20	counsel	271:1	17:24	234:21,23
244:15,	7:22 8:9,	CPLD	21:1,5	cycles
18,25	13 13:17	38:10,18	48:23	128:21
245:15	21:2 25:7	39:6,9,	49:2	160:23
246:16,21	33:2	16,21	62:16	235:1
247:19	49:22	40:9,13	209:9	cyclic
248:6,24	119:20	41:2,11	210:1	249:22
249:7	161:14	42:4,18,	custom	
250:3,17	162:7	25 272:18	53:8	D
251:1,15,	269:20	CPLDS	cutting	D-D-R
22 252:18		37:16		
253:2,8,		38:4		
21,24				
254:4,13				



800.211.DEPO (3376)
EsquireSolutions.com

54:13	21, 23, 24	11, 13, 19,	234:15	DDR
D-F-X	112:10,	20 189:5,	235:2, 3,	25:15
250:9	13, 24	15, 24	8, 11	52:25
D-I-M-M	115:4, 15	190:1, 5,	236:10,	53:10
54:11	116:17	12	16, 24	54:7
D-I-V-X	117:18	195:18, 21	237:2, 3, 4	56:24, 25
50:9	118:16	196:22	243:13, 18	57:11
daisy-	120:6	197:4, 25	244:2, 3	58:16, 22
chained	130:17	198:9, 15	247:18	60:6
82:1	142:25	199:5, 11	249:6, 11,	63:24
dashed	143:8, 22	200:5, 10,	16 260:15	66:22
116:8	144:19	18, 23, 24	262:4	67:9
data	145:20	201:3, 12,	263:20	69:23
37:17	150:22	13, 21	265:10, 15	82:21
43:11, 15,	151:15	202:7, 23	266:1	83:19
19 54:13	152:5, 9,	203:22	268:8	84:4, 17
58:20	21	205:14, 25	data-valid	85:24
60:21	153:19, 24	206:10, 17	273:15	135:7
62:20, 21	154:7, 15	207:18, 19	date	147:11,
63:4, 6,	156:14	209:2, 4,	19:25	16, 20, 21
16, 22	163:19	13, 15, 19,	20:11, 19,	157:3
64:4	164:10	20, 21	25 29:5	172:22, 25
65:4, 5, 9,	167:25	210:1, 2,	48:25	241:24
15, 17, 18,	169:16	3, 11, 16,	50:1	242:15
23 66:5,	170:8	19, 24, 25	146:8	250:8, 25
8, 12, 15,	171:2, 3,	211:7, 12,	231:3	251:11
17 67:2, 5	9, 16, 21	19, 24	dated	254:19, 25
72:3, 7	172:8, 14	212:1, 10	83:1	255:9, 15
74:3, 6	173:3, 11,	213:5, 7	86:24	256:2
75:11, 13,	15 175:9,	214:13,	87:6, 13,	258:7, 9,
22 76:9,	17, 25	15, 22	17, 24	11, 16
25 77:8,	176:1, 5,	215:2, 16,	DDR1	
9, 24	6, 8, 9	21 216:2,	138:18	57:5
78:6, 7	178:15, 16	17 218:2	246:14	69:9, 13
79:18	180:10,	219:25	day	70:11
80:1	14, 22	220:1, 3,	7:17 16:8	85:3
81:9, 15,	181:2, 16	10	260:25	86:13, 24
21, 24	182:2, 7,	225:11, 12	265:2	131:15, 19
89:8 92:5	19, 22	230:7, 11,	268:2	132:12, 17
98:8	183:1, 2,	17 231:5,	days	148:2, 15
102:5, 8,	10, 13, 25	11, 20, 21,	18:21, 22	235:20
17 103:20	184:2, 23	23 232:2,	DB	DDR2
104:5, 8	185:1, 3,	3, 4, 13,	81:13, 14,	57:6
111:9, 16,	19, 21	16, 17, 20,	21, 24	69:7, 13,
	186:20, 25	22, 23, 24		17 70:10
	187:1, 9,	233:10,		86:13
	11 188:4,	15, 22		



800.211.DEPO (3376)
EsquireSolutions.com

87:5	DDR3-800	97:10,14,	121:9	115:3,4
131:15,19	163:10	17 100:4,	174:10	130:5
132:13,17	164:4	9,13,15,	degrees	133:8
148:16	166:14	22 119:1,	14:20	153:14,
150:14,25	DDR4	2 120:25	164:9,14,	15,17,18
151:16	57:6	131:4	22 165:9	165:1
235:23	81:1,6,	147:2,12	166:6,9,	171:25
DDR3	16,20	162:17,21	14,16	173:12,
57:6	151:17	163:5,16	167:11,	17,22
69:15	DDR5	165:5	20,24	174:5
70:20,23	151:18	169:7	168:1	182:1
71:1,2	deal	170:20	171:25	184:10,14
78:19,22	164:22	175:3	173:9,12,	185:4,6,
79:6,9,20	decide	176:18	18,19,23,	11,12,13,
81:8	39:13	178:5,9	25 174:4,	16,17,20
86:13	decided	195:7,12	6,9,15	186:1,2,
87:13,17,	72:6	204:13,17	229:6	5,7,21,
24	decisions	222:14	delay	22,23
131:16,	40:16,18,	223:9	65:24,25	187:13,20
22,24	22,25	245:8	68:11	188:2,22
132:2,4,	declaration	260:6	80:6,16	189:7
19 134:16	10:24	263:2	92:5,16,	197:9
136:23	12:18	264:16	20,23	202:2
137:6	14:17	274:23	93:1,2,9,	206:25
138:6,17,	16:15	decoder	12,14	227:3,4,
24 139:5,	20:15	248:14,22	94:23	5,20
19 140:1,	22:2,5,	decreasing	95:5,11,	229:5,8
9,22	11,15,23	269:2	15,17,20,	237:19
142:10,14	23:3 25:4	defending	25 96:3,	238:17,
143:6	28:16,21	8:7	10,14,16,	20,25
146:2	29:1,4	defined	17,20	239:4,7,
148:16,25	30:5 31:4	72:24	97:4,7,22	11,17
149:8,21	32:4,9,	83:17	98:2,17,	243:2,4,
150:14	16,19,23	160:6	20 99:7,	16 245:14
151:1,16	33:10,16	161:3,5,	12,16,24	264:9,12,
152:10	34:1,21	6,8,12,21	102:7,17	20,21
153:5,10,	35:12	definition	104:24	265:4,22
19 154:19	36:2 50:1	34:20	105:2,5,	266:7
162:14,23	63:9	35:14	10	268:8,16,
163:9,17,	70:7,18	degree	106:18,	17,18
24 164:1	82:22	34:13,16	21,22,23	269:2
166:20	88:13	35:20,23	107:10	273:10,20
167:22	89:21	69:13	111:21	delayed
174:11	94:3	117:13	112:15,	92:18
236:2			16,18,19,	105:10
			21 113:23	109:14



800.211.DEPO (3376)
EsquireSolutions.com

110:19,20	depends	110:9	194:22	23 274:6,
114:21,25	39:23	113:15	198:4	17 275:8
115:7	54:2	114:4,13,	199:14	deposed
130:2	57:18,23	24 115:17	202:13	18:19
171:24	67:7 68:6	117:22	203:2	deposition
206:8,13,	77:2	118:10,21	204:1	7:9,16,21
14,17	79:23	119:9,23	206:12	8:14,25
208:23	117:22	120:11	208:3	11:19,23
226:19,22	119:5	121:15	212:13	12:9,12,
227:8,12,	134:10	124:9,18	217:16	20 13:11,
13,15,16,	172:9	125:8	218:5	15,22
17,19,23	186:5	126:7,19	222:1,8	14:4
228:3,13,	deponent	127:6,15,	224:7	15:8,21
14,16,18,	8:15,22	25 128:9,	225:4	16:3,6,
21,22	9:3 40:15	18 129:1,	236:14	11,15
229:4	41:5,14	9,16,24	237:10,	17:16
243:8,12	43:3 49:4	130:8	15,21	24:9
delaying	50:20	132:16	239:25	93:19
167:19	53:6 54:2	133:2,25	247:22	95:8
173:8,14	59:22	135:2,11,	248:10,17	97:18
207:21	60:4	24 136:7,	249:2,11,	275:7,18,
208:6,13	61:3,12	17 137:2,	21 250:7,	23
265:8,12,	62:3,14	10,18	20 251:4,	depositions
23	63:2 64:7	138:1,11	18,25	19:23
delays	65:21	139:14	252:7,21	describe
105:11	66:20	140:6,15	253:5,15,	47:15
112:20	71:23	141:4,13,	24 254:7,	66:18
164:22	73:11	21 142:7,	16 255:6,	89:15
186:8,12,	75:10,25	20 143:4,	13 256:7,	102:9
16 188:9	76:14,20	12,15	18 257:2,	107:9
189:13	77:2,21	144:7,24	10,20	122:11
201:24	78:11	145:10,	258:4,15,	191:23
202:6	80:15	16,24	24 259:9,	192:21
207:23	82:24	146:16	16	213:5
228:23	83:11	149:24	260:17,23	261:13
229:2	85:8 88:4	151:3,7,	261:9,17	262:6
263:5,6,	89:3 91:4	21 152:1,	262:2,17,	265:9
10	93:7	12 153:1	21,24	268:10
dense	96:6,24	154:3,11	263:16	describes
160:18	98:6	155:15	264:1,24	169:15
density	99:11	156:12	265:18	170:1
41:16	103:4	158:25	266:5	192:7,12,
depending	107:14,	161:20	267:5,10	13,18
117:23	20,23	162:6	268:6,14,	193:4,8
	109:14,	171:12	25 269:14	
	19,21	185:25	272:15	
		193:7	273:1,14,	



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 300
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 300

194:1	designs	24 96:13,	66:23	271:2
260:11	40:3 72:4	19,21	69:7,9,	272:8
266:2	desk	98:20	15,17	difference
269:9	49:9	determines	76:11	79:12
describing	destination	98:8	79:22	130:8
64:24	167:13	determining	82:21	154:23
212:7		96:16	84:17	174:4
213:1,3,	detail	97:21	85:3,24	175:13
4,25	76:22	99:16	86:14	180:1
215:13	91:17	208:7,14	87:6,13,	191:3,6,7
267:25	95:3	268:8	17,24	differences
268:7	120:12	273:9,19	135:17	190:3
description	135:13	develop	235:21,24	
113:6,7	139:20,21	37:1	236:3	difficult
138:7	142:15	developed	263:7	47:15
190:20	240:9	132:18	diagonal	71:4
194:17	detailed	development	238:19	difficultie
232:7	88:23	40:18	239:14	s
257:15,25	details	68:19	243:6	262:22
258:6	31:22	device	diagram	267:1
design	57:23	38:12	102:4,6,	digital
34:15	120:20	59:3	16 111:20	39:9,10,
35:23	147:21	62:12	142:22,24	11,20,24
36:12	detecting	65:19	190:24	44:4
37:24	213:20	70:20	191:1,4,	45:14,16
39:3,4,9,	detection	106:25	18,19	47:20
18 40:8,	122:14	107:2	192:3,5,	64:10
11 41:25	124:5	135:8	7,8,10,	107:4
42:8	determinati	163:10,20	19,22	124:10
46:16	on	164:1	193:5,13,	159:19
57:22,23,	95:15	166:22	14,15,16,	267:13
25 58:3,5	determine	167:7	17 194:6	269:10
59:15	64:19	182:7,9,	195:3	270:14,16
185:3	93:1	11 242:15	247:8,12,	272:6,22
218:6	96:3,9	252:9	15 251:14	274:14
245:2	118:2	devices	255:8	275:1
265:20	152:2	36:13	256:11,22	DIMM
designation	220:13	37:3,22	259:4	53:10
241:7	245:13	51:7	271:9,18	54:9,11
designed	268:16	56:15	diagrams	56:9
38:22	269:1	59:2,4,	91:5,7	58:23
133:17	determined	11,12	194:18,19	60:6 61:8
designer	95:12,23,	61:25	195:4	62:1,20
173:15		62:17	267:11	63:24
			270:25	66:22



800.211.DEPO (3376)
EsquireSolutions.com

67:9	249:1,20	32:12,16	204:17	147:5
71:11	250:5,19	33:12	254:8	204:19
72:9,15	251:3,17,	42:19	261:14	213:20,25
74:13	24 252:6,	100:2	discussed	262:22
75:2 76:4	20 253:4,	198:7	25:7	266:20
77:12,23	14,23	222:4	50:22	267:1
81:11	254:6,15	disagreed	95:1	distinction
139:4,11,	255:5,12	100:12	97:14	191:19
19 174:20	256:6,17	disagreement	101:11	distinguish
181:15,25	257:1,9,	t	110:13	72:6
201:22	19 258:3,	32:18	131:14	191:18
236:5	14,23	33:6 50:6	144:16	distributed
255:20	259:8	100:7,15,	162:16	81:10
DIMMS	273:13	17,21	164:8	176:7,9
52:25	direction	disappear	168:1	181:15
54:7	102:25	229:9	174:11,14	185:3
58:16,22	111:10	disbelieve	175:17	236:10
74:22	157:5	164:24	189:20	distributin
77:15	168:9,11,	disciplines	199:21	g
83:19	12,15	34:17	218:9,10	182:15
167:15	220:2,13	35:24	224:3	district
175:14	228:10	disclose	244:23	16:25
direct	directional	93:1	256:15,	17:2
63:1	63:11	217:17	20,24	19:8,16
71:22	directions	discloses	discusses	21:24
73:10	80:18	175:9	138:20	30:23
75:9,24	directly	180:9,12,	discussing	31:6
76:13,19	84:24	17 218:13	40:19	221:5,16
116:16,23	198:24,25	disclosing	95:4	divided
117:21	200:24	180:18,20	108:20,24	147:9
124:8,17	201:14,16	disclosure	147:9	164:13
126:6,18	216:21	225:6	159:10	166:15
127:14,24	266:21	disconnecte	169:1	Divx
135:1,10	disable	d	217:6	50:5,8,9,
141:3,12,	142:2	48:11	246:22	11
20 142:6	disabled	discovery	257:6,12	DLL
143:14	141:25	49:9	266:16	225:14
144:1,6	142:8	discuss	268:7	226:24
145:23	241:16	119:10	discussion	227:2
203:25	disadvantag	138:13	91:24	229:5
221:25	es	199:21	93:10	Doctor
222:7	253:18	discuss	99:20	8:20
223:1	disagree	129:16	100:16	document
237:9,14			115:20	
247:21			129:16	
248:9,16				



800.211.DEPO (3376)
EsquireSolutions.com

20:3,6, 10,14 33:3 56:20 58:6 87:20 160:18 162:17	145:20 150:22 151:15 152:9,21 153:19,24 163:19 164:10 166:21,24 167:4,25 168:5 171:8,16, 20 172:8 173:3 183:2,13 184:2,16, 23 185:5, 21 186:1 187:1,11 196:22 197:4,10, 12,15,25 198:9,15 199:1,5, 11 200:5, 10,18,23 201:5,11 202:9,23 203:3,22 204:5,7 206:23,25 207:13 209:5,20, 21 210:3, 17 212:9 214:12,24 215:1,22 216:9,11, 12,20,24 217:4,11 218:1,21, 24 219:25 220:9 226:14 231:21,23 232:3,5, 13,17,21 235:3	243:13, 18,22 247:18 DQ (IN) 210:20 212:20 214:20 215:4 216:3 235:10 DQ (OUT) 207:11,12 210:19 212:21 214:16, 18,19 216:1 233:7 235:4,12 DQS 63:16,18, 19,20 64:3 65:17 66:4,17 67:4,10, 11,12 74:3 76:9 92:13,15, 20 93:3 94:23 96:4 97:22 98:2 99:7 102:5,7, 21,24,25 103:9,17, 18,25 104:16,17 108:25 109:12,14 110:17 116:9,19 117:18 118:18	119:3 120:1,6 121:3 130:18 150:21 151:15 152:21 153:20,25 154:8,15 157:13, 16,19,23 158:2,16 159:23 160:9,13 163:18 164:9 166:21,24 167:3,19, 23 168:4 171:8,15, 20 172:7 173:2 183:2,12 184:1,16, 22 185:5, 13,21 186:3,25 187:10, 13,17,21 188:5,6, 10,12,16, 18,22 189:7,16, 17,23,25 190:15 196:18 197:3,10, 12,15,23 198:9,15 199:4,10 200:5,9, 18,23 201:5,11 202:9,22 203:3,21 204:5,7 206:23	207:1,13, 20 209:5 213:7 214:23,25 218:24 220:3 225:12 226:11,15 233:16 234:16 241:23 242:14, 19,24 243:4,8, 12,16,22 245:15 247:18 263:20 264:9,21 265:4,7, 8,12,24 DQS (IN) 207:10 210:12,23 DQS (OUT) 208:19,22 209:13,16 210:25 215:3,17 233:7,18, 23 234:8, 17,20 DQS-TO-DQ 163:24 DQS/DQS 241:18 DQS/DQS_UN 241:2 DR1 238:14, 16,25 239:17 DR2 239:17
--	--	---	--	---



800.211.DEPO (3376)
EsquireSolutions.com

DR_PDQ_OUT	Drawings	57:4	edges	11,17
243:19	190:21	70:16	157:3	240:9
DRAM	DRC	159:11	181:25	243:2,4
36:13	195:23,25	175:17	effective	elements
53:7	196:5,14	244:23	184:14	24:24
59:2,13	197:8	246:18	265:7,20	38:13
60:25	198:12,14	263:4	effectively	41:24
61:1,25	drive	264:4	70:10,15	51:8
62:12	47:8,13,	early	129:25	103:5
65:18	14	17:6	224:18	106:8,10,
66:16,18	driven	easier	effort	11 148:21
67:6	241:6,8	165:14,17	78:1	163:3
73:16	drives	easiest	elaborate	195:16
76:10	159:20	34:3	77:5	242:12
79:22	driving	easily	electrical	Ellsberry
139:4,10	47:7	60:23	34:13	27:16,20
167:15	DS	82:8	35:21	emailing
174:18	104:4,7,	Eastern	46:7	14:4
181:17	24 105:2,	221:5	48:14	embodiment
183:14,15	5,19	easy	64:13,14,	90:6,21
186:8,10	106:6,18,	42:15	15,18	91:9
198:24	21 110:21	172:20	68:9	101:7,17
201:24	112:17,19	204:22	121:10	102:6,9,
DRAM1	dual	229:21	130:9,14,	18 111:22
59:11	54:12	economic	20 191:9	122:13
80:12	56:10	39:18	Electronics	271:8,16,
DRAM4	due	40:17,25	7:11 8:2	20
80:11	65:24	edge	element	embodiments
DRAM5	DW0	107:6	78:12	89:16
80:7,8	239:7	156:23	92:4,6	120:14,
DRAM8	DW1	170:10	103:20	22,23
80:9	239:4,18	226:20	105:17	emerged
dramatic	DW2	227:9,24	106:9	56:16
40:4	239:18	229:1	110:25	emphasis
DRAMS	dynamic	edge-	112:12	188:24
58:13	202:15	aligned	113:1,2	enable
61:9,15		116:19	133:14	136:3,10,
75:14	E	117:12	138:2	12 141:5,
182:2		118:24	191:16	15 177:25
202:6		119:3,5	201:12	enabled
211:20,25		121:4,5	203:3	137:22
draw	earlier	173:5,6	238:14,	138:4
203:11		226:16	17,25	
			239:4,7,	



800.211.DEPO (3376)
EsquireSolutions.com

141:10,14	35:21,24	133:13	EXAMINATION	5,8,14,
142:1	39:17	134:13	10:4	17,20,25
241:14	41:25	211:22	260:1	28:7,10,
242:24	42:3	249:23	270:4	13,21
	53:13	Esquire	examined	29:1 30:5
enabling		7:20	10:2	32:5,24
144:15	engineers			33:11,16,
	83:21	essence	examining	25 34:6
end		205:23	58:6	35:13
20:16	enter			48:25
26:15	203:10	essentially	examples	50:1,13
49:25		42:5 49:1	57:1,2,5	51:21,25
50:13	enters	184:12	59:24	54:21,23
52:5 70:9	12:8	186:22		55:4,11,
131:3	109:7	225:2	exception	15 56:1,
137:12	entire	226:24	186:22	5,8,12
147:20	234:21		excess	57:13
167:23		estimate	18:2	58:9,25
171:1	entities	16:13		60:11,25
175:12	24:25	17:18,20	exclude	63:10,13
179:16	equal	18:8	172:1	64:23
216:15	141:7,18		222:22	70:18
233:19	153:2,3	estimates	excluded	71:1,7,
264:19	154:13	16:23	19:4	10,20
		et al	excuse	72:11,14
endeavor	equals	7:11	14:10	73:7
20:2	141:8			74:9,12
29:19	166:16	evaluate	exemplary	75:6
91:14		242:5	89:16	78:15,18
	equating		90:6,21	79:8
endeavored	225:9	evaluated	101:7	80:12,21,
26:2 76:2		149:2	120:14	24 81:4
149:17	equation			82:2,7,22
237:16	93:7	evaluating	exercise	84:3,18
	164:19	151:9	149:9	85:3,25
endeavoring	165:12	evening		86:25
242:4	166:1	275:9	exhibit	87:7,12,
			10:19,25	16,23
engaged	error	event	11:13	88:14
31:8	47:15	155:5	16:16	89:21
	81:3		19:18,23	90:11
engagement	133:18,	evidence	20:6,14	94:4
21:23	22,23	21:16	22:3,6,	97:10,14
	134:1	145:23	16,23	100:5
engineer	210:6	250:5	25:5,14,	101:2
10:10,13	213:21		19,23,24	115:22,23
63:19		evolved	26:5,8,	116:2,6,7
68:18	errors	56:23	11,16,19,	
	20:3	exact	23 27:1,	
engineering	55:24	95:20		
10:12	56:4			
34:14,17				



800.211.DEPO (3376)
EsquireSolutions.com

117:1	239:20, 24	expensive	54:10	250:8, 23
124:23	240:1, 4,	42:12	64:2	eye
125:12	10 241:22	experience	71:18	169:2, 3
131:5	242:10, 16	34:15, 18	73:8 75:7	172:16
134:17, 19	244:8, 12,	35:22, 25	77:19	173:16,
135:19	21 245:6,	38:15	79:9 81:5	18, 20, 22
136:1, 21	9, 13	74:20	89:12	265:7
137:21	246:5, 9,	79:1	90:25	266:7
138:7, 18,	13, 20	experiences	91:11, 18,	
23 139:19	247:1, 5,	175:19	25 92:9	<hr/>
140:1, 23	13 248:5	expert	94:12	F
142:11, 15	250:16, 25	14:12	95:10	<hr/>
143:20	251:9, 10	16:15	97:25	fact
144:20	252:16	18:23	102:24	25:23
145:5, 12	253:2	19:2, 3, 5,	103:1, 7	59:23
147:12	254:12	12, 23	111:9, 11	61:17, 22
154:20	255:2, 8	22:2, 5,	156:8	152:13
157:8, 13	256:3, 13,	15, 22	187:16	181:24
160:3	23	25:4	197:7	217:11
161:13	257:14, 25	28:20	205:13	270:19
162:13,	258:20	29:1, 4	217:17	factors
22, 24	259:4	30:4 31:4	249:18	93:11
163:6, 16	260:7	32:4 55:6	252:4	facts
168:21, 25	266:13	63:9	explained	145:22
169:7	270:7, 20	70:7, 18	45:9	250:4
175:8	exhibits	88:13	explaining	fail
176:15, 18	14:20, 23	89:21	230:10	121:20, 22
178:5, 9	25:12	91:25	explains	184:18, 20
179:17,	82:6	131:4	230:5	failover
18, 24	exist	147:1	explanation	254:20
180:8	189:14	176:17	88:22	fails
181:6	208:5	178:4, 8	99:23	121:9
190:18	existed	195:7	218:25	268:18
195:8, 12	132:12	204:13, 16	express	269:3
204:13,	236:6	223:8	22:8	failure
21, 23, 24	exists	expertise	expressed	46:16
205:5	86:9	43:8	33:6	fair
220:24	168:10	explain	extent	18:1
221:3, 8,	expect	38:17	28:23	21:14
14 223:9,	101:11	39:7	62:4 85:9	33:22
12	172:9	43:24	126:14	39:22
229:10,	expectation	44:7	150:5	48:9 49:3
14, 19	273:5	45:19	external	57:6, 24
230:20		48:2 53:3		
231:2, 14,				
18 234:12				
238:7, 17				



800.211.DEPO (3376)
EsquireSolutions.com

60:2 62:1	23:15	76:8,16,	207:1	121:12,23
70:10	36:7	21	243:20,23	122:3,10,
80:13	37:7,15	246:14,	244:1	16 124:23
81:18	38:3	20,24	249:12	125:1,15
89:1,18	43:11	247:1,13	263:20	126:1,15
90:4,19	50:23	248:23	figure	127:9,20
93:4 95:8	51:2	249:25	42:8	128:13
104:25	59:13	250:15	72:1,17	129:3,23
111:17	67:10	252:25	73:13	142:21,23
117:17	73:1	254:10,25	75:11	144:3,8
121:13	85:17	257:16	81:7	145:12,17
135:8	86:4,8,10	FBDIMMS	91:11	153:16
138:19	134:22	74:20	92:21,25	157:9,12
139:8	149:10	feature	93:2	158:5
147:7	191:20	139:16	94:24	159:1
154:1	245:3	fed	95:11	160:19
155:22	249:7	103:19	96:18	169:18
157:10,14	familiarity	227:20	97:22	175:21,23
158:1	37:12	feel	98:1,3,7,	176:14,24
161:13	38:5 51:2	95:2	13,15,21,	177:6,19
167:13	family	117:1	22,25	178:16
173:20	236:16	166:2	99:2,8,12	181:3
176:3	famous	179:14	100:1	182:22
178:2	68:16	181:6	101:19,	187:10
180:15	farthest	191:24	20,21,22	191:11,
182:23	133:14	234:12	102:4,12,	15,24
189:18	fast	felt	13,15,19,	192:2,4,
194:19	69:8,16	52:14	23 103:8,	7,8,10,
197:21	faster	86:19	19 104:5,	19,21
214:2	64:11	Ferenc	12 108:20	193:5,12,
225:2	69:24	8:4	109:1,10	13,14,15,
227:22	fastest	FFO	110:23	21,24
233:23	70:23	239:10	111:4,8,	194:6
235:15	favor	field	20 112:5,	195:11,
248:7	41:10	34:15,18	24	17,22,23
259:5	FBD	35:22,25	114:16,21	196:2,4,
274:14	257:25	83:8	115:1,5,	13,17,21
fairly	258:4	138:3	11	197:2,16,
91:16	FBDIMM	FIFO	116:11,	22 199:3,
falling	74:14,15,	186:23	12,18,20,	9,14
170:9	17 75:3,	187:19	25 117:2	203:21
falls	7,20	188:3	118:16,	205:5,15,
60:9	familiar	190:13	17,18,19	17,18
13:21	13:21		119:24	207:3
			120:2,7,	208:15,16
			19,21	209:12,15
				211:17



800.211.DEPO (3376)
EsquireSolutions.com

212:1,5	12,19	20:21	270:25	focusing
217:10	92:19	finally	271:1,9,	99:18
220:11	94:8,13	243:22	18 272:8	106:13
223:11,	95:11	find	flowing	191:15
15,19	96:4	11:9 24:8	79:19	214:17
224:22	97:15	87:2	flows	footnote
226:2,15	98:10	220:1	115:19	24:6
229:23,	99:6,19,	fine	fluidity	160:3
24,25	20 100:3,	94:19	242:12	form
230:5,7,	16,18	191:24	fly	39:14
14,17	101:1,6,	finish	95:24	40:14
231:1,4,	14 102:2	215:12	fly-by	41:4,13
7,11,16,	104:10	245:19	79:20,24	42:24
20 232:8,	105:8	firm	81:17,20,	43:2 53:5
12 233:1,	106:13	15:1,4	25 132:9,	54:1
6,8,14	116:6	30:24	11,18,23	57:10
234:6,14,	117:2	fixed	133:2,20,	59:21
19,25	120:7,21	185:12,15	21,25	60:3
235:7,10	193:15,16	186:2,21	134:6,14	61:2,11
237:16	194:17	187:3,13	138:24	62:2,13,
238:10,	204:18	264:9,21	182:17	25 63:21
13,16,22,	205:6,12	265:4,8,	186:5,7,	64:6
24 239:3,	206:3	13,24	12,16,20	65:20
16 240:3,	212:7	flaw	189:13	66:19
5,8,10,	213:24	266:9,10	190:3	76:19
13,17	214:6,8,	flaws	198:19,23	77:1,20
241:25	14 215:7	265:21	201:23	80:14
242:14,	216:3	flight	211:22	83:10
17,21	229:20	139:3,9	263:5,6,9	89:2 91:3
243:14,20	242:6	flip-flop	focus	93:5
247:7	267:11	44:8,9,	31:21	96:5,23
248:11	figuring	12,15,24	89:6	99:9
255:1,14	165:16	45:2,5,7,	157:22	103:3
256:9	file	11 124:13	181:9	109:20
257:21	7:14	flip-flops	188:10	110:8
259:3	51:22	37:18	228:9	113:14
267:18,24	filed	43:12,13	focused	114:3,12,
268:6,10,	12:23	44:11	27:11	23 115:16
22,25	13:4	124:10	51:15	118:9,20
271:5,16,	221:4	flow	93:22	119:8
18	files	267:11	121:1	120:10
figures	13:4,6		150:9	121:14
26:10,13	18:13		198:17	124:8,16
89:14	final		231:1,3	125:7
90:11,16,				127:5,24
20 91:1,				128:25



800.211.DEPO (3376)
EsquireSolutions.com

129:15, 22	196:25	117:1	functionali	134:12
130:7	197:20	181:6	ty	156:5, 13
132:15	200:1	234:12	144:16	157:4
133:1, 24	203:7, 18	from-the-	256:2	240:22
135:10	213:23	fresh	257:5, 12	251:25
136:16	214:5	94:2	270:12	267:12
140:5, 14	219:8	front	functions	269:10
144:23	forms	12:16	144:10	270:13, 16
146:15	74:22	13:3, 7, 9,	267:10	272:6, 22
149:23	226:11	11 19:16,	fundamental	274:13, 25
151:2, 6,	forward	18 72:8	202:17	generally
20	22:13	82:3	_____	45:12
152:11, 25	273:17	97:10	G	54:6 66:7
154:2, 10	forwarded	101:4	_____	67:15
155:14	103:22	108:21	G-A-T-E-O-N	68:9
156:11	forwarding	131:6, 10	240:24	69:23
158:24	79:17	162:14	gate	70:3
185:24	found	247:11	45:22	73:24
193:6	23:21	frozen	GATEON	89:6
198:3	24:4	262:17	240:14,	114:17
199:13	Foundation	frustration	21, 24	200:12
202:12	116:15, 22	s	241:4, 14,	generate
203:1, 25	117:20	213:10	15	227:3
206:11	142:5	full	GATEON_UN	generated
217:15	144:6	12:15	240:18	189:10
218:4	fourth	15:24	242:24	199:1
225:3	89:22	55:19	gave	225:14
250:6	FPGA	94:25	74:18	226:23
258:22	39:16, 22	fully	259:14	generates
259:8	40:9, 13	137:13	Gen1	190:15
266:3	41:2, 11	182:16	79:1	207:22
formed	42:4, 17	fully-	gener-	215:2
85:12	43:1	buffered	226:6	225:11, 25
151:4	244:18, 25	74:13	general	226:6
219:11	270:22	function	38:25	263:20
forming	272:2, 10,	103:6	40:1	generating
27:22	17 274:2,	145:6	43:18	184:8
84:2 85:1	10	180:4	53:2 60:7	223:16, 20
148:1, 23	FPGAS	224:12	66:25	224:11,
149:1, 6	38:13	functional	91:14	20, 24
150:2	42:11	191:15	130:23	225:11
153:8	free	193:24	133:18	226:3, 5,
168:17				10, 13, 18
171:6, 18				227:7, 22
185:8				
189:4				



800.211.DEPO (3376)
EsquireSolutions.com

228:2,15,	great	224:1	happy	21:3
24 263:21	76:21	229:7	21:1	117:3
generation	162:6	239:6	24:10	helps
69:22	greater	243:17	100:23	14:22
249:12	40:4 42:1	244:4	119:10	Henry
generations	78:13	271:14	135:15	10:1,7
56:24	95:3	guessing	148:5	hereto
generator	99:23	68:25	162:19	54:25
252:17,22	172:18		hard	115:25
give	229:8		127:15	179:20
8:25	242:11		hardware	205:1
33:24	greater-	H	44:2	229:12
41:21	than-the-	H-A-R-M-A-N	156:3	239:22
68:17,21	whole	50:10	Harman	246:7
69:18	172:17	H-O-P-P-E-R	50:6,8,9,	high
74:18	greatest	69:6	11	38:16,19
85:9	41:16	half	head	39:7
89:13	green	107:23	23:10	40:10
124:2	59:1	158:23	44:2 70:1	41:9
215:11	180:11	229:2	164:12	42:22
251:4	231:8	231:4,6	180:3	44:1,16
268:1	242:16	234:22	274:20	45:21
goal	ground	halfway	heading	47:22,25
88:24	241:20	192:14	35:9	64:15
205:21,	guarantee	hand	147:13	73:19
23,24	166:23	8:21 69:2	190:20	76:17
good	guess	93:24	headings	81:5
7:5,25	37:24	hands	54:18	156:25
17:17,19	47:23	82:8	heard	157:18,21
79:12	50:9	handy	7:12	158:4,11,
88:4	83:11	35:3	22:25	14,15,18,
90:15	106:17	220:25	31:13	22,23
156:15	110:13	happen	198:6	159:5,9,
174:1	113:10	114:19	219:2	10,14,15
220:17	115:17	157:1	heartbeat	160:16
269:23	117:15	203:16	45:17	176:1
275:9	148:21	209:25	held	177:25
Grace	160:25	212:15	7:16	207:11
68:16	177:23	happening	helped	246:21
grammatical	180:16	133:23	15:4	252:3
ly	185:13	happily	high-	impedance
91:6	189:2	13:20	helpful	159:13
	203:17		14:21	high-level
	223:24			



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 310
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 310

88:22	196:4,13,	182:6,21	honest	83:7
higher	17,21,25	183:10,24	31:16	Hyun
18:8 43:5	197:17,21	186:11,	47:5 73:6	31:10,14
77:25	198:18	20,25	84:8	
78:2,8	199:3,9,	187:9	96:24	
	20 203:18	188:20	168:2	<hr/>
highlighted	204:4,18	189:5,15		I
59:1	205:6,7,	196:1	Hopper	
195:18	8,12	205:14,21	68:17	I-O-B-I-S-T
230:19	206:16	206:3,9	69:6	250:9
231:5,7,	207:17	208:24	host	i.e.
17 240:10	212:16	209:2,15,	179:8	137:14
242:16	213:25	19	180:13,19	id
highlightin	216:3	210:11,15	hot	89:24
g	217:6,14,	212:8	202:16	idea
195:15	16 218:7,	215:15,20	hour	218:16
	23	216:6,22	17:23,25	219:5
hindsight	219:16,24	220:10	107:23	identical
219:5	223:11,	230:7	161:15	185:2
Hiraishi	16,19	262:3,4	hourly	identificat
26:18,22	224:14,22	historicall	17:25	ion
146:12	226:2	y	hours	54:24
147:9,25	229:20,	42:10,11	15:23,24	115:24
153:6,10,	23,24,25	hit	16:1,13,	179:19
13,17,18	230:2,5,	67:19	18 17:10,	204:25
174:21,23	15,17	113:9	19 18:5	229:11
175:4,8,	231:11,	hits	95:7	239:21
25	16,20	52:13,19	house	246:6
176:15,24	232:12,19	54:15	12:5	identified
177:20	233:1,6,	hold	huge	24:16,17
178:10,13	14	65:9,12	170:12	25:20
180:9,12	234:14,	68:21	hundred	31:10
181:3,12	19,25	69:1	17:19	identify
182:25	235:7,10	123:24	hynix	25:15
184:21	260:11	127:7	30:6 31:5	32:18
185:7,19	261:12	154:12	hyphen	50:3
188:13,16	262:5	172:19	63:11	191:7
190:18	263:5,10	206:12	hypothetica	225:8
191:17	264:8	holds	l	265:21
192:6,11,	265:4,9,	22:10	83:6 84:5	266:8
18,21	13,19	home	lly	identifying
193:3,8,	266:1,6	11:24	hypothetica	31:19
13,17	Hiraishi's	12:15		266:10
194:8	147:21	18:12		
195:11,	176:6,9			
18,22	181:19			



800.211.DEPO (3376)
EsquireSolutions.com

Idle 252:22	imagine 217:19 219:2	implementin g 41:18	256:2 included 20:10 256:13	61:4 92:23 104:18 110:2 157:6 158:8 269:15
illuminatin g 54:5	immediately 17:15 18:6 65:7 77:15	important 72:1 77:12 78:12 89:6 152:10 154:8,16	includes 112:15 122:14,17 172:7 175:25 248:13,23 249:6 254:11,25	indirectly 201:15,17 216:21
illustrate 90:20 101:7 128:1,3	impact 48:6 68:10	impossible 129:4,6	including 14:14 36:13 56:24 75:22 121:12 140:25 222:17	individual 73:16
illustrated 59:7 80:2,19 92:4 93:11 95:5	impedance 68:7	in-line 54:12 56:10	industry 36:25 51:16	
illustrates 58:25 71:11,14 72:15 74:13 78:19 80:25 81:8	implement 37:23 39:10,15 42:9 161:9 228:20 270:15 272:5,12	inaccurate 22:22 185:14	INB 176:25 177:2,5, 7,14,19 186:17 190:7 260:14	information 11:14 18:9 21:12 44:4,5, 17,23 45:7,16 50:21 64:8 65:11 77:22 129:10 197:3,10, 23 198:5, 8,12,25 199:4 200:12,14 201:8,11, 19,20 202:5 217:20 232:23 249:23
illustratin g 91:7 94:22 101:16,17 102:4,7, 16 111:20 122:9 191:9 271:9,19	implementat ion 40:5 271:3	inbound 190:7	inconsistent 76:22	
illustratio n 71:19 246:21	implementat ions 252:1 254:8	inches 67:24 68:3,13 69:1	incorporate d 224:19	
image 80:8 175:23	implemented 39:12,20 117:24 118:1 146:18 244:13,18 266:18 267:12 269:10 270:13,21 271:24 272:9,10, 16,21	inclined 45:21 48:5 66:7,9 69:18 92:3 125:23	incorrect 25:22,24 69:21	
images 254:21	include 171:7,15, 19,23 173:2 222:22		increased 41:21 increasing 268:18 incredibly 68:20 independent 95:18 indicating 34:23	



800.211.DEPO (3376)
EsquireSolutions.com

initial 254:1	inserted 53:21	91:15 118:24	Internet 13:23	237:2
initializat ion 215:10	inserting 53:12	121:3,5 139:9 181:6	84:12	invention 50:25
initialized 137:13	inside 178:19	intending 72:18	interval 98:9,12	89:17 91:13,20
initially 71:24	197:2,22 198:11	intent 48:12	intimately 211:10	244:13,17 266:18 270:15,21
input 44:18	199:3,9 202:21	176:4	introduce 7:22 33:4	271:1,6, 8,12,17, 21,24
45:4,23, 25 103:15	203:20	198:19	54:20	272:5,9, 12,16,21
109:11,12	255:10	intention 22:12	134:1	273:8,11, 19 274:1, 8,12,25
110:6	insist 119:3	24:12	179:17	inventions 90:7,21
111:14	instance 33:12	48:15	188:21	91:2
112:2,6, 7,20	207:11,12	intents 176:5	189:7	94:15
113:22	instances 188:17	interact 36:15	204:21	101:8
114:13	instantaneo us 184:12	interchange able 193:1	219:13	118:11
115:7,21	instantiate 39:13	interchange ably 193:4,11	229:13	150:17
123:18	instinct 62:10	interest 38:1	introduced 72:2,3	236:22
124:19	instincts 62:15	interesting 199:22	134:5	inventor 31:17
172:12	integrated 38:9	interface 39:3	146:5,10	inventors 31:9,15, 20 102:15
177:4	244:14	73:15	211:22	introducing 211:3
178:1	266:19	258:1,5, 7,9	introduces 186:2	intuition 74:25
189:15	integrity 138:23	interfacing 51:7	187:20	investigati on 135:13
195:22	Intel 38:24	interfere 47:10	198:20,23	involved 18:22
196:5,7, 14 199:7	intend 22:7	internal 225:13	introduces 186:2	39:2
219:25	intended 39:4 63:3	263:19,22	198:20,23	211:10, 21,25
223:19			introduces 186:2	214:1
224:20			187:20	involving 30:24
225:9			198:20,23	IO 242:17
241:1,9			introduces 186:2	
260:14			187:20	
inputs 122:20			198:20,23	
155:18			introduces 186:2	
158:9			187:20	
224:12			198:20,23	
inputting 214:13,15			introduces 186:2	



800.211.DEPO (3376)
EsquireSolutions.com

IOBIST	ITC	161:3	19:16	110:18
250:8	19:15	162:13		203:11
IOS	30:3, 6, 12	163:9		254:21
254:19	55:5, 8,	166:23	K	257:21
	13, 20	168:20, 24		
IP		246:13	key	labeled
237:22		247:2, 12	51:8 92:3	71:13
	J	248:1		72:17
IPR			Khatri	74:15
12:24	January	JESD79-2	32:10, 19	78:20
13:4	20:7	87:5	33:7, 13	80:8
14:12	Jayesh	JESD79-3	Khatri's	81:2, 12
16:20, 21,	31:11, 14	87:23	32:12	92:15
24 17:8				102:20
21:21	JEDEC	JESD79-3A	Kim	103:6, 11,
IPR2022-	28:9, 13,	87:13	27:24	16 104:7
00711	17, 20	JESD79-3C	28:2, 6	106:17, 18
7:15	36:7, 18,	28:10, 13	kind	122:15
Irell	24 43:22	87:17	75:1	125:5
8:6 10:17	50:24	JESD82-20	123:1	136:2, 9,
14:25	51:3, 4, 8,	246:14	231:2	12 138:11
15:1, 4	11, 13, 17		237:2	142:22
20:1, 7,	52:9, 12,	John		144:11, 25
20, 24	15 56:17	7:18	kinds	169:1
25:8	60:7, 9	Joint	40:21	176:25
30:25	63:24	221:3	Kirkland	188:18
irrelevant	67:8	Jonathan	7:1 10:23	190:13
94:11	73:3, 19	8:6	12:1	195:23
	74:5, 22		knew	214:16
issue	75:3 79:5	judge	31:18	215:17
80:16	82:21	19:2, 9		216:1, 3
97:1	83:19	55:15	knowing	234:8
117:11	84:3, 16		190:9	238:14
119:7	85:2, 14,	July	201:4, 9	239:12
182:18	18, 24	29:5, 11,	knowledge	240:14
187:18, 19	86:5, 8,	18 51:1	49:12	243:17,
202:17	12, 24	73:4 75:4	85:4	19, 24
219:15	87:12, 16	79:5		247:7
223:6	134:23	146:6	knowledgeab	248:21
	135:6, 17	jump	le	249:3, 11
issued	138:17	107:21	36:11	250:7
141:6, 17	139:5	264:14		252:21
	154:19		L	253:5
issues	157:16	June		254:12, 20
28:15	158:2, 16,	83:1 84:4		258:4
93:24	20 159:22	87:4	label	259:11
132:23	160:13	juries	107:8	
202:15				



800.211.DEPO (3376)
EsquireSolutions.com

labels	91:12,16	left	246:21	190:2,9
212:3	156:9	12:17	252:3	197:1,10,
249:14		65:2		22 198:10
257:2,13	LCKLR	80:3,17,	leveled	199:2,8
	224:2,12,	18 81:11	134:8	200:20,21
language	23 226:18	109:1	181:18,22	201:4,22
54:5	227:7	116:18,20	206:2,6	202:1,20,
273:23		122:2	leveling	21
274:8	LCLKR	125:2	131:20,	203:19,20
	223:21,23	127:17	22,25	204:17
largely	226:12,25	169:2,5,	132:2,4,	205:13,
37:22	228:4,13,	11,13,14	21,23	18,19,22,
51:15	17,23	201:25	133:11,	24 206:4,
54:4	229:6	205:6	12,16,22	9,16,18
71:23	263:23	223:15	134:4,8,	207:18
202:14		224:17	11 136:3,	208:24,25
larger	LCLKW	226:15	9,12	209:19,24
42:12,21	227:19,23	228:9	137:22	210:9,10,
		229:22	138:4,7,	15 211:7,
latch		230:1	12,19,21	12,14,19
124:12	lead	238:13	139:9,15,	212:8,14,
	40:11	240:5	20,22,23	18 213:2,
latches		241:25	146:2,7,	4,13,15,
66:12	leading	243:14	9,13,17,	16,18
124:10	260:22	248:13,17	18,21	214:2,3,7
	261:7,16	253:1	150:4	215:16,21
latest	262:1,16		171:3,7,	216:7,16,
151:18	263:15,25	legal	15,19	17,23,24
169:16	264:7,23	23:23,24	172:6,11	217:13
170:1	265:17		173:1	218:1,2,
	266:4	let alone	178:10,	20,22
law	267:4,21	60:7	13,14,18,	220:5
15:1,3	269:13	letter	25 179:7	222:23,24
30:24		47:1,3	180:1,9,	230:6,10,
	learn		13,17,21	13 232:20
layout	51:10	level	181:1,12,	233:2
202:10,		33:20	19 182:6,	237:7,12,
14,18	leave	38:16,20	9,13,18,	17 260:11
	61:13	39:7	21,23,25	262:3
layperson	148:22	40:10	183:7,11,	
38:17	271:14	41:9	18,21,25	levels
39:7		44:1,16	184:7,20	202:1
43:24	leaves	45:21	185:18	Levin
44:8	215:25	73:19	186:12,24	30:25
45:20		76:17	187:8	
48:2	leaving	81:5	188:21	limit
71:18	163:19	203:4	189:6,22	117:1
73:8 75:7	166:21	209:7		
77:19	226:15			
79:9 81:5				
90:25	Lee			
	31:10,14			



800.211.DEPO (3376)
EsquireSolutions.com

168:9	110:8	198:3	273:12,21	living
limitation	113:14	199:13	274:4,15	10:8
222:21	114:3,12,	202:12,25	275:10	load
limitations	23 115:16	203:24	lines	68:4,6,8,
121:11	116:15,22	206:11	60:22	9 77:10,
173:24	117:20	208:1	62:20	17,25
limited	118:7,9,	212:11	76:25	78:3
59:19	20 119:8,	217:15	77:8 78:7	175:18
148:2,14	19 120:10	218:4	79:15	176:1
Lindsay	121:14	219:19	90:1,5	local
8:5,6,19	124:7,16	220:17	92:14,16	223:24
15:15	125:7	221:24	94:5,7	225:18,
21:15	126:5,17	222:6,25	125:12	20,22,23
33:2	127:5,13,	224:5	126:11	263:19
40:14	23 128:7,	225:3	196:19,22	locally
41:4,13	16,24	236:12	197:4,24,	34:2
42:24	129:7,14,	237:8,13,	25	located
43:2	22 130:6	20,25	199:11,12	11:22
49:5,6	132:15	247:20	202:22,23	location
50:18	133:1,24	248:8,15,	203:22,23	140:12
53:5 54:1	134:25	25 249:9,	243:24	locations
59:21	135:9,22	19 250:4,	list	81:10
60:3	136:5,15,	18 251:2,	19:23	locked
61:2,11	25 137:8,	16,23	20:2	227:4
62:2,13,	16,24	252:5,19	22:10	logic
25 64:6	138:9	253:3,13,	listed	38:12
65:20	139:12	22 254:5,	30:1	39:9,10,
66:19	140:4,13	14 255:4,	listing	11,20
71:21	141:2,11,	11 256:5,	258:16	45:14
73:9	19 142:5,	16,25	literal	47:20
75:8,23	18 143:2,	257:8,18	41:16	241:21
76:12,18	11,13,25	258:2,13,	192:16	logically
77:1,20	144:5,22	22 259:7,	litigation	37:22
78:9	145:8,14,	19 260:2	16:25	53:10
80:14	22 146:15	261:3,11,	17:3	91:22
82:23	149:22	18 262:7,	live	138:13
83:10	151:2,6,	11,19,25	10:22,23	220:6
85:6 89:2	20,25	263:17	long	15:20
91:3 93:5	152:11,25	264:3,8	16:5,10	46:6 52:2
94:16	154:2,10	265:3,23	107:22	
96:5,23	155:14	266:3,11,		
98:4 99:9	156:11	24 267:8,		
103:3	158:24	17,22,24		
108:5	171:10	268:9,21		
109:18,20	185:23	269:7,12,		
	193:6	16		
	194:20	272:13,24		



800.211.DEPO (3376)
EsquireSolutions.com

145:25	258:19	64:21	management	16:16
155:5	259:1,3	73:12	253:21	22:2,5,
161:2,10	low	84:9	Manella	15,23
170:11	39:25	149:15	8:6 10:17	25:5
257:15	47:22,24	179:14	15:1,4	26:5,8,
258:25	64:16	219:17	20:1,7	11,15,19,
260:25	156:25	242:5	25:8	22 27:1,
268:2	157:17,	main	Mangione-	4,8,14,
longer	18,21	72:19	smith	17,20,25
107:24,25	158:3,10,	maintain	7:10 8:7	28:7,10,
159:2	14,15,17,	45:8	10:1,7,9	13,21
160:15	21,22	maintains	12:11	29:1 30:5
longish	159:2,5,	45:13	21:18	31:4
125:16	7,8	major	26:4 33:9	32:4,23
looked	160:16	191:15	49:21	33:11,16
69:12	207:12	192:1	55:2	35:8,11,
94:23	234:20	make	88:12	12 50:1
126:9	241:20	45:2,12,	108:14	54:23
135:12	low-level	24 53:4	162:12	55:11,14,
147:19,24	37:16	88:2	220:23	25 59:11
161:4	lower	94:20	235:15	63:9 65:2
163:1	41:20	108:16	245:25	70:18
170:12	42:22	151:13	259:12	82:21
194:13	LRDIMM	165:8,12	260:3,18	84:3,17
219:17	78:19,22	167:16	261:8	85:3,24
273:2	79:1,6,9,	173:25	266:25	88:14
loop	19,20	196:11	270:6	89:21
227:4	81:1,6,	200:15	275:6,19	90:11
losing	16,20	217:24	manufacturi	92:16
268:2	LRDIMMS	219:1	ng	94:4
lost	81:8	222:15	42:2	97:10,14
107:15	lunch	226:20	53:16	100:4
168:18	108:4,17	234:5	March	101:2
232:9		246:2	246:14	115:23
266:24		259:14	marginal	116:7
	M	275:13	42:22	124:23
lot		makes	mark	125:11
68:7,18	M-E-M-B-I-	29:20	54:21	131:5
84:21,22	S-T	38:24	115:22	134:16
86:6	250:10	40:21	239:24	138:6,17
91:16	made	44:23	244:8	139:19
92:6	14:11,21,	254:7	246:8	140:1,22
140:15	23 27:12	malfunction	marked	142:10,14
150:13	40:16,19	124:12	10:18,24	147:2,12
164:25				154:20



800.211.DEPO (3376)
EsquireSolutions.com

168:21,25	materials	MCS1	182:14	57:21
169:7	28:23	122:21,24	252:8	58:2,20
174:21	math	123:1,4,	media	59:2,3,4,
175:3,8	164:6,12	11,13,19	7:8	18 60:1
176:15,18	165:17	MDC	275:19	61:9,15,
178:5,9	mathematica	122:15	meeting	25 62:1,
179:18	l	MDC910	51:17	12 63:2,3
190:18	164:19	122:17	meetings	65:19
195:7,12	matter	meaning	15:14,20	67:13,15
204:13,24	7:10	11:20	members	68:3
223:9	10:15	22:6,16	132:7	69:7,9,
229:10	12:20	29:16	MEMBIST	15,17
238:7,16	14:9 15:5	43:15	250:2,8,	70:10,11,
239:20	16:9,19	52:25	10,14,22,	20 71:16,
240:4	17:23	53:2	23,25	24 72:22
241:4	21:20,21	62:21	251:12,	73:3,14
242:9	22:8	77:14	13,20	74:8,17
244:12	24:23	236:17	252:4,9,	75:3,18,
245:8,13	29:21	250:12	13,16	19,21
246:5,19	30:2,22,	means	memorialize	76:3,10,
247:13	23 31:5	21:21	181:6	25 77:8,
270:7,20	32:10	45:15	memories	10,14,18,
market	38:1,21	47:6	36:12	21 78:1,
62:8,16	50:3,11	53:20	37:9	7,19,22
79:4	61:17,22	60:19,21	211:1	79:6,10,
marketing	84:2 85:2	79:24	memorized	22 80:10,
40:18	223:5	125:24	99:22	25 81:1,
marketplace	matters	139:22	100:11	6,16
61:18	17:11	146:17	146:23	82:21
74:21	18:22	195:1,2	273:3	83:19,23,
marking	30:16	meant	memory	25 84:17
268:19	maximal	98:22	34:15	85:3,24
marks	121:17,20	122:3	35:22	86:13
7:8	maximum	170:23	36:16,18	87:5,13,
match	163:22	241:8	37:3,10	17,24
52:9	164:4	255:22,	39:3 51:7	91:8
matches	166:13	23,24	52:18,22,	119:11
34:19	268:16,20	measure	23 53:1,	130:12,19
234:3	MCS	156:13	7,18,20,	135:7
material	125:5,8,	measures	25 54:12,	138:24
94:11	14 126:2,	232:21	14,17	143:9,20,
148:21	13 127:3	mechanism	55:6	22 147:21
259:1	128:22	64:7	56:10,15	148:25
	129:21			149:8,21
				151:16,
				17,18,22
				153:5,10,



800.211.DEPO (3376)
EsquireSolutions.com

19 154:6	17,23	126:25	88:6	mistake
162:19	234:17	127:2	161:15	23:9,14
163:10,19	235:4,9,	method	162:4	24:15
164:1	12,16,17,	273:15	257:7	25:10,17
166:22	20,23	methods	259:20	87:22
167:7,12	236:2,6,	132:10,12	misaligned	mistakes
174:16,19	11,20,24	274:2	121:7,8	22:17
175:9,18	237:3	middle	125:15,	misundersta
176:7,10	241:24	60:12,16	21,23	nd
178:19,25	242:1,15	160:11	126:3	145:3
179:8,11	243:23	181:25	152:22	mode
180:6,10,	246:15	239:1	mishear	134:23
13,19	247:7,12,	250:1	22:24	135:4,6,
182:7,9,	17 250:2	255:1	misheard	7,20
10,11,20	252:11,25	midline	148:9	136:1,13,
187:1,11,	253:12	201:22	187:6	22,23
18,22	254:2,3	min	228:7	137:5,6,
188:23	255:9	160:6,7	misidentifi	13,21
189:8,14,	256:12,	161:8	es	138:2
18 196:1	14,22	mind	23:4	140:10,
197:24	257:16	88:24	misoperatio	23,24
198:1	258:20	117:12	n	141:5,16
200:6,10,	263:7	165:13	124:12,15	142:2
11,24	264:15	172:5	mispronounc	144:17
202:11	mention	219:15	ed	modes
209:3,5,	247:24	266:12	228:6	271:3
16,20,22	mentioned	268:3	missed	modified
210:2,3,	42:20	mine	213:22	225:19
10,16,18,	154:12	33:1	missing	modify
24 211:3,	241:10	minimal	50:12	147:20,24
6,8,9,14,	mentioning	269:3	misstatemen	module
23 212:2,	224:15	minimum	t	34:15
9,20	met	160:5	55:24	35:23
214:12,	201:1	161:25	misstatemen	52:19,22
21,24	metastabili	163:11	ts	53:1,18,
215:4,10,	ty	269:1,5	56:4	20,25
12,17,21,	122:14	Mintz	Misstates	54:12,15
25 216:8,	124:4,5,	30:25	78:9 93:6	56:10
24	9,18	minute	149:22	60:1
217:11,25	126:3,16	269:21	171:10	61:15
218:21	127:4,8	minutes	185:23	62:1,12
221:20	129:13,18		224:5	68:4 74:7
230:11	152:19			76:25
231:7,22,	metastable			77:8
24 232:3,				
5,14,22				
233:11,				



800.211.DEPO (3376)
EsquireSolutions.com

78:19	72:22	39:2	52:3 70:4	
79:10,19	73:4		77:14,15	N
80:25	74:17	move	81:10	
81:1,6,	75:4	43:5	87:3	named
11,16	78:23	80:16	160:23	31:9,14
91:9	79:6	94:19	175:23	names
109:23	83:23,25	moved	176:9	31:18
123:4	134:2	58:20	228:22	
125:1,4,5	147:22	129:3	248:11	nanosecond
126:1,13	148:25		253:19	67:17
127:3,11,	149:8,21	moves		68:3,14,
21	151:16,	273:16	multiples	20,23
128:14,22	17,19	MPR	229:9	
129:21	153:6,10	140:3,8,	234:1	nanoseconds
130:12,19	235:17	12,25	multiplexer	70:21
138:24	236:6	141:5,10,	103:17	71:1,5
153:19	237:3	15 142:3,	104:15,21	163:11
154:7		8,16,22,	112:3,4,	narrow
167:12	moment	24 144:3,	10 122:24	95:18
174:17,19	45:9 85:9	9,11,16,	240:25	
175:9,19	100:23	25 145:6,	241:9,15,	Navy
176:7,10	104:12	12	16,18	68:18
179:11	107:10			nearest
189:14	108:23	MR1	multiplexer	133:14
196:1,6,	124:2	138:2	s	
15 197:13	164:8		254:11,17	necessarily
200:4,8,	166:21	MR3	257:11	43:20
11,19,22	168:19	140:24		83:12
201:10	174:12	141:6,17	multiplexes	85:12
202:4,7,	181:9	142:7	112:6	86:10
11 215:10	183:6		multiplexor	234:1
235:16	200:17	MSC1	103:15	245:1
236:11,25	206:10	122:23	122:25	
247:18	215:11	Multi	123:3	needed
252:25	242:23	142:21		28:23
253:12	268:1	145:5	multipurpos	39:12
254:2	274:18		e	93:25
		multi-	142:25	132:4
		purpose	144:3	214:7
modules	momentary	140:2,7	145:1	
37:4	179:13	141:9,16		Netlist
52:24	morning	142:3,16	Murray	7:12 8:7
54:17	7:5,25	143:5,7	68:16	10:14
55:6		144:18		14:8
59:18	motherboard		mux	17:1,10,
61:9 63:2	53:11,22	multi-rank	103:16	22 18:2
70:4	58:23	58:16	254:12	21:19,23,
71:16	Motorola	multiple		24 23:6
		18:22		



800.211.DEPO (3376)
EsquireSolutions.com

29:22,25	nonrecov-	101:22	114:3,12,	202:12,25
30:6,17,	42:3	102:12,13	23 115:16	203:24
21 31:5,	nonrecurrin	221:10,	116:15,22	206:11
8,23	g	11,13	117:20	208:1
48:21	42:3		118:7,20	212:11
50:16			119:8	217:15
52:20,24	normal	o	120:10	218:4
54:16,19	21:17		121:14	221:24
221:14	173:1	oath	124:7,16	222:6,25
235:16,	203:5	8:15 10:2	125:7	224:5
20,23	213:3	object	126:5,17	225:3
236:2,5,	233:3	49:6	127:5,13,	236:12
10,23	notes	objection	23 128:7,	237:8,13,
237:6,11,	13:5,6	8:14,18,	16,24	20 247:20
18	85:13	19 21:15	129:7,14,	248:8,15,
Netlist's	noticing	40:14	22 130:6	25 249:9,
10:15	8:16	41:4,13	132:15	19 250:4,
25:16		42:24	133:1,24	18 251:2,
26:5	notion	43:2	134:25	16,23
55:4,25	86:4	50:18	135:9,22	252:5,19
246:19	199:16	53:5 54:1	136:5,15,	253:3,13,
Netlist/ samsung	November	59:21	25 137:8,	22 254:5,
19:7	87:21,24	60:3	16,24	14 255:4,
	138:18	61:2,11	138:9	11 256:5,
newer	NRES	62:2,13,	139:12	16,25
148:12	42:2,5	25 64:6	140:4,13	257:8,18
nibble	number	65:20	141:2,11,	258:2,13,
241:12,19	7:14	66:19	19 142:5,	22 259:7
nonfunction al	15:12	71:21	18 143:2,	260:16,
191:13,14	18:10	73:9	11,25	19,21,22
	24:17,18	75:8,23	144:5,22	261:7,15,
nonobviousn ess	25:14,20,	76:12,18	145:8,14,	25 262:1,
85:1	23 55:8	77:1,20	22 146:15	10,13,15,
148:23	103:5	78:9	149:22	16
149:6	114:5	80:14	151:2,6,	263:14,
150:3	247:6	82:23	20,25	15,24,25
153:8	251:5,7	83:10	152:11,25	264:6,22,
171:6	252:1	85:6 89:2	154:2,10	23 265:17
185:8	253:16	91:3 93:5	155:14	266:3,4
189:4	254:11	94:16	156:11	267:3,4,
200:2	255:11	96:5,23	158:24	9,20,21
203:8	256:10,21	98:4 99:9	171:10	268:4,12,
219:8	258:16	103:3	185:23	23
	275:19	109:18,20	193:6	269:12,13
	numbered	110:8	194:20	272:13,24
	88:17,19	113:14	198:3	273:12,21
			199:13	274:4,15



800.211.DEPO (3376)
EsquireSolutions.com

objects	253:17	12 233:2,	199:2,8	opposed
248:11		4,12	206:16	41:2
262:20	older	261:13	214:14	64:13
	148:10	262:3,5	216:6,22	95:24
obvious	one-clock-	263:11,18	217:2,7,	135:17
218:19,24	cycle	266:2	9,14,23	214:1
219:4	98:12	operations	218:22	231:6
occur	99:7	203:5	220:8	optimin
100:13	one-quarter	212:15	222:9,20	245:14
157:7	165:3	213:14	223:3,6	optimized
occurred	232:4	214:8	224:10	143:9,23
203:15	open	221:18,20	228:2,12	optimum
occurs	82:18	222:18,	251:18	245:14
50:14	87:3,8	22,23	260:24	273:9,20
124:10	116:3	265:10	262:8,12	options
246:4	134:18	opinion	264:2	31:24
offering	221:1	22:12	265:3	orange
222:16	opened	32:15	274:23	116:9,10
274:23	35:6	38:14	275:2	order
275:2	operate	52:23	opinions	37:2
office	121:18,	56:19	10:15	47:23
7:13	19,21	69:10	19:4	77:10
12:15	166:12	71:15	22:7,9,11	123:18
18:12	operated	72:21	27:22	133:3
49:8	70:10	74:16	32:13	199:6
officer	operating	78:21	33:12	275:15,16
8:14	70:23	82:19	84:2 85:1	orders
offset	121:11	85:12	148:1,23	275:13
245:14	operation	92:25	149:1,7,	ordinary
273:10,20	34:16	101:9	25 150:3,	29:5,10,
oftentimes	35:23	117:18	7,8,9	16,17
39:17	36:12	120:5	153:9	33:20,21
40:15	37:8	147:18	171:6	34:5,11
42:15	62:22,23	151:5,24	185:9	35:9,14,
46:24	91:7,8	152:7	189:5	19 36:4,
55:17	137:15	153:4	196:25	6,10
58:19	183:20,21	171:14,18	197:20	37:6,14
63:24	205:13	183:5,10	200:2	38:2
77:9	206:18	184:20	203:8,18	40:12,20,
83:20	213:3,19	185:18,22	213:23	22 43:10,
120:23	214:1	186:11,24	214:5	17 53:24
old-	215:4,8	187:8	219:8,11	71:15
technology	216:17	188:20	222:16	72:21,23
	230:6,10,	189:13	opportunity	
		197:15	33:10	
		198:10	41:21	



800.211.DEPO (3376)
EsquireSolutions.com

74:16	12, 15, 19	package	219:24	14:11
78:21	122:24, 25	104:19	225:10	16:22
82:20	123:3	packaged	230:14	20:1
83:6, 16,	177:5, 17	20:20, 21	232:19	21:24
24 84:6,	178:1	pages	244:7, 11,	24:23
14, 15, 22	182:8	19:22	20 245:6,	41:14
85:4, 16,	189:17	51:24	10 260:7,	100:2
23 86:7	207:19, 22	52:2, 6	10 261:5,	105:21
91:19	208:9, 10	97:13	12, 19, 20	132:8, 19
94:14	213:6	100:4, 11,	263:1	178:21, 22
120:4	224:17,	21 170:18	264:13, 16	190:9
147:18	24, 25	257:15	266:16, 21	199:7, 20
218:13	225:24	258:24	267:6	204:19
224:9	226:7, 9,	Paper	269:7, 8	210:9
244:24	11 235:11	35:8, 12	270:8, 11,	218:22
265:25	243:14	paragraph	19, 23	233:12
	263:20	23:17	271:5, 23	236:14
organiza-	outputs	32:5	274:2	266:17
n	46:5, 14	33:15, 18	275:4	268:14
51:3 86:8	122:22	34:7, 21	paragraphs	271:6, 11
191:13	123:22, 25	35:13	193:10	273:10, 18
orient	188:5	36:2	205:8	partic-
264:14	241:18	70:8, 9	212:25	236:21
oriented	outputting	131:13	229:21	parties
196:12	214:13, 15	147:1, 6,	230:1	19:10
origin	owned	7, 11	parallel	221:17
150:18	149:11	148:6	130:12, 18	parts
OUTB	owner	167:2	131:1	19:3 42:6
176:25	8:7 23:25	169:6	parameters	101:17
177:2, 5,	24:16	170:21,	118:1	120:23
8, 14, 19	Owner's	22, 23, 24	paraphrases	170:13
outcome	25:15	171:1	154:4	183:18
32:2	owns	175:4, 6,	paraphrasin	party
output	23:5	12, 16	g	42:6
44:19, 22	25:21	176:3	140:15	pass
45:5, 23,		178:8	pardon	80:3
25 46:2,		179:1	119:14	112:21
24 47:9,	P	180:25	133:19	178:1
13, 14, 17		190:17,	147:4	200:13
103:14, 23	p.10.	23, 25	parenthetic	225:1
104:1	221:14	192:18, 23	ally	242:25
110:10	p.m.	204:16	140:8	259:18
111:1	275:23	207:17	part	passage
112:1		213:7		125:16
115:11,		216:15		



800.211.DEPO (3376)
EsquireSolutions.com

passages	94:9,15	130:9,14,	peak	267:11
194:13	95:12	21 131:1	70:3,15	performs
passed	96:2,9,	185:11	penalty	182:23
110:10	16,22	186:17	8:24	period
112:12	97:15,21	190:4,7	pending	44:3
268:19	99:17	204:2,3,6	119:20	70:20
269:4	101:2,7,	paths	penetration	96:7,10,
passes	8,14,20	193:25	62:8	14,17,19,
103:10	102:3,19,	195:16	people	20,22
184:23	23 104:13	217:3	14:5	99:13
passing	107:9	pattern	24:25	156:3
188:8	108:21	132:20	31:19	158:17
past	109:10	145:13,21	40:19	159:21
16:10	110:24	252:17,22	42:19	164:7
17:9 18:1	111:5,8	patterns	44:12,13	183:19
25:2	112:24	144:20	83:23	209:8
50:17	113:7	pause	84:21	228:13
52:15,22	116:7	111:12	86:6	229:8
patent	118:5,10,	pay	percent	periodic
7:13,15	15 120:5,	31:17	153:14	155:1,3
8:7	11,16	payment	perfectly	224:3,8,9
10:16,18,	121:13,24	84:10	117:15	periods
19 14:14	122:8,11	Pazmandi	125:18	96:11
17:2	123:7	8:4	127:22	208:21
23:4,5,7,	124:23	PC	128:2,5,	perjury
25 24:17,	125:11,13	53:11	10,11,14	8:24
18,22	128:12	PDF	perform	permit
25:15,16,	146:6,20	11:2,5,13	165:11	78:7
17,20,21	221:19	12:17	262:5	176:1
26:5,8,	235:18	13:4,6	265:14	206:9
11,15	236:7	19:19,22	performance	225:1
29:6	246:25	20:22	41:22	permitted
31:10,15	247:2	22:1 30:4	167:17	163:25
40:23	patents	51:22,24	202:16	166:13,20
50:25	17:5	88:17	performed	170:5
58:5	24:24	221:10	91:8	174:11
88:22	25:1,13,	PDFS	178:13,18	person
89:5,7,	15 89:5	12:23	179:7	29:5,10,
15,22	236:16	13:2	180:22	17 33:21
90:5,7,	path	PDQS_OUT_UN	181:2	34:5,11
10,17,20,	102:24	243:18	206:19	35:9,14,
22 91:1,	103:5		211:12,14	19 36:4,
21 92:1	104:14		230:13	6,10
93:18	105:13			
	108:24			
	111:9			



800.211.DEPO (3376)
EsquireSolutions.com

37:6,14	33:19	244:5	230:6	207:7,8
38:2	34:20	PI_R_NDQ	233:3	271:12
40:11,20, 21,22	Petitioners	244:6	274:20	points
43:10,17	27:11	pick	places	100:12
53:24	Ph.d.	109:2	243:1,10	119:2
54:5	86:21	picking	plan	134:3
71:15	phase	95:25	190:12	167:18
72:21,23, 25 74:16, 22 78:21	207:24	picosecond	plans	portfolio
82:19	220:2,14	169:1	25:3	246:19
83:6,16, 24 84:6, 8,13,15, 22 85:4, 16,22	228:20	170:15	PLL	portions
86:7	229:6	picoseconds	248:18	19:7
91:18	phone	71:5	plurality	158:5
94:13	13:24	163:13, 20,23,25	206:24	POSAS
120:4	15:9,10, 13 107:13	164:7,8	point	86:7
147:18	phrase	165:6,7, 16 166:3, 5,14,15	24:9 44:6 53:4,13, 16 70:1	position
218:13	53:25	167:4	72:5	274:19,24
244:24	54:17	picture	91:21	possibly
265:25	120:13	56:9	92:3	31:12
266:6	125:20	piece	100:25	144:11
personally	128:5,11, 19 147:16	44:2,4,17 64:8	118:23	188:24
13:21	phrasing	68:22	119:9	217:20
36:3	252:12	150:19	124:19	potential
perspective	physical	156:2	129:25	254:3
29:9	11:20	170:19	131:2,3	power
193:23	38:21	pin	135:3,15	41:19
194:23	59:12,15	104:16,17	146:4	59:17
226:17	60:22	111:1,3, 15,25	154:25	137:14
227:6,21	63:6	115:14	159:1	power-on
petition	64:12	189:12	162:20	254:1
34:24,25	133:7	pins	184:9	power-up
35:1,8,11	191:12	104:19	190:14	137:20
Petitioner	202:10, 14,18	PL_R_PDQ	219:20	practical
8:2 23:8	11:22	244:5	227:11	40:7
263:11	physically	place	228:14	Pre-defined
Petitioner's	physics	81:10	246:24	142:25
23:23	184:10	205:14	269:3	preamble
	PI	215:9	275:14	159:23
			pointed	160:1,4, 6,14
			144:8	233:16, 20,21
			pointing	
			169:19	



800.211.DEPO (3376)
EsquireSolutions.com

234:1,4, 16,20	present 25:3	principal 114:5	proceeded 114:14	202:1,3 267:13
Preambles 159:25	55:22 189:14	principle 128:2 182:11	proceeding 34:11 35:18	prone 46:16
precise 38:14 70:14 86:5	204:8,9, 10 267:14	printed 12:19	process 14:12 17:8 20:1 41:25 42:8 173:2 271:10,19	pronounce 177:2 223:23,25
precisely 173:9 235:1,13	271:1,6, 12,17,21, 24 273:8 274:1,8	prior 24:23 26:19,22 27:1,4 50:22 78:9 80:8,11 93:6 97:4 146:12, 19,22 171:10 185:23 224:5 246:25		propagate 181:24
precision 173:24	presentation 247:25		produce 20:21	propagation 65:25 68:10 80:6,15 130:9,14, 21 133:8 182:1
predefined 144:19 145:6,13, 21	55:15 200:13	presumed 185:1	produced 42:6 103:25	proper 24:12 96:21 137:15 221:17
predetermined 95:16,20, 23,25	pretty 23:19 146:18 147:23	problem 41:23 47:11 124:9 134:5 153:24 159:17 172:24 177:12 182:17	produces 44:22	properly 154:8 224:13
preface 88:23	prevent 133:22		producing 21:16 42:22	
preferred 213:12 271:8,16, 20	previous 19:1 30:23 221:18,19 222:18,22	problematic 91:6	product 39:5	properties 48:14 130:9,14, 20
preparation 16:9,14 93:18,21, 22 97:18 274:9	previously 29:22 41:8 61:8 77:13 79:16 93:21 156:20 211:11 222:11 224:3 234:4	problems 46:8 134:5 152:18,23	products 37:2 43:4 61:18 149:12 151:12	property 156:5,6
prepare 15:7,21 16:6,11 18:6		procedure 21:17	profession 10:10	protect 249:23
prepared 16:2 95:2		proceed 8:11 108:18,19	professional 67:20	provide 10:12,14 11:13 14:12 22:6 40:3 41:15 50:21 131:20,24 147:21
preparing 17:15 95:7	primary 77:7		programmable 38:11	
			programmed 136:23 137:6 201:23	



800.211.DEPO (3376)
EsquireSolutions.com

provided	39:13	230:22,25	21 156:4	102:25
20:11	53:10	234:11	170:8	104:13,
31:1	67:22	256:19	176:2	15,16
111:15	78:1 82:8	267:23		105:9,11,
132:3	107:25		rational	21 110:17
136:22	115:1	questions	218:25	111:10
137:5	149:2	11:21	RDIMM	113:19,23
138:18	177:24	22:14	72:16,19,	120:11
	181:7	29:9,14	22 73:3,	122:15,18
providing	190:13	49:11	8,18,19	123:7,23
55:5	220:24	88:23,25	74:2,5	131:20,
	229:14	111:13		21,24
PTAB		143:17	RDIMMS	132:3,22
13:16	puts	260:4	73:1	134:11
	13:10	269:17	132:13,17	137:18
publicly		275:6		138:12
84:11	putting		RDQS	139:23
	236:19,24	quick	104:2	141:7,18
published	237:2	18:15	110:13,16	143:8,9,
148:3		48:17	113:24	22 144:19
		245:18	114:9,20,	145:6
pull			25 115:4,	146:2,7,
34:2	Q	quickly	6 116:12	9,13,16,
164:16		48:20,23	117:7,8	17,21
	qualified		RDRAMs	150:4
pulse	18:23	quote	202:3	154:7,15
160:5		147:20		156:16
	quarter		re-	160:5,6
purple	165:17,21		initialized	169:9
254:18		R	137:14	171:3,7,
	question		re-times	15,19
purpose	12:14	raise	263:19	172:6,11
38:23,25	13:1	8:21		173:1
64:1	22:24,25	range	re-timing	178:14,24
142:21	29:20	161:22	263:18	180:9,12,
145:5	68:1 71:4			20,21
218:7	79:13	rank	read	181:1,12,
267:13	89:11	58:12,15,	16:15	17,19
269:10	118:13,14	17 59:1,4	26:5,18,	182:6,9,
270:13,16	119:19,21	77:13	25 27:7,	13,18,21,
272:6,22	140:19,21		16,24	23,25
274:13	148:8,13	ranks	28:9	183:7,11,
275:1	151:24	58:25	56:17	18,21,24
	161:18	175:23,24	58:13	184:7,20
purposes	164:6		62:23	185:18
34:10	180:3	rate	63:4,5	186:11,24
35:18	182:11	17:25	67:16	187:8
84:1	187:6	54:13	74:7	
171:2	196:8,11	70:24	91:7,22	
253:16	206:7	155:5,8,		
put				



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 327
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 327

188:21, 25	168:3	56:2, 3, 20	263:4	231:12
189:6, 22	169:11	57:7 58:7	266:9, 15,	232:3, 5
190:2, 9	190:4	67:21	20 271:14	263:6
197:1, 9,	210:13, 21	69:5, 14		264:10
22 198:10	212:22, 24	73:5, 6	recalled	
199:2, 8	257:13, 20	75:17	31:20	receiving
200:20, 21	266:6	79:7	receive	65:23
201:3, 22		81:24	133:5	114:18
202:1, 20	Readout	86:21	197:2, 23	134:3
203:4	145:12	90:24	199:4, 10,	196:18, 22
204:2	reads	92:7	11, 18	199:15, 24
205:24	143:1, 8,	93:9, 15	200:5	216:20
210:4	21	96:25	201:14,	recent
211:18	ready	97:5	16, 17, 18,	19:7
212:17	108:17, 19	99:22	19	recently
213:14, 16		100:17,	202:21, 23	136:19
216:14, 18	real	20, 23	203:3, 21	160:18
221:14	159:17	101:18	216:7, 12,	
222:2, 23	reason	103:8, 11	23 217:4	reception
223:24	41:1, 3	112:19	228:3	98:9
225:15	67:21	115:19	231:21, 23	recess
228:10	69:20	117:9	232:13, 16	49:18
230:6, 10,	127:1	118:21, 23	235:8	88:9
12, 13, 18	164:23	120:16	received	108:10
231:12	218:16	123:5	78:4	162:9
232:20	229:3	126:8	103:9	220:20
233:2, 4,	reasonable	131:22	133:9, 10	238:3
12 235:2	166:7, 9,	132:3	203:14	245:22
237:12, 16	17 232:7	135:2, 4,	235:2	259:23
242:9		11 146:23		270:1
243:13	reasons	148:18	receiver	recited
249:12	22:9	160:1	64:17	275:4
257:3	41:7, 10	162:19	66:8, 11	
260:11	132:6	168:8, 14	113:4, 13,	recollectio
261:23	Rebecca	176:11	16, 19, 21	n
262:4	7:20	177:10	122:13	28:1
263:20		192:25	158:8	30:24
266:22	recall	212:17	205:25	56:21
267:5, 16	14:23	217:6	receives	68:12
read/write	25:13	219:13	113:22	69:12
213:12	26:10	222:10	195:22	70:6
	31:12	233:25	199:16	76:16
reading	32:17	241:7	201:10, 20	97:20
92:1	47:5	246:22	215:3	173:4
120:4	51:12	247:25	216:11	216:13
125:16	55:9, 10,	250:21	230:18	223:7
160:1	23, 24	252:13		225:7



800.211.DEPO (3376)
EsquireSolutions.com

233:25	redirection	240:4,6	68:9	3,16,21,
238:18	108:25	244:8,11	113:17	25 143:5,
242:11	reduce	245:12	146:13,21	7 144:3,
248:3	77:10	266:12	150:14	7,9,12,
264:11	175:18	270:7,11	159:22	15,17,18
reconstruct	176:1	referenced	160:4	145:5
ed	reducing	113:11	241:11	178:15,16
106:4	77:17	referred	reflect	180:10,
record	redundancy	37:21	46:4	14,22
7:6 8:13	249:22	40:8 42:2	reflects	181:2
10:6	refer	46:24	45:3,25	182:22
21:12	36:19	60:6,12,	refresh	183:1,11,
49:15,17,	38:12	17 61:1	70:6	25 184:2,
20 88:8,	41:15	113:15	93:23	24 185:19
11 108:6,	46:17	119:13,15	97:20	187:9
9,12	58:19	167:18	119:11	188:4,11,
161:15,16	63:19	174:9	151:22	13 189:5,
162:4,8,	65:14	referring	162:19	15,24
11	78:25	15:18	refreshing	190:1
220:19,22	81:25	24:16	215:12	195:18,21
238:2,5	114:24	25:10	regenerated	205:14
245:21,24	120:1	30:6 31:3	106:4	207:18
259:22,25	131:15	36:23	region	209:13
262:23	146:16	41:3,5	129:18	210:17,19
266:23	164:25	45:18	register	211:7,12
267:2	170:14	46:10	43:23	212:1,10
269:19,24	175:4	47:25	44:2,14,	213:5
270:3	reference	64:3	16 73:13,	214:22
275:12,21	25:21	81:12	15,18,20,	215:22
record's	26:19,22	83:5 99:2	23 74:2,	216:2,18
260:4	27:1,4,8,	105:18	3,5,6	218:2
records	10,14,17,	106:9	124:13	219:25
48:20	20,24	114:10	133:6	220:1,10
rectangular	28:7	129:23	134:23	230:7,11,
248:11	32:21	132:9	135:4,6,	18 231:3,
red	33:1	138:15	20 136:9,	6,12
59:1	85:15	165:6	12,13,24	232:20,
169:12	119:24	167:6	137:7	23,24
195:19	120:18	173:8,10	138:2	233:10,
230:19	140:2	174:10	140:3,7,	15,22
231:13	190:24,25	247:23	11,23,24	234:15
240:10	204:22	251:13	141:5,6,	235:8,11
redirect	229:21	255:18	9,16,17,	243:9,12
273:13,22	238:7	refers	24 142:1,	registered
		63:16		72:15
				80:4



800.211.DEPO (3376)
EsquireSolutions.com

243:13	relationshi	181:16	196:11	representin
269:5	p	205:25	228:6	g
registering	101:19	210:1	230:22	7:20
79:15,16,	102:2,10,	relied	256:19	60:19
18	11 172:13	23:22	repeated	reprinted
registers	180:2	149:4	193:19	240:3,5
37:18	240:7	150:5,6	repeats	require
43:12,14	relative	203:12	143:21	95:16
66:13	150:22	204:8	rephrase	201:13
107:5	152:9	242:13	206:7	217:17
135:7	164:10	rely	replied	required
136:1,22	165:6	170:13	148:19	41:17
137:5,13,	167:25	260:12	report	95:19
21 145:1	171:23	relying	19:3,8	270:15
regular	172:1	199:16	119:10,	requires
17:25	181:18	remember	15,24	83:18
45:17	186:9	15:24	120:1	173:11
155:4,8,	189:23	21:3	reporter	reset
21 156:4	207:24	132:16	7:19	137:15
183:20	208:6	179:25	8:10,12,	248:18
213:13,	relevance	remembering	20,23	resided
19,25	226:12	24:6	50:8	180:4
215:4,8	relevant	remind	54:9,24	resistors
Reidt	12:20	13:15	69:4	191:9
7:18	92:6,8	reminder	115:24	resources
relate	94:7,8	49:22	179:19	41:17
148:10,11	99:16	remote	204:25	respect
related	100:8	8:15	229:11	17:2 29:6
10:15	148:15,25	11:19	239:21	33:20
14:5 17:2	149:8,21	remove	246:6	37:3
21:23	150:4,25	186:12	reports	48:21
30:20	151:5,16	removed	19:5 31:2	91:13,20
50:5	152:4	19:8	represent	94:14
52:19	153:5,7,	reorient	72:18	118:15
132:23	10,12	230:21	164:23	144:16
151:11	267:15	reorienting	representat	203:19
198:24,25	reliable	105:6	ion	226:3
222:23	206:9	repeat	13:20	240:22
232:21	reliably	12:25	34:19	273:7
relates	64:18	140:19	55:7	respond
89:8 90:6	77:22	187:7	represented	97:5
91:2	78:4		69:20	
148:9	124:20			
	173:16			



800.211.DEPO (3376)
EsquireSolutions.com

responded	18:8 23:2	254:18	runs	S5
219:17	50:2		51:24	178:10,18
Respondents	85:10	rigor	52:4	179:7,14
23:25	93:18	69:13	Ryan	180:1,6,
responding	94:2	rising	201:1,2	12,17,20,
181:23	95:4,17	129:17	_____	21
rest	100:24	169:16	S	211:13,23
48:11	101:10	170:9	_____	sales
225:5	118:8	226:20		79:4
restate	135:15	227:9,24	S4	sample
217:2	148:5	228:25	178:10,	67:14
result	189:1	Romano	13,24	109:25
122:22	225:4	7:20	179:14	115:7
123:22,25	242:6	room	180:1,5,	155:17
126:3,14	reviewed	11:20	9,20	158:9
127:4,8	15:12	12:3,6,8	181:1,9,	172:14
130:13,20	16:17	roughly	12,19	181:16
133:13,	28:5,11	24:4 68:3	182:6,21,	205:25
19,22	32:9	139:6	25	sampled
134:2,7	62:18	routing	183:11,24	67:3
183:24	65:3	102:5,7,	184:20	114:1
216:16	76:21	16 111:21	185:18	122:22
resulting	93:15	row	186:11,24	123:22,25
59:3	95:14	127:21	187:8	124:21
results	97:17	128:15	188:21	126:25
126:25	104:10	135:20	189:6,22	127:1
127:1	111:18	157:12	198:22	156:15
214:4,9	117:7	163:10	202:20	173:16
resume	135:3	rows	203:4,19	sampler
162:5	136:19	57:21	204:17	109:8,9,
retain	145:25	58:2	205:13,21	16,22,25
200:14	149:1	rule	206:3,9,	113:12,
retained	160:17	13:21	209:7,19	17,18
10:14	237:22	rules	210:10,15	122:17,19
retiming	reviewing	13:16	211:6,11,	123:12,
261:13	56:20	run	18 212:8	17,20,22
262:5	248:1	24:13	213:4	155:17
263:11	revision	46:7 70:4	215:15,20	samples
reversed	87:20	74:23	216:24	65:23
47:23	revisions	161:7	218:1	66:12
review	88:2	running	220:4	109:11,22
	right-hand	258:18	230:6,12	110:6
	103:10		232:20	113:22
	142:24		233:2	115:20



800.211.DEPO (3376)
EsquireSolutions.com

122:21	75:9, 24	262:1, 15	140:6	209:20
123:12	76:13, 19	263:15, 25	142:20	210:3
158:14, 15	116:16, 23	264:23	147:9, 13	233:16
sampling	117:21	267:4, 21	222:14	234:15
114:19	124:8, 17	268:5, 24	250:25	sending
123:19	126:6, 18	269:13	251:11	64:8 78:2
157:1, 7	127:14, 24	273:13, 22	258:8, 10	209:3, 4,
158:13	128:8, 17,	screen	sections	5, 16
172:12	25 129:8,	55:2	57:17	212:9
173:7	15, 23	scroll	58:1	213:21
206:10	130:7	261:19	sees	233:11
Samsung	135:1, 10,	263:1	77:14	sends
7:11 8:2	23 136:6,	267:18	select	210:11, 16
Samsung's	16 137:1,	SDRAM	103:17	215:16, 21
25:13, 17	9, 17, 25	36:13	104:14	233:22
sat	138:10	56:15, 23	241:9	235:3
219:14	139:13	57:1, 2, 5,	selected	sense
satisfy	140:5, 14	10, 11, 16,	105:9, 12	16:8
60:5	141:3, 12,	19, 21, 25	112:8	29:20
Saturday	20 142:6,	84:20	264:21	45:13
15:10, 11,	19 143:3,	133:4	selector	46:1
14, 15, 22	13 144:1,	135:17	188:2	167:16
scenarios	6, 23	136:23	242:20, 25	207:24
78:12	145:9, 15,	137:6	selects	217:24
scheduled	23 203:25	183:4, 6	104:15	226:20
15:23	221:25	236:21	112:10	254:7
schematic	222:7	SDRAMS	240:25	sentence
190:24	223:1	232:17	sell	141:4
191:3, 18,	236:13	search	37:2	219:23
25 192:4,	237:9, 14	24:4	61:18	261:11,
7, 22	247:21	33:10	seminal	20, 23
193:5, 13,	248:9, 16	52:12, 15,	150:19	263:17
16, 17	249:1, 10,	18 54:14	send	264:19
194:7, 18	20 250:5,	searched	11:6 34:1	266:22
195:3	19 251:3,	52:8, 21	35:2	267:6
schematics	17, 24	113:5, 10	sentences	273:2
191:8	17, 24	searching	54:22	140:17
195:4	252:6, 20	32:25	64:20	separate
scope	253:4, 14,	97:6	65:11	53:7, 11
63:1	23 254:6,	section	77:22	144:17
71:22	15 255:5,	23:1	78:7	261:13
73:10	12 256:6,	100:24	82:16	262:5
	17 257:1,	138:11	186:25	
	9, 19		187:10	
	258:3, 14,			
	23 259:8			
	260:21			
	261:16			



800.211.DEPO (3376)
EsquireSolutions.com

separated	153:2	169:4	243:20	side
16:24	154:12	196:9	248:5	102:20
separately	172:18	214:12	251:9,14	103:10
211:13	183:19	215:8	253:1	111:11
September	shift	240:7	254:12,25	116:18,20
87:6,11,	220:2,14	268:11	256:3,11,	125:2
14 221:5	226:24	shown	21	142:24
sequence	227:1	31:3	shows	168:4
133:4	231:22	63:20	75:11	170:5,8
145:7	shifted	64:23	92:5,11	180:11
158:6	126:14	72:1 74:6	93:14	188:8,25
series	short	76:14	96:12	223:15
30:19	68:20	79:11	98:8	238:13
serve	220:16	80:12	125:1	240:5,6,
38:22	237:24	81:9	126:1	17 241:25
served	266:15	86:25	145:12,20	254:19
39:11	shorter	87:6	157:9,11,	sides
set	231:22	92:12,13,	13,16	170:5
58:12	show	21 93:8	158:2	177:16
63:6 65:6	56:8	96:4,18	163:10,17	signal
80:3,17	93:2,8	98:17	168:25	44:19,20,
86:2	145:19	99:8,25	175:24	22,25
112:16	158:5	118:19	176:24	45:1,24
134:23	170:7	120:2,7	177:6	47:7,8
135:6,20	192:3,15,	125:15	191:13	60:22
136:2,13,	16 196:4,	126:15	193:24	63:17,22
24 137:7	13,18,21	127:11	205:5,17,	64:5,9,
140:10,	197:18	137:21	18 207:4	13,14,15,
23,24	199:15	144:3,7	209:15	19,20
141:5,16	207:9	160:9	212:1	65:6,15,
142:4,8	212:8	176:14	223:19,22	18 66:1,
144:17	214:15	178:16	226:2	3,17
174:5	215:8	180:8,11	229:19	67:2,5,
214:18	217:10	182:22	232:12	10,13
224:23	254:16	187:9	233:1,14	68:2,11,
sets	255:15	196:2	234:14,	12 73:22,
135:7	showed	203:15	19,25	23,25
setting	246:20	217:3	235:7,10	80:7,9,10
268:17	showing	220:10	238:14,24	92:13,17,
setup	51:13	224:17	239:3	21 93:3
65:4,5,12	81:23	230:14	242:14	96:4
127:7	157:19	231:13	255:9	97:22
	159:5	232:8	256:9	98:2
	160:19	240:25	sic	102:25
		241:6,8	224:2	103:21
		242:17,21		104:16,



800.211.DEPO (3376)
EsquireSolutions.com

17,24	157:9,11,	25 212:9	66:5,6,24	6,9,10,23
105:2,5,	13,17	213:7,21	73:17,21	201:5,14
11,12	158:3,17,	214:17,	74:3	202:9,22,
106:2,18,	21	18,23,25	75:11,12,	23 203:3,
20,21,22,	159:15,19	215:16,	13,21	14,21,22
24 108:25	160:14	22,25	76:3,6,9	204:10
109:16,	163:18,19	216:2,8,	78:8	206:21,22
23,25	164:10	12,23	79:18,19,	207:5
110:1,5	167:3,4,	217:3,11,	22 80:1	217:5
111:9,14,	19,23,25	25 218:20	81:9,18,	226:15
16,23,24	168:4	219:24	21,24	232:17
112:10,	171:8,9,	220:2,3,9	98:9	233:10
14,17,18,	16,20,21	223:21	106:5,17,	247:19
20,25	172:8,15	224:2,3,	20 112:7	260:13
113:24	173:3,9,	8,12,23,	114:1	263:7
114:18,20	11 177:7,	25 225:1,	120:8	significanc
115:4,6	13,22	2,12,17	121:2	e
116:18,20	183:2,13	226:13,18	125:5	194:4
117:10,	184:1,2,	227:7,9,	127:19	significant
18,19	22,23	25 228:4,	130:5,10,	40:17,25
118:16,18	185:21	12,17,23	12,15,21,	41:6 42:1
120:6	186:3	229:4	23,25	79:11
123:1,4,	187:1,4,	231:21,23	133:5,9	150:18
17 125:6,	10,11,14,	232:3,5,	134:8	224:15
14 126:2,	17,21	14,22	138:25	silicon
13 127:2,	188:5,6,	233:17	153:14	41:17
3,10,11,	9,11,12,	234:16,	156:5,6	silly
21,22	18,22	20,22	157:3,20	166:2
128:13,	189:7,16,	235:3,8,	164:1	similar
14,22	17,23,25	11 237:19	166:21	81:8
129:20,21	195:22,25	240:18,	167:12	269:1
130:17,18	196:5,14	21,24	168:6	similarly
134:3	197:8	241:4,23	177:9,11,	80:10
138:23	198:9,14,	242:15,	15 181:24	211:22
150:22	15	20,24	182:15,16	simpler
151:15,16	199:10,12	243:5,9,	184:8	53:9
152:9,21,	200:18	12,17,18,	186:1,8,	simplicity
22	206:2,6,	22 244:2,	18 187:3,	157:22
153:20,	8,13,14,	3 245:15	12 196:5,	simply
24,25	17,23,25	263:21	7,14,18,	83:24
154:8,16,	207:1,20,	264:9	22 197:3,	100:22
24,25	23,25	265:4,12,	4,11,12,	101:16
155:3,7,	208:22	24	16,24,25	173:8
13,15,20	209:2,17,	signals	198:13	
156:1,9,	20,21,22	60:23	199:1,5,	
10,12,14,	210:11,	64:18	15,17,18,	
16,19,24	16,18,23,		23 200:5,	



800.211.DEPO (3376)
EsquireSolutions.com

179:25	situation	72:22,24	254:1,4	52:25
200:13	84:13	74:17	257:11	sound
225:7	117:23	78:22	socket	52:10
236:18	172:10	82:20	53:12	166:7,17
248:2	situations	83:6,16,	sold	sounds
249:13	152:12,	24 84:6,	75:2	62:15
257:20	13,14,17	14,16,22	149:12	131:18
simultaneou	172:11,20	85:4,16,	151:17	165:22
sly	174:2	23 86:7	solemnly	166:9
109:13	193:2	91:19	8:23	220:17
single	SK	94:14	solid	spaces
80:2	30:6 31:5	120:4	92:16	52:3
176:8	skew	147:19	116:10	sparse
single-	139:3,10,	218:13	Solutions	146:18
spaced	17	244:24	7:21	speak
52:2	163:18,	265:25	solve	63:19
sir	22,25	skilled	153:24	117:16
12:2	164:4,7	267:15	son's	260:20
15:2,19	166:3,4,	slash	201:1	speaking
16:4 47:2	10,11,13,	250:9	sort	109:13
181:11	19 167:11	slide	41:10	spec
192:9	168:1,3,	69:11	45:17	163:23
259:16	7,10,11,	247:16	57:12	167:14
sit	14 169:1	slightly	62:8 63:3	specific
32:17	170:4,5,	100:21	71:25	38:23
50:14	15	140:20	75:1	43:20
56:22	174:10,14	155:2	83:19,25	51:13
62:15	198:19,23	slow	89:9	66:22
75:17	skewed	253:17	103:1	93:21
94:1	164:9	slower	125:21	95:15
95:13	166:25	42:11	157:19	104:10
96:25	skill	small	186:4	152:5
100:10	29:6,10,	31:2	192:14	172:10
138:14	17 33:21	39:25	204:22	254:8
152:7	34:5,12	201:24	230:19,23	266:19
222:9	35:9,15,	253:17	231:1,4	specificall
248:3	19 36:4,	smaller	238:25	y
249:5	6,10	41:18	241:22	16:20
275:3	37:6,14	42:10	253:1	35:13
sits	38:2	SMBUS	254:19	51:10
73:13	40:12,20,	252:25	265:10,14	92:23
sitting	22 43:10,	253:6,8,	sorts	97:1,6
49:7	17 53:24	11,20	40:15	120:17
100:16	71:16			



800.211.DEPO (3376)
EsquireSolutions.com

164:3	95:6	151:18	start	273:14
222:17		154:19	21:19	stated
270:24	spot	157:16	82:14	22:11
	165:18	158:2,16,	147:8	29:8
specificati	166:2	20 159:22	175:5	32:15
on	stages	160:13	248:7	143:10
83:22	112:16	161:4		175:16
91:24		162:14,23	started	180:23
135:12,16	stall	163:9,17,	21:23	206:10
152:6	165:24	24 166:20	114:15	261:5
159:4	stand	167:22	117:6	
166:12	47:3	168:9,20,	211:3	statement
174:18	58:18	25 174:11	starting	14:7 22:7
267:14	75:16	246:13	8:16	33:20
specificati	151:22	247:13	11:22	34:4
ons	standard	248:1	30:17	85:20
36:19	28:10,13	253:11	34:6	132:25
37:2	51:11	258:25	102:25	states
65:10,13	60:7	standardize	111:10	7:12
151:11	62:20	d	154:25	47:19,21
specifies	63:24	56:16	258:10	48:1
120:12	66:22	73:3 75:3	starts	145:5
specs	67:9	79:6	51:21	219:24
151:11	69:23	247:2	233:16	244:19,20
speed	74:5	standards	234:15	statically
39:25	82:21	23:23	state	161:6
40:4	83:2	28:17,20	7:23 8:24	stating
41:20	84:3,4,17	36:8,14,	10:6	22:12
64:10	85:2,14,	24 37:1	45:15	stay
69:8,9,	18,24	43:22	46:9,20,	182:9
16,17	86:11,24	50:24	25 48:3,	
70:3,11,	87:5,13,	51:5,8,14	4,5,10	stenographi
15,16,22	17,24	60:9 84:9	61:8	c
78:13	131:15,	85:18	107:5,7	262:23
121:17,19	16,19,20,	86:5,9,13	156:15	267:2
speeds	24 132:5,		157:5	step
69:23	13	standing	159:11,	103:2
70:5 78:8	134:16,24	275:13	13,16	111:12
spell	138:6,17	stands	175:12	171:8,15,
50:7 54:9	139:5,19	38:8,11	177:17,	20 172:7
69:4	140:1,9,	54:11,13	18,25	173:2
spent	22	65:5,9	226:1	196:10
16:19	142:10,14	81:14	254:25	206:21
17:10,23	143:6	250:2	255:9,15	
	146:2	252:7	256:2	stepped
	148:3	253:20	263:9	51:9



800.211.DEPO (3376)
EsquireSolutions.com

steps	104:5, 8,	11, 12, 19,	strobes	suggesting
273:16	13, 16	22 189:7,	182:2	70:14
stock	105:1, 9,	16, 17, 23,	stroke	132:18
31:23	12 108:25	25 196:18	110:1	suggests
stop	110:17, 19	197:3, 23	struck	225:17, 19
107:18	113:23	198:9, 15	181:21	summary
141:1	114:6, 9,	199:1, 4,	structure	91:22
159:21	11, 17, 18	10 200:5,	37:8 82:1	100:3
stops	115:4	9, 18, 23	133:3	178:2
155:21	116:19	202:22	students	supercomputing
store	117:18	203:21	51:5, 12	68:19
44:3	118:18	207:20	stuff	supplement
77:24	120:6	213:7	12:15	25:4
stored	130:18	215:16	stumbled	supplied
44:24	139:4, 10	220:3	86:19	225:12
77:24	150:21	223:16, 20	subject	support
216:17	151:15	224:11,	261:1	35:14
stores	152:9, 22	20, 23, 24	submitted	supposed
232:23	153:20, 25	225:11,	19:25	127:17
story	154:8, 15,	12, 17, 24	20:6, 20,	185:20, 25
68:16	24 155:7,	226:3, 5,	24 32:9	surprise
straight	13, 15, 19	7, 10, 13,	submitting	63:12
219:15	156:1, 5,	17 227:6,	21:1	90:23
stricken	6, 10, 13,	21 228:2,	subsequentl	146:24
19:3	16, 19, 23	15, 24	y	162:18
strobe	157:3, 13,	233:16	168:5	surprised
63:17, 22,	17, 23, 24	234:16,	substance	161:8
25 64:5,	158:3, 7,	20, 22	13:18	surprising
8, 20	17, 21	237:19	14:5	62:6
65:17	159:23	241:23	subsumed	suspect
66:17, 24	160:14, 15	242:14, 19	194:25	218:17
67:4 74:3	163:18	243:5, 9,	succeeded	swear
75:12	164:9	12, 16	209:10	8:11
76:9	167:19, 23	245:15	suggest	switch
92:5, 20	169:17	247:19	125:17	139:23
93:3	170:1	260:13	261:1	sworn
94:23	171:8, 16,	263:21	suggested	7:24
96:4, 20	20 172:7,	264:9	42:13	symmetric
97:22	15 173:3,	265:15	74:24	168:8, 15
98:2 99:7	9, 10	266:7	241:19	
102:24	183:2, 12	268:8		
103:20	184:1, 22	269:9		
	185:21	strobe-		
	186:25	centering		
	187:4, 10,	263:13		
	14, 21			
	188:5, 6,			



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 337
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 337

Sync	134:12	taking	204:2	99:12
252:21	172:22, 25	167:19	206:20, 22	118:5, 11,
synchroniza	_____	talk	212:14	15 128:13
tion	T	49:4, 22	213:18	138:22
45:14	_____	63:8	255:14, 21	140:10
225:13	T0	89:14	270:24	143:7
263:22	231:12	97:7	271:2	150:21
synchronize	T10	103:4	talks	154:14
d	234:23	108:6	68:17, 21	160:13
225:16	T4	147:2	150:23	207:17
synchronous	234:3	198:16	152:1	232:19
45:15	T5	212:16	266:17	244:12
107:4	232:4, 6	219:2	task	245:13
159:19	233:15,	talked	39:12	256:13
system	19, 21	41:8 76:5	85:19	270:12, 20
36:16	234:3, 15,	79:16	151:8	273:25
37:10	21	104:15	taught	teaching
45:13	T6	107:3	43:25	91:1, 13,
46:19	233:21	123:14	51:4, 6,	20 94:13,
53:7	234:21	125:21	12, 16	25 98:10
58:21	235:1, 13	130:22	95:12	150:25
77:3	t8	133:7	96:22	272:11, 16
84:25	92:12, 18,	138:2	144:20	teachings
121:9, 10	24 98:14	170:16	153:21	147:11, 20
145:7	99:13, 15	175:21	tck	148:2, 14,
178:19	t9	216:25	161:25	24 149:7,
179:8	92:18, 24	224:7	tdh	21 150:4
181:15	98:14	273:1	65:8	151:14
184:18, 19	99:14, 16	talking	tdqsq	153:5, 9
187:1, 11,	table	23:4	169:2, 4,	267:14
22 188:23	162:22	24:22	13, 15, 23	technical
189:8, 18	163:1, 9,	47:20	170:1	31:21
190:15	17 257:24	54:4	tds	41:2, 7
211:14	258:11, 15	68:23	65:2	91:17
233:11,	takes	72:25	teach	155:2
17, 22	78:3	89:9	96:2, 9	262:22
234:16	103:20	98:16	98:1 99:6	267:1
235:4, 12	108:25	117:6	technique	133:11
253:21	155:6	156:7	126:12	134:4
254:3	205:13	167:17	154:5	146:22
systems	230:6	168:3	teaches	152:5
36:18		173:14	96:7, 13	153:23
71:24		174:4	97:21	269:9
76:6		178:24	98:6	
		188:7		



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 338
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 338

techniques	181:21	20:2 55:6	190:6	71:24
132:21	191:23	78:10	202:15	78:3
technologies	222:11	93:6	208:18	88:4, 8, 11
s	252:9	94:20	thinking	92:12, 24
152:10	terminates	99:5	24:3, 14	96:7, 10,
technology	207:1	108:17	85:15	11, 14, 17,
37:24	terminology	119:1, 6,	228:8	18, 21
40:5	194:12, 14	18 149:23	thought	98:8, 12
51:16	terms	171:11	98:19, 22	99:24
55:4, 10,	24:4	185:24	100:6, 7	107:15
14, 21, 25	40:17	224:6	123:14	108:3, 9,
56:2	41:17	246:2	128:9	12 111:19
57:1, 2, 5	59:16	259:14	131:21	124:20
70:16	128:21	261:4, 10	148:8	126:10
72:2	155:2	262:12	178:24	134:3
76:21	164:22	264:4	210:23	139:3, 9
83:21	166:14	265:1	224:21	145:25
147:16	193:1	testing		146:1, 6
148:11,	194:3	268:15, 17	thousand	151:8
12, 15, 16		Texas	17:17	155:5
150:13	test	31:6	three-	156:4, 13
151:1	250:3, 12,	221:5	quarters	159:20
246:19	15 251:22	text	232:6	160:18
272:19	252:4, 8,	89:15	Thursday	161:7
telling	9, 11	169:21	7:1	162:8, 11
67:14	268:18	264:1	tight	170:12
tells	269:3, 4	texting	117:25	172:17,
271:23	testified	14:4	time	18, 19
ten	10:3	Theodore	7:6 8:12	184:10, 14
16:13	19:11	8:1	12:9	186:20
18:20	31:1	thing	13:11	208:21
275:20	93:20	11:7	16:3, 6,	220:19, 22
tend	97:24	133:17	24, 25	229:8
40:3	260:25	158:14	17:23	230:18
41:19	testify	194:15	26:3	231:12,
43:5	55:18	234:6	31:13	17, 22
94:10	testifying	things	42:8	232:4, 6,
term	57:7	13:23, 24	44:3, 5, 6	21 233:15
23:24	263:5	25:1	45:8 46:7	234:2, 23
43:21	testimony	48:19	49:17, 20	235:9, 13
53:1	8:24	53:15	50:24	238:2, 5
58:15	13:18	54:6	55:19	245:21, 24
66:13, 16	14:6 16:9	125:24	62:23	258:19
72:8, 23	19:24	132:13, 20	65:4, 5, 9,	259:18,
			12 67:1	22, 25
				266:15
				269:24



800.211.DEPO (3376)
EsquireSolutions.com

270:3	262:4	45:8	town	transitioni
275:16,21	title	161:11	55:18	ng
times	145:17	200:17	Trademark	157:18,20
18:5,18,	251:11	201:2	7:13	transitions
20 19:14,	257:21	211:11	train	157:4
17 86:20	titled	tolerable	213:5	158:4
119:4,13,	140:7,25	163:22	trained	160:16
16,22	142:20	164:4	183:22	207:10,13
127:7	252:23	tolerate	training	234:22
153:2	today	168:14	183:19	travel
154:13	7:19 8:8	top	198:22	68:13
159:6	12:13	11:16	203:4	130:12,18
161:25	14:6	23:10	209:8	167:12
164:13	15:21	25:9 41:7	210:9	traveling
166:16	21:2	44:1	212:18	68:7
173:19	29:8,15	63:21	213:2,13,	travels
182:3	31:19	70:1,19	15,16	68:2
201:8	36:20,22	88:14	214:1,4,	166:24
217:1	56:22	89:20	7,10,11	241:24
232:14,18	62:15	94:3	215:9,14	treat
274:7	80:25	104:23	271:19	84:2 85:2
timing	93:19	116:10	tran-	tri-state
91:5,6	95:8	126:22	8:10	37:17
117:25	100:17	136:22	transaction	43:12,13
133:13	151:18	137:4	s	45:19,22
134:5	246:3,18	143:20	78:13	46:3,5,
145:7	259:15	145:4	transfer	14,18,22
172:23	261:4	157:9	176:2	47:18
182:7,8	262:12	163:9	transistors	48:3,9,
183:1,7,	263:4	169:20	191:10	10,15
12 184:1,	264:4	177:23	transition	103:14,24
9,16,22	today's	195:23	64:21	110:11,22
186:17	15:7	223:11	127:18	112:2
187:2,12	16:3,6,	231:6	156:20,25	115:12
188:10	11,14	239:8	157:6	177:20,24
190:3	97:18	254:17	158:12	184:11
200:9	Tokuhiro	274:20	169:16	188:1
201:11	26:25	topology	170:2,9	189:11
207:4,10,	27:4	138:24	transistors	192:17
19,22	85:13	total	191:10	236:19
208:9,10,	238:7,11,	16:18	transition	trial
23 210:7	13,16,19,	59:4	64:21	7:13
213:6	22,24	touching	127:18	19:11,24
230:9,12	told	261:1	156:20,25	55:13,18,
233:1			157:6	
260:12,14			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	
			64:21	
			127:18	
			156:20,25	
			157:6	
			158:12	
			169:16	
			170:2,9	
			transistors	
			191:10	
			transition	

22	169:6	44:4,20	14,21	200:1
triangle	176:17	47:24,25	27:3,13,	203:7
177:24	178:4	58:15,21	19 28:6,	212:13
triangles	190:9	89:4	12 36:25	215:7
177:16	195:6	107:6	39:19	217:14
tricky	199:7	156:24	45:10	219:7,10,
46:1	204:12	183:17	48:8	11,16
triggers	210:3	227:2	53:25	226:2
158:12	223:8	228:21	54:6 78:5	233:13
tripped	224:18	250:11	83:7,9,12	241:3
206:24	238:6,22		90:16	249:4,13
trouble	244:7		101:13	252:23
140:18	260:6	U	120:3,5	254:22
trpe	266:12		149:20	264:25
160:6	268:10	U.S.	150:8	understood
trpre	270:6	10:19	163:2,3	13:19
160:7,14,	turned	UDIMM	165:8,10	14:1,2
19 161:8	46:2,15,	71:12,14,	182:10	28:19
true	18,23	16,19	183:9	86:2 96:1
212:6	47:12	ultimately	189:21	188:14
trust	184:17	65:24	213:11	205:10
67:22	190:8	190:11	214:6	213:24
193:19	191:24	UN	218:14	214:8
truth	260:14	240:24	242:4	230:3
9:1,2	turning	241:7,11	249:15	240:11
turn	271:9	unbuffered	251:21	242:2
28:25	turns	71:11	253:7	undo
51:20	190:7,8	72:8	266:6	134:4
56:5,12	tutorial	175:14	understandi	unequal
57:13	55:5,11,	unclear	ng	130:3,5
58:9	14,25	34:22	26:9,12,	unfortunate
63:13	56:3	uncommon	17 27:6,	124:19
71:7	247:16	61:21	12,21	unheard
72:10	tutorials	63:5	28:8,14,	191:22
74:9	55:21	191:21	22 34:20	unit
78:14	type	underlying	43:18,20	7:8 92:24
80:20	37:25	87:20	76:16,23	216:18
82:12	39:8	underspecif	90:18	United
88:13	types	ied	94:8	7:12
111:4	36:18,20,	121:15	101:15	units
121:23	22 37:12	understand	102:1	275:20
typically	44:10	14:3,7	138:14	unmarked
		26:7,10,	157:23	12:22



800.211.DEPO (3376)
EsquireSolutions.com

unrelated	202:3	video-	walk	35:12
263:12	217:4	recorded	241:23	85:22
	241:10	7:9		97:9,13,
unsure	245:14	videoconfer	wanted	17 100:3,
246:24		ence	100:24	15,18
up-front	variable	8:16	109:2	120:25
42:1,21	160:21		148:5	149:25
	185:11,20	view	217:21	151:10
update	186:5	53:13,16	218:6	
44:21,25	188:22	184:10	264:14	week
	189:7	191:8		16:10
updated	238:17,	193:23	warned	93:22
44:5	20,25	194:18,	107:15	95:8
107:5	239:3,6,	19,25	Washington	
	11,17	217:25	7:1 10:23	weird
updating	243:5	227:11	12:1	181:21
107:7		228:15		199:20
upper	verb		watch	
122:2	114:11		64:17	well-known
177:6		views		61:25
195:17	versa	194:23	ways	175:13
205:6,7	62:24		44:12	
229:22,23	76:11	virtue	114:6	Western
231:2	195:5	201:4	134:10	31:6
241:11,19	versus	visible	152:3	wide
248:13,17	7:11	103:7	270:22	59:3
	16:24	Visually	272:11	60:25
usage	30:6 31:5	248:10		61:10
78:11	50:11	voltage	weaknesses	
253:11	156:9	121:20,22	67:20	width
	194:15	volts	Wedig	59:4,19
usual	195:3	47:13,14	85:13	62:11
79:2 89:4			86:16,18	160:5
	vertical		93:23	widths
v	105:14	volume	97:1	59:16,19,
		42:23	98:7,20	22,24
	vertically	43:5	126:8	61:9,15,
valid	105:24	volumes	148:19	25
169:16		75:1	149:2,4,	
170:1	vice		15 150:5,	William
172:14	62:23		8 199:21	7:10
	76:11	W	203:11	10:1,7
values	195:5		219:12	275:19
112:20	video		242:5,12	window
114:7,9,	12:18	wait	266:9	273:15
10,13,14	262:17	260:19		
115:7	266:24	waiting	Wedig's	windows
161:7	275:13,	107:18	33:25	87:3
181:16	15,20		34:4	
183:23				



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 342
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 342

wire	44:16	62:22	237:6,17	112:7,8,
46:12	52:24	63:4,6		11,20
47:17	54:16,19	67:14	write-	114:15
48:6	64:4	86:9 91:7	enable	
64:1,15	83:25	131:20,25	45:1	year
67:25	110:4	132:3,23		17:9 18:2
68:14,22,	114:2,5	134:11	writes	31:5
24 166:24	121:10	136:2,9,	60:17	48:22
167:12	125:25	12 137:22	written	50:17
	144:24	138:4,7,	58:13	86:25
wired	150:19	12,19,20	74:7	
46:5	152:20	139:8,15,	137:14	years
	210:9	20,22	244:4	30:2
wires	245:2	146:7,13,		34:14,17
63:7		21	wrong	35:22,25
64:9,12	worked	178:14,24	24:16	44:1
67:2,12	30:17	180:9,12,	46:16	62:18
80:3,4,17	50:4	20,21	56:21	
133:7	74:22	181:1	67:22	yesterday
174:16		183:18	105:21	15:12,14
	working	203:19,20	166:1	16:1 23:3
word	16:19	204:3,17	169:12	
11:5	83:18	205:13,	210:21	Z
52:17	84:20,23	17,18,21	212:23,25	
117:24	159:21	206:4,9,	216:13	
156:20		15,18	217:1	Zhong
251:19	works	207:18	232:10	15:16,17
	76:17	208:24,25		
words	88:22	209:7,9,	wrote	zoom
29:16	190:12	10,19,24	210:5	7:16
95:24	208:4	210:1,2,		12:18
105:1	226:4	8,10,15	X	15:10,11,
135:24	269:6	211:6,11,		14,22
140:16		13,18	x8	16:12
166:23	worse	212:8,14,	60:12	107:21
233:3	167:11	18 213:2,		234:12
235:17	worst	3,4,18,19	Y	262:20
271:13	152:19	214:1,2,		
		3,7,8	YA	
work	worst-case	215:4,8,	103:17	
14:16,19,	166:11	15,20	112:7	
22 15:5		216:6,16,		
21:19,25	worth	17,22,24	YB	
29:21,24	100:8	217:12	102:20,25	
30:20,25	224:15	218:1,20,	103:9,17	
31:2		22 220:5	111:10,	
34:14,18	writ	222:23	14,25	
35:22,25	237:3			
39:5	write			
	44:20			



800.211.DEPO (3376)
EsquireSolutions.com

Samsung Ex. 1046, p. 343
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711

Samsung Electronics Co., Ltd.
Samsung Ex. 1075, p. 343