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APPEARANCES :

FOR THE PETITIONER :

BAKER BOTTS L.L.P.
Attorneys at Law
1801 Century Park East, Suite 2400
Los Angeles, California 90067
BY: THEODORE W. CHANDLER, ESQ.

BAKER BOTTS L.L.P.
Attorneys at Law
101 California Street, Suite 3200
San Francisco, California 94111
BY: FERENC PAZMANDI, ESQ.

FOR THE PATENT OWNER :

IRELL & MANELLA LLP
Attorneys at Law
840 Newport Center Drive, Suite 400
Newport Beach, California 92660
BY: JONATHAN M. LINDSAY, ESQ.

IRELL & MANELLA LLP
Attorneys at Law
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067
BY: HONG ANNITA ZHONG, ESQ.

ALSO PRESENT :

DANA BACHMANN, VIDEOGRAPHER

I N D E X

SAMSUNG VS. NETLIST
NO. IPR2023-00847
JUNE 4, 2024

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EXAMINATION BY MR. CHANDLER:		242

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Exhibit 1046	U.S. Patent No. 10,860,506	20
Exhibit 1076	Declaration of Dr. William Henry Mangione-Smith dated 1/31/2023	21
Exhibit 1075	Deposition of Mangione-Smith dated May 4, 2023	22
Exhibit 2014	JEDEC Standard JESD79-2F, DDR2 SDRAM Specification	42
Exhibit 2015	JEDEC Standard JESD79-3F, DDR3 SDRAM Standard	43
Exhibit 2018	JEDEC Standard JESD79, Double Data Rate, DDR, SDRAM Specification	43
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Exhibit 1020	JEDEC Standard JESD79-3C, DDR3 SDRAM	45
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I N D E X

SAMSUNG VS. NETLIST
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WITNESS: DR. WILLIAM MANGIONE-SMITH

MARKED/IDENTIFIED EXHIBITS

NUMBER	DESCRIPTION	PAGE
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Exhibit 1021	Memory Systems Cache, DRAM, Disk, Bruce Jacob, et al.	91
Exhibit 1080	'608 Patent Figures 15 and 16	146
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Exhibit 1070	Reprints several of the paragraphs from the Hiraishi reference marked as Exhibit 1005	214
Exhibit 1069	Simple picture of Hiraishi	248

1 BE IT REMEMBERED that on JUNE 4, 2024, at
2 9:06 A.M., the remote videotaped deposition of
3 DR. WILLIAM MANGIONE-SMITH was taken before
4 Monna J. Nickeson, Certified Realtime Reporter,
5 Registered Professional Reporter, Certified
6 LiveNote Reporter, Certified Court Reporter
7 (WA 3322), Certified Shorthand Reporter
8 (ID 1045), (OR 16-0441), (CA 14430), the
9 following proceedings took place:

10 * * * * *

11 THE VIDEOGRAPHER: Good morning. We're
12 now on the record at 9:06 a.m. Pacific time on
13 June 4th, 2024. This begins the videoconference
14 deposition of Dr. William Mangione-Smith taken
15 in the matter of Samsung Electronics Co., Ltd.,
16 versus Netlist, Inc., filed in the U.S. Patent
17 and Trademark Office before the Patent Trial and
18 Appeal Board. Cause number IPR2023-00847.

19 My name is Dana Bachmann. I'm your
20 videographer today. Our court reporter is
21 Monna Nickeson. We're both representing Esquire
22 Deposition Solutions.

23 Would all present please identify
24 themselves, beginning with our noticing
25 attorney.

1 MR. CHANDLER: Good morning. This is
2 Ted Chandler from the law firm of Baker Botts on
3 behalf of the petitioner, Samsung Electronics
4 Co. Limited.

5 With me is my colleague, Dr. Ferenz
6 Pazmandi. And during the deposition we may be
7 joined by summer associates Miles Cooper and
8 Kelsey Edwards.

9 MR. LINDSAY: And this is Jonathan
10 Lindsay from Irell & Manella, joined with my
11 colleague, Dr. Annita Zhong, representing --
12 defending Dr. Mangione-Smith today.

13 THE VIDEOGRAPHER: Thank you very much.

14 Madam Reporter, would you kindly swear in
15 our witness.

16 DR. WILLIAM MANGIONE-SMITH.
17 having been first duly sworn to tell the truth, the
18 whole truth, and nothing but the truth, testified as
19 follows:

20 EXAMINATION

21 BY MR. CHANDLER:

22 Q. Please state your name for the record.

23 A. William Henry Mangione-Smith.

24 Q. What do you for a living,

25 Dr. Mangione-Smith?

1 A. I'm an engineer.

2 Q. Dr. Mangione-Smith, were you retained by
3 Netlist to provide opinions in this case related to
4 Netlist's '608 patent?

5 A. Yes, I was.

6 Q. And the '608 patent is marked as
7 Exhibit 1001 and is U.S. Patent Number 10268608,
8 correct?

9 A. Yes, sir.

10 Q. Given that this is a remote deposition,
11 meaning, we're not in the same physical room
12 together, there are a few questions I need to ask,
13 starting with, where are you physically located right
14 now during this deposition?

15 A. In my home office at 4146 118th Avenue
16 Northeast, Kirkland, Washington.

17 Q. Is there anyone else in the room with you
18 right now?

19 A. No, there's not.

20 Q. Given that I cannot see the room that
21 you're in, will you please let us know if someone
22 else enters the room at the any time before the
23 deposition ends?

24 A. I will do that.

25 Q. Dr. Mangione-Smith, did you bring

1 anything with you to your deposition today?

2 A. That's difficult to answer. It's my home
3 office. It's stocked with things.

4 Q. Is there anything in front of you besides
5 your computer, such as any printed documents that you
6 brought specifically for the deposition today?

7 A. No.

8 Q. Given that I cannot see whether you have
9 anything in front of you that you're looking at, will
10 you please let us know if you or anyone else puts
11 anything in front of you at any time before this
12 deposition ends?

13 A. I will.

14 Q. Is there anything on your computer screen
15 right now besides the video feed and the exhibits for
16 this IPR?

17 A. Yes. I've got a web browser open.

18 Q. And why?

19 A. I was interested in knowing what Doctor,
20 I think you said, Pazmandi's area of expertise was.

21 Q. In general, you won't need to look
22 anything up on the internet, and you should not look
23 things up on the internet or text with other people
24 without letting the rest of us know that you're doing
25 so during the deposition, understood?

1 A. Okay.

2 Q. I will take breaks throughout the
3 deposition, but I want to remind that you during
4 those breaks you should not consult with your counsel
5 about the substance of your testimony; is that
6 understood?

7 A. Yes, sir.

8 Q. And to be clear, you understand that
9 during the deposition you should not be emailing or
10 texting other people?

11 A. Sure -- certainly. I mean, while the --
12 while I'm being questioned I'm not emailing or
13 texting anybody.

14 Q. Do you have any questions for me about
15 the procedure for today's deposition?

16 A. No.

17 Q. What did Netlist ask you to do in this
18 matter?

19 MR. LINDSAY: Bill, I would just caution
20 you to answer the question generally and not get
21 into the substance of any specific conversations
22 you may have had with Netlist's counsel.

23 THE WITNESS: Understood.

24 So it's been a little while, but my
25 recollection was I was asked to consider the

1 arguments put forth to the PTAB, P-T-A-B,
2 regarding this patent by Samsung, as well as
3 supporting arguments by Dr. Wedig.

4 BY MR. CHANDLER:

5 Q. What did you do to prepare for today's
6 deposition?

7 A. I have reviewed my own declaration and
8 elements of the various documents that I cited in my
9 declaration.

10 Q. And how long approximately did you spend
11 in preparation for today's deposition?

12 A. That's -- I don't have a precise number,
13 but I would argue -- excuse me, I've got a little bit
14 of a cough today. I would argue that everything I've
15 done regarding this patent is in preparation for this
16 deposition, building up to it.

17 Q. In the past two weeks approximately how
18 much time have you spent preparing for today's
19 deposition?

20 A. Maybe 10 to 16 hours.

21 Q. And did you meet with anyone to prepare
22 for today's deposition?

23 A. Yes, I did. Not physically.

24 Q. And who did you meet with?

25 A. I met with counsel from Irell.

1 Q. Anyone else?

2 A. No.

3 Q. And for how long did you meet with
4 Netlist's counsel to prepare for today's deposition?

5 A. Probably five to six hours.

6 Q. And who did you meet with, the names?

7 A. That would be Jonathan Lindsay and
8 Annita Zhong.

9 Q. And anyone else?

10 A. No.

11 Q. As part of your work for Netlist on this
12 matter, did you personally talk to anyone besides
13 counsel at Irell, such as the inventors or anyone
14 else with experience in the field?

15 A. Not in the context of my efforts for this
16 IPR activity, no.

17 Q. Were there other contexts related to the
18 '608 patent where you spoke with other people, such
19 as the inventors or others with experience in the
20 field?

21 A. I don't think I've, to the best of my
22 recollection, ever spoken with the inventors. I have
23 had several conversations with Netlist's CTO, but
24 I don't think it was in the context of this
25 particular patent.

1 Q. And what's the name of Netlist's CTO that
2 you had several conversations with?

3 A. That would be Scott Milton.

4 Q. Approximately how many hours in total
5 have you spent working on this matter, related to the
6 '608 patent?

7 A. Yeah, I don't really have a good
8 estimate. I could certainly -- well, yeah, I guess
9 I'll just leave it with that. I don't have a good
10 estimate. I'm not even sure if I could produce a
11 good estimate.

12 Q. How much are you charging Netlist per
13 hour for your time spent on this matter?

14 A. My standard hourly rate, and I believe
15 that is \$750.

16 Q. Per hour?

17 A. Yes, yes.

18 Q. And it would be fair to say that you
19 billed Netlist in excess of \$100,000 related to
20 litigation against Samsung?

21 A. That's probably accurate, yeah.

22 Q. Approximately how many times have you
23 been deposed before?

24 A. I don't really know. More than 20 days.
25 Some of the depositions for single matters covered

1 multiple days.

2 Q. And how many times have you testified at
3 trial as an expert?

4 A. I have testified many times in trial and
5 at the ITC, and I believe four to five times in front
6 of district court.

7 Q. And how many times have you testified as
8 an expert at trial on behalf of Netlist?

9 A. So there were two matters at the ITC, and
10 I believe only two of the matters in the district
11 court, but I'd have to go back and verify. It might
12 have been three, but I think it was two.

13 Q. And the district court that you're
14 referring to is the United States District Court for
15 the Eastern District of Texas; is that correct?

16 A. Yes, that's correct.

17 Q. Could you please turn to your expert
18 declaration marked as Exhibit 2013? Let me know when
19 you have it in front of you. I previously put it in
20 the chat for everyone.

21 (Exhibit 2013 was identified.)

22 THE WITNESS: Okay. I have it open in
23 front of me.

24 BY MR. CHANDLER:

25 Q. And if you go to PDF page 126 of your

1 expert declaration marked as Exhibit 2013, does the
2 top of that page provide your current address,
3 telephone number, and email address?

4 A. It does.

5 Q. And do PDF pages 129 through 148 of your
6 expert declaration marked as Exhibit 2013 list all of
7 your prior expert engagements in which you were
8 either deposed or testified at trial?

9 A. As of the date that was -- that document
10 was produced, that version of my CV was produced.

11 Q. All right. What about since, since then?

12 A. I -- pardon me. Could you repeat that?

13 Q. What about since then, what additional
14 engagements have you had in which you were either
15 deposed or testified at trial since the date that you
16 prepared the CV attached to your expert declaration
17 marked as Exhibit 2013?

18 A. I'm not sure. I'm just noticing that it
19 only goes up through 2022. I expect there were
20 entries from 2023, but I'd have to go back and
21 double-check.

22 Q. Do you remember? It was only -- 2023 was
23 only six months ago.

24 A. Yeah. So, no. No, I don't, because I've
25 picked up some new clients. But for, you know, which

1 ones I've provided declarations, some of them
2 I wouldn't list here at all, because even though I'm
3 engaged with a letter I haven't done any work for
4 them. So until I actually bill somebody I don't list
5 them down here.

6 Q. Have you done additional work for Netlist
7 since 2022?

8 A. Sure. There was a Micron trial that just
9 occurred.

10 Q. Anything else?

11 A. The effort on this IPR.

12 Q. Anything else?

13 A. Maybe. I don't recall. But, yeah,
14 I guess I'll just leave it at that.

15 Q. When did you start your work for Netlist
16 on this IPR?

17 A. I think it was sometime last fall, but
18 I would have to go back and check. I'm not certain
19 of that.

20 Q. And when you say, "I'd have to go back
21 and check," what would you have to check?

22 A. I would check my email and see when there
23 was first some discussion about the patent addressed
24 in this IPR.

25 Q. And that email is on the computer in

1 front of you?

2 A. I would believe so, yeah. Sure.

3 Q. Is your expert declaration marked as
4 Exhibit 2013 complete, meaning, does it provide a
5 complete statement of all the opinions you intend to
6 express in this matter, along with the basis and
7 reasons for those opinions?

8 A. I don't have any intention to express any
9 opinions at all.

10 Q. Could you say that again?

11 A. I don't have any intention to express any
12 opinions at all. I'll be asked questions and I'll do
13 my best to respond to those questions, but I don't
14 have a set of opinions that I intend to stand up and
15 express on my own, as I sit here today.

16 Q. That's a little bit different from the
17 question I asked.

18 I was asking about Exhibit 2013, and as
19 you see in paragraph 1 and paragraph 3, you talk
20 about your opinions, correct?

21 A. Yes. My recollection, though, is you
22 asked if 2013 contains all the opinions that I intend
23 to express. And I was answering that question or
24 doing my best to.

25 Q. Is your expert declaration marked as 2013

1 complete, meaning, does it provide a complete
2 statement of all the opinions you intend to express
3 in this matter, along with the basis and reasons for
4 those opinions?

5 A. I have no intention to express any
6 opinions in this matter. I will answer questions as
7 they come up. I'm not driving this. I'm just an
8 expert witness.

9 And if somebody asks my opinion and I've
10 stated it in my declaration and I have an opinion,
11 I'll do my best to answer that. If -- going forward,
12 if nobody asks my opinion, I have no intention of
13 expressing anything on my own.

14 Q. So what's your expert declaration marked
15 as Exhibit 2013? Does it create -- sorry, does it
16 reflect your opinions?

17 A. Yes, it does.

18 Q. And does it reflect all of the opinions
19 that you have in this matter, along with the basis
20 and reason for those opinions?

21 A. Probably not. But I can't think of
22 anything in particular that is missing from it as
23 I sit here. I intended to form my opinions and come
24 up with a thorough and sufficient response to the
25 arguments put forward in particular by Dr. Wedig.

1 You know, that doesn't mean I necessarily beat a dead
2 horse.

3 Q. In preparation for your deposition today,
4 did you find that Exhibit 2013 was missing any
5 opinions that you currently have related to this
6 matter?

7 A. No, nothing -- nothing occurred to me
8 that was missing.

9 Q. Is your expert declaration marked as
10 Exhibit 2013 accurate, meaning, it does not have any
11 mistakes as far as you're aware?

12 A. I know of one mistake that was pointed
13 out to me. There was an exhibit number that was
14 misnumbered. Beyond that, I'm not aware of any
15 errors in it.

16 Q. And can you tell me what exhibit number
17 was misnumbered?

18 A. I would be happy to. I'd have to turn to
19 my email. Is that okay? Just to look up that
20 number.

21 Q. Well, tell me this. I mean, did you
22 think that it was easy to figure out the mistake?

23 A. Yeah, I think so. I mean, there was
24 not -- compared to many other declarations and
25 reports I've written, there was not an extensive set

1 of exhibits referenced. And I think if anybody went
2 through it, they would probably pretty quickly notice
3 the typo or the error.

4 Q. And do you recall what exhibit it was?

5 A. No, I don't.

6 Q. I mean, not the number, but what the
7 subject matter of the exhibit was that was
8 misnumbered?

9 A. No, I don't.

10 Q. Do you have any present plans to correct
11 or supplement your expert declaration marked as
12 Exhibit 2013?

13 A. No, I do not. I don't even know if
14 that's possible. If it is, and counsel for Netlist
15 asks me to do that, I'd certainly be willing to do
16 that. I just don't know whether the procedures even
17 support it.

18 Q. Have you carefully read Netlist's
19 '608 patent marked as Exhibit 1001?

20 A. I have.

21 Q. Do you believe that you understand the
22 '608 patent marked as Exhibit 1001?

23 A. I do have an understanding of it, yes.

24 Q. Do you believe you understand the figures
25 in the '608 patent marked as Exhibit 1001?

1 A. I believe I have an understanding of
2 them, yes.

3 Q. And do you believe that you understand
4 the claims at the end of the '608 patent marked as
5 Exhibit 1001?

6 A. I have an understanding of them,
7 certainly.

8 Q. I'm going to put into the chat
9 Exhibit 1046.

10 (Exhibit 1046 was marked.)

11 BY MR. CHANDLER:

12 Q. Which is U.S. Patent Number 10,860,506,
13 sometimes referred to as the '506 patent. Let me
14 know when you have it in front of you.

15 A. Okay. I have it.

16 Q. The '506 patent marked as Exhibit 1046 is
17 a continuation of the '608 patent marked as
18 Exhibit 1001, as shown on the cover page of the
19 '506 patent, correct?

20 A. Yes, that's correct.

21 Q. And you have patents of your own,
22 correct?

23 A. Yes.

24 Q. And you previously provided testimony to
25 the patent office about the '506 patent, correct?

1 A. Yes, that's correct.

2 Q. I'm going to put into the chat
3 Exhibit 1076 which is a new exhibit.

4 (Exhibit 1076 was marked.)

5 BY MR. CHANDLER:

6 Q. It's your declaration on the '506 patent
7 dated January 31st, 2023, which was Exhibit 2006 in
8 IPR 2022-00711. Let me know when you have
9 Exhibit 1076 in front of you.

10 A. Okay. I have it in front of me.

11 Q. Is that your signature on the first page
12 of Exhibit 1076?

13 MR. LINDSAY: I'm going to object to the
14 introduction of this exhibit as beyond the scope
15 of his direct testimony.

16 THE WITNESS: Yes, that is my signature.

17 BY MR. CHANDLER:

18 Q. Did you declare that all statements made
19 in Exhibit 1076 based on your own knowledge are true
20 and that all statements made containing information
21 are believed to be true, correct?

22 A. Yes, that's what it says.

23 Q. Are you aware of any false statements or
24 testimony in Exhibit 1076 that you would like to
25 change?

1 MR. LINDSAY: Objection. Beyond the
2 scope.

3 THE WITNESS: Not that I recall, although
4 this was written more than a year and a half ago
5 and I haven't reviewed it since then.

6 BY MR. CHANDLER:

7 Q. As far as you recall, do you stand by
8 your declaration marked as Exhibit 1076?

9 MR. LINDSAY: Objection. Beyond the
10 scope.

11 THE WITNESS: Yes, as far as I recall.

12 BY MR. CHANDLER:

13 Q. I'm going to introduce a new exhibit,
14 1075, which is your deposition on the '506 patent
15 dated May 4th, 2023, which was Exhibit 1046 in
16 IPR 2022-00711.

17 (The Court Reporter requested
18 clarification.)

19 BY MR. CHANDLER:

20 Q. IPR 2022-00711. And let me know when you
21 have Exhibit 1075 in front of you.

22 (Exhibit 1075 was identified.)

23 THE WITNESS: I have it in front of me
24 now.

25 MR. LINDSAY: Object to this exhibit as

1 well.

2 BY MR. CHANDLER:

3 Q. At the bottom of page 8 of Exhibit 1075
4 and carrying over to the top of page 9 of
5 Exhibit 1075, you stated under penalty of perjury
6 that your testimony, your deposition, would be the
7 truth, the whole truth, and nothing but the truth,
8 correct?

9 MR. LINDSAY: Objection. Beyond the
10 scope of direct.

11 THE WITNESS: Yes, that's correct.

12 BY MR. CHANDLER:

13 Q. Are you aware of any false statements or
14 other testimony in Exhibit 1075 that you would like
15 to change?

16 MR. LINDSAY: Objection. Beyond the
17 scope of direct.

18 THE WITNESS: Not that I recall as I sit
19 here today.

20 BY MR. CHANDLER:

21 Q. And do you still stand by your testimony
22 in your deposition marked as Exhibit 1075?

23 MR. LINDSAY: Objection. Beyond the
24 scope of direct.

25 THE WITNESS: I see no reason to disavow

1 any of it, but I haven't reviewed it in more
2 than a year.

3 BY MR. CHANDLER:

4 Q. In your declaration marked as
5 Exhibit 1076, could you turn to the second page that
6 has the table of contents and let me know when you're
7 there?

8 A. I'm there.

9 Q. So in your declaration marked as
10 Exhibit 1076, on the second page, in the table of
11 contents, do you see in the middle that your
12 declaration talked about the '506 patent starting on
13 page 12, and then a little further down your
14 declaration talked about the Hiraishi reference
15 marked as 1005, the Butt reference marked as
16 Exhibit 1029, and the Tokuhiko reference marked as
17 Exhibit 1006?

18 A. Yes, I see that.

19 Q. Just for clarity, I will represent to you
20 that at the beginning of today's deposition, when
21 I gave you the Hiraishi reference marked as
22 Exhibit 1005, the Butt reference marked as
23 Exhibit 1029, and the Tokuhiko reference marked as
24 1006, those are the same exhibits in this IPR that
25 you discuss in your previous deposition marked as

1 Exhibit 1076 and in your previous deposition marked
2 as Exhibit 1075, understood?

3 A. Understood.

4 Q. And I'll also represent to you that the
5 '506 patent marked as Exhibit 1046 in this IPR is the
6 same as the '506 patent that was previously marked as
7 Exhibit 1001, in your previous declaration marked as
8 Exhibit 1076, and in your previous deposition marked
9 as Exhibit 1075, understood?

10 A. Understood.

11 Q. Have you carefully read the Hiraishi
12 prior art reference marked as Exhibit 1005?

13 A. Yes.

14 Q. Do you believe that you understand the
15 Hiraishi prior art reference marked as Exhibit 1005?

16 A. I have an understanding of it, certainly.

17 Q. Have you carefully read the Tokuhiko
18 prior art reference marked as Exhibit 1006?

19 A. Yes, I have.

20 Q. Do you believe that you understand the
21 Tokuhiko prior art reference marked as Exhibit 1006?

22 A. I believe that I have an understanding of
23 it, certainly.

24 Q. Have you carefully read the Butt
25 reference marked as Exhibit 1029?

1 A. Yes, I have.

2 Q. Do you believe that you understand the
3 Butt reference marked as Exhibit 1029?

4 A. Yes, I believe I have an understanding of
5 the Butt reference.

6 Q. Please turn to your expert declaration
7 marked as Exhibit 2013 and go to paragraph 35, and
8 let me know when you are there. It's on PDF page 21,
9 printed page 17.

10 (The Court Reporter requested
11 clarification.)

12 BY MR. CHANDLER:

13 Q. Printed page 17.

14 A. Okay.

15 Q. In your expert declaration marked as
16 Exhibit 2013, did you use July 2012 as the date for a
17 person of ordinary skill in the art for the
18 '608 patent?

19 A. Yes.

20 Q. Unless stated otherwise, could you please
21 answer my questions today from the perspective of a
22 person of ordinary skill in the art as of July 2012?

23 A. Yes, with regards to the '608 patent,
24 I will endeavor to do exactly that.

25 Q. And could you also please answer my

1 questions today in a way that is consistent with the
2 ordinary and custom meaning of words to a person of
3 ordinary skill in the art as of July 2012?

4 A. Yes, I will endeavor to do that with
5 regards to the '608 patent.

6 Q. And to be clear, I mean, we'll talking
7 about more than just the '608 patent.

8 So unless stated otherwise, will you
9 understand that my questions and your answers should
10 be from the perspective of a person of ordinary skill
11 in the art of the '608 patent as of July 2012?

12 A. No.

13 Q. Explain why not.

14 A. The question of what a POSITA would
15 understand with regards to --

16 (The Court Reporter requested
17 clarification.)

18 THE WITNESS: The word I used was POSITA,
19 a person of ordinary skill in the art, or
20 P-O-S-I-T-A.

21 So it's my understanding that that
22 concept with the date applies to the '608.
23 You've asked me a number of questions today that
24 I answer from my perspective today. And
25 I anticipate you might ask me more questions in

1 the future that don't really relate to any date
2 in 2012, let alone July.

3 So certainly with regards to '608
4 technology, or any other question where it's
5 clear, you make it clear to me that you want me
6 to answer from the point of view of a POSITA as
7 of that date, I will endeavor to answer from
8 that perspective.

9 BY MR. CHANDLER:

10 Q. And that's what I'm doing right now. I'm
11 trying to make it clear to you that, from this point
12 on, all of my questions and all of your answers
13 should be from the perspective of a person of
14 ordinary skill in the art, what you refer to as a
15 POSITA, or POSITA, as of July 2012, understood?

16 A. Understood.

17 Q. In paragraphs 35 and 36 of your expert
18 declaration marked as Exhibit 2013, you state that
19 you adopted Samsung's proposed level of skill for a
20 person of ordinary skill in the art as stated in the
21 petition starting on page 2, correct?

22 A. Yes, that's what it says.

23 Q. And then you should have the petition in
24 the chat. So could you pull up the petition, it's
25 paper number 1, and go to page 2 where it talks about

1 person of ordinary skill in the art, and let me when
2 you're there?

3 A. Okay.

4 Q. And so you see that on page 2 of
5 Samsung's petition marked as paper number 1, carrying
6 over to the top of page 3, there's a section that
7 provides person of ordinary skill in the art,
8 correct?

9 A. Yes, I see that.

10 Q. For purposes of this IPR, do you agree
11 that a person of ordinary skill in the art would have
12 been familiar with the JEDEC industry standards,
13 correct?

14 A. I have -- let me see. For the purposes
15 of my analysis and opinions stated here, yes, she
16 would have been familiar with the JEDEC industry
17 standards.

18 Q. For purposes of this IPR, do you agree
19 that a person of ordinary skill in the art would have
20 been knowledgeable about the design and operation of
21 computer memories, including DRAM and SDRAM devices
22 that were compliant with various standards and how
23 they interact with other components of the computer
24 system, such as memory controllers, correct?

25 A. Yes, that is correct.

1 Q. For purposes of this IPR, you agree that
2 a person of ordinary skill in the art would also have
3 been familiar with the structure and operation of
4 circuitry used to access and control computer
5 memories and other components of a memory system,
6 including sophisticated circuits such as ASICs and
7 CPLDs, as well as low-level circuits, such as data
8 buffers, tri-state buffers, flip-flops, and
9 registers, correct?

10 A. Yes, that's correct.

11 Q. And at a high level, what is an ASIC?

12 A. That is an acronym that stands for
13 application-specific integrated circuit.

14 Q. And at a high level, what's a CPLD?

15 A. That, at a high level, it's an acronym
16 standing for complex programmable logic devices.

17 Q. And from a general standpoint, what are
18 some common situations in which a person of ordinary
19 skill in the art would use an ASIC or a CPLD?

20 MR. LINDSAY: Objection. Form.

21 THE WITNESS: If they were designing
22 circuitry for which there was not an
23 on-the-market available solution with some
24 moderately high level of digital electronics in
25 such circuitry where they desired to incorporate

1 the circuits in a single package, perhaps
2 because they anticipated ultimately selling it
3 in a single package.

4 BY MR. CHANDLER:

5 Q. And at a high level, what design choices
6 would lead a person of ordinary skill in the art to
7 use an ASIC rather than a CPLD, or vice versa?

8 MR. LINDSAY: Objection. Form.

9 THE WITNESS: There are a wide range of
10 cost and performance benefits. An ASIC will
11 generally be more expensive and have -- it has
12 more expensive startup and design costs. For
13 long-running production, it may ultimately end
14 up being less expensive than a CPLD.

15 A CPLD tends to have a lower performance
16 ceiling and will generally consume more power,
17 but is realizable with a shorter time schedule.

18 BY MR. CHANDLER:

19 Q. And could you explain just a little bit
20 more what you mean by a CPLD is realizable with a
21 shorter time schedule?

22 A. Yes. CPLDs are programmed whereas ASICs
23 are designed circuitry. So depending on what -- the
24 specific details of a CPLD that's used, the circuitry
25 that they implement can be designed and programmed

1 into them instantaneously or within a few minutes.

2 Q. At a high level, what is a tri-state
3 buffer?

4 A. A tri-state buffer is -- provides an
5 isolation gate, I would say, interrupting a signal
6 line so that the signal on an input side can be
7 selectively blocked from moving forward and the
8 output -- on the output line.

9 And when it is blocked, the output state
10 is in what we call a high-Z state such that it will
11 not adversely affect signals generated by other
12 circuitry to which it is directly linked.

13 Q. And I assume a tri-state buffer has three
14 states, so how would you characterize what those
15 three states are?

16 A. So, generally, that would be called zero
17 or off, 1 or on, and then the high-Z state that
18 I just mentioned.

19 Q. And does the tri-state buffer have a
20 control signal that turns on and off the high-Z
21 state?

22 MR. LINDSAY: Objection. Form.

23 THE WITNESS: Yeah. I think that's a
24 reasonable characterization. There's an
25 input -- there's a signal input, there's a

1 signal output, and then there is a third wire,
2 which is an input and is essentially a control
3 input for activating or deactivating the high-Z
4 state.

5 BY MR. CHANDLER:

6 Q. I have sometimes heard the phrase "high
7 impedance." Is that the same thing as the high-Z
8 state or something else?

9 A. That is the high-Z state, yes.

10 Q. And what are some common situations in
11 which a person of ordinary skill in the art would
12 want to use a tri-state buffer and would want to use
13 the high-Z state?

14 MR. LINDSAY: Objection. Form.

15 THE WITNESS: So the buffers that can be
16 turned on or off in one mode or another are
17 particularly useful in situations for power
18 savings where, if you have no intention to
19 actually drive a signal from one location to
20 another, it makes sense to not accidentally drive
21 that and consume power.

22 Now, the specific form of a tri-state
23 buffer is useful when you want to have multiple
24 output sources connected together and you need
25 to avoid a situation where one of them is trying

1 to drive a wire to the state zero and another
2 one is trying to drive a wire to the state 1.

3 Well, what state will the single physical
4 wire be in? It's difficult to say. It's a bad
5 design choice. And as an engineer, you need to
6 try to avoid those situations.

7 So there should only be one that is
8 actually on at any point in time. And you use
9 the tri-state buffer to make sure that only one
10 of them is on and actively driving a signal at
11 any particular point in time.

12 BY MR. CHANDLER:

13 Q. And what's a collision? Have you heard
14 the term "collision"?

15 MR. LINDSAY: Objection. Form.

16 THE WITNESS: Yeah, I have. It means
17 different things in different contexts. But one
18 might refer to buffers connected together as
19 colliding if they're trying to drive a common
20 output to a contradictory state.

21 BY MR. CHANDLER:

22 Q. And can a tri-state buffer be used to
23 avoid collisions and, if so, how?

24 A. I thought we just discussed that. But,
25 sure, a tri-state buffer --

1 Q. That's fine. If that's what you were
2 trying to say, that's --

3 A. Yeah, that's what I was trying to say.
4 Yeah.

5 Q. At a high level, what is a flip-flop?

6 A. A flip-flop is a -- usually a single-bit
7 memory device.

8 Q. Are you done?

9 A. Yes, I'm done. Yeah. It's a very
10 high-level description, but, yeah.

11 Q. What are some common situations in which
12 a person of ordinary skill in the art would use a
13 flip-flop?

14 A. If there's a piece of information that
15 the circuit needs to retain for a period of time,
16 particularly if that retention extends beyond the
17 time when that information was first presented to the
18 circuit.

19 Q. At a high level, what is a register?

20 A. A register is a circuit that holds
21 information for some period of time. People
22 sometimes think of flip-flops as single-bit
23 registers. But usually when I hear people talk about
24 registers, I'm inclined to think of multiple bits.

25 Q. So multiple flip-flops in the register,

1 is that what you're trying to say?

2 A. Sometimes it's multiple flip-flops.
3 Sometimes a register is built with different memory
4 circuitry.

5 Q. What are some common situations in which
6 a person of ordinary skill in the art would use a
7 register?

8 MR. LINDSAY: Objection. Form. Outside
9 the scope of direct.

10 THE WITNESS: Certainly, they would use a
11 register in the circumstances where they would
12 use a flip-flop. If -- yeah, there's just such
13 a wide range of different types of registers.
14 They're used in central processing units, CPUs,
15 to hold very complex, sophisticated data in an
16 organized manner. That's very different from
17 using a flip-flop as a register, for example.

18 BY MR. CHANDLER:

19 Q. I think you said at a high level that
20 both a flip-flop and a register can store a bit of
21 data for a period of time; is that correct?

22 MR. LINDSAY: Objection. Misstates prior
23 testimony. Outside the scope of direct.

24 THE WITNESS: I'm not looking at the
25 real-time, but that sounds consistent with my

1 understanding, sure.

2 BY MR. CHANDLER:

3 Q. And how is that period of time
4 determined?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct. And form.

7 THE WITNESS: That period of time is
8 determined by the circuitry surrounding the
9 register or flip-flop which provides, depending
10 on the exact implementation of the register or
11 flip-flop, various control signals.

12 BY MR. CHANDLER:

13 Q. So can you explain a little bit more how
14 a flip-flop or register would retain a bit of data
15 for a period of time?

16 MR. LINDSAY: Objection. Outside the
17 scope of direct.

18 THE WITNESS: Well, in the context of a
19 CPU register, an instruction would be executed
20 that wrote some data into a register in the
21 general purpose register file.

22 So the instruction might say, for
23 example, write the value of 5 into register
24 three. And then that value of 5 would be in
25 register three going forward until power was

1 removed or a different instruction was executed
2 to write a different piece of data into register
3 three.

4 BY MR. CHANDLER:

5 Q. And how does data come out of flip-flop
6 or register after a period of time?

7 MR. LINDSAY: Objection. Outside the
8 scope of direct.

9 THE WITNESS: Well, in the context of a
10 general purpose register file and a CPU, an
11 instruction needs to be executed that -- in my
12 experience, that reads that data out. So it's
13 stored in the register file and, subsequently,
14 it has to be read out in order to be used.
15 Reading it out does not destroy the information.
16 It's still in the registry file.

17 For a flip-flop, once the data is stored
18 in a flip-flop, it's immediately available on
19 the output.

20 BY MR. CHANDLER:

21 Q. And is the answer that you just gave
22 applicable to the field of art of the '608 patent?

23 A. I believe so, in general, yeah. I will
24 say, there are a wide range of flip-flops, some of
25 which have some delay on the output. But when they

1 do, it's usually very small, like, half a clock cycle
2 or a clock cycle, and that are programmed in slightly
3 different ways.

4 Q. And is that true for registers as well?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct.

7 THE WITNESS: I think it's less true.
8 There's less variability in the sort of general
9 purpose registers for a CPU that I have been
10 speaking about.

11 BY MR. CHANDLER:

12 Q. What about, again, in the context of the
13 field of art in the '608 patent?

14 MR. LINDSAY: Objection. Form. Outside
15 the scope of direct.

16 THE WITNESS: I --

17 BY MR. CHANDLER:

18 Q. Just for clarity, I mean, in my review of
19 the '608 patent I didn't see that it was talking
20 about general purpose CPUs. The '608 patent field of
21 art seemed more along the lines of memory modules, as
22 stated on, you know, page 2 of the petition where it
23 defines a person of ordinary skill in the art that
24 you use for this IPR.

25 So I just want to make sure that we're

1 still talking about the field of art for the
2 '608 patent when you're giving your answers.

3 A. Sure. The field of art relates to
4 general purpose register files as well. Yeah,
5 I don't see any disagreement with that.

6 Q. So just to follow up, you seemed to
7 suggest there's less variability with respect to
8 registers than with flip-flops. What did you mean by
9 that?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct.

12 THE WITNESS: The general purpose
13 register files in the context of a CPU that
14 I was referring to generally have -- they -- the
15 data gets stored into it and read from it, and
16 the registers have an address.

17 As opposed to flip-flops, where there can
18 be what are called D flip-flops or T flip-flops.
19 They can have an erase line or they might not
20 have an erase lines. That tends to be --
21 they're lower-level structures that tend to have
22 more variability.

23 BY MR. CHANDLER:

24 Q. At a high level, what's a memory device
25 and what's a memory module?

1 A. At a high level, a memory device -- well,
2 it depends on the specific context. One could
3 certainly say a single DRAM, dynamic random access
4 memory chip, is a memory device.

5 In the context of what -- one could say
6 that if that chip, that what we -- that package
7 device has multiple silicon chips in it, one might
8 say that each one is a memory device.

9 From another perspective, one might say
10 that the entire module on a dual in-line memory
11 module, sometimes pronounced DIMM, is a memory
12 device, but that's less common.

13 I think a memory module is a -- is
14 generally a component that has memory devices on it
15 and communicates with a host memory controller for
16 its operation.

17 Now, there generally has been, I believe,
18 an agreed upon construction for memory module, to the
19 best of my recollection, among the parties in
20 litigation on this matter.

21 So I'm not trying to provide that
22 construction, although I think that was the
23 appropriate construction, in part, because I don't
24 have it, you know, in front of me. I don't remember
25 exactly how it was phrased.

1 Q. Are there JEDEC standards for memory
2 devices and for memory modules?

3 A. Yes, there are.

4 Q. I'm going to put in the chat
5 Exhibit 2014, which is the JEDEC standard JESD79-2F
6 (indecipherable) --

7 (The Court Reporter requested
8 clarification.)

9 BY MR. CHANDLER:

10 Q. JEDEC standard JESD79-2F for DDR2 memory
11 devices. And this exhibit was previously marked as
12 Exhibit 2002 in IPR 2022-00711.

13 Do you have Exhibit 2014 in front of you?

14 A. I do.

15 (Exhibit 2014 was identified.)

16 BY MR. CHANDLER:

17 Q. And in your opinion, would a person of
18 ordinary skill in the art have known about
19 Exhibit 2014, the JEDEC standard for DDR2 memory
20 devices?

21 A. I would expect they would have some
22 familiarity with it.

23 Q. Let me put in the chat Exhibit 2015,
24 which is the JEDEC standard JESD79-3F for DDR3 memory
25 devices, which I'll note was previously marked as

1 Exhibit 2003 in IPR 2022-00711.

2 (Exhibit 2015 was identified.)

3 BY MR. CHANDLER:

4 Q. Do you have Exhibit 2015 in front of you?

5 A. Not yet. Okay. There it is. I've got
6 it now.

7 Q. In your opinion, would a person of
8 ordinary skill in the art have known about the JEDEC
9 standard JESD79-3F for DDR3 memory devices marked as
10 Exhibit 2015?

11 A. I would expect they would be aware of it,
12 yes.

13 Q. Let me put another exhibit in the chat.
14 It's Exhibit 2018, the JEDEC standard JESD79 for DDR
15 memory devices, which I'll note for the record was
16 previously marked as Exhibit 2010 in IPR 2022-00711.

17 And let me know when you've got
18 Exhibit 2018 in front of you.

19 (Exhibit 2018 was identified.)

20 THE WITNESS: Okay. I have it in front
21 of me now.

22 BY MR. CHANDLER:

23 Q. And in your opinion, would a person of
24 ordinary skill in the art have known about the JEDEC
25 standard JESD79 for DDR memory devices marked as

1 Exhibit 2018?

2 A. Yes, I expect that they would have some
3 familiarity with it.

4 Q. Let me put in the chat Exhibit 2019 which
5 is the JEDEC standard JESD79-3A for DDR3 memory
6 devices. And I'll note that this was previously
7 marked as Exhibit 2011 in IPR 2022-00711. And let me
8 know when you have Exhibit 2019 in front of you.

9 A. Will do. Okay. I have it in front of me
10 now.

11 (Exhibit 2019 was identified.)

12 BY MR. CHANDLER:

13 Q. In your opinion, would a person of
14 ordinary skill in the art have known about
15 Exhibit 2019, the JEDEC standard JESD79-3A for DDR3
16 memory devices?

17 A. I expect that a person of ordinary skill
18 in the art -- sorry about that. I don't know if you
19 heard, there was an incoming phone call.

20 I would expect that a person of ordinary
21 skill in the art would have been aware of this
22 specification.

23 Q. And I think I previously gave to you
24 Exhibit 1020, but if not, I'll put in the chat
25 Exhibit 1020, which is a JEDEC standard JESD79-3C for

1 DDR3 memory devices, which was also marked as
2 Exhibit 1020 in IPR 2022-0071 --

3 (The Court Reporter requested
4 clarification.)

5 BY MR. CHANDLER:

6 Q. Exhibit 1020 is JEDEC standard JESD79-3C
7 for DDR3 memory devices, and it was also marked as
8 Exhibit 1020 in IPR 2022-00711.

9 Do you have Exhibit 1020 in front of you?
10 (Exhibit 1020 was identified.)

11 THE WITNESS: Yes, I do.

12 BY MR. CHANDLER:

13 Q. And do you believe a person of ordinary
14 skill in the art would have known about Exhibit 1020,
15 the JEDEC standard JESD79-3C for DDR3 memory devices?

16 A. Yes. I think a person of ordinary skill
17 in the art would have been aware of JESD79-3C for
18 DDR3 SDRAMs.

19 Q. Putting in the chat Exhibit 1059, which
20 is the JEDEC standard JESD82-20 for FBDIMM, which is
21 a new exhibit in this IPR, was previously marked as
22 Exhibit 1053 in IPR 2022-00711.

23 And let me know when you have
24 Exhibit 1059 in front of you.

25 (Exhibit 1059 was marked.)

1 MR. LINDSAY: I'm going to object to the
2 exhibit.

3 THE WITNESS: I have it in front of me
4 now.

5 BY MR. CHANDLER:

6 Q. Do you believe a person of ordinary skill
7 in the art would have known about Exhibit 1059 the
8 JEDEC standard JESD82-20 for FBDIMM advanced memory
9 buffer?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct.

12 THE WITNESS: So I believe a person of
13 ordinary skill in the art would have been
14 somewhat less likely to be familiar with or to
15 know, to be aware of this document in general,
16 and in particular, anything disclosed in it,
17 JESD82-20, in comparison, for example, to the --
18 I think all the ones we have looked at thus far,
19 the -- particularly the ones related to DDR3
20 memories, because the FBDIMMs were a particular
21 class of memory modules that were much less
22 used, designed, known.

23 But to the extent that this is a JEDEC
24 standard regarding DIMMs, I would expect that a
25 person of ordinary skill in the art would likely

1 at least be aware that it existed.

2 BY MR. CHANDLER:

3 Q. Let me put in the chat Exhibit 1018.

4 (Exhibit 1018 was identified.)

5 BY MR. CHANDLER:

6 Q. Which is the JEDEC standard 21-C for
7 RDIMM memory modules. And I'll note for the record
8 this was also marked as Exhibit 1018 in IPR
9 2022-00711.

10 Do you have Exhibit 1018 in front of you?

11 A. I do.

12 Q. And do you believe a person of ordinary
13 skill in the art would have known about Exhibit 1018,
14 the JEDEC standard 21-C for RDIMM memory modules?

15 A. This seems to just be a portion of the
16 JEDEC -- an excerpt from a JEDEC specification, if
17 I'm reading it right.

18 But given that it is a JEDEC document
19 related to DDR DIMMs dated 2002, I would expect a
20 person of ordinary skill in the art would likely have
21 been aware of it.

22 MR. CHANDLER: Why don't we take our
23 first break. Off the record.

24 THE VIDEOGRAPHER: Off the record at
25 10:08 a.m. Pacific time.

1 (A recess was taken.)

2 THE VIDEOGRAPHER: On the record at
3 10:15 a.m. Pacific time.

4 BY MR. CHANDLER:

5 Q. Dr. Mangione-Smith, can you please
6 confirm that during the break you did not talk with
7 counsel or anyone else about the substance of your
8 testimony so far today?

9 A. I did not talk to counsel or anyone else
10 with regards to my testimony today.

11 Q. And do you have any corrections or
12 clarifications you'd like to make to any of your
13 earlier testimony today?

14 A. No, I do not.

15 Q. I'd like to introduce a new exhibit
16 number which will be 1077.

17 (Exhibit 1077 was marked.)

18 BY MR. CHANDLER:

19 Q. It's Netlist's technology tutorial, which
20 was previously marked as Exhibit 1047 in IPR
21 2022-00711. Let me know when you have Exhibit 1077
22 in front of you.

23 A. I have it open in front of me now.

24 MR. LINDSAY: I'm going to object to the
25 exhibit as well.

1 BY MR. CHANDLER:

2 Q. Dr. Mangione-Smith, you have seen the
3 technology tutorial marked as Exhibit 1077 before,
4 correct?

5 A. Likely. It looks familiar, somewhat
6 familiar, yes.

7 Q. Turn to page 3 of Exhibit 1077 and let me
8 know when you're there.

9 A. I'm there.

10 Q. Do you generally agree a person of
11 ordinary skill in the art would have understood that
12 SDRAM emerged in the 1990s, were standardized by
13 JEDEC, and evolved in several generations, including
14 DDR, DDR2, and DDR3?

15 MR. LINDSAY: Objection. Outside the
16 scope of direct. And form.

17 THE WITNESS: I don't have any particular
18 recollection regarding the dates.

19 BY MR. CHANDLER:

20 Q. But a person of ordinary skill in the art
21 would have understood what SDRAM was, that it was
22 standardized by JEDEC, and that it involved in
23 several generations, including DDR, DDR2, and DDR3,
24 correct?

25 MR. LINDSAY: Objection. Form.

1 THE WITNESS: I think that's generally
2 accurate.

3 BY MR. CHANDLER:

4 Q. Please turn to page 5 of Exhibit 1077.
5 Let me know when you're there.

6 A. Okay. I'm there.

7 Q. Do you agree that a person of ordinary
8 skill in the art understood that a rank is a set of
9 DRAMs that are written to or read from together?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct.

12 THE WITNESS: Yeah, I think that a person
13 of ordinary skill in the art would have a
14 general understanding that a rank is a set of
15 DRAMs that are written to or read from together.

16 BY MR. CHANDLER:

17 Q. And would it be fair to say page 5 of
18 Exhibit 1077 illustrates the concept of two ranks,
19 highlighted in green and red, where each of those
20 ranks comprises eight DRAM memory devices where each
21 DRAM memory device is 8 bits wide, resulting in each
22 rank of memory devices having a total bit width of
23 64 bits?

24 MR. LINDSAY: Objection. Outside the
25 scope of direct.

1 THE WITNESS: Yes, I think a person of
2 ordinary skill in the art looking at this figure
3 would have an understanding of that.

4 BY MR. CHANDLER:

5 Q. And do you agree that a person of
6 ordinary skill in the art would understand that DQ
7 refers to a data line?

8 A. Yes. That is a convention that is often
9 used to indicate a data line, particularly a data
10 line connected to a memory controller.

11 Q. And as an example, do you agree that a
12 memory controller can read or write 64 bits at a time
13 using 64 DQ data lines?

14 A. If it is a memory controller configured
15 as is generally shown here, I would anticipate this
16 is indicating that there would be 64 DQ lines
17 connected to the memory controller. Of course, there
18 are other types of memory controllers with somewhat
19 different data bus widths.

20 Q. And do you agree a person of ordinary
21 skill in the art understood that DQ data lines
22 typically are bidirectional, meaning, that the same
23 DQ data line used for reading data can also be used
24 at a later time for writing data, and vice versa?

25 A. I think it depends on the specific

1 context. There are memory systems where the data
2 lines are not bidirectional.

3 Q. But there are also memory systems,
4 including JEDEC standardized memory modules, where
5 the DQ data lines are bidirectional, meaning, the
6 same DQ data line used to read data can also be used
7 to write data, correct?

8 A. Indeed. JEDEC does define memory modules
9 where the DQ lines are bidirectional.

10 Q. Please turn to page 6 of Exhibit 1077.
11 Let me know when you're there.

12 A. I'm there.

13 Q. Do you agree that a person of ordinary
14 skill in the art understood that DQS refers to a data
15 strobe signal?

16 MR. LINDSAY: Objection. Outside the
17 scope of direct as it relates to the exhibit.

18 THE WITNESS: Yes. It's my
19 understanding, particularly in the context of
20 the JEDEC standards, that a signal named DQS is
21 often used to refer to a strobe signal for
22 controlling use of the data on the DQ lines.

23 BY MR. CHANDLER:

24 Q. And one nanosecond is one billionths of a
25 second, correct?

1 A. I don't recall. I wouldn't -- I wouldn't
2 say it wasn't. I just don't recall.

3 Q. All right. Let's --

4 A. I'm sorry. It says it right there.
5 I assume that's accurate.

6 Q. Do you agree that DDR3 memory devices use
7 a clock speed that was faster than the clock speed
8 for DDR2 memory devices, which, in turn, used a clock
9 speed that was faster than the clock speed for DDR1
10 memory devices?

11 A. I haven't looked at DDR2 or DDR1 much
12 recently at all.

13 I would say that, in my experience,
14 I would expect that these DDR technologies generally
15 have a range of clock speeds over which they can
16 operate. And it's fairly typical for the low range
17 of a new generation to overlap the high range of a
18 previous one, which is to say, does DDR3, for
19 example, have a higher clock rate than DDR2?

20 I believe it supports a higher clock rate. But it
21 could be programmed to work at a lower clock rate,
22 I believe, than a high-end DDR2 module would support.

23 Q. Could you turn back to Exhibit 2015 and
24 let me know when you have it in front of you? That's
25 the JEDEC standard for DDR3 memory devices.

1 A. I have in front of me now.

2 Q. And go to page 141 of Exhibit 2015, which
3 is PDF page 155, and let me know when you're there.

4 A. Okay. I'm there.

5 Q. Page 141 of the DDR3 standard marked as
6 Exhibit 2015 shows clock periods labeled tCK ranging
7 from 2.5 nanoseconds in the upper left to
8 0.938 nanoseconds in the middle on the right,
9 correct?

10 A. Yes, that appears to be correct.

11 Q. So the fastest clock period shown on this
12 page of the DDR3 standard marked as Exhibit 2015 is
13 less than one nanosecond, which is less than one
14 billionths of a second, correct?

15 A. Yes, that appears to be correct.

16 Q. And according to this page, a DDR3 memory
17 device with a clock period of 2.5 nanoseconds can
18 operate at a speed of 800 megahertz, correct?

19 A. (No audible response.)

20 Q. And while a DDR3 memory device with a
21 clock period of 1.25 nanoseconds can operate at a
22 speed of 1600 megahertz and a DDR3 memory device with
23 a clock speed of 0.938 nanoseconds can operate at a
24 speed of --

25 (The Court Reporter requested

1 clarification.)

2 BY MR. CHANDLER:

3 Q. 0.9385 nanoseconds can operate at a speed
4 of 2133 megahertz; is that fair?

5 A. Yeah, I don't recall.

6 MR. LINDSAY: Objection. Form.

7 BY MR. CHANDLER:

8 Q. As shown at the top of the column for
9 each of those clock periods?

10 A. Yeah, my recollection is that notation
11 refers to mega transactions per second, which, in a
12 perfect world, which is actually impossible to meet,
13 that might be equivalent to the operating megahertz.
14 I simply don't recall.

15 Q. And 2133 megahertz can also be referred
16 to as 2.133 gigahertz; is that fair?

17 A. Yes, I would agree with that.

18 Q. All right. Turn back to Exhibit 1077 and
19 go to page 7 and let me know when you're there.

20 A. Okay.

21 Q. Do you agree that page 7 of Exhibit 1077
22 illustrates an unbuffered DIMM, also known as a
23 UDIMM?

24 MR. LINDSAY: Objection. Outside the
25 scope of direct.

1 THE WITNESS: It is labeled UDIMM. And
2 at a very high level, I do believe it represents
3 a view of an unbuffered DIMM, or UDIMM.

4 BY MR. CHANDLER:

5 Q. And you agree a person of ordinary skill
6 in the art understood what a UDIMM memory module is?

7 MR. LINDSAY: Objection. Outside the
8 scope of direct as it relates to the exhibit.

9 THE WITNESS: Yes. I believe that they
10 would have at least been aware of JEDEC
11 publishing specifications related to UDIMMs.

12 BY MR. CHANDLER:

13 Q. And at a high level, would it be fair to
14 say that a UDIMM typically has bidirectional data
15 lines between the memory controller and the memory
16 devices, but there's no buffer anywhere along those
17 bidirectional data lines?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct. And form.

20 THE WITNESS: I think it's fair to say
21 that the UDIMMs are generally understood to have
22 bidirectional data lines and not requiring any
23 buffers beyond whatever is present inside the
24 DRAM chips themselves.

25

1 BY MR. CHANDLER:

2 Q. So there's no additional buffer on the
3 UDIMM memory module along the bidirectional data
4 lines; is that fair?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct.

7 THE WITNESS: I -- I think that that's
8 fair.

9 BY MR. CHANDLER:

10 Q. On page 8 of Exhibit 1077, do you agree
11 that illustrates a registered DIMM, also known as an
12 RDIMM?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE WITNESS: Yes. Page 8 illustrates a
16 connection between a memory controller and a
17 JEDEC registered DIMM, or RDIMM, at a very high
18 level.

19 BY MR. CHANDLER:

20 Q. And do you agree a person of ordinary
21 skill in the art understood what an RDIMM memory
22 module was?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct.

25 THE WITNESS: Yes. I believe they would

1 have been aware of the concept of an RDIMM.

2 BY MR. CHANDLER:

3 Q. And would it be fair to say that an RDIMM
4 memory module has a register on the module that
5 buffers the address command and clock signals from
6 the memory controller, but the RDIMM memory module
7 does not have any additional buffers on the memory
8 module for buffering any of the bidirectional data
9 lines?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct. And form.

12 THE WITNESS: I think that that's a
13 reasonable characterization, with the caveat
14 that there are buffers built into the DRAM chips
15 themselves. But at a high level, there's no
16 additional buffering on the DQ data lines.

17 BY MR. CHANDLER:

18 Q. Or on the DQS strobe lines, correct?

19 MR. LINDSAY: Objection. Outside the
20 scope of direct.

21 THE WITNESS: That's correct. The DQS
22 strobe lines have no additional buffering beyond
23 what would be present in the DRAM chips
24 themselves.

25

1 BY MR. CHANDLER:

2 Q. On page 9 of Exhibit 1077, do you agree
3 that illustrates a fully buffered DIMM, also known as
4 an FBDIMM?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct.

7 THE WITNESS: Yes. My understanding is
8 that page 9 illustrates a memory controller
9 interfacing to a fully buffered DIMM, or an
10 FBDIMM.

11 BY MR. CHANDLER:

12 Q. And an FBDIMM has an AMB, advanced memory
13 buffer, on the module, correct?

14 MR. LINDSAY: Objection. Outside the
15 scope of direct.

16 THE WITNESS: Yes. Under the JEDEC
17 specification for an FBDIMM there is a component
18 called an AMB present on a fully buffered DIMM.

19 BY MR. CHANDLER:

20 Q. And so, for example, Exhibit 1059 that we
21 looked at a moment ago is the JEDEC standard that
22 corresponds to the AMB, advanced memory buffer, for
23 an FBDIMM such as what's illustrated at a high level
24 on page 9 of Exhibit 1077; is that fair?

25 MR. LINDSAY: Objection. Outside the

1 scope of direct.

2 THE WITNESS: I would say that's fair to
3 the extent that we did look at the FBDIMM
4 specification. I don't recall what exhibit
5 number it was, but I have no reason to doubt
6 your accuracy there.

7 BY MR. CHANDLER:

8 Q. And would it be fair to say at a high
9 level that an FBDIMM buffer is all of the signals on
10 the memory module using the AMB, advance memory
11 buffer, so that would include the address command and
12 clock signals from the memory controller, as well as
13 all of the data signals on the bidirectional data
14 lines?

15 MR. LINDSAY: Objection. Outside the
16 scope of direct. And form.

17 THE WITNESS: I think that's likely the
18 case, but it's been quite a long time since
19 I looked at the FBDIMM specification in any
20 detail. That certainly seems to be indicated by
21 this figure.

22 BY MR. CHANDLER:

23 Q. Please turn to the '608 patent marked as
24 Exhibit 1001 and let me know when you're there. And
25 go to column 9.

1 A. Okay.

2 Q. And why don't you just read to yourself
3 real quickly, or refresh your recollection, column 9,
4 line 63, just a couple sentences to column 10,
5 line 6, and let me know when you've just read that
6 yourself again.

7 A. All right. I've reviewed that portion.

8 Q. According to the '608 patent marked as
9 Exhibit 1001, when the clock speed is 800 megahertz,
10 the clock cycle time is less than 1.2 nanoseconds,
11 resulting in a signal that travels about 15
12 centimeters during one clock cycle, correct?

13 A. Yes, that's what it says.

14 Q. And my understanding is that
15 15 centimeters is a little bit less than six inches.
16 Does that sound about right to you?

17 A. Let's see. Sure. It's less than
18 six inches.

19 Q. And according to the '608 patent marked
20 as Exhibit 1001, when the clock speed is
21 1600 megahertz, then a signal travels less than eight
22 centimeters during one clock cycle, correct?

23 A. Yes.

24 Q. And my understanding is that
25 eight centimeters is around three inches; does that

1 sound fair?

2 A. That sounds fair.

3 Q. And so according to the '608 patent
4 marked as Exhibit 1001, as you get to these faster
5 clock speeds, which I believe are consistent with
6 some of the clock speeds we were looking at for DDR3
7 memory devices, a module control signal line can have
8 multiple module control signals on the line at the
9 same time, i.e., before one module control signal
10 reaches an end of the signal line, another module
11 control signal appears on the signal line, correct?

12 A. Yes, I see that it says that.

13 Q. Does that make sense to you?

14 A. It does if the module control signals are
15 being sent on every clock signal.

16 Q. Take a look at Figure 2C of the
17 '608 patent marked as Exhibit 1001, and let me know
18 when you're there.

19 A. Okay. I'm there.

20 Q. Figure 2C of the '608 patent marked as
21 Exhibit 1001 shows a memory module with a module
22 controller in the middle identified as 116, and then
23 there are big arrows off to the left and to the right
24 representing control address and clock signals,
25 correct?

1 A. Yes, I think that's accurate.

2 Q. And as we just discussed a moment ago, at
3 faster clock speeds, such as the higher clock speeds
4 permitted by the standard for DDR3 memory devices,
5 the control address and clock signals sent from the
6 module controller in the middle of the memory module
7 may not reach the left and the right sides of the
8 memory module before the next set of control address
9 and clock signals are sent by the module controller
10 on the next clock cycle, correct?

11 A. I would have to look deeper. I'm not
12 sure that that's accurate. That's accurate with
13 regards to the clock signal, at least.

14 Q. And what's your concern, or what would
15 you have to look deeper into?

16 A. Well, for example, there -- if the memory
17 controller is doing a read or a write, there's one
18 read or write command. So they'll -- so, yeah,
19 they'll be one read or write command that will
20 cover -- operate over multiple clock signals. So
21 that command only needs to be sent once.

22 It's possible that looking at the
23 protocol, in some cases, there would be a subsequent
24 related command that would be sent on the next clock
25 cycle. As I sit here, I don't see the need for it,

1 but it's possible.

2 Similarly, the address signals, if the
3 host memory controller is going to want to address a
4 single location in memory, in principle, if you
5 deliver that address in one clock cycle, you won't
6 have another read or write transaction to a different
7 address until quite some time in the future.

8 Q. I think I understood what you're saying,
9 which is the clock signal will always be sent once
10 every clock period, in which case, at the higher
11 speeds, there can be a second clock signal being sent
12 out before the first clock signal has reached the
13 left or right side of the memory module. Whereas,
14 for control and address signals, you may or may not
15 need to send those every clock cycle, so it may or
16 may not be the case that you have control and address
17 signal being sent out before the previous control and
18 address signal has reached the left or right side of
19 the memory module; is that fair?

20 A. That's right. I need to look through the
21 timing diagrams to verify that one way or the other.
22 This concept is sometimes referred to as wire
23 pipelining because when -- there's multiple signals
24 on one wire at a time.

25 Q. And both you and Dr. Wedig have used the

1 term "fly-by delay" and "flight time delay."

2 What do you mean by those two terms? And
3 when you use those two terms, are you generally
4 trying to refer to the same thing or are you trying
5 to draw a distinction when you use one term or the
6 other term?

7 MR. LINDSAY: Objection. Form.

8 THE WITNESS: I think that I've tried to
9 use them consistently to cover the same concept.

10 BY MR. CHANDLER:

11 Q. What that's concept?

12 A. So when a signal like a right command is
13 sent from the memory controller -- these figures can
14 be a little bit confusing. I've had people think
15 they're indicating that, for example, a command
16 signal emerging from 116 and moving to the left would
17 go into the first memory, come out of it, and go into
18 the second, which is not what happens. There's a
19 single line that goes from 116 all the way to the
20 left edge, and each one of the memory devices is
21 connected to that line. So the signal does go into
22 each memory, but it doesn't come out and get sent
23 forward.

24 But the concept of fly-by is just to say
25 the signal first reaches the closest DRAM chip and

1 then it reaches the second closest, and it sort of
2 flies by all of these memory devices.

3 Q. I'm going to introduce a new exhibit,
4 1078.

5 (Exhibit 1078 was marked.)

6 BY MR. CHANDLER:

7 Q. Which is an annotated version of
8 Figure 2C of the '608 patent marked as Exhibit 1001,
9 as well as it reprints the text that we were looking
10 at in column 9 from line 52 through column 10 at
11 line 6 of the '608 patent.

12 Do you have Exhibit 1078 in front of you?

13 A. I do.

14 Q. So Exhibit 1078 illustrates in color
15 Figure 2C of the '608 patent, with the module
16 controller in the middle highlighted in red, with the
17 big arrow highlighted in brown going off to the left
18 illustrating control, address, and clock signals for
19 the DRAM memory devices in green, and a similar arrow
20 in brown below that illustrating command and clock
21 signals for the data buffers highlighted in blue,
22 understood?

23 A. Yes.

24 Q. And on page 1 at the bottom, we've added
25 these images of a clock: Zero degrees, 60 degrees,

1 120 degrees, 180 degrees, 240 degrees, 300 degrees;
2 do you understand that?

3 A. Yeah, generally. Sure.

4 Q. And so as shown in Exhibit 1078, using
5 the annotation of Figure 2C of the '608 patent, the
6 same control address and clock signals will reach
7 different DRAM memory devices at different times, as
8 conceptually represented by the different clocks
9 below each data buffering in blue, correct?

10 A. Yes, I think that's correct.

11 Q. And would it be fair to say that this is
12 trying to illustrate the concept of the fly-by
13 arrangements in the horizontal direction that you
14 were discussing a moment ago?

15 A. I think that's a fair characterization of
16 what I expect this -- a fair characterization that it
17 represents the behavior of the fly-by phenomenon that
18 we were discussing previously.

19 Q. And then page 2 of Exhibit 1078 is
20 similar, except that it's trying to illustrate a
21 faster clock speed where the clock signal has a
22 shorter clock period, meaning, that by the time the
23 clock signal reaches the left side of the memory
24 module, the next clock signal is being sent out by
25 the module controller in red; is that understood?

1 MR. LINDSAY: Objection. Form.

2 THE WITNESS: Yes, that's -- I have that
3 understanding. It appears to be indicating at
4 least multiple clocks on the clock line at an
5 instant in time.

6 BY MR. CHANDLER:

7 Q. And is that page 2 of Exhibit 1078
8 generally consistent with -- as a concept, with what
9 is described in the '608 patent at that passage from
10 column 9, line 52 through column 10, line 6 at the
11 end where it's discussing that before one module
12 control signal reaches an end of the signal line,
13 another module control signal appears on a signal
14 line?

15 A. Yes. I believe it's -- yes, that's the
16 case.

17 Q. I want to introduce a new exhibit, 1079.
18 (Exhibit 1079 was marked.)

19 BY MR. CHANDLER:

20 Q. Which shows an annotated version of
21 Figure 7 of the Hiraishi reference marked as
22 Exhibit 1005. And let me know when you have
23 Exhibit 1079 in front of you.

24 A. Okay.

25 Q. Figure 7 of the Hiraishi reference marked

1 as Exhibit 1005 has a fly-by arrangement in the
2 horizontal direction for both the memory chips
3 highlighted in green in Exhibit 1079, as well as the
4 data register buffers highlighted in blue in
5 Exhibit 1079; is that fair?

6 A. Yes, that's my understanding of what
7 they're attempting to illustrate here.

8 Q. And the fly-by arrangement in Hiraishi as
9 illustrated in Exhibit 1079 is generally similar to
10 the fly-by arrangement in the '608 patent, as
11 illustrated in Exhibit 1078 that we just looked at;
12 is that fair?

13 MR. LINDSAY: Objection. Form.

14 THE WITNESS: I think that it's generally
15 similar, yes.

16 BY MR. CHANDLER:

17 Q. And Exhibit 1079 on page 1 illustrates
18 the concept of a slower clock speed where the signal
19 reaches the end of the line within a single clock
20 period. Whereas, page 2 of Exhibit 1079 illustrates
21 the concept of the faster clock speed where a second
22 clock signal is sent out on the line before the first
23 clock signal has reached the furthest memory chip in
24 the furthest data register buffer; is that fair?

25 A. I think that's fair. However, I don't

1 recall Hiraishi discussing this sort of situation.
2 Maybe they did. And if so, you can point me to it
3 and I'd review it.

4 But I don't recall them specifically
5 talking about operating at high enough speeds where
6 wire pipelining would occur on the fly-by lines.

7 Q. But Hiraishi certainly does talk about
8 this fly-by arrangement for the memory chips and the
9 data registry buffer, and a person of ordinary skill
10 in the art would understand that concept, correct?

11 A. Yes. My recollection is that I think
12 they were focused on DDR3 where a lot of these issues
13 were not fundamentally present as a problem, but they
14 were anticipated as becoming a problem eventually.

15 Q. And as shown conceptually on
16 Exhibit 1079, one full clock cycle can be referred to
17 as 360 degrees, correct?

18 A. That appears to be what they're
19 indicating. I wouldn't normally refer to it as
20 360 degrees, but I understand that representation.

21 Q. And a quarter of a clock cycle can be
22 referred to as 90 degrees, correct?

23 A. Sure. I don't think that's unreasonable.

24 Q. And half a clock cycle would be
25 180 degrees under that understanding, correct?

1 A. Yes, I agree with that.

2 Q. And then another nomenclature that is
3 sometimes used is the letter T, a capital T, to refer
4 to clock periods or portions of a clock period. So,
5 for example, T0 can refer to a starting time, T0.5
6 can refer to 180 degrees or half a clock cycle, T1
7 can refer to a full clock cycle, T2 can refer to two
8 full clock cycles, and so on; is that fair?

9 A. I have seen indications like that, with
10 the general exception of fractions. Usually it's T0,
11 T1, T2, referring to the start of a clock cycle.

12 Q. And after 360 degrees a clock repeats
13 itself, meaning, that a clock at 450 degrees will
14 essentially look the same as a clock at 90 degrees,
15 as conceptually illustrated on the bottom right of
16 page 2 of Exhibit 1079; is that fair?

17 A. I think that's generally fair from the
18 point of view of the data register buffer and the
19 memory chips shown above that image of the clock.
20 The clock -- the 90-degree clock and the 450-degree
21 clock would look the same.

22 Q. I'd like to introduce a new exhibit,
23 1085, which is a presentation dated 2008 about read
24 and write leveling for DDR3 memory modules. And let
25 me know when you have Exhibit 1085 in front of you.

1 (Exhibit 1085 was marked.)

2 THE WITNESS: I have it in front of me
3 now.

4 BY MR. CHANDLER:

5 Q. As shown --

6 MR. LINDSAY: Objection.

7 (Indecipherable.)

8 (The Court Reporter requested
9 clarification.)

10 MR. LINDSAY: Registering an objection to
11 the introduction of the exhibit.

12 BY MR. CHANDLER:

13 Q. As shown on page 3 of Exhibit 1085, and
14 I think consistent with what you said just a moment
15 ago, with the introduction of DDR3 memory modules,
16 JEDEC introduced the fly-by arrangement, which was
17 not commonly used in the previous DDR2?

18 A. I'm sorry, which page are you at?

19 Q. Page 3 of Exhibit 1085.

20 MR. LINDSAY: Objection. Outside the
21 scope of direct.

22 BY MR. CHANDLER:

23 Q. So as the industry moved from DDR2 to
24 DDR3 memory modules, one of the changes was the
25 introduction, or at least the common use of the

1 fly-by arrangement for DDR3 memory modules, which was
2 not commonly used with the DDR2 memory modules; is
3 that fair?

4 MR. LINDSAY: Objection. Outside the
5 scope as it relates to the exhibit.

6 THE WITNESS: Yeah. I don't recall
7 reviewing this exhibit before, but maybe I did
8 and it simply eludes me. This is written very
9 oddly. It's got a line referring to
10 termination. And it says, for DDR2, address
11 none. For DDR3, it says, address fly-by.
12 Fly-by is not termination.

13 I don't know what this document is trying
14 to indicate. It seems to be using the terms in
15 an inconsistent manner or a manner that I'm not
16 familiar with.

17 BY MR. CHANDLER:

18 Q. On page 4 of Exhibit 1085 there's
19 illustration of the general routing of address
20 control and clock signals for DDR2 memory modules
21 which looks like a tree. Whereas, on page 5 of
22 Exhibit 1085, there's illustrated the routing for a
23 DDR3 memory module which is consistent with what you
24 have described as a fly-by arrangement; is that fair?

25 MR. LINDSAY: Objection. Outside the

1 scope of direct.

2 THE WITNESS: I don't recall the -- a
3 tree routing structure being used in DDR2.
4 Figure -- page 4 does refer to address control
5 and clocks for DDR2 being tree routed, but
6 I don't have any particular recollection of
7 that.

8 And then DDR -- slide 5 does show that --
9 huh, that's interesting. No, it's not showing
10 fly-by in the manner that we just stalked about.

11 BY MR. CHANDLER:

12 Q. Well, this is for an unbuffered DIMM, so
13 there's no register in the middle.

14 So the signals just go from left to right
15 across the entire module, correct?

16 A. Not really, no.

17 Q. Well, they come up the middle, go to the
18 left, and then they fly-by from left to right,
19 correct?

20 A. That's not --

21 MR. LINDSAY: Objection. Outside the
22 scope.

23 THE WITNESS: That's not what this says.

24 BY MR. CHANDLER:

25 Q. Okay. Well, explain to me how it worked

1 with DDR3 memory modules.

2 A. I haven't reviewed DDR3 memory modules
3 for this particular aspect much recently. This
4 indicates that the address control and clocks are
5 daisy-chained. That's a term of art that I mentioned
6 previously when talking about fly-by, might be --
7 might appear to be suggested to somebody that was
8 unfamiliar with it, but was not the case in fly-by.

9 So daisy-chaining indicates that this is
10 not a fly-by design.

11 Q. Page 3 of Exhibit 1085 indicates DDR3 is
12 a fly-by design, and that's consistent with your
13 testimony, correct?

14 MR. LINDSAY: Objection. Outside the
15 scope of direct as it relates to the exhibit.

16 THE WITNESS: Page 3 indicates that the
17 termination or address line says "fly-by" which,
18 as I said, makes no sense to me. That's not a
19 thing. Fly-by is not a matter of termination.

20 A fly-by -- a system where fly-by effects
21 need to be accounted for can have multiple
22 termination modes. These are orthogonal issues.

23 (The Court Reporter requested
24 clarification.)

25 THE WITNESS: Orthogonal.

1 BY MR. CHANDLER:

2 Q. Page 7 of Exhibit 1085 illustrates on the
3 left the fly-by topology for DDR3 memory module
4 conceptually, correct?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct.

7 THE WITNESS: I don't know. I don't
8 recall looking at this. As I just said, based
9 on what we saw just in the previous slides,
10 I would not call that -- that's not a fly-by
11 technology. And this seems to be -- I think
12 this figure is consistent with that.

13 I think that they've mislabeled it. But,
14 you know, I haven't reviewed this any time
15 recently.

16 BY MR. CHANDLER:

17 Q. To be clear, you said "fly-by
18 technology," but I said and the slide says "fly-by
19 topology," correct?

20 A. I take your representation that I said
21 technology, yes.

22 Q. In a fly-by topology, in the situation of
23 a read operation, the read data will come out to the
24 memory controller and arrive at memory controller at
25 different times as conceptually illustrated on the

1 left side of page 7 of Exhibit 1085, correct?

2 MR. LINDSAY: Objection. Outside the
3 scope as it relates to the exhibit.

4 THE WITNESS: No, I wouldn't say that.

5 BY MR. CHANDLER:

6 Q. So this is important. So how would you
7 say it?

8 A. I don't want to say it. I mean, I --
9 I don't know exactly what you're -- what you're
10 getting at.

11 Q. I'm getting at the fly-by topology for
12 DDR3 memory devices as illustrated, for example, in
13 Figure 2C, as illustrated, for example, on Figure 7
14 of Hiraishi, and I believe it's illustrated, or at
15 least it's conceptually illustrated, on page 7 of
16 Exhibit 1085.

17 But, you know, why don't you tell me how
18 it works.

19 MR. LINDSAY: Objection. Form.

20 THE WITNESS: So as I said. Looking at
21 this figure, it's showing -- to me, it's showing
22 a daisy-chain design, not a fly-by design. The
23 signals don't fly by all of the chips. It's
24 daisy-chained. So --

25

1 BY MR. CHANDLER:

2 Q. It says -- I mean, it says "fly-by
3 topology," right? It doesn't show an input to the
4 first memory device and an output to the second
5 memory device. It shows --

6 (The Court Reporter requested
7 clarification.)

8 BY MR. CHANDLER:

9 Q. It doesn't show an input to the first
10 memory device and an output from the first memory
11 device. It just shows the same signal line has a
12 connection to each memory device, which I believe is
13 what you described previously as a fly-by
14 arrangement.

15 A. I believe that's consistent with my
16 explanation of a fly-by arrangement. And I'll agree
17 that this figure is labeled "Fly-by topology."

18 But if you'll notice, the yellow lines go
19 from the top, for example, come down into sort of the
20 first memory device at the top, and then there's a
21 dot. That's used to indicate in circuit diagrams
22 that there's a wire with multiple connections.

23 So it comes into the first chip, and the
24 first chip makes use of that information, and then it
25 goes out of the first chip into the second chip.

1 That's not a fly-by technology or
2 topology, regardless of what the labeling on the
3 figure says.

4 Q. Right. So let's stick with fly-by
5 topology as you understand it --

6 A. Okay.

7 Q. -- for DDR3 memory devices.

8 Does the fly-by topology for DDR3 memory
9 devices result in read data being output at different
10 times and then received at a different times by the
11 memory controller as conceptually illustrated by the
12 orange arrows on the left side of page 7 of
13 Exhibit 1085?

14 MR. LINDSAY: Objection. Beyond the
15 scope of direct. And form.

16 THE WITNESS: It might. It depends on
17 exactly what the specific system design utilizes
18 in response to the fly-by effect. It doesn't
19 have to be the case that the signals come out at
20 different times. That could be adjusted for
21 inside the DRAMs, for example.

22 BY MR. CHANDLER:

23 Q. And so what is read leveling for DDR3
24 memory modules, or more accurately, for DDR3 memory
25 controllers?

1 A. So read leveling is a technique that's
2 used to address the fact that in some memory modules,
3 and I'm saying that because, like I said, I haven't
4 reviewed the DDR3 technology closely in quite a
5 while, but if there is a fly-by effect in the
6 individual -- well, on the memory module, and is --
7 so, conceptually, it's -- read leveling is a
8 technique for responding or counteracting the fly-by
9 effect by adding some timing variation.

10 That can be done in a number of places.
11 As I suggested, it could be done in the DRAMs. It
12 could be done in the memory controller. If there's a
13 buffer, a data buffer between the DRAMs and the
14 memory controller, it can be done in the data buffer.

15 Q. And what was the common approach for DDR3
16 memory modules for how read leveling or where read
17 leveling was performed?

18 A. Well, the common approach I know for DDR4
19 and DDR5 is to do it in the data buffers. I do not
20 recall if read leveling for DDR3 is done, or if it's
21 done in the DRAM chips, or if it's done in the memory
22 controller. I haven't looked at that issue in quite
23 some time.

24 Q. And then page 9 of Exhibit 1085 refers to
25 write leveling for DDR3 at the top, correct?

1 A. Yes, I see that.

2 MR. LINDSAY: Objection. Outside the
3 scope as it relates to the exhibit.

4 BY MR. CHANDLER:

5 Q. And page 9 of Exhibit 1085 shows the
6 clock signal in a fly-by arrangement across the
7 different memory devices on the DDR3 memory module,
8 correct?

9 MR. LINDSAY: Objection. Outside the
10 scope of direct.

11 THE WITNESS: I wouldn't say that.

12 BY MR. CHANDLER:

13 Q. So you see write clock with the purple
14 lines?

15 A. Yes.

16 Q. In DDR3 memory modules, it was common for
17 the clock signal to be in a -- what you described as
18 fly-by topology, correct?

19 A. I don't recall. My understanding is that
20 the yellow line carries -- the yellow line
21 illustrated on the right-hand element carries
22 command, address, and clock.

23 And as I said previously, there was a
24 reference to daisy-chaining. And this figure, again,
25 indicates to me that those signals are daisy-chained,

1 in which case, the clock would not be in a fly-by
2 topology. You wouldn't see the fly-by effects.

3 Q. But your testimony is that the common
4 arrangement for DDR3 memory modules was the fly-by
5 topology for the address, control, and clock signals,
6 correct?

7 MR. LINDSAY: Objection. Misstates prior
8 testimony.

9 THE WITNESS: No, I wouldn't say that.

10 BY MR. CHANDLER:

11 Q. Do you understand what write leveling for
12 DDR3 memory modules is?

13 A. I understand write leveling. I don't
14 recall details of how it was done in DDR3. But I do
15 understand the concept of write leveling.

16 Q. And what's the relationship between write
17 leveling and the fly-by delays for DDR3 memory
18 modules?

19 A. I don't know as I sit here because, as
20 I mentioned, this set of slides that I don't recall
21 viewing seems to be presenting inconsistent
22 information regarding whether DDR3 used a daisy-chain
23 topology or a fly-by topology. It seems to me it's
24 saying it uses a daisy-chain topology. And I haven't
25 reviewed write leveling in DDR3 to any significant

1 depth anytime recently.

2 Q. Well, I mean, I think all the references
3 refer to write leveling. I mean, I think the
4 '608 patent talks about write leveling. I think
5 Hiraishi talks about write leveling. I believe
6 Tokuhiko talks about write leveling. I think the
7 DDR3 standard talks about write leveling.

8 You don't recall any recollection of
9 write leveling for DDR3?

10 A. I do have --

11 MR. LINDSAY: Objection. Form.

12 THE WITNESS: -- an understanding of
13 write leveling in general. My recollection of
14 the previous question was that you were tying it
15 to the concept of fly-by delays, and so I was
16 talking about that.

17 BY MR. CHANDLER:

18 Q. Yes.

19 So is there a connection between write
20 leveling for DDR3 memory modules and fly-by delays?
21 And, if so, can you explain it?

22 MR. LINDSAY: Objection. Form.

23 THE WITNESS: No. This seems to indicate
24 to me, this particular figure and other figures
25 that we've discussed, that at least Altera

1 believes that fly-by is not used in DDR3.

2 Now --

3 BY MR. CHANDLER:

4 Q. But you know (indecipherable) --

5 (Parties speaking simultaneously.)

6 (The Court Reporter requested

7 clarification.)

8 BY MR. CHANDLER:

9 Q. But you know that fly-by is used in DDR3,
10 correct?

11 A. As I just said, I haven't reviewed DDR3
12 in any great depth anytime recently. Write leveling,
13 my recollection, is used in DDR3. And it's used, in
14 large part, to respond to or to correct for timing
15 delays of signals as they propagate across the memory
16 module.

17 Q. Can you explain that a little more?

18 A. Sure. So I think that this figure shows
19 that there is a certain phase delay for a write clock
20 that goes to the memory module for DQS for group
21 zero, and then it comes out of that -- that chip and
22 goes to the next one. And it will have a greater
23 phase delay. So that's shown as the DQS phase delay
24 for group one.

25 So write leveling is used to account for

1 the delay in those signals as they propagate from one
2 chip to the next.

3 Q. If you look at Exhibit 1020, the DDR3
4 memory standard, on page 42, you know that the -- as
5 stated at the top of page 42, that DDR3 memory module
6 adopted fly-by topology for commands, address,
7 control signals, and clocks, correct?

8 A. I don't recall that. It's a 211-page
9 document that I haven't memorized. And I haven't
10 looked closely at DDR3 devices in the context, for
11 example, of like accused products. It wouldn't
12 surprise me. I just don't recall.

13 Q. Do you have Exhibit 1020, page 42, in
14 front of you?

15 A. I have it in front of me. I didn't get
16 to page 42 because you -- I missed which page number
17 was said. So page -- PDF page or labeled page 42?

18 Q. Both.

19 (The Court Reporter requested
20 clarification.)

21 BY MR. CHANDLER:

22 Q. Both, b-o-t-h.

23 So you understand as stated at the top of
24 page 42 of Exhibit 1020, the JEDEC Standard for DDR3
25 memory devices --

1 (The Court Reporter requested
2 clarification.)

3 BY MR. CHANDLER:

4 Q. You understand as stated at the top of
5 page 42 of Exhibit 1020, the JEDEC standard for DDR3
6 memory devices, that DDR3 memory modules adopted
7 fly-by topology for the commands, addresses, control
8 signals, and clocks, correct?

9 A. No. It doesn't say that on the page.

10 Q. At the top of page 42, Exhibit 1020,
11 under the heading 4.8, "Write leveling."

12 A. The top of page 42, starts with
13 3.4 registered definitions continued.

14 Q. On my PDF it's numbered PDF page 42, but
15 it's also printed page 42, both in the upper left and
16 the bottom right. So that's what I'm referring to.

17 And throughout this deposition, I will
18 refer -- the page number is the one that's printed on
19 the bottom right with the exhibit number, just for
20 clarity.

21 A. Okay.

22 Q. So are you now at page 42 of
23 Exhibit 1020, the JEDEC Standard for DDR3 memory
24 devices?

25 A. Yes. That's PDF page 57. And I see it

1 says under the heading 4.8 "Write leveling" it says:

2 The DDR3 memory modules adopted fly-by
3 topology for the commands.

4 Q. And also for addresses, controls signals,
5 and clocks, right?

6 A. Yes.

7 Q. And in forming your opinions in your
8 expert declaration marked as Exhibit 2013, did you
9 take that into consideration?

10 A. Yes. For every accused product that
11 I was considering whether it infringed a DDR3
12 specification, I took into account this --

13 Q. Time out. I apologize for interrupting,
14 but I think I confused you.

15 I mean, there are no accused products in
16 the IPR, right? This is not infringement?

17 A. I know that, yeah.

18 Q. So in forming your opinions in your
19 expert declaration marked as 2013, did you take into
20 consideration that DDR3 memory modules adopted a
21 fly-by topology for commands, addresses, control
22 signals, and clocks as stated on page 42 of
23 Exhibit 1020?

24 A. Perhaps. We'd have to review my
25 declaration and see if I relied upon that. I was

1 aware of this document, but that doesn't mean as
2 I sit here I recall relying upon this portion of it.

3 Q. I mean, respectfully, you spent you say
4 16 hours preparing for today's deposition?

5 A. Around probably that, yeah.

6 MR. LINDSAY: Objection. Argumentative.

7 BY MR. CHANDLER:

8 Q. And you can't tell me whether or not you
9 took into consideration that DDR3 memory modules
10 adopted a fly-by topology for commands, addresses,
11 control signals, and clocks?

12 MR. LINDSAY: Same objection.

13 THE WITNESS: I think that's accurate.

14 I don't recall as I sit here. I'd be happy to
15 review my declaration further.

16 BY MR. CHANDLER:

17 Q. Turning back to Exhibit 1085. Can you
18 pull that up again and let me know when you have it
19 in front of you?

20 A. Yes, I see that.

21 Q. I want you to assume for purposes of my
22 questions that Exhibit 1085 does, in fact, illustrate
23 a fly-by topology consistent with the statement in
24 the DDR3 JEDEC standard marked as Exhibit 1020 that
25 DDR3 memory modules have a fly-by topology for

1 address, control, and clock signals, understood?

2 MR. LINDSAY: Objection. Form. Outside
3 the scope of direct.

4 THE WITNESS: Understood.

5 BY MR. CHANDLER:

6 Q. And so using just the conceptual
7 illustration of memory module on page 7 of
8 Exhibit 1085, and with the assumption that it does
9 actually intend to illustrate the fly-by topology
10 used in a DDR3 memory module, are you with me so far?

11 A. Yes.

12 Q. We -- you discussed earlier that read
13 leveling can be used to account for the dispute in
14 the data signals that are output and received --
15 output by a memory module and received by the memory
16 controller; is that fair?

17 A. I'm sorry, could you repeat the question?

18 Q. For a DDR3 memory module, read leveling
19 can be used to account for the skew of data signals
20 that are output by the memory module and received by
21 the memory controller; is that fair?

22 A. Yes, I think that that's fair.

23 Q. And then write leveling can be used to
24 account for the skew in the other direction, which is
25 when the memory controller is sending data signals to

1 the DDR3 memory module, which is going to have the
2 address, control, and clock signals calling the DDR3
3 memory module in a fly-by topology, meaning, that
4 there will be fly-by delays for those address
5 controlling clock signals; is that fair?

6 A. Those address, control, and clock signals
7 will be skewed, and write leveling can be used to
8 allow the system to operate correctly in the context,
9 in the face of those skews.

10 MR. CHANDLER: Why don't we take a short
11 break. Off the record.

12 THE VIDEOGRAPHER: Off the record at
13 11:23 a.m. Pacific time.

14 (A recess was taken.)

15 THE VIDEOGRAPHER: On the record at
16 11:41 a.m. Pacific time.

17 BY MR. CHANDLER:

18 Q. Dr. Mangione-Smith, during the break were
19 you able to locate the typo in your expert
20 declaration marked as Exhibit 2013 that you referred
21 to at the beginning of the deposition?

22 A. Yes, I was.

23 Q. And what's the correction to the typo
24 that should be made?

25 A. So in paragraph 24 of my declaration,

1 I referred to Exhibit 2012, parentheses, Jacob, at
2 405. And it should actually be Exhibit 1021. But
3 the page number is the same.

4 Q. All right. I put Exhibit 1021, the Jacob
5 textbook, in the chat. Do you have that exhibit in
6 front of you?

7 A. I do.

8 (Exhibit 1021 was identified.)

9 BY MR. CHANDLER:

10 Q. So Exhibit 1021 is a textbook by
11 Professor Jacob and others titled "Memory Systems
12 Cache, DRAM, Disk," correct?

13 A. Yes.

14 Q. And you've seen Exhibit 1021 before,
15 correct? And you cited it a few times in your
16 declaration marked as Exhibit 2013, correct?

17 A. That's correct.

18 Q. Do you believe a person of ordinary skill
19 in the art would have known about the textbook by
20 Professor Jacob marked as Exhibit 1021?

21 A. Sure.

22 Q. Do you consider Professor Bruce Jacob to
23 be an expert in the field?

24 A. He is both an expert and a friend.

25 Q. And just out of curiosity, how do you

1 know Professor Bruce Jacob?

2 A. We work in the same general professional
3 area, and I'm fairly certain -- he graduated from
4 Michigan. I don't recall who his advisor was, but it
5 was either my advisor or a good friend of mine.

6 Q. Please turn to page 326 of the Jacob
7 textbook marked as Exhibit 1021. And let me know
8 when you are there. And I'll -- again, it's the page
9 number on the bottom right which matches the page
10 number in the upper left. In my version of Acrobat,
11 I can just type in 326 and it goes to the right page,
12 but I suppose in other versions of PDF readers it may
13 not work. So to the extent it helps, the PDF page
14 may be 103.

15 A. I'm there.

16 Q. So on page 326 of Exhibit 1021 on right
17 side, Professor Jacob begins a discussion of
18 synchronous DRAMs, also known as SDRAMs, correct?

19 A. Yes, sir.

20 Q. And in the middle of the paragraph on the
21 right side of page 326 of Exhibit 1021,
22 Professor Jacob explains that a synchronous DRAM uses
23 an internal clock signal for timing its operations;
24 is that fair?

25 A. I'm sorry. Where were you at? I believe

1 that's accurate, but I'm not tracking you.

2 Q. Pretty much halfway down the paragraph on
3 the right side of page 326 under the heading of
4 "Synchronous DRAM." There's a reference to an
5 internal clock signal. I think you can probably
6 search for the word "internal."

7 A. Good idea. Okay. Yes, I see that.

8 Q. And the use of clock signals provides
9 several benefits to SDRAM as explained by
10 Professor Jacob, including making the memory
11 operations more predictable, having less skew, and
12 having higher throughput; is that fair?

13 A. Yes, I think that's fair.

14 Q. And then if you move ahead a few pages to
15 page 333 of Exhibit 1021, in the upper left
16 Professor Jacob draws a distinction between single
17 data rate SDRAM, and then on right there's a
18 discussion of double data rate SDRAM, correct?

19 A. Yes, I see that.

20 Q. And single data rate is often abbreviated
21 SDR while double rate is often abbreviated DDR,
22 correct?

23 A. Likely. DDR I completely agree with.
24 Single data rate is so old I don't recall anybody
25 calling it SDR, but that seems not unreasonable.

1 Q. Well, for example, on page 327 of
2 Exhibit 1021, Professor Jacob at the bottom refers to
3 SDR SDRAM, and he's talking about single data rate
4 SDRAM in Figure 7.15 as opposed to, for example,
5 double rate memory devices; is that fair?

6 A. Sure. I'm just saying that, you know,
7 I don't recall seeing SDR used. But seeing it, it
8 makes sense in the context of discussing double data
9 rate as what came previously. But it's far enough in
10 the past that I just don't recall ever seeing that
11 naming for it.

12 Q. So going back to page 326 of
13 Exhibit 1021, Professor Jacob explains that a clock
14 signal can be used to control the internal latches of
15 an SDRAM; is that generally fair?

16 A. Sure.

17 Q. And on page 327 of Exhibit 1021 in
18 Figure 7.15, in that figure, which is for a single
19 data rate SDRAM, not a double data rate SDRAM, the
20 clock signal is used to determine when there is valid
21 data to output on the DQ data line of the memory
22 device; is that fair?

23 A. Well, that's true for both SDR and DDR.
24 The clock is used to control the entire SDRAM --
25 well, the clock is used to control the entire SDRAM

1 chip. All the operations within it are synchronized
2 to a clock.

3 Q. But what we'll get to in a moment is, DDR
4 introduced the strobe signal, the DQS strobe signal,
5 which did not exist in the earlier single data rate
6 technology, correct?

7 A. I don't -- I don't recall. The notion of
8 a data strobe is certainly -- was certainly known
9 prior to DRAM technology. And the notion of, if
10 you've got a clock, you can control the SDR DDR on
11 both edges without having a strobe. But, for
12 example, in DDR3 and DDR4, strobes are, in fact,
13 present for controlling part of the operation.

14 Q. And on page 326 of Exhibit 1021, towards
15 the bottom right, Professor Jacob explains that
16 another feature of SDRAM that it has a programmable
17 register, which can be used, for example, to define
18 the burst length for a data transfer, correct?

19 A. Yes, I see that. Right.

20 Q. And you mentioned just a second ago that
21 the strobe signal is used in DDR3, but it was also
22 used in DDR2 in the first generation of DDR as well,
23 correct, the DQS strobe signal?

24 A. Likely. I don't recall. I haven't
25 looked at DDR2 even as recently as I have looked at

1 DDR3.

2 Q. I want to talk a little bit about the
3 difference between single data rate DRAMs and double
4 data rate DRAMs sort of at a high level.

5 So do you have that in mind?

6 A. Yes.

7 Q. So single data rate SDRAMs use a single
8 edged clock to synchronize all of the transmissions,
9 including control, address, and data, while DDR
10 memory devices transmit data at both the rising and
11 the falling edge of the clock, which is why they're
12 referred to as double data rate. Is that fair at a
13 high level?

14 A. At a high level, but I wouldn't say it
15 that way because -- excuse me -- the clock hasn't
16 changed. The clock always has two edges. But it's
17 correct that with SDR only one of the clock edges is
18 being used for reading or writing data. Whereas,
19 with DDR, both clock edges are being used.

20 Q. And if you look at page 334 of
21 Exhibit 1021, the textbook by Professor Jacob, he
22 illustrates what I think you were just trying to say,
23 which is that for SDR SDRAM as illustrated at the top
24 of Figure 7.20, there is just one piece of data per
25 clock cycle. Whereas, for DDR SDRAM as shown on the

1 bottom of Figure 7.20 there's two pieces of data for
2 every clock period; is that fair?

3 A. Yes.

4 Q. And on -- turning back just a little bit
5 to page 333 of Exhibit 1021 at the bottom right,
6 Professor Jacob explains that in the single data rate
7 SDRAM memory devices shown at the top of Figure 7.20
8 on the next page, which he refers as to 7.20A, the
9 transitions of the clock signal can be used directly
10 to drive data onto the bus, as well as to read data
11 off of the bus, correct?

12 A. Again, that sounds correct. I'm not --
13 oh, I see. Okay. Yeah, I see that.

14 Q. And then consistent with that statement
15 as shown on page 334 at the top with Figure 7.20, the
16 data transition for SDR DRAM memory devices happens
17 at the time when the clock has a corresponding rising
18 edge; is that fair?

19 A. Yes, I think that's fair.

20 Q. And it would be fair that the rising edge
21 can be used to drive the data, and the falling edge
22 of the clock can be used to read the data for the
23 single data rate SDRAM memory devices?

24 A. Yeah, I think that's -- that it could be
25 used in that way. Sure.

1 Q. And as shown at the top of Figure 7.20 on
2 page 334 of Exhibit 1021, the falling clock
3 transition from high to low occurs in the middle of
4 the data eye for single data rate SDRAM memory
5 devices; is that fair?

6 A. Yes, I think that's fair.

7 Q. And that falling clock transition in the
8 middle of the data eye can be used to latch the data
9 in a way that's reliable because the data's being
10 sampled away from transitions of the data signal; is
11 that fair? In other words, you're aiming for the
12 middle of the data eye, and that's why the falling
13 clock transition works in this situation?

14 A. I think that that's accurate. The
15 falling edge can be used to latch the data. It's
16 shown here as being roughly in the middle of the data
17 eye. That's certainly the intent.

18 Q. And then, in contrast, in the double data
19 rate SDRAM memory device scenario shown at the bottom
20 of Figure 7.20, which on the upper left of page 334
21 in the text is referred to as Figure 7.20(b), there
22 are fewer clock edges per data transmission that can
23 be used for synchronization, correct?

24 A. There are a fewer clock edges that can be
25 used directly for data synchronization. But a clock

1 edge could be processed delayed, for example, and
2 then used for latching the data.

3 Q. But the standard approach for DDR SDRAM
4 memory devices, as explained by Professor Jacob on
5 page 334 on Exhibit 1021 on the left side in the
6 second paragraph, is that for DDR memory devices,
7 some other mechanism must be introduced to get
8 accurate timing for both driving data and sampling
9 data to compensate for the fact that there are fewer
10 clock edges; is that fair?

11 A. Yes. I think that's consistent with what
12 I just testified, but, yes, I agree.

13 Q. And that some other additional mechanism
14 is what we now call the DQS data strobe; is that
15 fair?

16 A. That is the approach in the JEDEC
17 standard, but as I was saying, there are other
18 approaches.

19 Q. And the phrase that Professor Jacob uses
20 in that passage is that a dual-edged signaling scheme
21 needs an additional mechanism beyond the clock, and
22 that additional mechanism for DDR memory devices is
23 the DQS strobe signal; is that fair?

24 A. Yes. And I think that's accurate for the
25 JEDEC DDR devices for simply -- which is, I think,

1 the context that he's discussing here, simply for DDR
2 devices in general. As I was saying, there are other
3 mechanisms that could have been used, but JEDEC did
4 not choose to select them.

5 Q. As Professor Jacob explains on the bottom
6 left of page 334 for Exhibit 1021, for write
7 operations the memory controller provides a center
8 aligned DQS data strobe that the DDR SDRAM can use
9 directly to sample the incoming data, correct?

10 A. Yes, that is what he says here.

11 Q. And that's consistent with your
12 understanding of how it works for JEDEC standard DDR
13 memory devices; is that fair?

14 A. No. It's consistent for some of the
15 JEDEC DDR memory devices, but not all of them.

16 Q. And then for read operations, according
17 to the Professor Jacob in the same passage on the
18 bottom left of page 334 of Exhibit 1021, the DQS data
19 strobe is edge aligned with the data coming out of
20 DDR SD memory device.

21 So that means that when the memory
22 controller receives that data, the memory controller
23 has to adjustment the DQS strobe from being edge
24 aligned to being center aligned, correct?

25 MR. LINDSAY: Objection. Form.

1 THE WITNESS: So I think that's accurate
2 for some of the JEDEC devices, but not all of
3 them.

4 BY MR. CHANDLER:

5 Q. But, certainly, that was a known approach
6 for DDR memory devices as taught by Professor Jacob
7 on page 334 of Exhibit 1021; is that fair?

8 A. It was known that that approach could be
9 used for some of the DDR memory devices, yes.

10 Q. Turn to page 342 of Exhibit 1021. Let me
11 know when you're there. Just a few pages forward.

12 A. Okay. I'm there.

13 Q. On page 342 of Exhibit 1021, in the upper
14 left Professor Jacob discusses CAS latency, correct?

15 A. Yes.

16 MR. LINDSAY: Objection. Outside the
17 scope of direct.

18 BY MR. CHANDLER:

19 Q. At a high level, how would you explain
20 what CAS latency is?

21 MR. LINDSAY: Objection. Outside the
22 scope of direct.

23 THE WITNESS: Historically, CAS, C-A-S,
24 stands for column address strobe. And CAS
25 latency has referred to the time between when

1 the read operation, for example, begins and when
2 the CAS signal is asserted.

3 These days, the term "CAS" there's a
4 similar phenomenon, but it's not really a column
5 address strobe, but there is a similar signal,
6 and the term "CAS" is still used.

7 BY MR. CHANDLER:

8 Q. So when did you say that CAS latency
9 would begin and when would it end, in the example you
10 were giving?

11 MR. LINDSAY: Objection. Outside the
12 scope of direct.

13 THE WITNESS: My recollection was that
14 the CAS latency is between the start of the
15 operation, the read or write, and when the CAS
16 signal is asserted.

17 BY MR. CHANDLER:

18 Q. And do you agree a person of ordinary
19 skill in the art would have known about CAS latency?

20 A. Yes, I believe that's true.

21 Q. And then in the upper left of page 342 of
22 Exhibit 1021, Professor Jacob states that, under the
23 JEDEC approach, CAS latency is programmed at system
24 initialization in the -- is that correct?

25 A. Yes, that's correct.

1 Q. And is that consistent with the
2 understanding of a person of ordinary skill in the
3 art?

4 A. I would think it's not necessarily
5 inconsistent, although this is getting beyond the
6 structure and the specifications for DDR memory
7 devices, as well as DIMMs. It's a system-level
8 issue.

9 So a person working with BIOS, B-I-O-S,
10 software or computer system initialization would be
11 much more likely to run into that aspect of it than a
12 memory designer or person building a memory module.

13 Q. Professor Jacob goes on to state that
14 after CAS latency is programmed at system
15 initialization, it's never set again while the
16 machine is --

17 (The Court Reporter requested
18 clarification.)

19 BY MR. CHANDLER:

20 Q. Professor Jacob goes on to state in the
21 upper left of page 342 of Exhibit 1021 that after CAS
22 latency is programmed at system initialization, it is
23 never set again while the machine is running,
24 correct?

25 MR. LINDSAY: Objection. Outside the

1 scope of direct.

2 THE WITNESS: Yes, I see that passage.

3 BY MR. CHANDLER:

4 Q. And is that generally consistent with
5 your understanding of how CAS latency is commonly
6 used?

7 MR. LINDSAY: Objection. Outside the
8 scope.

9 THE WITNESS: I think it's consistent
10 with how it's commonly used. I don't know of
11 any factor that would make it such that CAS
12 latency could never be set again. But at the
13 same time, I don't know of any reason why it
14 would change or would be changed.

15 BY MR. CHANDLER:

16 Q. Could you pull up Exhibit 1020, the
17 JEDEC standard for DDR_e memory devices, and go to
18 what's labeled page 18. And let me know when you're
19 there.

20 A. Okay. I'm there.

21 Q. According to the JEDEC standard for DDR3
22 memory devices as shown in the last paragraph of page
23 18 of Exhibit 1020:

24 Prior to normal operation, the DDR3 SDRAM
25 must be powered up and initialized in a

1 predefined manner.

2 Correct?

3 MR. LINDSAY: Objection.

4 THE WITNESS: Yes, I see that passage.

5 MR. LINDSAY: Outside the scope of
6 direct.

7 (The Court Reporter requested
8 clarification.)

9 MR. LINDSAY: It was outside the scope of
10 direct.

11 BY MR. CHANDLER:

12 Q. And then on the next page, which is
13 page 19 of Exhibit 1020, the JEDEC standard for DDR3
14 memory devices states at the top that:

15 The following sequence is required for
16 power up and initialization.

17 And then there are a number of steps,
18 including steps 6, 7, 8, and 9 which require issuing
19 MRS commands to load application settings into the
20 registers labeled MR0, MR1, MR2, and MR3; is that
21 fair.

22 A. Yes, it is --

23 MR. LINDSAY: Objection. Outside the
24 scope of direct. Let me get my objection in
25 there.

1 THE WITNESS: Sorry about that. I've
2 been doing pretty well so far, but I've stomped
3 on you the last two questions.

4 Yes, I see that discussion of different
5 MRS commands that need to be set to program the
6 device during initialization.

7 BY MR. CHANDLER:

8 Q. And on page 33 of Exhibit 1020, the JEDEC
9 standard for DDR3 memory devices, there's a command
10 truth table, and the first row shows that MRS stands
11 for mode register set command, correct?

12 MR. LINDSAY: Objection. Outside the
13 scope of direct.

14 THE WITNESS: Yes, I see that.

15 BY MR. CHANDLER:

16 Q. And the mode register set command is when
17 the signals CS, RAS, CAS, and WE are low, correct?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct.

20 THE WITNESS: Those signals need to be
21 low, according to this table. Not sure if there
22 aren't any other signals that need to be in some
23 particular configuration, but I don't spot any
24 as I sit here.

25

1 BY MR. CHANDLER:

2 Q. And when an MRS mode register set command
3 is asserted, the address lines are used to convey an
4 operation code; is that fair?

5 MR. LINDSAY: Objection. Outside the
6 scope of direct.

7 THE WITNESS: Yes, I see that. That's
8 correct.

9 BY MR. CHANDLER:

10 Q. And then if we turn back to page 23 of
11 Exhibit 1020, the JEDEC standard for the DDR3 memory
12 devices discusses mode register MR0, which is one of
13 the registers that must be programmed by the MRS mode
14 register set command during initialization, correct?

15 MR. LINDSAY: Objection. Outside the
16 scope of direct.

17 THE WITNESS: Yes, that's correct.

18 BY MR. CHANDLER:

19 Q. And as shown by the table in the bottom
20 left of page 23 of Exhibit 1020, mode register MR0 is
21 selected by the address lines BA1 and BA0 being set
22 to zero, which can also be referred to as being low,
23 correct?

24 MR. LINDSAY: Objection. Outside the
25 scope of direct.

1 THE WITNESS: Yes, that's correct. The
2 two bank address signals when set low will be
3 used, assuming everything else is set correctly,
4 to address mode register zero.

5 BY MR. CHANDLER:

6 Q. And as shown on the bottom right of page
7 23 of Exhibit 1020, the mode register MR0 is used to
8 program the CAS latency value in the DDR3 memory
9 devices, correct?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct.

12 THE WITNESS: Yes. Addresses A2 through
13 A6 are used according to the detail specified in
14 this chart, this table, to program the CAS
15 latency.

16 BY MR. CHANDLER:

17 Q. And according to the JEDEC standard for
18 DDR3 memory devices, the permissible CAS latency
19 values are five clock cycles, six clock cycles, seven
20 clock cycles, eight clock cycles, nine clock cycles,
21 or ten clock cycles, or optionally, 11 clock cycles
22 for 1600 DDR3 memory devices; is that correct?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct.

25 THE WITNESS: Yes, that is what it

1 indicates in that table.

2 BY MR. CHANDLER:

3 Q. And then on the next page, which is
4 page 24 of Exhibit 1020, the JEDEC standard for DDR3
5 memory devices explains in the second sentence of the
6 bottom paragraph about CAS latency that DDR3 SDRAM
7 does not support any half clock latencies, correct?

8 MR. LINDSAY: Objection. Outside the
9 scope of direct.

10 THE WITNESS: Yes, I see where it
11 indicates that.

12 BY MR. CHANDLER:

13 Q. So with DDR3 memory devices, your only
14 choices for CAS latency are full cycles,
15 specifically, five, six, or seven clock cycles and so
16 on, as shown on the previous page?

17 MR. LINDSAY: Objection. Outside the
18 scope of direct.

19 THE WITNESS: I don't think that's -- I'm
20 not sure. I don't think that's accurate.
21 Excuse me. That may be accurate with regard to
22 just the CAS latency, but the overall read
23 latency has, for example, this other term,
24 there's an AL term and there's I believe a
25 PL term. I don't think those are constrained to

1 be full clocks, but I'm not sure.

2 BY MR. CHANDLER:

3 Q. Why don't you take is a look at page 27
4 of Exhibit 1020 towards the bottom which discusses
5 additive latency.

6 A. Okay.

7 Q. And as shown on page 27 of Exhibit 1020,
8 additive latency can be set to zero, correct?

9 MR. LINDSAY: Objection. Outside the
10 scope of direct.

11 THE WITNESS: Yes, that's correct.

12 BY MR. CHANDLER:

13 Q. And the JEDEC standard for DDR3 memory
14 devices does not list any half clock cycle latencies
15 for additive latency, correct?

16 MR. LINDSAY: Objection. Outside the
17 scope of direct.

18 THE WITNESS: Table 4 indicates that it's
19 got values of zero, CL minus one, CL minus two,
20 and reserved.

21 BY MR. CHANDLER:

22 Q. Am I correct there's no listing of any
23 half clock cycle latencies or fractional clock cycle
24 latencies for additive latency? In other words,
25 there are only integer values permitted by Table 4

1 for additive latency?

2 MR. LINDSAY: Objection. Outside the
3 scope of direct.

4 THE WITNESS: That's correct.

5 BY MR. CHANDLER:

6 Q. And so turning back to page 24 of
7 Exhibit 1020 at the bottom where it discusses CAS
8 latency, there's also a simple formula that's given
9 for read latency, abbreviated RL, which is that:

10 Read latency is defined as additive
11 latency, abbreviated AL, plus CAS latency,
12 abbreviated CL.

13 Correct?

14 A. Yes, I see that.

15 Q. And as we discussed just a moment ago,
16 additive latency can be zero, in which case, the read
17 latency will just be equal to the value programmed
18 for the CAS latency, correct?

19 A. That is correct with the caveat that
20 there is another term, as I mentioned, called PL,
21 that's at least present in DDR4. I don't recall if
22 it was present in DDR3. But they don't refer to PL
23 in any place that I see here in this passage.

24 Q. And if you turn -- well, just to follow
25 up on that.

1 When additive latency is zero, that means
2 that the permissible read latency values for the DDR3
3 memory device would be five, six, seven, eight, nine,
4 or ten clock cycles, or optionally 11 clock cycles
5 for the 1600 megahertz part; is that fair?

6 MR. LINDSAY: Objection. Outside the
7 scope of direct.

8 THE WITNESS: That's my understanding
9 according to this specification, yes.

10 BY MR. CHANDLER:

11 Q. And you mentioned DDR4.

12 Was DDR4 prior art as of July of 2012?

13 A. I'm sorry, could you repeat that?

14 Q. You mentioned DDR4 a moment ago, and my
15 question is whether DDR4 was prior part as of July of
16 2012.

17 A. I don't remember the DDR4 publication
18 date. The only reason I brought it up is that there
19 is the ability to do a parity check on the command
20 signals coming in in the SDRAM device, and that adds
21 parity latency.

22 I don't recall if that was introduced in
23 DDR4 or if it existed in earlier designs. But
24 I don't see it referred to here.

25 Q. And then I don't think you mentioned DDR4

1 in your declaration. If you do a quick search for
2 DDR4, I don't think it comes up; is that fair?

3 A. Let me check. That is correct.

4 Q. So turn back to page 27 of Exhibit 1020.
5 Let me know when you're there.

6 A. Okay.

7 Q. On page 27 of Exhibit 1020 under the
8 heading "Additive latency" there is reference in the
9 second to last line to another parameter, which is
10 CAS write latency, abbreviated CWL, correct?

11 A. Yes.

12 Q. And then if you go forward to page 30 of
13 Exhibit 1020, in the second paragraph there's a
14 discussion of CAS write latency, abbreviated CWL,
15 correct?

16 A. Yes, there is a discussion of CWL here on
17 page 30.

18 Q. And write latency, abbreviated WL, is
19 defined as additive latency, abbreviated AL, plus CAS
20 write latency, abbreviated CWL, correct?

21 A. Yes, sir, that's correct.

22 Q. And as we discussed a moment ago,
23 additive latency can be zero, in which case, the
24 write latency would simply be equal to the CAS write
25 latency programmed at initialization; is that fair?

1 A. Yes. According to this passage, that is
2 accurate.

3 Q. And if we go back to page 29 of
4 Exhibit 1020, in the bottom right there's a table
5 that shows that the permissible CAS write latency
6 values that can be programmed during initialization
7 are five clock cycles, six clock cycles, seven clock
8 cycles, and eight clock cycles; is that correct?

9 A. Yes, I see that.

10 Q. And on page 30 of Exhibit 120, back in
11 the second paragraph about CAS write latency, in the
12 third line it again states that:

13 DDR3 SDRAM does not support any half clock
14 latencies.

15 Correct?

16 A. Yes, that's correct.

17 Q. If you go forward to page 56 of
18 Exhibit 1020. Let me know when you're there.

19 A. Okay.

20 Q. Page 56 of Exhibit 1020 in Figure 25
21 towards the top of the page, shows an example of the
22 timing of a read operation for a DDR3 memory device
23 after initialization has been completed and the CAS
24 latency and additive latency and other values have
25 been programmed, correct?

1 A. I think that that's accurate.

2 Q. And in this example of Figure 25,
3 additive latency was programmed to be zero and CAS
4 latency was programmed to be five, resulting in a
5 read latency of five clock cycles. Is that correct
6 in this example?

7 I'm looking, for example, at note 1,
8 where it gives the values, and then it also shows the
9 values in the sort of bottom left of the timing
10 diagram.

11 A. Thank you. Yes, I see that now. And,
12 yes, additive latency is programmed at zero and CAS
13 latency is programmed with a value of five.

14 Q. And so the net result is that the read
15 latency is equal to five clock cycles in this
16 example, correct?

17 A. Yes, that would be correct.

18 Q. And so what this timing diagram Figure 25
19 on page 58 -- page 56 of Exhibit 1020 is illustrating
20 is that after the initialization has been completed
21 and the DDR3 memory device performs a normal read
22 operation, in this example, there is a delay of five
23 clock cycles from the time a DDR3 memory device
24 receives the read command until the time that the
25 DDR3 memory device outputs the first piece of data on

1 the DQ data line; is that fair?

2 A. Yes. There's a delay of five clock
3 cycles from when it starts until -- when it starts
4 doing the read operation until the first piece of
5 data for the data burst is available.

6 This does also seem to indicate, just
7 getting back to something we talked about quite a
8 while ago, that there's only one command, as well as
9 one address, on the wires at any point in time.

10 Q. And as shown in this timing diagram, on
11 the command, there's a read command, but then right
12 after it, there's an NOP or a no op command that's
13 issued at the next clock cycle, correct?

14 A. Yes, although it doesn't -- note 3 says
15 it doesn't have to be a no op. That's just an
16 example of what command could be issued in that slot.

17 Q. So for clarity, this Figure 25 does
18 actually show the possibility of one command being
19 sent, and then a second command being sent all on the
20 same line at the next cycle, and then a third command
21 being sent on the same line in the next clock cycle
22 after that, correct?

23 A. Yes, at the next clock cycle. I would
24 agree with that.

25 Q. And as shown by this timing diagram in

1 Figure 25 on page 56 of Exhibit 1020, the read data
2 that's output by the DDR3 memory device on the DQ
3 data line is edge aligned with the DQS data strobe
4 signal, correct, as opposed to center aligned? It's
5 not center aligned, it's intended to be edge aligned
6 because it's a read operation?

7 A. That's right. It appears to be edge
8 aligned, and it is intended to be edge aligned.

9 Q. Go forward to page 71 and let me know
10 when you're there.

11 A. Okay. I'm there.

12 Q. Page 71 of Exhibit 1020 in Figure 71
13 towards the top of the page shows an example of the
14 timing of a write operation for a DDR3 memory device
15 after initialization has been completed and the write
16 latency has been programmed by setting, in this
17 example, additive latency to zero and CAS write
18 latency to five clock cycles, correct?

19 A. Yes, I see that.

20 Q. So in this example, there's a delay of
21 five clock cycles from the time the DDR3 memory
22 device receives the write command until the DDR3
23 memory device receives the first piece of data on the
24 DQ data line, and in this example, that first piece
25 of DQ data is center aligned with the DQS data strobe

1 signal, correct?

2 A. Yes. This shows the write latency of
3 five clocks with the additive latency being
4 programmed to zero, and then the data on the DQ
5 signal lines being available such that the DQS line
6 is aligned with, as best they can, the center of the
7 eye for that data.

8 MR. CHANDLER: I'll just note for the
9 court reporter, I think you understand, but it's
10 w-r-i-t-e. I know that the computer is doing a
11 rough translation, but it's not r-i-g-h-t in
12 this colloquy, it's w-r-i-t-e.

13 THE COURT REPORTER: I've been trying to
14 catch it, but I do know that.

15 MR. CHANDLER: Well, it's confusing
16 because sometimes we are talking about things
17 going off to the right, r-i-g-h-t, but in other
18 situations like this one, we're talking about
19 write as opposed to read.

20 THE COURT REPORTER: Thank you.

21 MR. CHANDLER: All right. I think now is
22 a good time to break for lunch, so why don't we
23 go off the record and negotiate how much time
24 everyone would like.

25 THE VIDEOGRAPHER: Off the record at

1 12:31 p.m. Pacific time.

2 (A recess was taken.)

3 THE VIDEOGRAPHER: On the record at

4 1:16 p.m. Pacific time.

5 BY MR. CHANDLER:

6 Q. Please turn to page 26 of Exhibit 1020,
7 and let me know when you're there.

8 A. Okay.

9 Q. On page 26 of Exhibit 1020, the JEDEC
10 standard for DDR3 memory devices discusses mode
11 register (audio disruption)?

12 (The Court Reporter requested
13 clarification.)

14 MR. CHANDLER: There was an echo.

15 BY MR. CHANDLER:

16 Q. Did you hear me, Dr. Mangione-Smith?

17 A. It sounded like somebody in the
18 background. More than an echo to me. But
19 I definitely heard something, yeah.

20 Q. On page 26 of Exhibit 1020, the JEDEC
21 standard for DDR3 memory devices discusses mode
22 register MR1, which is another one of the registers
23 that must be programmed by the MRS mode register set
24 command during initialization, correct?

25 MR. LINDSAY: Objection. Outside the

1 scope of direct.

2 THE WITNESS: That's my recollection.

3 I think all the mode registers come up in an

4 undefined status. And so, yeah. And based on

5 what we saw previously, I think they do all need

6 to be configured during initialization before

7 actively using the memory to do reads and

8 writes, for example.

9 BY MR. CHANDLER:

10 Q. On the left side of page 26 of

11 Exhibit 1020, the JEDEC standard for DDR3 memory

12 devices permitted write leveling during

13 initialization by setting address bit A7 to 1 in the

14 mode register MR1, correct?

15 A. I'm sorry, I missed the page number.

16 Q. Same page, page 26.

17 A. Oh, same page. I'm sorry, I thought you
18 switched the page.

19 MR. LINDSAY: Objection. Outside the
20 scope of direct.

21 THE COURT REPORTER: Excuse me, I'm
22 having a problem. Can we go off the record for
23 a second?

24 THE VIDEOGRAPHER: Off the record at
25 1:19 p.m. Pacific time.

1 (An off-the-record discussion was held.)

2 THE VIDEOGRAPHER: On the record at
3 1:19 p.m. Pacific time.

4 THE WITNESS: Can you repeat the
5 question, please? Thank you.

6 BY MR. CHANDLER:

7 Q. Sure.

8 As shown on the left side of page 26 of
9 Exhibit 1020, the JEDEC standard for DDR3 memory
10 devices permitted write leveling during
11 initialization by setting address bit A7 to 1 in the
12 mode register MR1, correct?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE WITNESS: Yes, that seems to be
16 what's indicated in this decoding flow chart.

17 BY MR. CHANDLER:

18 Q. And page 42, of Exhibit 1020 provides a
19 discussion starting on that page about how write
20 leveling can be performed with DDR3 memory devices
21 during initialization, correct?

22 MR. LINDSAY: Objection. Outside the
23 scope of direct.

24 THE WITNESS: Yes, it discusses how DDR3
25 SDRAMs support a write leveling feature to

1 compensate for the skew.

2 BY MR. CHANDLER:

3 Q. And the skew you're referring to is
4 caused by the fly-by topology that DDR3 memory
5 modules adopted for the commands, addresses, control
6 signals, and clocks as discussed at the top --

7 (The Court Reporter requested
8 clarification.)

9 BY MR. CHANDLER:

10 Q. And the skew that you're referring to is
11 caused by the fly-by topology that was adopted by
12 DDR3 memory modules for the commands, addresses,
13 control signals, and clocks as discussed at the top
14 of page 42 of Exhibit 1020, correct?

15 A. Yes, that is reflected in text in the
16 first paragraph under write leveling.

17 Q. On page 31 -- actually, strike that.
18 Do you still have page 42 in front of
19 you?

20 A. No, but I'll flip back. Okay.

21 Q. You may have said this, but for clarity,
22 write leveling, if enabled during initialization for
23 DDR3 memory devices, can be used to adjust the strobe
24 to clock relationship in the fly-by topology of DDR3
25 memory modules; is that fair?

1 A. So the second paragraph does say:

2 The memory controller can use the write
3 leveling feature and feedback from DDR3 SDRAM to
4 adjust the DQS to clock relationship.

5 Q. And that could also be referred to as the
6 strobe to clock relationship; is that fair?

7 A. Sure, yes.

8 Q. All right. On page 31 of Exhibit 1020,
9 the JEDEC standard for DDR3 memory devices discusses
10 mode register MR3, which is another one of the
11 registers that must be programmed during
12 initialization by the MRS mode register set command,
13 correct?

14 A. Yes. I see there a description of what
15 mode register 3 configures.

16 Q. And as shown by the table on the bottom
17 left of page 31, mode register MR3 is selected by the
18 address lines BA1 and BA0 being set to 1 or high,
19 correct?

20 MR. LINDSAY: Objection. Outside the
21 scope of direct.

22 THE WITNESS: That seems to be what this
23 table is indicating.

24 BY MR. CHANDLER:

25 Q. On the bottom of page 31 of Exhibit 1020,

1 the JEDEC standard explains that DDR3 memory devices
2 include a multipurpose register, abbreviated MPR,
3 that could be used to read out a predefined system
4 timing calibration bit sequence, correct?

5 A. Yes, I see that.

6 MR. LINDSAY: Objection. Outside the
7 scope of direct.

8 THE WITNESS: I see that.

9 BY MR. CHANDLER:

10 Q. And the standard goes on to explain in
11 the next sentence that the MPR multipurpose register
12 can be enabled by issuing an MRS mode register set
13 command to mode register MR3 with the address bit A2
14 set to 1, consistent with what's shown in the table
15 above the text on page 31 of Exhibit 1020, correct?

16 MR. LINDSAY: Objection. Outside the
17 scope of direct.

18 THE WITNESS: That's correct. That's
19 what it says. But I have no particular
20 recollection of studying this passage of the
21 standard.

22 BY MR. CHANDLER:

23 Q. Starting on page 48 of Exhibit 1020, the
24 JEDEC standard for DDR3 memory devices provides some
25 more details about the multipurpose register; is that

1 fair?

2 MR. LINDSAY: Objection. Outside the
3 scope of direct.

4 THE WITNESS: Yes. There is a
5 section 4.10 which is labeled "Multi Purpose
6 Register."

7 BY MR. CHANDLER:

8 Q. And as stated at the top of page 48 of
9 Exhibit 1020, if enabled, the MPR multipurpose
10 register in the DDR3 memory devices can be used to
11 read out a predefined system timing calibration bit
12 sequence, correct?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE WITNESS: It does say the
16 multipurpose register function is used to read
17 out a predefined system timing calibration bit
18 sequence. Maybe that means when it's enabled or
19 not, I'm not sure. I don't recall reviewing
20 this material previously.

21 BY MR. CHANDLER:

22 Q. Well, the only point I was trying to make
23 is, as we saw back on page 31, it's not required to
24 use the multipurpose register during initialization;
25 it's an option. Another option would be to not use

1 it before proceeding to normal operation; is that
2 fair?

3 MR. LINDSAY: Objection. Outside the
4 scope of direct.

5 THE WITNESS: Maybe. I don't recall
6 seeing that it was an option. We talked about
7 how some of the MPR values need to be set during
8 initialization. But I don't know a full list of
9 them.

10 BY MR. CHANDLER:

11 Q. If you turn back to page 31 of
12 Exhibit 1020, if the address bit A2 is set to zero in
13 mode register MR3, then there will be normal
14 operation according to the standard, correct?

15 MR. LINDSAY: Objection. Outside the
16 scope of direct.

17 THE WITNESS: Yes, that's correct.
18 I just don't know if you needed to put in the
19 other mode during initialization or not.

20 BY MR. CHANDLER:

21 Q. On page 50 of Exhibit 1020, there the
22 heading 4.10.4, the JEDEC standard for DDR3 memory
23 devices again states that the MPR multipurpose
24 register can be used to do system level read timing
25 calibration based on predetermined and standardized

1 patterns, correct?

2 MR. LINDSAY: Objection. Outside the
3 scope of direct.

4 THE WITNESS: Yes, I see that following
5 the word "description."

6 BY MR. CHANDLER:

7 Q. And then on the next page, which is
8 page 51 of Exhibit 1020, in the second bullet point,
9 the JEDEC standard for DDR3 memory devices explains
10 that the memory controller can repeat these
11 calibration reads until read data capture at the
12 memory controller is optimized, correct?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE WITNESS: Yes, it says that.
16 Although, my understanding is that nothing in
17 this section is a -- is required by the
18 standard.

19 BY MR. CHANDLER:

20 Q. And then as shown in the fourth bullet
21 point on the same page, which is page 51 of
22 Exhibit 1020, after that read calibration is done,
23 the address bit A2 can be set to the bit value of
24 zero to get back to normal operation, meaning, that
25 all subsequent read and write accesses will be

1 regular reads and writes from or to the DRAM array;
2 is that fair?

3 MR. LINDSAY: Objection. Outside the
4 scope of direct.

5 THE WITNESS: Not quite. I wouldn't say
6 that. I would say that the fourth bullet point
7 does indeed say:

8 MRS MR3, opcode A2 equals zero and A1 to
9 zero equals valid data but values don't care.

10 And then below that, it says:

11 All subsequent read and write accesses
12 will be regular read and writes from/to the DRAM
13 array.

14 BY MR. CHANDLER:

15 Q. And that bit value of A2 being set to
16 zero, that's what we discussed just a moment ago on
17 page 31 of Exhibit 1020 that indicates normal
18 operation, correct?

19 MR. LINDSAY: Objection. Outside the
20 scope of direct.

21 THE WITNESS: That is my recollection,
22 yes.

23 BY MR. CHANDLER:

24 Q. Could you turn to page 59 of
25 Exhibit 1020? Let me know when you're there.

1 A. Okay. I'm there.

2 Q. So page 59 of Exhibit 1020 is where the
3 JEDEC standard for DDR3 memory devices provides some
4 more details about the timing for read operations; is
5 that fair?

6 MR. LINDSAY: Objection. Outside the
7 scope of direct.

8 THE WITNESS: Yes. It's -- the section
9 4.13.2.2 is titled "Read Timing; Data Strobe to
10 Data Relationship."

11 BY MR. CHANDLER:

12 Q. And in Figure 29 on this page, there's a
13 timing diagram that includes a line for the clock CK,
14 the command, there's a line for the address, there's
15 a line for the DQS strobe signals, and then at the
16 bottom there's a line for all the DQ data lines
17 collectively; is that fair?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct.

20 THE WITNESS: It has basically those
21 labels. I'm not sure what DQ -- all DQ
22 collectively means. And my understanding is
23 that this figure is not showing required
24 behavior according to JEDEC.

25

1 BY MR. CHANDLER:

2 Q. What do you mean by that? I mean, on the
3 one hand, I understand that Figure 29 is just an
4 example and that there are other examples.

5 But what do you mean by Figure 29 doesn't
6 show required behavior?

7 A. My recollection is that JEDEC says that
8 examples in figures do not describe or illustrate
9 required behavior in any implementation.

10 Now, that being said, it's also my
11 understanding that they can go back and say, oh, by
12 the way, Figure 29 is exactly how it needs to
13 operate. But it doesn't appear that they've done
14 that here.

15 Q. Well, just to be clear, to take an
16 example, we discussed earlier that during
17 initialization, read latency can be set to five clock
18 cycles by setting additive latency to zero and CAS
19 latency to five, correct? That's, I think, a
20 permissible example?

21 A. Yes, I believe so.

22 Q. And if that's done, which is what
23 Figure 29 is showing an example of happening, once
24 that's done, the JEDEC standard requires the read
25 latency to be five clock cycles, and Figure 29

1 illustrates what the read latency of five clock
2 cycles is required to be.

3 Isn't that sort of a fair explanation of
4 Figure 29 and other figures like it in Exhibit 1020?

5 MR. LINDSAY: Objection. Form.

6 THE WITNESS: JEDEC has been pretty
7 clear, we can go back and look for the language,
8 that figures and examples do not show required
9 behavior. That's not to say that they don't
10 match expected and/or required behavior, but
11 they do not show required behavior.

12 BY MR. CHANDLER:

13 Q. And I'm not saying that it's required
14 that you set the CAS latency to five.

15 But isn't it fair that if the CAS latency
16 is set to five and the additive latency is set to
17 zero as this example in the notes of Figure 29, it is
18 required that there be a latency of five clock cycles
19 between the lead data and the first -- read command
20 and the first piece of read data that comes out?

21 That's not optional, I mean, right? That's required.

22 I mean, if read latency set to five, it's
23 against JEDEC for the memory device to say, well,
24 I want to output it at seven or ten or some other
25 number of clock cycles; isn't that fair?

1 MR. LINDSAY: Objection. Form.

2 THE WITNESS: Yeah, I think that's fair.
3 I'm just saying, not as a consequence of what
4 appears in Figure 29.

5 BY MR. CHANDLER:

6 Q. Can you explain a little bit at a high
7 level the difference between what a DQS data strobe
8 signal is and a clock signal?

9 A. A clock signal is a signal that has a
10 certain periodicity or frequency, and that is used to
11 provide a regular timing source that controls
12 synchronous digital circuitry.

13 And you asked for a DQS signal for
14 contrast, right?

15 Q. (Nodded head.)

16 A. Okay. A DQS signal has none of those
17 characteristics. I mean, it's not -- it has no
18 particular frequency. It is intended to be used for
19 grabbing ahold of some data at a particular point in
20 time, but just very different.

21 Q. Well, to be fair, under the JEDEC
22 standard, it's not entirely correct to say that DQS
23 has no particular frequency.

24 There's a relationship between the
25 frequency of the DQS strobe signal when it's being

1 used and the frequency of the clock signal, correct?

2 MR. LINDSAY: Objection. Form.

3 THE WITNESS: No.

4 BY MR. CHANDLER:

5 Q. Why not?

6 A. There isn't.

7 Q. So you're trying to tell me that
8 Figure 29 does not show any relationship between the
9 frequency of the DQS strobe signal and the frequency
10 of the clock signal?

11 A. Yeah. Figure 29 clearly indicates that
12 the DQS has a frequency of zero for much of the
13 figure, and then it does -- its frequency changes,
14 and then it goes back to zero.

15 Q. That's what I was getting at. So --

16 A. And it -- go ahead.

17 Q. So the DQS strobe signal, at certain
18 points it can stop, and then at other points in time
19 it can start up again. And when the DQS strobe
20 signal starts up and starts running, the frequency of
21 the DQS strobe signal is intended, at least, to match
22 the frequency of the clock signal; is that fair?

23 A. I wouldn't say that. I would say that
24 the -- there is a relationship between the edges of
25 the DQS signal and the clock. But when you're active

1 for eight time periods, that's, in my opinion, too
2 short to say it's got a certain particular frequency.
3 It is, to some extent, synchronized with the clock.

4 Q. So, for example, in Figure 29 of
5 Exhibit 1020, the DQS strobe signal is intended to be
6 synchronized with the clock signal between time T5
7 and time T8, correct?

8 A. Yes. I mean, not exactly synchronized,
9 but there is a clear relationship between the two,
10 yeah.

11 Q. And then I think, as you said before, the
12 clock -- I forget exactly the word you used, whether
13 you said it's periodic or it's free running, but the
14 clock signal is going to be going up and down,
15 essentially, indefinitely. Whereas, that's not the
16 case for the strobe signal. I think, as you said,
17 the strobe signal sometimes it's not transitioning at
18 all even though the clock is transitioning, correct?

19 MR. LINDSAY: Objection. Form.

20 THE WITNESS: Yes, I think that's
21 accurate. The clock signal is understood to be
22 running all the time while the memory module is
23 operatable. Of course, they often support a low
24 power down state where the clock might stop.
25 But in operation, the clock should be running.

1 And then the DQS signals are asserted
2 periodically. Every once -- without a
3 periodicity, every once in awhile. Whenever a
4 read or a write transaction is being done, only
5 then they will be used.

6 BY MR. CHANDLER:

7 Q. So in Figure 29 on page 59 of
8 Exhibit 1020, it illustrates a read command being
9 received by the DDR3 memory device at time T0, and
10 then approximately five clock cycles later, given the
11 CAS latency, CL, was programmed to be five during
12 initialization and additive latency, AL, was
13 programmed to be zero, the DDR3 memory device starts
14 to output data signals on the DQ data line starting
15 at approximately time T5; is that fair?

16 MR. LINDSAY: Objection. Form.

17 THE WITNESS: That seems to be what it's
18 indicating. But, for example, it's got two
19 lines, DQ last data valid and DQ first data no
20 longer valid. I don't know -- I'm just saying,
21 I don't know what those are.

22 BY MR. CHANDLER:

23 Q. In this example of Figure 29 on page 59
24 of Exhibit 1020, if you look at the line for the DQS
25 strobe signal, it is driven low at time T4, which is

1 before the first piece of DQ data is output by the
2 memory device, and then the DQS strobe signal starts
3 to have a periodic transitioning at time T5 through
4 at least time T8, correct?

5 A. Yes, that seems to be accurate.

6 Q. And then I think you referred to a little
7 bit of a misalignment, if you will, between the edge
8 of the DQ data signal and the edge of a DQS strobe
9 signal.

10 And Figure 29 of Exhibit 1020 actually
11 has a parameter that's referring to that slight
12 misalignment, and that parameter is tDQSQ, correct?

13 A. I see that on the figure.

14 Q. And the parameter tDQSQ is illustrating
15 in Figure 29 of Exhibit 1020 a difference -- slight
16 difference in time between the transition of the DQS
17 strobe signal and the corresponding transition of the
18 DQ data signal for the DDR3 memory device, correct?

19 A. That seems to be reflected in this
20 figure, yes.

21 Q. And then footnote 6 of Figure 29 states
22 that tDQSQ defines the skew between the DQS strobe
23 signals and the data, correct?

24 A. Yes, that's what it says.

25 Q. And the JEDEC standard for DDR3 memory

1 devices does not permit a large amount of skew
2 between the DQS strobe signal and the DQ data signal.

3 To the contrary, it requires a very tight
4 tolerance between the DQS strobe signal and the DQ
5 data signal as reflected by the permissible range of
6 values for tDQSQ; is that fair?

7 A. I have no idea.

8 Q. So, for example, if you look on page 164
9 of Exhibit 1020, the permissible values for tDQSQ and
10 the DDR3 standard range from 200 picoseconds to
11 100 picoseconds, correct?

12 A. This is page 164?

13 Q. Yes, there's the heading "Data Timing"
14 and there's the first row. And if you look in the
15 second column, the symbol is tDQSQ. And the
16 permissible range -- the maximum range on the entire
17 range for tDQSQ is 200 picoseconds, correct?

18 MR. LINDSAY: Objection. Form. Outside
19 the scope of direct.

20 THE WITNESS: It says that there is a --
21 the options configurations listed here, there is
22 a maximum of 200 picoseconds.

23 BY MR. CHANDLER:

24 Q. And what's the range between picoseconds
25 and nanoseconds? I mean, what are we talking about

1 here?

2 A. I think it's off by a thousand, so
3 another factor of 10 to the 3, is my recollection.

4 Q. So JEDEC standard for DDR3 memory devices
5 does not permit a large amount of skew between the
6 DQS strobe signal and the DQ data signal. There's a
7 limit on amount of skew that's permitted, and that's
8 what the tDQSQ parameter is, correct?

9 MR. LINDSAY: Objection. Outside the
10 scope of direct.

11 THE WITNESS: I wouldn't say that.

12 BY MR. CHANDLER:

13 Q. And why not?

14 A. Well, as I mentioned to begin with,
15 I have no recollection of reviewing that figure or
16 this value tDQSQ. I don't know what else it says
17 about that value potentially elsewhere in the
18 specification.

19 And in any case, even if this was
20 precisely where it was the only place or this was a
21 controlling location, I would say, reading this for
22 the first time in my recollection, this passage, it
23 appears to say that there is a range of a minimum of
24 zero and a maximum of 200 picoseconds. But whether
25 that's large or not is in the eye of the beholder.

1 Q. Well, in the eye of your beholder, as
2 shown in Exhibit 1076 on page 65, there's a very
3 tight tolerance between DQS strobe signal and the DQ
4 data signal, correct?

5 A. 1076, which page?

6 Q. 65.

7 A. Okay.

8 MR. LINDSAY: Objection. Outside the
9 scope of direct.

10 THE WITNESS: Yes, I see it characterized
11 now as a very tight tolerance.

12 BY MR. CHANDLER:

13 Q. So it would be fair to say that the JEDEC
14 standard for DDR3 memory devices does not permit a
15 large amount of skew between the DQS strobe signal
16 and DQ data signal.

17 To the contrary, it could fairly be
18 characterized as requiring a very tight tolerance
19 between the DQS strobe signal and the DQ data signal,
20 correct?

21 MR. LINDSAY: Objection. Outside the
22 scope of direct.

23 THE WITNESS: Yes, it requires a very
24 tight tolerance.

25

1 BY MR. CHANDLER:

2 Q. If you could turn back to page 59 of
3 Exhibit 1020? Let me know when you're there. It is
4 Figure 29 again. Do you have it in front of you?

5 A. Yes. You said -- yes, almost. Okay.
6 I'm there.

7 Q. In Figure 29 on page 59 of Exhibit 1020,
8 the JEDEC standard for DDR3 memory devices shows the
9 parameters TR3 and tRPST, which I would pronounce
10 tR Post, correct? And that's on the line for the DQS
11 strobe signal?

12 A. I see pre. Yes, okay. I see the tRPST
13 as well.

14 Q. And those parameters are related to
15 the -- what could be described as the preamble and
16 the post-amble of the DQS strobe signal for a read
17 command; is that fair?

18 A. Yes, I think that's fair.

19 Q. And in particular, the DQS strobe signal
20 for a DDR3 memory device is driven low during the
21 time periods tRPRE and tRPST; is that fair?

22 A. Yes, that's my understanding.

23 Q. And the read preamble tRPRE lasts for
24 approximately one full clock cycle, while the
25 post-amble tRPST lasts for approximately half a clock

1 cycle; is that fair?

2 A. Yes, I think that's fair.

3 Q. All right. Why don't you go forward to
4 page 68 of Exhibit 1020.

5 A. Okay.

6 Q. So starting on page 68 of Exhibit 1020,
7 the JEDEC standard for DDR3 memory devices describe
8 write operations, including various timing parameters
9 for write operations, correct?

10 A. Yes, that's correct.

11 Q. In section 4.14.2.2, on page 68 of
12 Exhibit 1020, the JEDEC standard for DDR3 memory
13 devices warns that if the data to strobe timing
14 requirements are violated for any of the strobe edges
15 associated with a write command, then the wrong data
16 might be written to memory, correct?

17 MR. LINDSAY: Objection. Outside the
18 scope of direct.

19 THE WITNESS: Yes, that's a reasonable
20 characterization of what it says in that
21 passage.

22 BY MR. CHANDLER:

23 Q. And it would be reasonable to say a
24 person of ordinary skill in the art would try to
25 avoid having that happen, would try to avoid having

1 the wrong data written to memory as a result of the
2 data to strobe timing requirements being violated; is
3 that fair?

4 MR. LINDSAY: Objection. Outside the
5 scope of direct.

6 THE WITNESS: Yes, that's fair.

7 BY MR. CHANDLER:

8 Q. And is it fair to say that one of the
9 reasons that the data to strobe timing requirements
10 are important for DDR3 memory devices is because they
11 do not have a built-in mechanism to center the DQS
12 data strobe signal into the data eye?

13 A. I'm sorry, could you repeat the question?

14 Q. Is it fair to say that one of the reasons
15 that the data to strobe timing requirements are
16 important for DDR3 memory devices is because they do
17 not have a built-in mechanism to center the DQS data
18 strobe signal into the data eye?

19 A. I think that's fair, yeah.

20 Q. On page 69 of Exhibit 1020, the JEDEC
21 standard for DDR3 memory devices shows Figure 43,
22 which provides an example of write timing definitions
23 and parameters, correct?

24 MR. LINDSAY: Objection. Outside the
25 scope of direct.

1 THE WITNESS: I'm not sure if you're
2 waiting for me. I said -- I stepped again on
3 the objection.

4 But, yes, that's -- it's talking about
5 write timing definitions and parameters.

6 BY MR. CHANDLER:

7 Q. And in the example on Figure 43 of
8 Exhibit 1020, there is a write command received by
9 the DDR3 memory device at time T0, and then
10 approximately five clock cycles later, given that CAS
11 write latency, CWL, was programmed to be five during
12 initialization and additive latency, AL, was
13 programmed to be zero, the DDR3 memory device starts
14 to receive data signals on the DQ data line starting
15 at approximately time T5; is that fair?

16 MR. LINDSAY: Objection. Form. Outside
17 the scope of direct.

18 THE WITNESS: Yes, I see that in the
19 figure.

20 BY MR. CHANDLER:

21 Q. And then Figure 43 on page 69 of
22 Exhibit 1020, it provides three different timing
23 scenarios. So I want to focus for now on the middle
24 of the figure corresponding to the scenario where the
25 DQS data strobe signal has the label next to it

1 tDQSS, parentheses, nominal, understood?

2 A. Yes, understood.

3 Q. And the nominal portion of Figure 43 of
4 Exhibit 1020 shows that on the DQS strobe lines,
5 there's a preamble before any of the data is
6 transmitted, correct?

7 A. Yes, that's correct.

8 Q. And after the preamble period labeled
9 tWPRE, the DQS strobe signal transition is aligned
10 with the center of the data eye on the DQ line; is
11 that fair?

12 A. It looks like it's aligned with the
13 center of the DQ data eye.

14 Q. And then after the last transition on the
15 DQS strobe line, there is a post-amble period labeled
16 tWPST, which I would pronounce tW Post, where the DQS
17 signal is driven low, correct?

18 A. Yes, that appears to be correct for this
19 figure.

20 Q. And, again, the write preamble tWPRE is
21 about one clock cycle, and the write post-amble
22 period tWPST is approximately half a clock cycle,
23 correct?

24 A. Yes, I think that's accurate.

25 Q. And during the write preamble period,

1 tWPRE, the DQS strobe signal transitions from high to
2 low, but there's no corresponding data on the DQ line
3 at that point in time, correct?

4 A. Figure 43 seems to illustrate at the time
5 of the transition during the write preamble where the
6 DQS signal goes from high to low, there at that point
7 in time there is no data on the DQ lines themselves.

8 Q. And for clarity, that's at approximately
9 time T4 and a half; is that fair?

10 A. Sure.

11 Q. Could you turn back to the '608 patent
12 marked as 1001? Let me know when you have it in
13 front of you.

14 A. Okay.

15 MR. CHANDLER: Do you know what? Why
16 don't we take a -- just like a five-minute break
17 before we get back to the '608 patent.

18 THE VIDEOGRAPHER: Off the record at
19 2:00 p.m. Pacific time.

20 (A recess was taken.)

21 THE VIDEOGRAPHER: On the record at
22 2:09 p.m. Pacific time.

23 BY MR. CHANDLER:

24 Q. Please turn to Figure 15 of the
25 '608 patent marked as Exhibit 1001. Let me know when

1 you're there.

2 A. Okay. I'm there.

3 Q. And have you reviewed Figures 15 and 16
4 of the '608 patent marked as Exhibit 1001, and do you
5 believe that you understand them?

6 A. Yes.

7 Q. All right. I'd like to introduce a new
8 exhibit, which I'll mark as Exhibit 1080, which is
9 really just annotated versions of Figures 15 and 16
10 of the '608 patent marked as Exhibit 1001. And then,
11 for ease of reference, on the left side I've
12 reprinted the corresponding discussion about those
13 figures from the specification from column 16,
14 line 47 through column 17, line 60.

15 Let me know when you have Exhibit 1080 in
16 front of you, and let me know if you understand
17 generally what it's intending to represent.

18 (Exhibit 1080 was marked and/or
19 identified.)

20 THE WITNESS: Yes, I have 1080 in front
21 of me. And I -- yes, I understand what the
22 underlying figure is intending to illustrate.

23 BY MR. CHANDLER:

24 Q. And on the first page of Exhibit 1080,
25 I've annotated Figures 15 and 16 of the '608 patent

1 to show the direction of a read operation, and I've
2 annotated the second page of Exhibit 1080 to show the
3 direction of a write operation, understood?

4 A. Yes, I believe I see that.

5 Q. And do you agree that in Figures 15 and
6 16 of the '608 patent, the read direction is to the
7 left and the right direction is to the right,
8 r-i-g-h-t?

9 A. Yes, I see that.

10 Q. Figure 15 of the '608 patent illustrates
11 a DQS routing circuit, correct?

12 A. I believe so. Yeah, that's my
13 recollection.

14 Q. And it's explained, for example, in
15 column 17, around line 14 of the '608 patent, the DQS
16 routing circuit of Figure 15 selects either a read
17 strobe signal received via DQS pin 1502A or a read
18 strobe signal received via DQS pin 1502B, based on
19 one or both of the enable signals ENA or ENB which
20 are highlighted in red in Exhibit 1080, correct?

21 A. Yes, I see that.

22 Q. And for a read command, the ENB signal
23 also has to disable the transmitter 1530B discussed
24 in column 17, around line 4, because that transmitter
25 is for write commands, not read commands; is that

1 fair?

2 A. Yeah, generally. It would likely cause a
3 collision along the lines of what we had discussed
4 previously.

5 Q. That's what I was going to say, is that a
6 person of ordinary skill in the art would understand
7 that you would want to disable transmitter 1530B
8 during a read operation because that transmitter's
9 pointing in the write direction and, therefore, could
10 cause a collision potentially, correct?

11 A. Yeah. I'm not sure why there is separate
12 control for 1530A and 1530B. It seems like -- well,
13 for a read operation they should both be off. But,
14 I guess, if nothing else is driving the YA DQS signal
15 it doesn't really matter if 1530A were to be on.

16 Q. But it would also be reasonable for a
17 read command to disable the transmitter 1530A using
18 the ENA signal because, again, that transmitter is
19 pointing in the write direction, so you would want to
20 avoid collisions, and also there could potentially be
21 power savings benefit as well, correct?

22 A. There certainly would be some power
23 saving benefits. All I was saying is that it seems
24 to me if the YA DQS signal -- if only one of those YA
25 or YB DQS signals can be asserted at a time, and

1 I think that's probably the case, you don't have to
2 avoid collision. But as you say, it still would not
3 be a bad idea in order to save power.

4 Q. As explained in column 17, around
5 line 15, in Figure 15 of the '608 patent the selected
6 read strobe signal is delayed by a delay circuit 1560
7 and a sampler circuit 1570 in accordance with the
8 delay signal DS and a clock signal CK0; is at that
9 fair?

10 A. Yes, I believe that's fair.

11 Q. And the output of the sampler circuit
12 1570 is coupled to a transmitter 1580, correct, as
13 shown in Figure 15 of the '608 patent?

14 A. That's correct.

15 Q. And a person of ordinary skill in the art
16 would understand that 1580 and Figure 15 of the
17 '608 patent is a tri-state buffer that would be
18 enabled during read operations and should be disabled
19 during write operations, again, to avoid collisions
20 and if for no other reason but to save power; is that
21 fair?

22 A. Yes, I think that's fair.

23 Q. Now, a tri-state buffer as we discussed
24 previously has an input signal, an output signal, and
25 a control input signal; is that fair?

1 A. Yes, I think that's fair.

2 Q. And Figure 15 of the '608 patent doesn't
3 expressly show any control input signal to the
4 tri-state buffer 1580, but it'll be reasonable for a
5 person of ordinary skill in the art to understand how
6 and when to enable and disable the tri-state buffer
7 1580; is that fair?

8 A. I think that that's fair, yes.

9 Q. In Figure 15 of the '608 patent the
10 output of the sampler circuit 1570 is also coupled to
11 the RDQS input of the sampler circuit 1670 in
12 Figure 16 as shown by the vertical dashed orange line
13 in Exhibit 1080, correct?

14 A. I'm just flipping back to the original
15 circuits to be sure. Yes. The -- an output of the
16 sampler is shown on Figure 15 being labeled RDQS and
17 emerging from the top of Figure 15, and then
18 entering -- in Figure 16, entering from the bottom
19 into element 1670.

20 But it looks like I answered your
21 question in reverse. You were probably asking with
22 regards to -- well, why don't I leave it there. If
23 I didn't answer your question, repeat it or rephrase
24 and I'll do my best.

25 Q. Figure 16 of the '608 patent illustrates

1 a DQ routing circuit, correct?

2 A. Yes, I think that's fair.

3 Q. And the DQ routing circuit in Figure 16
4 of the '608 patent receives the same clock signal
5 CK0, delay signal DS, and control signals ENA and ENB
6 as the DQS routing circuit of Figure 15; is that
7 fair?

8 A. Yes, that's fair.

9 Q. And as explained in column 17, around
10 line 53, the control signals ENA and ENB can select
11 the DQ pin 1602B in Figure 16, which corresponds to
12 the selected strobe signal on DQS pin 1502B in
13 Figure 15 as annotated in Exhibit 1080; is that fair?

14 A. Perhaps. Give me a moment to refresh my
15 mind on one aspect of this. Okay.

16 Now, I'm sorry, could you repeat the
17 question?

18 Q. The control signals ENA and ENB can
19 select the DQ pin 1602B in Figure 16, which
20 corresponds to the selected strobe signal on DQS pin
21 1502B in Figure 15, as illustrated in Exhibit 1080,
22 correct?

23 A. There are two different DQS output pins,
24 1502A and B and 1602A and B but they're in different
25 embodiments.

1 Q. Well, to be clear, so Figure 16 is the
2 DQ, not the DQS, the DQ data, and then Figure 15 is
3 the DQS strobe, correct?

4 A. That's correct.

5 Q. And so in the situation where the ENA and
6 ENB enable signals have selected 1602B for the DQ
7 data signal, that would correspond to 1502B being
8 selected for the DQS strobe signal; is that fair?

9 A. If these two embodiments were put
10 together, yeah, I would expect that when the B path
11 of 16 was activated, the B path of 15 would be
12 activated.

13 Q. And just so we're on the same page, when
14 you say these two embodiments, what are you getting
15 at? Because the memory module needs both DQ data and
16 DQS strobe. So it's not like Figures 15 and 16 are
17 alternatives.

18 Figures 15 and 16 can be used together in
19 the same embodiment; is that fair?

20 A. In the same embodiment of the complete
21 invention, yes. They're different embodiments of
22 those -- well, they're embodiments of the sub
23 portions. You could put them together. You could
24 presumably practice the invention by using a
25 different structure, although I don't have one in

1 mind as I sit here.

2 Q. The clock signal CK0 and the delay signal
3 DS control the delay circuit 1660 in Figure 16
4 similar to how they control the delay circuit 1560 in
5 Figure 15; is that fair?

6 A. CK0 and DS are shown controlling the
7 delayed circuit 1660 and 1560, presumably in a
8 similar, but maybe not identical manner.

9 Q. In your opinion, would you say that the
10 delay signal DS is in the data path?

11 A. I would say that that delay signal when
12 it is received by 1660, the information within it is
13 certainly within the data path. However, there also
14 is a line showing how the -- that information is
15 conveyed to 1660, and I would not say those wires are
16 in the data path.

17 Q. And would it be fair to say that there is
18 a different structure not shown in Figure 15 or
19 Figure 16 that generates the value for the delay
20 signal DS?

21 A. Yes. It has to come from somewhere, and
22 it is not -- it's coming from somewhere else. So
23 there has to be some other circuit that generates it.

24 Q. And in your opinion, is the other circuit
25 that generates the delay signal DS in the data path?

1 A. It depends on where that signal
2 originates from, but I don't see it originating
3 within the data path. And so I would expect it's at
4 least anticipated that it's not in the data path, or
5 that it may not be in the data path.

6 Q. In Figure 16, the sampler circuit 1670
7 uses the RDQS strobe signal to sample the output of
8 the delay circuit 1660; is that fair?

9 A. Yes, I see that.

10 Q. And in Figures 15 and 16 of the
11 '608 patent, the RDQS strobe signal is different from
12 the clock signal CK0; is that fair?

13 A. Yes, that's fair. The RDQS will be
14 different from the clock signal.

15 Q. And a person of ordinary skill in the art
16 would understand how to sample using a clock signal
17 such as CK0 and how to sample using a strobe signal
18 such as RDQS; is that fair?

19 A. Depending on the context of what they
20 wanted to sample, yes, clocks are often used for
21 sampling and, similarly, strobe signals are often
22 used to control sampling.

23 Q. The '608 patent does not go into any
24 further details about how the sampler circuit 1570
25 uses the clock signal CK0 to sample signals or how

1 the sampler circuit 1670 uses the RDQS strobe signal
2 to sample signals; is that fair?

3 A. I would have to double-check. I don't
4 recall as I sit here.

5 Q. I mean, I did a quick search for 1570 and
6 1670 and I only saw the one sentence about sampling
7 without further details.

8 Is there anything else that you're aware
9 of or that you see on a quick review?

10 A. Not that I'm aware of, but it's a 43-page
11 patent. If I was aware of something as I sit here,
12 I would certainly mention it.

13 Q. And to be clear, you've read the 43-page
14 '608 patent, right?

15 A. Yes, I have.

16 Q. And you also read the 40-some-odd page
17 '506 patent that has the same specification and
18 figures as the '608 patent, correct?

19 A. That's correct.

20 Q. On page 2 of Exhibit 1080, that shows the
21 annotation of Figures 15 and 16 in the write
22 direction. Is that fair, as we discussed a moment
23 ago?

24 A. Okay. I'm reoriented. Could you repeat
25 the question?

1 Q. Do you have in front of you page 2 of
2 Exhibit 1080, which is intended to annotate
3 Figures 15 and 16 in the write direction, w-r-i-t-e?

4 A. Yes, I do now. Yes.

5 Q. As explained in column 16, starting
6 around line 57, in the DQS routing circuit of
7 Figure 15, which is shown at the bottom of page 2 of
8 Exhibit 1080, the strobe signal is received at DQS
9 pin 1501 on the left, and then buffered by write
10 strobe buffer 1510; is that fair?

11 A. No, I don't think that's accurate. Write
12 strobe path includes a -- so you were suggesting that
13 it -- the strobe is received, if I recall and heard
14 right, 6 -- 1602B, and then buffered by 1610.

15 Q. No.

16 A. Sorry.

17 Q. I said 1501 and then 1510. And I can ask
18 the question again.

19 But just to point you in the right
20 direction first, page 2 of Exhibit 1080, Figure 15 at
21 the bottom, I'm essentially I'm going to be tracing
22 the dashed orange line, starting at 1501 and then to
23 1510.

24 But are you with me, and then I'll ask
25 the question in a nice neat --

1 A. I am with you, yes.

2 Q. As explained in column 16, starting
3 around line 57, in the DQS routing circuit of
4 Figure 15 shown at the bottom of page 2 of Exhibit
5 1080, the strobe signal is received at DQS pin 1501
6 on the left and then buffered by write strobe buffer
7 1510, correct?

8 A. Yes, that is correct.

9 Q. And although it's not shown in Figure 15
10 of the '608 patent, a person of ordinary skill in the
11 art would understand that during a write operation,
12 that you would want to have a control signal that
13 disables the tri-state buffer 1580 to avoid potential
14 conflicts with the incoming strobe signal and also
15 for the benefit of conserving power; is that fair?

16 A. Yes, that's fair.

17 Q. And then as explained in column 16,
18 starting around line 57, in Figure 15 of the '608
19 patent, after the strobe signal leaves buffer 1510,
20 it is sampled by receiver 1520 according to the clock
21 signal CK0, correct?

22 A. Yes, that's correct.

23 Q. Is it fair to say that when the strobe
24 signal is sampled by the clock signal, that that
25 process would create some amount of delay of the

1 strobe signal?

2 A. It depends. There are latches or
3 registers. I think that's what -- that has to be an
4 element of 1620. There is circuitry there. There
5 will be some amount of delay. Depending on how the
6 sampler is implemented, it may be so small as to be
7 trivial.

8 Q. And focusing just for a moment on 1520,
9 where the strobe is sampled by 1520 using the clock
10 signal CK0 highlighted with the dashed red line in
11 Exhibit 1080 on page 2, what is your expectation
12 about whether the sampling occurring at 1520 would
13 result in some delay of the strobe signal?

14 A. I believe it would introduce some delay
15 in the strobe signal. I don't know that it would
16 introduce a significant enough delay that it would
17 have to be accounted for in the rest of the
18 circuitry.

19 Q. And would it be fair to say that the
20 output of 1520 only changes at the time that the
21 clock signal CK0 transitions?

22 A. I would expect that there is a CK0
23 transition that is associated with the output
24 changing. But as you said, or suggested, the
25 disclosure of how those various samplers work is

1 pretty thin.

2 So there will be a clock edge that's
3 associated with an output change, I just don't know
4 exactly how soon the output will change based on the
5 associated clock edge.

6 Q. As explained in column 16 of the
7 '608 patent, starting around line 60 and carrying
8 over to the top of column 17, in Figure 15, the ENA
9 and ENB control signals select which of the write
10 strobe transmitters 1530A and 1530B are used to
11 transmit the sampled strobe signal from the receiver
12 1520, correct?

13 A. Yes, that's correct.

14 Q. In the write direction, w-r-i-t-e, the
15 delay of the strobe signal is set by the receiver
16 1520 in accordance with the clock signal CK0; is that
17 fair?

18 A. Could you repeat that again?

19 Q. In the write direction, w-r-i-t-e, the
20 delay of the strobe signal is set by the receiver
21 1520 in accordance with the clock signal CK0; is that
22 fair?

23 A. If there's some discussion about that you
24 can point me to, I'd be happy to review it. But like
25 I said, I don't recall any discussion of what kind of

1 sampler is done there and, consequently, what kind of
2 delay is introduced.

3 Whatever delay is introduced will be
4 timed out -- will begin, at least, when -- with an
5 associated clock edge. But it's not determined by
6 the clock.

7 Q. If you look, for example, at column 16,
8 around lines 59 and 60, the '608 patent teaches that
9 the receiver 1520 samples the strobe according to the
10 clock signal CK0; is that fair?

11 A. Yes, that's fair.

12 Q. And would it be fair to say that to the
13 extent that there's a delay of the strobe signal, it
14 would be set by the receiver 1520 in accordance with
15 the clock signal CK0?

16 A. No, I wouldn't say that. The delay
17 itself is not set in accordance with CK0. The start
18 of the delay period is set in accordance with CK0.
19 But whatever the delay is, is not -- the delay itself
20 is not in accordance with CK0.

21 Q. Would it be fair to say that if the clock
22 signal CK0 itself is delayed, that that would delay
23 the strobe signal going through 1520?

24 A. Likely.

25 Q. The strobe signal from receiver from 1520

1 is also transmitted to the DQ routing circuit of
2 Figure 16 as the WDQS strobe signal as shown, for
3 example, by the vertical dashed orange line on page 2
4 of Exhibit 1080, correct?

5 A. Yes, I see that. In the case where these
6 two are paired together, yes.

7 Q. And as explained in column 17, starting
8 around line 29, in Figure 16, the data signal
9 received at DQ pin 1601 is buffered by the write data
10 buffer 1610 and then sampled by receiver 1620,
11 according to the WDQS strobe signal from the DQS
12 routing circuit in Figure 15, correct?

13 A. I think that's generally accurate, sure.

14 Q. And similar to our previous discussion,
15 the '608 patent does not go into further details
16 about how receiver 1620 samples the data signal
17 according to the RDQS strobe signal, but a person of
18 ordinary skill in the art would understand how to
19 sample the data using the strobe signal RD -- WDQS;
20 is that fair?

21 A. Yes. I think a POSITA would be able to
22 design the circuitry for 1620 such that WDQS was used
23 to sample the data coming out of 1610.

24 Q. And would it be fair to say that it's
25 possible to configure 1520 to delay the strobe signal

1 WDQS coming out of 1520?

2 A. It's possible. We really don't know much
3 of anything about what's in 1520. There could be
4 just about anything in there.

5 Q. And in that situation where the WDQS
6 strobe signal is delayed, would it be fair to say a
7 person of ordinary skill in the art would still be
8 able to sample the data at receiver 1620 using that
9 delayed stroke signal WDQS?

10 A. It would depend dramatically on the
11 amount of delay and timing parameters for the rest of
12 both of those circuits.

13 Q. Can you explain that a little bit more?

14 A. Sure. If it delayed WDQS by ten clock
15 cycles, then likely all of the data has flown through
16 Figure 16 already.

17 If it provided just a very small and
18 de minimis delay, for example, if it used something
19 that's often called a transparent latch, then it
20 likely would work fairly straightforward.

21 And then there's a whole range between
22 those two sort of endpoints.

23 Q. In Figure 16 on the far right, the same
24 ENA and ENB control signals that select which strobe
25 transmitter is used to output the strobe in Figure 15

1 are also used to select which of the output pins
2 1602A and 1602B is used to transmit the data signal;
3 is that fair?

4 A. If these two circuits for the different
5 components were put together, I would assume that a
6 common ENB line would be used and a common ENA line
7 would be used, yes.

8 Q. In Figures 15 and 16 of the '608 patent,
9 the delay signal DS is not used to set the delay of
10 any signal going in the write direction, and that's
11 spelled w-r-i-t-e, correct?

12 A. I think that's correct. It appears to --
13 at least based on what's disclosed in these figures,
14 it's only going to 1560 and 1660, which are used on
15 the read path rather than write path.

16 Q. Would it be fair to say that a person of
17 ordinary skill in the art would understand that in
18 Figures 15 and 16 of the '608 patent that the signals
19 in the write direction, w-r-i-t-e, can be delayed by
20 delaying the clock signal, CK0?

21 A. Possibly. They could also be -- have the
22 delay reduced by increasing or adding a delay to the
23 clock signal. It depends on exactly how the circuits
24 are implemented.

25 Q. Can you turn to Figure 17 of the

1 '608 patent, marked as Exhibit 1001. Let me know
2 when you have it in front of you.

3 A. Okay. I have it in front of me.

4 Q. And as explained in column 17 of the
5 '608 patent, starting around line 61, Figure 17
6 illustrates an implementation of the delay circuits
7 1560 and 1660, correct?

8 A. Yes, I believe that's accurate.

9 Q. In Figure 17 of the '608 patent, there
10 are a plurality of delay stages 1710, 1720, and 1730,
11 each delaying a read data or read strobe signal by a
12 predetermined amount, correct?

13 A. That appears to be the case.

14 Q. And would it be fair to say that a person
15 of ordinary skill in the art knew how to delay a data
16 or strobe signal by a predetermined amount?

17 A. Yes, I think that's fair to say, in
18 general.

19 Q. In the example of Figure 17, how would
20 you explain that the delay stages 1710, 1720, and
21 1730 are used to delay a data or strobe signal by a
22 predetermined amount?

23 A. They are configured to introduce a
24 predetermined amount of delay. Now, it could be the
25 case that the input from the right-hand side in the

1 upper right where it says from 1550/1560 enters into
2 1710, exits it and goes into 1720, exits it and goes
3 into 1730, or it could be the case as we saw with
4 some of the memory designs, that information could
5 fly-by all three of them. I don't recall as I sit
6 here.

7 The reason I bring that up is you could
8 have one common delay element that introduced a
9 5 nanosecond delay, and by putting them in sequence,
10 you could then select no delay, 5 nanoseconds, 10, or
11 15.

12 Or, alternately, you could build three
13 different delay elements that, on their own,
14 implemented 5, 10, and 15 nanoseconds' worth of
15 delay.

16 Q. And is what you just told me, is that
17 spelled out in the '608 patent?

18 MR. LINDSAY: Objection. Form.

19 THE WITNESS: I don't -- I don't recall.
20 I think this is -- it's just two different ways
21 as I read this figure that it could be
22 implemented with physically identical 1710,
23 1720, and 1730 circuits. Or they could be
24 structurally similar but different.
25

1 BY MR. CHANDLER:

2 Q. How is the clock signal used in Figure 17
3 of the '608 patent to delay a data or a strobe signal
4 by predetermined amount?

5 MR. LINDSAY: Objection. Form.

6 THE WITNESS: Well, let me turn to the
7 discussion of Figure 17. So I'm on column 17,
8 coincidentally, near the bottom, around line 61.
9 It doesn't seem to specify how CK interacts with
10 a delay circuit much at all.

11 BY MR. CHANDLER:

12 Q. And in Figure 17 of the '608 patent, what
13 does the delay signal DS do?

14 A. It's used to select which one of those --
15 which one of the delays that was generated is
16 actually used.

17 Q. And so, for clarity, is your
18 understanding that in Figure 17, that the delay
19 signal DS simply selects a signal that has already
20 been delayed by 1710, 1720, or 1730, or does the
21 delay signal DS actually create an additional delay?

22 A. It's selecting which one of the
23 pregenerated delay signals to utilize. And that
24 passage that I was looking at a moment ago referred
25 to these delay elements as staged, which, again, to

1 me, suggests that the signals go into one and then
2 out and then into the next one and then out and then
3 into the third one.

4 Q. Please turn to Figure 6 of the
5 '608 patent and let me know when you're there.

6 A. Okay. I'm there.

7 Q. As explained at column 2, line 54 of the
8 '608 patent, Figure 6 illustrates a control circuit
9 in a data buffer, correct?

10 A. That looks to be the case, yeah.

11 Q. And as explained at column 12, around
12 line 4 of the '608 patent, the control circuit
13 illustrated in Figure 6 can be implemented in 118,
14 which the '608 patent sometimes refers to 118 as a
15 data buffer and other times refers to 118 as an
16 isolation device; is that fair?

17 A. Yes, I think that's fair.

18 Q. And so, for example, if you look at
19 Figure 2C of the '608 patent, 118 is identified as DB
20 where DB stands for data buffer as explained, for
21 example, at column 3, line 27?

22 A. Yes, I see that. You said 2C. 2C does
23 indeed identify the DB elements, yes.

24 Q. And those are labeled 118, correct?

25 A. Yes.

1 Q. And turning back to Figure 6 of the
2 '608 patent, at the bottom of Figure 6, there are DB
3 command signals where, again, DB is referring to data
4 buffer, correct?

5 A. Yes, I see that.

6 Q. And as explained in column 12, around
7 line 13 of the '608 patent, those data buffer command
8 signals in Figure 6 are part of the MCS, which stands
9 for module control signals; is that fair?

10 A. Yes, module control signals are
11 abbreviated as MCS.

12 Q. And if we look back to Figure 2C of the
13 '608 patent again, the DB command signals are sent by
14 the controller 116 in the middle of the memory module
15 out to the data buffers 118 off to the left and to
16 the right, correct?

17 A. Yes, that's correct.

18 Q. And it would be fair to say that, as we
19 discussed earlier, the data buffers 118 in Figure 2C
20 of the '608 patent are in a fly-by arrangement; is
21 that fair?

22 A. Yes, I think that's fair.

23 Q. Turning back to Figure 6 of the
24 '608 patent, the command processing circuit 640
25 inside of the data buffer will receive the DB command

1 signals that were sent by the controller 116 that was
2 in the middle of the memory module; is that fair?

3 A. I believe that that's fair, yes.

4 Q. And then as explained at column 12,
5 starting around line 31, the command processing
6 circuit 640 inside of the data buffer includes a
7 delay control circuit 650 which determines the delay
8 amount sent via delay signal DS; is that fair?

9 A. So it does say:

10 In one embodiment, the ID control circuit
11 310 further includes a delay control circuit 650
12 that receives one of the module control signals
13 and either a data signal or a strobe signal and
14 determines a delay amount to be used by the DQ
15 routing circuit 320 and the strobe returning
16 circuit 620. The delay amount is provided to the
17 DQ routing circuit 320 and the strobe routing
18 circuit in a delay signal DS.

19 Q. And the DQ routing circuit 320 and the
20 strobe routing circuit 620, those are what's shown in
21 Figures 15 and 16 of the '608 patent that we
22 discussed earlier, correct?

23 A. Yeah. It's my understanding those are
24 examples of ways to implement these components.

25 Q. So the delay control circuit 650, which

1 is inside the data buffer which is also sometimes
2 referred to as the isolation device, provides the
3 determined delay amount via the delay signal DS to
4 both the DQ and DQS routing circuits 320 and 620 that
5 are illustrated in more detail in Figures 15 and 16;
6 is that fair?

7 A. Yes, I think that's fair.

8 Q. Please turn to Figure 19 of the
9 '608 patent. Let me know when you're there.

10 A. Okay.

11 Q. If Figure 19 of the '608 patent, there is
12 a box 650 similar to the box 650 in Figure 6 that we
13 just discussed a moment ago, identified as delay
14 circuit 650 at column 12, line 32; is that fair?

15 A. I believe so, yes.

16 Q. And as explained in column 19, starting
17 around line 1, in Figure 19 of the '608 patent, the
18 delay signal DS from the delay control circuit 650
19 only controls the clock regeneration circuit 1920; is
20 that fair?

21 MR. LINDSAY: Objection. Form.

22 THE WITNESS: Well, it says:

23 As shown in Figure 19, the ID control
24 circuit 310 includes a clock regeneration circuit
25 1920 that regenerates the clock signal CK

1 received from the control circuit 116, according
2 to the delay signal DS.

3 BY MR. CHANDLER:

4 Q. And if you look at the illustration of
5 Figure 19, you can see that delay signal DS going
6 from the delay control circuit 650 to the clock
7 regeneration circuit 1920, and the delay signal DS
8 does not go to any other component illustrated in
9 Figure 19; is that fair?

10 A. In Figure 19, it appears to only be
11 showing the delay signal DS emerging from element 650
12 and being provided to element 1920.

13 Q. And as explained in column 18, starting
14 at line 66, in Figure 19 of the '608 patent, the
15 delay signal DS is not provided to the DQ and DQS
16 routing circuits 320 and 620, which as we've
17 discussed, are shown in Figures 15 and 16; is that
18 fair?

19 A. I'm at column 18. Which line were you
20 looking at again?

21 Q. At the bottom, sort of around line 66.

22 A. Okay. So it does say:

23 In certain embodiments, especially the
24 embodiments shown in Figure 2D, the delay circuit
25 1560 and 1660 shown in Figures 15 and 16 are not

1 needed to provide alignment of the read data.

2 Q. And then if you continue reading for the
3 next few sentences in the top of column 19, the
4 '608 patent explains that in Figure 19 of the
5 '608 patent, the delay signal DS is sent to the clock
6 regeneration circuit 19, which generates the clock
7 signal CK0 with the proper amount of delay, correct?

8 MR. LINDSAY: Objection. Form.

9 THE WITNESS: Yes, I think that's
10 accurate to what's discussed in this passage.

11 BY MR. CHANDLER:

12 Q. So in this embodiment of the data buffer
13 shown in Figure 19, the delay circuits 1560 and 1660
14 in Figures 15 and 16 are not needed because, instead,
15 the clock signal CK0 is delayed by the proper amount;
16 is that fair?

17 A. I don't see a problem with that as I sit
18 here, no.

19 Q. And so, for example, if you look back at
20 Exhibit 1080 which has the annotations of Figures 15
21 and 16, it's possible for a delayed clock signal CK0
22 to be used in both Figures 15 and 16 to delay both
23 the DQ data signal and the DQS strobe signal by the
24 proper amount; is that fair?

25 A. Give me a moment. Yes, it's possible to

1 use 15 -- figure -- the circuitry in Figure 15 and 16
2 without 1560 and 1660 according to the disclosure,
3 that embodiment that we were just looking at.

4 Q. All right. Do you have Exhibit 1080 in
5 front of you?

6 A. I do.

7 Q. Would it be fair to say that a person of
8 ordinary skill in the art would understand that when
9 there is a read operation in Figures 15 and 16 of the
10 '608 patent as illustrated, for example, on page 1 of
11 Exhibit 1080, that the DQ data signal coming out of
12 the left side of Figure 16 on line 322 should be edge
13 aligned with the DQS strobe signal coming out of the
14 left side of Figure 15 on line 324?

15 A. Yes.

16 Q. And if you turn to page 2 of
17 Exhibit 1080, would it be fair to say that a person
18 of ordinary skill in the art would understand that
19 when there is a write operation, w-r-i-t-e, in
20 Figures 15 and 16 of the '608 patent, the DQS strobe
21 signal coming out of the right side, as opposed to
22 left side, the right side of Figure 15, on line YB
23 DQS needs to be center aligned with the DQ data
24 signal coming out of the right side, not the left
25 side, but the right side of Figure 16 on the line YB?

1 A. Yes. I think a POSITA would have that
2 understanding.

3 MR. CHANDLER: Why don't we take a short
4 break. Off the record.

5 THE VIDEOGRAPHER: Off the record at
6 3:09 p.m. Pacific time.

7 (A recess was taken.)

8 THE VIDEOGRAPHER: On the record at
9 3:18 p.m. Pacific time.

10 BY MR. CHANDLER:

11 Q. Do you have any corrections to any of the
12 testimony that you've given so far?

13 A. No, I do not.

14 Q. Could you turn back to Exhibit 1078 and
15 let me know when you have it in front of you?

16 A. All right.

17 Q. On page 2 of Exhibit 1078, there is
18 illustrated an example where the control address and
19 clock signals are delayed by more than one clock
20 cycle by the time they reach the furthest memory
21 device in green and the furthest data buffer in blue;
22 do you see that?

23 A. Yes, I see that represented here.

24 Q. And in that scenario where you have a
25 delay of 450 degrees, as an example, it looks similar

1 to a delay of 90 degrees; is that fair?

2 MR. LINDSAY: Objection. Form.

3 THE WITNESS: In some ways, yes, it looks
4 similar.

5 BY MR. CHANDLER:

6 Q. And that can potentially create some
7 complexity if you're trying to remove delays greater
8 than one clock cycle; is that fair?

9 A. Not -- I don't think the fact that it has
10 some similarities with the delay of 90 degrees, but
11 the fact that it is delayed by 450 degrees does add
12 some complexity.

13 Q. Can you explain that a little more, what
14 the complexity is?

15 A. It's got a long delay. All the delays
16 need to be accounted for, addressed, responded to.

17 Q. And in your opinion, did a person of
18 ordinary skill in the art know how to correct for
19 delays greater than one clock cycle?

20 MR. LINDSAY: Objection. Form.

21 THE WITNESS: Perhaps. I don't recall
22 much of the art at all dealing with delays
23 greater than one clock cycle. The delay present
24 has to be dealt with in some respect. It
25 doesn't matter which one of these delay values

1 you're seeing, at least in some respects.

2 BY MR. CHANDLER:

3 Q. And in Figures 15 and 16 in the
4 '608 patent, do you recall any particular discussion
5 of how those figures can correct for delays that are
6 greater than one clock cycle as opposed to delays
7 that are less than one clock cycle?

8 A. I just recall them indicating that a
9 delay signal can be used. I don't recall if they
10 were talking about less than or greater than one
11 clock cycle.

12 Q. Could you pull up the Tokuhiro reference
13 marked as Exhibit 1006, and let me know when you have
14 it?

15 (The Court Reporter requested
16 clarification.)

17 BY MR. CHANDLER:

18 Q. Could you pull up the Tokuhiro reference
19 marked as Exhibit 1006, and let me know when you have
20 it in front of you?

21 A. Is it in the chat?

22 Q. I thought it was, but I can certainly put
23 it back. We've got more where that came from. We're
24 giving them away for free today. And there you go.

25 A. Thank you. Okay.

1 Q. And please turn to Figure 7 of the
2 Tokuhiro reference marked as Exhibit 1006. Let know
3 when you've got it.

4 A. I have it.

5 Q. As explained starting at column 13,
6 line 4, Figure 7 in the Tokuhiro reference marked as
7 Exhibit 1006 describes Tokuhiro's write leveling
8 function, correct?

9 A. Yes. It says:

10 Figure 7 is an explanatory diagram for
11 explaining the write leveling function of the
12 first delay time control unit in the information
13 processing apparatus according to the first
14 embodiment.

15 Q. And if you look at Figure 7 of the
16 Tokuhiro reference, the memory controller is on the
17 left and the DIMM memory module is on the right,
18 correct?

19 A. Yes, that's correct.

20 Q. And if you look at Figure 7 of the
21 Tokuhiro reference, on the left there are variable
22 delay circuits labeled DW-1 through DW-N, as in
23 Nancy, that correspond to the DQS strobe lines DQS-1
24 through DQS-N, as in Nancy, and as explained in
25 column 13, around lines 43 and 50; is that fair?

1 A. I see it in Figure 7. Do you want me to
2 flip to that column quotation?

3 Q. Sure. Just take a quick look. We'll be
4 going back and forth so you might as well have them.

5 A. Where was that again?

6 Q. Column 13, around lines 43 and 50.

7 A. Okay.

8 Q. And the point I'm simply trying to get
9 across is that in Figure 7 there are the delay
10 circuits labeled DW-1 through DW-N, as in Nancy,
11 which correspond to the DQS strobe signals labeled
12 DQS-1 through DQS-N, as in Nancy, which correspond to
13 the SDRAM memory devices SDRAM-1 through SDRAM-N, as
14 in Nancy; is that fair?

15 A. Yes, I think that's fair.

16 Q. And is it fair that the goal of Figure 7
17 of Tokuhiko is to set different time delays with the
18 first time delay DT1-1 corresponding to SDRAM-1, and
19 the nth time delay DT1-N corresponding to SDRAM-N?

20 A. I believe that's one of the goals of what
21 they are illustrating here in Figure 7.

22 Q. And, for example, as shown in Figure 7 on
23 the bottom right, and as discussed in column 13
24 between lines 48 and 54, there is a delay time DT1-N,
25 as in Nancy, corresponding to the variable delay

1 circuit DW-N, as in Nancy, so that strobe signal
2 DQS-N, as in Nancy, matches up with the clock signal
3 CK1 at SDRAM-N, as in Nancy; is that fair?

4 A. Yes, I think that's a fair representation
5 of what this figure is showing.

6 Q. And then if you turn to the next column
7 in the Tokuhiro reference marked as Exhibit 1006 in
8 column 14, starting around line 55, it explains that
9 the delay times DT1-1 to DT1-N corresponding
10 respectively to SDRAM-1 to SDRAM-N, as in Nancy, are
11 set so as to become gradually longer, correct?

12 A. Yes, that's correct.

13 Q. Could you pull up the Butt reference
14 marked as Exhibit 1029? I gave it to you previously,
15 but I can give it to you again if you would like.

16 So do you have Exhibit 1029?

17 A. I do. I have it open now.

18 Q. All right. Please turn to Figure 2 of
19 the Butt reference marked as Exhibit 1029, and let me
20 know when you're there.

21 A. Okay. I'm there.

22 Q. On the right side of Figure 2 of the Butt
23 reference, marked as Exhibit 1029, there is a big
24 block 106 with one or more DDR memories; is that
25 fair? And you can look at paragraph 15 for some

1 description, if you would like.

2 A. I believe that's fair.

3 Q. And then in the middle of Figure 2 of the
4 Butt reference there is circuit 104, which, if you
5 look at the figure, shows on the far right is
6 connected to the -- one or more DDR memory devices by
7 capital N lines carrying DQ data and capital N
8 divided by eight lines carrying the corresponding
9 data strobe signals DQS; is that fair?

10 A. Yes, I see that.

11 Q. And in Figure 2 of the Butt reference,
12 the circuit 104 includes a number of physical read
13 data paths 114, and that's also discussed in
14 paragraph 17, correct?

15 A. It contains a number of elements marked
16 114, labeled PHY DP.

17 Q. And PHY DP is referred to as the physical
18 data path; is that fair?

19 A. I don't recall. That wouldn't surprise
20 me, but --

21 Q. It's sort of like, I don't know, a third
22 of way down in paragraph 17. Physical read data
23 paths, parentheses, DPs 114.

24 A. Okay. Yes, I see that.

25 Q. And then looking back at Figure 2 of the

1 Butt reference marked as Exhibit 1029, the number 8
2 to the right of the physical data paths 114 means
3 that each of the data paths 114 receives 8 DQ data
4 signals and 1 corresponding DQS data strobe signal;
5 is that fair?

6 So I'm referring to sort of the slash 8
7 on the line going into the physical data path of 14
8 for the DQ line, and then the DQS line does not have
9 the slash 8.

10 A. Yeah, understood. I was just trying to
11 verify that. Yes, that appears to be accurate.
12 There are eight DQ lines going into the PHY DP, the
13 PHY DP, and what I think is an indication of one DQS
14 line going in.

15 Q. And then -- say the last part again.

16 A. I'm sorry. I -- to each of them. The
17 DQS line, the one DQS line goes into each of the five
18 DPs.

19 Q. In Figure 2 of the Butt reference, and
20 it's also discussed in paragraphs 18 and 19, each of
21 data paths 114 outputs DQ data via the signals
22 DR_PDQ_out and DR_NDQ_out, and also outputs the
23 corresponding data strobe via the signals PDQS_out,
24 and NDQS_out; is that fair?

25 A. Yes, I see that.

1 Q. In Figure 2 of the Butt reference, the
2 data in strobe signals, after they come out of data
3 path 114, go to the asynchronous FIFO 112 as shown in
4 Figure 2 and discussed in paragraphs 17 and 18; is
5 that fair?

6 A. When those signals emerge from element
7 114, they go to element 112, which is labeled ASYNC,
8 A-S-Y-N-C, short for asynchronous, FIFO.

9 Q. And in particular, as explained by
10 paragraph 19 of the Butt reference marked as
11 Exhibit 1029, the read data DR_PDQ_out and DR_NDQ_out
12 are written to the FIFOs 112 in response to the
13 strobe signals PDQS_out and NDQS_out, correct?

14 A. Yes. It says that that read data is
15 generally written into the FIFO based on those DQS
16 signals.

17 Q. And in paragraph 19 of the Butt reference
18 marked as Exhibit 1029, it indicates another way of
19 putting it is that the FIFOs 112 are clocked by the
20 strobe signals PDQS_out and NDQS_out; is that fair?

21 A. You read it accurately. I would not say
22 that. I wouldn't say that they're clocked by it, but
23 they are controlled by those signals.

24 Q. But that is how Butt characterized it in
25 Exhibit 1029; is that accurate?

1 A. Yeah, I believe so.

2 Q. In Figure 2 and in paragraph 17 of the
3 Butt reference marked as Exhibit 1029, there is a
4 programmable gating signal generating circuit 118
5 which generates the gating signal labeled GATEON, in
6 all caps, correct?

7 A. I was working through the last question,
8 so I'm sorry, I'm behind on your question. I was
9 just going to point out that he doesn't say in
10 paragraph 19 that -- there's this odd -- what I find
11 as odd parenthetical comment saying that the FIFOs
12 are written in response to, and then it says, "e.g.,
13 clocked by."

14 That's why it -- I wouldn't call that
15 clocked by. It sounds like he's saying, well, it's
16 kind of like that, but it's not literally that.

17 Now, with that apology, if you could
18 reorient me to your most recent question.

19 Q. In Figure 2 and in paragraph 17 of the
20 Butt reference marked as Exhibit 1029, there is
21 disclosure of a programmable gating signal generating
22 circuit 118, which generates a gating signal labeled
23 GATEON, spelled in all caps, correct? And one word,
24 GATEON.

25 A. Yes, I see that.

1 Q. As explained in paragraph 24 of the Butt
2 reference marked as Exhibit 1029, the GATEON signals
3 may be used to gate the DQS data strobe signals,
4 correct?

5 A. Yes. It says:

6 The signal GATEON may be used to gate the
7 read data strobe signal DQS received from the
8 memory device 106.

9 Q. And what is your understanding of what
10 that means or how would you explain that to me as to
11 what that's doing?

12 A. A gate, as we talked about with tri-state
13 buffers, is usually a term that describes the ability
14 to allow a signal to either pass or to be blocked.
15 So I believe this is talking about controlling a gate
16 to pass or block those signals.

17 Q. Okay. I'm going to ask you the next
18 question, but I got to warn you, there's all these
19 acronyms. And I think they're all in paragraph 24.
20 But just sort of to preview it -- actually,
21 paragraph 7, I think, at the end of it -- 17, rather.

22 There's this concept of lower nibble and
23 upper nibble. Are you familiar with that concept?

24 A. Yes, I am.

25 Q. And I'll ask you about all these acronyms

1 in a moment, but these acronyms end in LN for lower
2 nibble and UN for upper nibble.

3 Does that make sense to you so far?

4 A. Yes, it does.

5 Q. And just quickly, how would you explain
6 the concept of lower nibble and upper nibble?

7 A. Somebody in computer history thought it
8 would be amusing to say, we've got the concept of a
9 byte, which is not spelled like taking a bite of
10 something, but b-y-t-e. And if you have only part of
11 that, well, it's a nibble because it's something
12 smaller.

13 So the low order -- the lowest -- the
14 bits in a byte are ordered from zero through 7, the
15 low order bits are the lower nibble and the high
16 order bits are the higher nibble.

17 (The Court Reporter requested
18 clarification.)

19 THE WITNESS: The lowest four bits of a
20 byte are the lowest nibble -- are the low
21 nibble, and the highest four bytes -- the
22 highest four bits of a byte is the upper nibble.

23 BY MR. CHANDLER:

24 Q. And as explained by the end of
25 paragraph 17 of the Butt reference marked as

1 Exhibit 1029, capital L, capital N, is referring to
2 signals for the lower nibble, and capital U,
3 capital N, is referring to signals for the upper
4 nibble; is that fair?

5 A. That's my recollection, yes.

6 Q. So if you look at Figures 3A and 3B, the
7 gated DQS strobe signals are output by data path 114
8 as the signals PDQS_out_LN, referring to lower
9 nibble, PDQS_out_UN, referring to upper nibble,
10 NDQS_out_LN, referring to lower nibble, and
11 NDQS_out_UN, referring to upper nibble; is that fair?

12 A. That's a fair characterization of how
13 Butt discusses this figure. It's not how I would
14 discuss the figure, but it's a fair characterization
15 of how he discusses it.

16 Q. And as explained in paragraph 17 of Butt
17 and as shown in Figure 2 of the Butt reference marked
18 as Exhibit 1029, there's another embodiment that
19 doesn't have the lower nibble and upper nibble;
20 instead, there is simply an embodiment where the
21 gated DQS strobe signals output by data path 114 are
22 simply referred to as PDQS_out and NDQS_out; is that
23 fair?

24 A. Yes, I see that. It's fair that those
25 labels appear on the outputs of element 114.

1 Q. And then in paragraph 47 of the Butt
2 reference marked as Exhibit 1029, in the middle of
3 the paragraph, there's reference that the GATEON
4 signal, all caps, one word, can be trained according
5 to a training process; is that fair?

6 A. Yes. It says:

7 A read GATEON training process, described
8 in a co-pending application, which is not filled
9 in.

10 Yeah, it talks about training the GATEON
11 device.

12 Q. It refers to -- in paragraph 47 that the
13 GATEON training process is described in a co-pending
14 application filed July 1st, 2005 and incorporated by
15 reference, correct?

16 A. Yes, I see that.

17 Q. I'd like to introduce Exhibit 1084, which
18 is U.S. Patent Number 7,215,584, filed on July 1st,
19 2005 by Butt, which I will call the Butt 2 reference.
20 Let me know when you have it in front of you.

21 (Exhibit 1084 was marked and/or
22 identified.)

23 MR. LINDSAY: I object to the reference.

24 THE WITNESS: I have it in front of me
25 now.

1 BY MR. CHANDLER:

2 Q. The title of the Butt 2 reference marked
3 as Exhibit 1084 is "Method and/or Apparatus for
4 Training DQS Strobe Gating" and it was filed on
5 July 1st, 2005 as application number 11/173,529,
6 correct?

7 MR. LINDSAY: Objection. Outside the
8 scope of direct.

9 THE WITNESS: Yes, I believe that's
10 correct.

11 BY MR. CHANDLER:

12 Q. And I will represent to you that the
13 Butt 2 reference marked as Exhibit 1084 is what is
14 incorporated by reference in paragraph 47 of the Butt
15 reference marked at Exhibit 1029 as attorney docket
16 number 1496.00419, understood?

17 A. Understood. Although, I don't recall
18 reviewing this document as I sit here, partly
19 because -- well, I didn't have access to the
20 attorney's docket files. But, yes, it's --
21 I understand that.

22 Q. Well, and to be fair, and just so you
23 understand how I know that Exhibit 1084 is
24 incorporated by reference into Exhibit 1029, is that
25 the patent office has a website patent center,

1 USPTO.gov, where you can see the attorney docket
2 number. And so you can make the correlation between
3 Exhibit 1084 and paragraph 47 of Exhibit 1029.

4 But I have done that, and I'll make you a
5 representation that they do correspond, understood?

6 A. Understood. And you learn something new
7 every day. I thought the attorney docket numbers
8 were not universal and useful only to them, but
9 I guess I was wrong.

10 Q. And Figures 1, 2, 3A, and 3B appear to be
11 the same in both the Butt reference marked as Exhibit
12 1029 and the Butt 2 reference marked as Exhibit 1084,
13 correct?

14 MR. LINDSAY: Objection. Outside the
15 scope of direct.

16 THE WITNESS: Yes, based on a quick
17 review here, they do appear to be the same.

18 BY MR. CHANDLER:

19 Q. In the Butt 2 reference marked as
20 Exhibit 1084, as explained in column 2, around
21 lines 30 to 32:

22 Figure 14 is a timing diagram illustrating
23 an example of a delayed data strobe gating
24 signal.

25 Correct?

1 MR. LINDSAY: Objection. Outside the
2 scope of direct.

3 THE WITNESS: Column 2, and you're
4 referring to Figure 14, the comment on it?

5 BY MR. CHANDLER:

6 Q. Yeah, at lines 30 through 32.

7 A. Yes. I see that it says those words,
8 yes.

9 Q. And then if you turn to Figure 14 of the
10 Butt 2 reference marked as Exhibit 1084, in the
11 middle of that figure is a timing example for the
12 GATEON signal, all caps, all one word, correct?

13 MR. LINDSAY: Objection. Outside the
14 scope of direct.

15 THE WITNESS: There is a signal line
16 corresponding labeled "GATEON internal." It's
17 not really clear to me how to read that, how to
18 read the passage next to it, which is marked
19 T_GATEON_DELAY.

20 BY MR. CHANDLER:

21 Q. Well, there's --

22 A. Go ahead.

23 Q. There's a clock that's shown at the top
24 of the figure with clock periods labeled 1, 2, 3, 4,
25 5, 6, 7, 8, 9; is that fair?

1 MR. LINDSAY: Objection. Outside the
2 scope of direct.

3 THE WITNESS: Yes. Yes, I see that.

4 BY MR. CHANDLER:

5 Q. And then near the bottom of Figure 14 of
6 the Butt 2 reference marked as Exhibit 1084 is the
7 DQS strobe signal, which is what the GATEON signal is
8 gating as shown by the curved dashed lines; is that
9 fair?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct.

12 THE WITNESS: I wouldn't say that.
13 I haven't studied this figure enough to comment.

14 BY MR. CHANDLER:

15 Q. Is there something else that you would
16 say, or are you saying you haven't studied it enough
17 to comment?

18 A. Just I haven't studied it enough to
19 comment.

20 Q. In Figure 14 of the Butt 2 reference
21 marked as Exhibit 1084, the GATEON signal is enabled
22 between around time 5.5 and time 6.75; is that fair?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct.

25 THE WITNESS: It goes from low to high

1 around 5.5, and it transitions from high to low
2 something more than 6.5. So, yeah, I don't know
3 if that constitutes the active state or not.

4 Yeah.

5 BY MR. CHANDLER:

6 Q. And then as shown by the curved dashed
7 lines, time 5.5 corresponds to approximately the
8 middle of the preamble of the DQS strobe signal and
9 time 6.75 corresponds to approximately the middle of
10 the post-amble of the DQS strobe signal; is that
11 fair?

12 MR. LINDSAY: Objection. Outside the
13 scope of direct.

14 THE WITNESS: I don't know. I don't know
15 of any DDR system that will do just a length to
16 burst. I guess it's possible, but I haven't
17 reviewed this. I don't have an opinion.

18 BY MR. CHANDLER:

19 Q. But you're familiar with the preamble of
20 a DQS strobe signal being approximately one full
21 clock cycle and the post-amble being approximately
22 half a clock cycle; is that fair?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct.

25 THE WITNESS: I'm familiar with that in

1 the context of the -- for example, the DDR3
2 systems we were previously looking at.

3 BY MR. CHANDLER:

4 Q. And you explained a few moments ago that
5 gating a DQS strobe signal, or gating a signal more
6 generally -- maybe you should explain, what does
7 gating a signal accomplish?

8 MR. LINDSAY: Objection. Form.

9 THE WITNESS: So it can have multiple
10 meanings. In general, what it means is to
11 selectively block another signal. Now, that can
12 be -- that function can be implemented with what
13 we call a logic gate, but there -- it could be
14 implemented with a tri-state buffer or a number
15 of other techniques.

16 BY MR. CHANDLER:

17 Q. Would it be possible, in your opinion,
18 that in Figure 14 of Exhibit 1084, when the GATEON
19 signal transitions at approximately 5.5, it stops
20 blocking the DQS strobe signal, thus, permitting the
21 DQS strobe signal to transition from low to high and
22 from high to low around time T6 and time T6.5, and
23 then after that, the GATEON signal goes low and
24 presumes blocking the DQS strobe signal?

25 MR. LINDSAY: Objection. Form. Outside

1 the scope of direct.

2 THE WITNESS: That could be what this is
3 suggesting, but I really don't have an opinion
4 as I sit here today.

5 BY MR. CHANDLER:

6 Q. And in Figure 14 of the Butt reference
7 marked as Exhibit 1084, the two transitions of the
8 DQS strobe signal around time T6 and time T6 and a
9 half correspond to the two pieces of read data on the
10 DQ data line directly below it labeled the D0 and D1;
11 is that fair?

12 MR. LINDSAY: Objection. Outside the
13 scope of direct.

14 THE WITNESS: They might. I really don't
15 know. They don't appear to be well-aligned. Is
16 this -- is this a read or a write operation?
17 This is a read operation, I guess. Okay. Yeah,
18 then they're aligned.

19 BY MR. CHANDLER:

20 Q. In Figure 3A of both the Butt reference
21 marked as Exhibit 1029 and the Butt 2 reference
22 marked as Exhibit 1084, there's a schematic of how
23 the GATEON signal is used, correct?

24 MR. LINDSAY: Objection. Outside the
25 scope of direct as to Exhibit 1084.

1 THE WITNESS: There is a schematic
2 indicating one use for the GATEON UN signal and
3 there's probably a -- I guess there's not a
4 GATEON LN signal. This must just be the upper
5 nibble.

6 BY MR. CHANDLER:

7 Q. Well, and Figure 3B shows the lower
8 nibble with GATEON_LN, correct?

9 A. Got it. Yes.

10 Q. And do you believe a person of ordinary
11 skill in the art looking at Figures 3A and 3B of the
12 Butt reference marked as Exhibit 1029 and the Butt 2
13 reference marked as Exhibit 1084 would understand the
14 schematic illustrating the use of the GATEON signal
15 to gate the DQS strobe signal?

16 MR. LINDSAY: Objection. Outside the of
17 direct as to Exhibit 1084.

18 THE WITNESS: Not in a way that was
19 consistent with the figure we were just looking
20 at previously.

21 BY MR. CHANDLER:

22 Q. And why do you say that?

23 A. Well, there's an input to that
24 multiplexer 123A which is ground --

25 (The Court Reporter requested

1 clarification.)

2 THE WITNESS: Labeled 123A, and that
3 input is a ground input. And that timing
4 diagram, if I recall right, seemed to show a
5 high-Z output when GATEON wasn't asserted.

6 BY MR. CHANDLER:

7 Q. What makes you say that as opposed to
8 GATEON being low?

9 A. I'm not following you. When GATEON is
10 low, the multiplexer we're looking at indicates to me
11 that it should probably be driving the output of the
12 top input -- driving to the -- to its output the
13 value of the top input, which is ground.

14 Q. I think you might be a little confused
15 because in Figure 14 of Exhibit 1084, that's showing
16 the DQS strobe signal being in the high-Z state, not
17 the output of the multiplexer, correct?

18 MR. LINDSAY: Objection. Outside the
19 scope of direct. And form.

20 BY MR. CHANDLER:

21 Q. So when the GATEON is low, the gated DQS
22 strobe signal is also low?

23 MR. LINDSAY: Same objection.

24 THE WITNESS: As I said, I don't really
25 know exactly what this timing diagram is

1 showing, but it's not showing that.

2 BY MR. CHANDLER:

3 Q. A person of ordinary skill in the art
4 understands a multiplexer and the GATEON selection
5 signal, right? Being able to select between either
6 ground or the DQS signal, fair?

7 MR. LINDSAY: Objection. Outside the
8 scope of direct.

9 THE WITNESS: Yes, I would agree with
10 that.

11 BY MR. CHANDLER:

12 Q. So when the GATEON signal is low, the
13 gated DQS signal will be -- can be low because that's
14 the ground input, fair?

15 MR. LINDSAY: Objection. Outside the
16 scope of direct.

17 THE WITNESS: Yes, that's correct.

18 BY MR. CHANDLER:

19 Q. And when the GATEON signal is in the
20 other state, the output will be whatever the input is
21 on the DQS strobe line, which may be high-Z or may be
22 DQS strobe signal, correct?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct.

25 THE WITNESS: It will select -- the

1 multiplexer will select for its output whatever
2 signal is on the DQS lines. But the discussion
3 we're just having now is still inconsistent with
4 what we're looking at Figure 14.

5 BY MR. CHANDLER:

6 Q. Why do you say that?

7 A. Figure 14 doesn't show the behavior that
8 we just discussed. It shows different behavior.

9 Q. Can you explain it a little more?

10 A. Sure.

11 MR. LINDSAY: Objection. Outside the
12 scope of direct as well.

13 THE WITNESS: So you'll see that, for
14 example, during the first timing period, GATEON
15 is low, but the output is not low -- the output
16 of DQS is not low.

17 MR. CHANDLER: Why don't we go off the
18 record for just a moment. Let me take a look
19 and we'll come back in just a few minutes.

20 THE VIDEOGRAPHER: Off the record at
21 4:05 p.m. Pacific time.

22 (A recess was taken.)

23 THE VIDEOGRAPHER: On the record at
24 4:12 p.m. Pacific time.

25

1 BY MR. CHANDLER:

2 Q. What does FIFO stand for?

3 A. FIFO stands for first in, first out. And
4 it's written all in upper case F-I-F-O.

5 Q. In the Butt reference marked as about
6 1029, as well as the Butt 2 reference marked as
7 Exhibit 1084, the gated strobe signal is PDQS_out and
8 NDQS_out, correct?

9 MR. LINDSAY: Objection. Outside the
10 scope of direct as to Exhibit 1084.

11 THE WITNESS: Perhaps. Which figure was
12 that in?

13 BY MR. CHANDLER:

14 Q. Well, it's in Figure 2, and then the
15 upper nibble and lower nibble versions are in
16 Figures 3A and 3B, correct?

17 A. Yes, I see that.

18 Q. And so the DQS strobe signal is not the
19 gated strobe signal. The gated strobe signal is
20 PDQS_out and NDQS_out, correct?

21 A. Yes, I think that's fair.

22 Q. So in Figure 14 of Exhibit 1084, that's
23 showing the DQS strobe signal, not the gated strobe
24 signal, correct?

25 MR. LINDSAY: Objection. Outside the

1 scope of direct.

2 THE WITNESS: It is labeled DQS.

3 BY MR. CHANDLER:

4 Q. And then --

5 A. I don't know if that's -- I don't know if
6 that's an abbreviation for the -- the P and the N
7 versions are because they're -- they use what's
8 called complementary signaling where the same signal
9 is sent both high and low.

10 I don't know if they're using DQS just to
11 refer to the aggregate signal or the input, which was
12 just DQS.

13 Q. But in Figures 3A and 3B of the Butt
14 reference marked as Exhibit 1029 and the Butt 2
15 reference marked as Exhibit 1084, the multiplexer
16 receives as an input the DQS strobe signal and the
17 GATEON signal, and then the output is what
18 contributes to the gated PDQS_out and NDQS_out,
19 correct?

20 MR. LINDSAY: Objection. Form. And
21 outside the scope of direct.

22 THE WITNESS: Yeah. The output from the
23 multiplexer 123B gets presented as PDQS_out_LN
24 and NDQS_out_LN.

25

1 BY MR. CHANDLER:

2 Q. And then in Figure 3A the output of
3 multiplexer 123A --

4 (The Court Reporter requested
5 clarification.)

6 BY MR. CHANDLER:

7 Q. In Figure 3A the output of multiplexer
8 123A is output of the upper nibble, versions of those
9 two same signals, correct?

10 MR. LINDSAY: Objection. Outside the
11 scope of direct as it relates to Exhibit 1084.

12 THE WITNESS: Yes, that's correct.

13 BY MR. CHANDLER:

14 Q. And so the way the multiplexer works is,
15 in one state, the GATEON signal can select the DQS
16 input to be the output, and in the other state, the
17 GATEON signal would select ground to be the output of
18 the gated strobe signal, correct?

19 A. That appears to be its function looking
20 at this Figure 3A and 3B.

21 Q. So in Figure 14 of Exhibit 1084, I think
22 you were suggesting that the output of the gated
23 strobe signal doesn't match up with Figure 14. But
24 my understanding is that Figure 14 is showing the
25 input of the DQS strobe signal into the multiplexer

1 in and Figures 3A and 3B of exhibits 1029 and 1084.

2 Do you understand the difference?

3 MR. LINDSAY: Objection. Outside the
4 scope of direct. And form.

5 THE WITNESS: Yes, I do.

6 BY MR. CHANDLER:

7 Q. And so in that situation, or with that
8 understanding, when the GATEON signal is low, then
9 the output of the gated DQS strobe signals would be
10 ground, also referred to as low. And then,
11 conversely, when the GATEON signal is high, the
12 output of the gated strobe signal would be whatever
13 is on the DQS line; is that fair?

14 MR. LINDSAY: Objection. Outside the
15 scope of direct.

16 THE WITNESS: I wouldn't say that.

17 BY MR. CHANDLER:

18 Q. Why?

19 A. I'd have to go back and review this
20 further.

21 Q. And is the reason you wouldn't say it
22 because you have to go back and review it further or
23 because there's something I said that you believe is
24 incorrect?

25 A. I'd have to go back and -- the reason is

1 because to be confident in that answer I'd have to
2 review it further, not that I identified anything
3 that you said that I fundamentally disagreed with.

4 Q. In paragraph 73 of the Butt reference
5 marked as Exhibit 1029, which corresponds to
6 column 12, line 58, of the Butt 2 reference marked as
7 1084, they both teach that the asynchronous FIFOs 112
8 are generally reset before a read operation to ensure
9 a fresh start for memory reads, correct?

10 MR. LINDSAY: Objection. But just, Ted,
11 I'm not sure you meant paragraph 73. I don't
12 think there's a paragraph 73.

13 THE WITNESS: Well, I've got the '584 in
14 front of me, and I am at column 12, but could
15 you remind me of which line number you wanted me
16 to look at?

17 BY MR. CHANDLER:

18 Q. Column 12, line 58, it starts around 58.

19 A. I see that.

20 Q. And what is the benefit of resetting the
21 FIFO before a read operation? How does that ensure a
22 fresh start for memory reads?

23 MR. LINDSAY: Objection. Outside the
24 scope of direct. Form.

25 THE WITNESS: I don't know. Maybe they

1 were worried about there being what we would
2 refer to as stale data in there, but I don't
3 know why there would be stale data.

4 BY MR. CHANDLER:

5 Q. Could you turn to the Hiraishi reference
6 marked as Exhibit 1005?

7 A. Okay.

8 Q. And look at Figure 5. Let me know when
9 you're there.

10 A. Okay.

11 Q. On the left side of Figure 5 of the
12 Hiraishi reference marked as Exhibit 1005 is data
13 line L0, which includes a DQS signal at terminal 350
14 and a DQ signal at terminal 340, correct?

15 A. Yes, I see that.

16 Q. And in Figure 5 of the Hiraishi reference
17 marked as Exhibit 1005, a read operation goes from
18 right to left and a write operation, spelled
19 w-r-i-t-e, goes from left to the right as shown, for
20 example, by the direction of the arrows for the write
21 FIFO 301 and the read FIFO 302; is that fair?

22 A. Yes.

23 Q. And as explained by paragraph 84 of the
24 Hiraishi reference marked as Exhibit 1005, and as
25 illustrated in Figure 5, in the case of a write

1 operation, w-r-i-t-e, the write FIFO circuit 301
2 buffers the DQ data from terminal 340 with the DQS
3 data strobe signal from terminal 350, correct?

4 A. Yeah, I believe so. It says:

5 The FIFO write circuit 301 buffers data DQ
6 that is supplied via an input/output terminal 340
7 with a data strobe signal DQS that is supplied
8 via an input/output terminal 350.

9 Q. And that's also illustrated in Figure 5;
10 is that fair?

11 A. I believe so, yes.

12 Q. So Figure 5 of the Hiraishi reference
13 shows the DQS data strobe terminal from 350 is used
14 by the write FIFO 301, correct?

15 A. Yes. It shows the signal -- the DQS
16 signal being received, passing through the input
17 buffer labeled INB, and then being sent to the write
18 FIFO circuit 301.

19 Q. And would it be fair to say that a person
20 of ordinary skill in the art would understand that
21 the DQS data strobe signal from terminal 350 can be
22 used to sample the data in the write FIFO 301?

23 A. Yes. They might infer that from this
24 figure, sure.

25 Q. On the right side of Figure 5 of the

1 Hiraishi reference is data line L1, which includes a
2 DQ signal at terminal 314 and a DQS signal at
3 terminal 351; is that fair?

4 A. Yes, I see that.

5 Q. As explained by paragraph 84 of the
6 Hiraishi reference marked as Exhibit 1005, in the
7 case of a read operation using data line L1, the read
8 FIFO circuit 302 buffers the DQ data from terminal
9 341 with a DQS strobe signal from terminal 351, and
10 then Figure 5 shows that DQS data strobe signal from
11 terminal 351 is delayed by delay circuit 372 before
12 it goes into the read FIFO 302, correct?

13 A. There is a path from terminal 351
14 receiving DQS through a second read side input buffer
15 into selector 332, from there, into delay circuit
16 372, and then being shown driven down into FIFO read
17 circuit 302.

18 Q. And then there's a similar path using
19 data line L2 where account read FIFO circuit 302
20 buffers the data from terminal 342 with the DQS data
21 strobe signal from terminal 352 that gets delayed by
22 delay circuit 372; is that fair?

23 A. Well, there is a path from 342 through,
24 again, an input buffer, and then into a selector, and
25 then into that same FIFO that we've been talking

1 about, the FIFO read circuit labeled element 302.

2 Q. And Figure 5 of the Hiraishi reference
3 illustrates that the DQS data strobe signal is used
4 by the read FIFO 302 after being delayed by the delay
5 circuit 372, correct?

6 A. This figure on its own does show that the
7 signal is delayed before it arrives at 302.

8 Q. And would it be fair to say that a person
9 of ordinary skill in the art would understand that
10 the delayed DQS data strobe signal coming out of 372
11 can be used to sample the DQ data signal in the read
12 FIFO 302?

13 A. Perhaps. I think it depends. And
14 I would expect them to turn to further discussion of
15 those various components, particularly 302.

16 Q. Could you turn to Figure 1 of the
17 Hiraishi reference, and let me know when you have it
18 in front of you?

19 A. Okay. I have it.

20 Q. And are you familiar with Figure 1 of the
21 Hiraishi reference?

22 A. Yes, I have some familiarity with it.

23 Q. Figure 1 of the Hiraishi reference marked
24 as Exhibit 1005 is a schematic diagram for memory
25 module 100, according to paragraph 13, among other

1 places, correct?

2 A. That seems to match my recollection.

3 Q. And as shown in Figure 1 of the Hiraishi
4 reference marked as Exhibit 1005, there is a data
5 line L1 that is -- actually, there are multiple data
6 lines L1, each of which are longer than the data
7 lines labeled L2; is that fair?

8 A. Yes. That appears to be the case.

9 Q. And so, for example, the data line L1
10 connects a given data buffer 300 to the corresponding
11 memory chips in the top row, while the shorter data
12 line L2 connects a given data buffer corresponding to
13 the memory chips in the bottom row, which are closer
14 to the data buffer; is that fair?

15 A. I think that's fair.

16 Q. In your expert declaration marked as
17 Exhibit 2013, on page 72 you provide an annotated
18 version of Figure 1 to the Hiraishi reference marked
19 as 1005, correct?

20 A. Okay. I've got 2013 open. Can you
21 remind me which figure or page you were suggesting?

22 Q. Printed page number 72, which is PDF
23 page 76.

24 A. Okay. All right. Yes, I see that.

25 Q. And you explain in paragraph 122 of your

1 declaration marked as Exhibit 2013 that in your
2 annotated version of Figure 1 of the Hiraishi
3 reference shown on page 72, you have highlighted
4 memory chip 200-0 and data register buffer 300-0 in
5 red, and you have highlighted memory chip 200-19 and
6 data register buffer 300-4 in green, correct?

7 A. Yes.

8 Q. And so in your annotation of Figure 1 of
9 the Hiraishi reference marked as Exhibit 1005, the
10 memory chip 200-0 highlighted in red is further away
11 from the corresponding data buffer 300-0 in red as
12 compared to the memory chip 200-19 highlighted in
13 green is from the corresponding data buffer 300-4
14 highlighted in green, correct?

15 A. Yes.

16 Q. Or to put it another way, in your
17 annotation of Figure 1 of the Hiraishi reference
18 marked as Exhibit 1005, the memory chip 200-0
19 highlighted in red uses the longer data line L1 while
20 the memory chip 200-19 highlighted in green uses the
21 shorter data line --

22 (The Court Reporter requested
23 clarification.)

24 BY MR. CHANDLER:

25 Q. To put it another way, in your annotation

1 of Figure 1 of the Hiraishi reference marked as
2 Exhibit 1005, the memory chip 200-0 highlighted in
3 red uses the longer data line L1 while the memory
4 chip 200-19 highlighted in green uses the shorter
5 data line L2, correct?

6 A. Yes, that's correct.

7 Q. And it would be fair to say that a person
8 of ordinary skill in the art would understand that to
9 mean that for a read operation, it will take a longer
10 amount of time for the data from memory chip 200-0 in
11 red to reach the corresponding data buffer 300-0 in
12 red as compared to the amount of time it takes for
13 data from the memory chip 200-19 in green to reach
14 the corresponding data buffer 300-4 in green,
15 correct?

16 A. I think that's correct. They're arrayed
17 in this physical manner. There's a longer path for
18 the red signals to cover than the green, so they
19 should take a longer time.

20 The time difference may end up being
21 insignificant and something that doesn't need to be
22 addressed, but it depends on how big that time
23 difference is.

24 Q. And so in this example where we've been
25 discussing data line L1 versus data line L2, there

1 are different delays in the vertical direction which
2 sometimes may be referred to as a flight time delay
3 or a fly-by delay, and this is in contrast to the
4 fly-by delays in the horizontal direction with
5 respect to the control address and clock signals; is
6 that fair?

7 MR. LINDSAY: Objection. Form.

8 THE WITNESS: So I wouldn't -- as
9 illustrated here, I would not call them fly-by
10 delays, but flight time delays I don't have any
11 objection to. And those are different delays
12 from the fly-by delays incurred in -- because of
13 signal propagation in the horizontal direction.

14 BY MR. CHANDLER:

15 Q. So at a high level, in Figure 1 of the
16 Hiraishi reference marked as Exhibit 1005, we have
17 flight time delays in the vertical direction for the
18 data and strobe signals, and then we also have other
19 flight time or you could call it fly-by delays in the
20 horizontal direction for the control address and
21 clock signals; is that fair?

22 A. Yes, I believe that's fair.

23 Q. On page 73 of your expert declaration
24 marked as Exhibit 2013, you show part of Figure 15 of
25 the Hiraishi reference marked as Exhibit 1005,

1 correct?

2 A. Yes, that's correct.

3 Q. And Figure 15 of the Hiraishi reference
4 shows a timing diagram for read data, correct?

5 A. Yes.

6 Q. And as shown on page 73 of your expert
7 declaration, marked as Exhibit 2013, Figure 15 of the
8 Hiraishi reference shows the time A required for read
9 data from memory chip 200-0 to data register buffer
10 300-0 is less than the time A required for read data
11 from memory chip 200-19 to data register buffer
12 300-4, correct?

13 A. Yes, I see that.

14 Q. And that's the opposite of what we just
15 discussed in Figure 1 of the Hiraishi reference where
16 the timing relationship in your annotation would be
17 exactly the opposite, which is, in your annotation
18 shown on page 72 of Exhibit 2013, the time from the
19 memory chip 200-0 in red to the data register buffer
20 300-0 in red would be longer than the time from
21 memory chip 200-19 in green to data register buffer
22 300-4 in green; is that fair?

23 MR. LINDSAY: Objection. Form.

24 Misstates prior testimony.

25 THE WITNESS: No. The two are completely

1 consistent.

2 BY MR. CHANDLER:

3 Q. The numbering of the memory devices and
4 data buffers in Figure 1 does not correspond to the
5 numbering of the memory devices and data buffers in
6 Figure 15, and does not correspond to the time
7 required for read data on data line L1 compared to
8 read data on data line L2, correct?

9 MR. LINDSAY: Objection. Form.

10 THE WITNESS: Figure 15 does not identify
11 the delays for read data on L1 and read data on
12 L2 at all.

13 BY MR. CHANDLER:

14 Q. Well, it's the flight time. I don't know
15 if you were calling a delay a flight time.

16 But it's showing the time from the read
17 command at the memory chip until that data is
18 received at the data buffer, which would include a
19 flight time delay, correct?

20 A. Maybe I'm misunderstanding your question.
21 But there are two related but different flight time
22 delays here as I thought we agreed to refer to as
23 sort of the vertical and the horizontal.

24 Q. Right.

25 A. And Figure 15 is largely talking about

1 what happens as a consequence of the horizontal. The
2 annotated figure that we were looking at previously
3 is focused on the vertical. And the vertical flight
4 time delays are -- for either the red or the green
5 path are going to be significantly less than the
6 horizontal flight time or fly-by delays.

7 Q. And so is that the understanding that you
8 used in forming your opinions in your expert
9 declaration marked as Exhibit 2013?

10 A. I certainly intended to, yes.

11 Q. Let me mark -- actually, this has
12 previously been marked as Exhibit 1070. I'll put it
13 in the chat. And let me know when you have it.

14 (Exhibit 1070 was identified.)

15 Do you have Exhibit 1070?

16 A. Yes, I do.

17 Q. And Exhibit 1070 is -- it's mainly for
18 convenience. It reprints several of the paragraphs
19 from the Hiraishi reference marked as Exhibit 1005.
20 It shows Figure 5 in the upper left. And it shows
21 part of annotated Figure 15 in the upper right and
22 part of annotated Figure 11 in the bottom.

23 Do you see all of that?

24 A. Yes, I do.

25 Q. So Figure 15 is a timing chart for

1 explaining the read leveling operation, correct?

2 A. Yes, I believe so. Yeah.

3 Q. And then Figure 11 is a timing chart for
4 explaining a read operation -- what is sometimes
5 referred to as sort of a normal read operation after
6 initialization; is that fair?

7 A. Yes, I think that's fair.

8 Q. And so in Figure 15 during the read
9 leveling operation, that would occur at
10 initialization as we discussed previously, correct?
11 And this is what Hiraishi refers to as step S4 of the
12 initialization process, correct?

13 A. Yeah, let me see. Okay. I'm following
14 you.

15 Q. And so in the -- in Figure 15 during read
16 leveling, time A is measured, correct?

17 A. In essence, yes.

18 Q. And time A includes as you see above, the
19 blue rectangles includes a flight time, correct?
20 Write part of time A?

21 A. Yes, I see that.

22 Q. So the first five clock cycles of delay
23 are because of a CAS latency, which in this example
24 is five clock cycles, and then the amount of delay
25 after the fifth clock cycle is due to a flight time

1 delay, correct?

2 A. Yes, that seems to be what they're
3 indicating here.

4 Q. And for the read data, the flight time
5 delay of that data is in the vertical direction,
6 correct?

7 A. For the read data, the flight time of
8 that delay is in the horizontal and the vertical
9 direction.

10 Q. The read command has a horizontal flight
11 time delay, but the read data is going in the
12 vertical direction.

13 And so any flight time delay for the read
14 data is in the vertical direction; is that fair?

15 A. Yes. I thought you were talking about
16 the read delay, so that was my confusion.

17 Q. And so in Figure 15, the flight time
18 delay that's being measured there is from the memory
19 chip in green, which is going to output the data at
20 approximately time T5 given a CAS latency of five
21 clock cycles, down to the data register buffer below
22 it which, you know, is some distance away in the
23 vertical direction, which adds some flight time delay
24 to time A; is that correct?

25 A. Plus the flight time in the horizontal

1 direction.

2 Q. And so the flight time delay in the
3 vertical direction will be different depending on
4 whether that memory chip is in the top row, which is
5 further away and is connected with the longer data
6 line L1, versus whether that memory chip is in the
7 bottom row and is closer to the data buffer and is
8 connected with the shorter data line L2; is that
9 fair?

10 A. Yes, I think that's fair.

11 Q. And the longer flight time delay in the
12 vertical direction corresponds to the memory chip
13 using data line L1, and the shorter flight time delay
14 in the vertical direction corresponds to the memory
15 chips using data line L2; is that fair?

16 A. I think that's fair.

17 MR. CHANDLER: Why don't we take a short
18 break.

19 THE VIDEOGRAPHER: Off the record,
20 Counsel?

21 MR. CHANDLER: Yeah.

22 THE VIDEOGRAPHER: Off the record at
23 4:47 p.m. Pacific time.

24 (A recess was taken.)

25 THE VIDEOGRAPHER: On the record at

1 4:53 p.m. Pacific time.

2 BY MR. CHANDLER:

3 Q. Are there any clarifications or
4 corrections you'd like to give any of your testimony
5 from earlier today?

6 A. No, not that I can think of at the
7 moment.

8 Q. Turn to Figure 15 as shown in black and
9 white in the Hiraishi reference marked as
10 Exhibit 1005. So look at the full figure, not just
11 my annotation or your annotation, but the full
12 Figure 15, and let me know when you have it.

13 A. Okay. I have it with me.

14 Q. So the top section of that figure is a
15 timing diagram with reference to the
16 command/address/control register buffer, correct?

17 A. Yes.

18 Q. And that's essentially the controller in
19 the middle of the memory module; is that generally
20 fair?

21 A. Yes, I think that's generally fair.

22 Q. And so the timing diagram in Figure 15
23 shows at time T0 according to the line clock out, the
24 controller will send out to the memory devices and
25 the data register buffers a read command, correct?

1 A. The read command is sent out a little bit
2 earlier than that. It looks like it's trying to use
3 the clock to center the eye of the read command.

4 Q. I just want to make sure we're looking at
5 precisely same thing, which is that if you look at
6 the top clock line labeled clock out there's a T0,
7 and the read command that is sent out by the
8 controller is centered on time T0, which is how
9 commands are normally aligned, correct? They're
10 center aligned with the clock?

11 A. Yes, that's what I was getting at. It's
12 centered on T0. It's not sent out on T0. It's sent
13 out a little bit earlier.

14 Q. But it would be conventional to refer to
15 this read command as being transmitted at time T0;
16 would that be fair?

17 A. It is being transmitted during time T0,
18 sure. Or you could say it's received at time T0.

19 Q. Well, but it's not received at time T0.
20 I mean, that's one thing I want to be clear about.

21 Because what this Figure 15 is talking
22 about is the controller sending out a read command in
23 the horizontal direction to the memory chips and to
24 the data register buffers, correct?

25 A. Yes, but is it showing these command

1 values at the memory controller or at the memory
2 devices?

3 Q. Well, that's what we're going to get to.
4 It shows both, right? It shows in the top section of
5 Figure 15 under the rectangle command/address/control
6 register buffer, it's showing the timing within the
7 controller, which is that at clock out of the
8 controller at time T0, there is a read command
9 centered at time T0 in the clock out, which is sent
10 out towards the memory chips and data register
11 buffers.

12 Are we so far so good?

13 A. Yes, I see that now. I see what you're
14 getting at. But continue, please.

15 Q. And then below that line, that vertical
16 line from T0 on clock out, you see that there's the
17 first flight time delay. And this would be between,
18 you know, the timing diagram for the
19 command/address/control register buffer, and then we
20 get down to the timing diagram for the memory chip,
21 and Figure 15 is indicating that there is a flight
22 time delay for that read command as it goes from the
23 controller in the center of the memory module out to
24 the memory chip as well as out to the data register
25 buffer.

1 And that's the horizontal flight time
2 delay for the read command, correct?

3 A. Yes, that's correct.

4 Q. And so when the memory chip and also the
5 data register buffer receive the read command, that
6 is indicated as time zero on the clock in of the
7 memory chip as well as time zero of the clock in for
8 the data register buffer, correct?

9 A. Yes.

10 Q. So that first flight time delay shown on
11 the left side of Figure 15 is referring to the
12 horizontal flight time delay for the read command; is
13 that fair?

14 A. Yes, I think that's fair.

15 Q. All right. And at the memory chip, it
16 receives in the read command at time zero in the
17 clock in signal, and in this example, there's a CAS
18 latency of five clock cycles. And so at time T5 on
19 clock in for the memory chip is when the memory chip
20 is going to output data on the line DQ out; is that
21 fair so far?

22 A. Yes.

23 Q. And then after the memory chip outputs
24 data on the line DQ out, according to the memory
25 chips time T5 on clock in, that data is going go down

1 to the data buffer in the vertical direction on a
2 data line that is shown, for example, in Figure 1,
3 correct?

4 A. Yes.

5 Q. And there's going to be a vertical flight
6 time delay as the data travels from the memory chip
7 down the data line to the data register buffer that's
8 vertically below it, correct?

9 A. Yes, that's correct.

10 Q. And Figure 15 shows that vertical flight
11 time delay as the arrows between T5 and maybe T5.3 or
12 so; is that --

13 A. Something like that, sure.

14 Q. And the total time from T0 until time,
15 say, 5.3, is labeled as time A for memory chip 200-0
16 to data register buffer 300-0, correct?

17 A. Sure.

18 Q. And that time A comprises the CAS latency
19 delay of five cycles, plus the vertical flight time
20 delay, which looks like is perhaps 0.3 clock cycles
21 for the time A corresponding to the memory chip 200-0
22 to data register buffer 300-0; is that fair?

23 A. It looks like that is -- yeah, that might
24 be an estimate. I don't think these -- as
25 eyeballing, the delay is supposed to be --

1 Q. Yeah.

2 A. -- really reliable. Sometimes one of
3 them will be greater, sometimes the other, of the
4 flight times.

5 Q. But what is sort of reliable and clear is
6 that the time A comprises the CAS latency delay of
7 five clock cycles, plus the flight time delay in the
8 vertical direction for the read data as it travels
9 from the memory chip down to the data register
10 buffer; is that fair?

11 A. Yes, that's fair. Starting with when the
12 read command is received at the data buffer, yeah.

13 Q. And that also corresponds to the time the
14 read command is received at the memory chip, correct,
15 in this figure?

16 A. They're shown to be very close. And
17 I would expect them to be very close. They might be
18 identical. But I would also expect there to be some
19 small iterations between them.

20 Q. And then if we turn back to Figure 1 of
21 the Hiraishi reference marked as Exhibit 1005, the
22 flight time delay in the vertical direction will be
23 greater for the data line L1 connected to memory
24 chips at the top as compared to the flight time delay
25 for the data on data line L2 that's connected to the

1 memory chips in the bottom row; is that fair?

2 A. Yes, the length of the wires for L1 is
3 greater than the length of the wires for L2, so the
4 delay should be greater.

5 Q. Could you turn to Figure 7 of the
6 Hiraishi reference, and let me know when you're
7 there?

8 A. Okay.

9 Q. Now, Figure 7, as explained in
10 paragraph 12, is a connection diagram of the memory
11 module 100, correct?

12 A. Okay.

13 Q. And Figure 7 of Hiraishi uses a lot of
14 the same labels that appear in Figure 1, such as L1
15 and L2 and -- for example, correct?

16 A. Yes.

17 Q. But there are also some differences.
18 I mean, Figure 7 doesn't look the same as Figure 1
19 and, for example, Figure 7 is labeling the closest
20 memory chip and data buffer as zero and the furthest
21 memory chip and data buffer as 4, which is sort of
22 different from Figure 1, correct?

23 A. I don't remember how figure -- yeah,
24 I think Figure 1 might have labeled them in the
25 opposite direction.

1 Q. Right.

2 A. But, regardless, I certainly agree this
3 figure is different. It's a different
4 representation.

5 Q. And, for example, Figure 1 shows,
6 I guess, five data buffers off to the left and four
7 data buffers off to the right, but then Figure 7
8 shows five data buffers off to the right; is that
9 fair?

10 A. Yes.

11 Q. In Hiraishi's memory module, the data
12 register buffers 300 are each coupled to respective
13 data connectors 120 with a corresponding data line L0
14 as explained, for example, in paragraph 103 of
15 Hiraishi; is that fair?

16 A. I believe that's -- yes, that's
17 consistent with my understanding.

18 Q. And the data line L0 transfers both data
19 signals DQ-Pre, and the corresponding strobe signals
20 DQS-Pre, correct?

21 A. Yes, that is how Figure 7 is labeled.

22 Q. And data lines L1 and L2 connect the data
23 register buffer to respective memory devices,
24 correct?

25 A. Yes, that's correct.

1 Q. Each of data lines L1 and L2 transfer
2 both data signals DQ-Post and corresponding strobe
3 signals DQS-Post, correct?

4 A. Yes, that's accurate.

5 Q. And -- we should put that aside.

6 Would it fair to say, Dr. Mangione-Smith,
7 that Netlist did not invent the memory module?

8 A. I would agree that that's fair.

9 Q. And Netlist did not invent DDR memory
10 devices, correct?

11 A. Well, they did not -- they were not the
12 original inventors of DDR memory devices, that's
13 true.

14 Q. And they did not invent DDR2 or DDR3
15 memory devices, correct?

16 A. I think that's accurate.

17 Q. Netlist did not invent the buffered DIMM
18 memory module, correct?

19 A. My recollection is that Netlist did not
20 invent the fully buffered DIMM memory module.

21 Q. And Netlist did not invent distributed
22 data buffers for a memory module, correct? For
23 example, the Hiraishi reference is prior art to the
24 '608 patent and the Hiraishi reference has
25 distributed data buffers, right?

1 A. Netlist has claimed to have invented a
2 particular kind of distributed data buffer. I'm
3 accepting that Hiraishi is prior art. I haven't gone
4 through and verified that myself. And I don't know
5 that I would characterize it as a distributed data
6 buffer. I haven't really thought about it.

7 Q. Netlist did not invent tri-state buffers,
8 correct?

9 A. That's correct.

10 Q. Netlist did not invent DQ data signals or
11 DQS data strobe signals or clock signals, correct?

12 A. That's correct, they did not invent any
13 of those three types of signals.

14 Q. And Netlist did not invent the fly-by
15 topology and memory modules, correct?

16 A. That's correct.

17 Q. Netlist did not invent read leveling or
18 write leveling, correct?

19 A. Yeah, I think that's a fair
20 characterization.

21 Q. Netlist did not invent sampling signals,
22 correct?

23 A. Well, they use sampling signals.
24 I wouldn't say that they invented the concept.

25 Q. Netlist did not invent the ability to

1 delay a strobe signal or a data signal, correct?

2 A. I would say that's correct.

3 Q. Are there any corrections or
4 clarifications you'd like to make to your testimony
5 that you have given to me today?

6 A. Not that I feel like I need to make as
7 I sit here.

8 MR. CHANDLER: All right. I pass the
9 witness.

10 MR. LINDSAY: Let's go off the record.

11 THE VIDEOGRAPHER: I'm sorry, Counsel.
12 Did I hear "off the record"?

13 MR. CHANDLER: Yes, off the record is
14 fine. Why don't we go off of the record and
15 then, John, you can tell us how long you want.

16 THE VIDEOGRAPHER: Off the record at
17 5:12 p.m. Pacific time.

18 (A recess was taken.)

19 THE VIDEOGRAPHER: On the record at
20 5:27 p.m. Pacific time.

21 EXAMINATION

22 BY MR. LINDSAY:

23 Q. Dr. Mangione-Smith, do you recall earlier
24 today testifying about whether or not you took into
25 consideration that DDR3 memory modules adopted a

1 fly-by topology for commands, addresses, and control
2 signals, and your response was that you don't recall,
3 but you would be happy to review your declaration
4 further; do you recall that?

5 A. Yes, I do.

6 Q. Okay. Could you, in your declaration,
7 then, Exhibit 2013, turn to paragraph 125?

8 A. Okay.

9 Q. In the first sentence -- can you read the
10 first sentence for the record, please?

11 A. Yes. The first sentence says:

12 Because Hiraishi assumes that the
13 differences in fly-by delays is always less than
14 one clock cycle, Hiraishi simply sets the
15 buffer's latency to the next higher clock cycle
16 to adequately address all expected flight delays.

17 Q. So did you consider the fact that
18 Hiraishi adopted a fly-by delay topology in rendering
19 your opinions?

20 A. Yes, I did. That was an element of
21 Dr. Wedig's arguments, and I was considering his
22 arguments.

23 Q. And could we turn to paragraph 64 of your
24 declaration (audio disruption)? And once you're
25 there, if you could just read the first sentence for

1 the record.

2 A. So paragraph 64, the first sentence says:
3 Tokuhiro discloses a fly-by topology for
4 command/address/clock wiring between the memory
5 controller 12 and the SDRAM devices mounted on
6 DIMM module 11.

7 Q. So did you consider the fact that
8 Tokuhiro adopted a fly-by delayed topology in
9 rendering your opinions?

10 A. Yes, absolutely. That was a significant
11 component of -- or it was at least a component of
12 Dr. Wedig's analysis and arguments.

13 Q. Thank you.

14 Could you pull up what was introduced as
15 Exhibit 1079?

16 A. Yes, I have it in front of me.

17 Q. Is this representing an annotated version
18 of Hiraishi Figure 7?

19 A. Yes, I believe it is.

20 Q. Do you recognize what additional
21 information has been added to this that was not in
22 Hiraishi's Figure 7?

23 A. Well, first of all, the coloring in
24 general was added. But more significantly, the
25 clocks that show the various degrees of delay for

1 horizontal flight times on the bottom of this exhibit
2 were added to Hiraishi.

3 Q. Thank you.

4 So I apologize for jumping back and
5 forth, but if you could look at your declaration
6 paragraph 120.

7 A. Yes, I'll switch to that. I'll also say
8 that I think the clocks at the bottom of the second
9 page were also added. But I will turn to 120. Okay.
10 I'm sorry, which exhibit, 1020?

11 Q. Sorry. Your declaration, Exhibit 2013.

12 A. Okay. I'm there.

13 Q. And so in paragraph 120, could you just
14 read the first sentence for me?

15 A. Yes, once I get there.

16 So the first sentence of 120 I state:

17 Hiraishi does not envision delays
18 exceeding one clock cycle, as is evident from
19 Figure 15, which is -- a partial reproduction is
20 below.

21 Q. So the annotated Figure 7 that we just
22 looked at a moment ago that was introduced as
23 Exhibit 1079 that shows clock -- that shows delays
24 greater than one clock cycle, was that a concept
25 envisioned by Hiraishi?

1 MR. CHANDLER: Objection. Form.

2 THE WITNESS: I didn't find flight time
3 delays greater than one clock cycle considered
4 in Hiraishi at all.

5 BY MR. LINDSAY:

6 Q. And also with respect to Exhibit 1079,
7 there's an annotation that was added showing the
8 possibility of two commands being on the same line at
9 the same time; do you recall that?

10 A. Yes, I do.

11 Q. Does Hiraishi -- well, strike that.

12 What was that (indecipherable)?

13 (The Court Reporter requested
14 clarification.)

15 MR. CHANDLER: Yes, same request, John.
16 Something blipped out so I couldn't hear the
17 question to see if it's objectionable.

18 BY MR. LINDSAY:

19 Q. The concept of having two commands on the
20 same line at the same time, you gave that a name
21 earlier today. What was that?

22 A. I called it wire pipelining.

23 Q. Right.

24 Does Hiraishi describe wire pipelining?

25 A. No.

1 Q. Do you recall any disclosure in Hiraishi
2 that would suggest he envisioned the possibility of
3 there being two commands on a line at the same time?

4 A. No.

5 Q. Is it inherent that you would have more
6 than one command on a line at the same time in a
7 device such as Hiraishi's?

8 A. No. And, in fact, that usage greatly
9 complicates system design and timing. And in my
10 experience, engineers try to avoid it as much as
11 possible.

12 Q. Do you recall earlier today testifying
13 about read leveling being used to account for a skew
14 of data signals in the context of the DDR memory
15 module?

16 A. Yes, I do.

17 Q. With that in mind, can you turn to
18 paragraph -- page, actually, 78, printed page 7-8?

19 MR. CHANDLER: I'm sorry, it clipped out,
20 Jonathan. Where? Where?

21 BY MR. LINDSAY:

22 Q. So Exhibit 2013, page 78, begins
23 paragraph 133.

24 A. Yes, I'm there.

25 Q. Hiraishi describes what it calls an S4

1 read leveling operation.

2 Is that what you're discussing here in
3 paragraph 133?

4 A. Yes, this --

5 MR. CHANDLER: Objection. Form.

6 THE WITNESS: The section reads:

7 Hiraishi S4 read leveling operations
8 adjust the activation timing of Hiraishi's input
9 buffers.

10 BY MR. LINDSAY:

11 Q. And can you read for the record the last
12 sentence of that paragraph 133?

13 A. The last parenthesized sentence or the
14 one before that?

15 Q. A fair point. Starting with the unquoted
16 sentence at the end, adjustment.

17 A. Adjustment to the timing of when the
18 input buffers INB are turned -- maybe
19 that's an error, it probably should
20 be turned on -- is carried out to
21 ensure they are active when data --
22 that's another broken sentence.

23 But what I was trying to say is that the
24 input buffers are ensured to be turned down when read
25 data is present.

1 Q. And then the quoted passage that follows
2 that from Hiraishi, is that describing what Hiraishi
3 regards as S4 read leveling?

4 MR. CHANDLER: Objection. Form. And
5 objection leading.

6 THE WITNESS: Yes, it is. It says:
7 The time is dot, dot, dot, used in an
8 adjustment of the activation timing of the input
9 buffer circuit INB and the like.

10 BY MR. LINDSAY:

11 Q. So does Hiraishi describe read leveling
12 in the same way that the DDR3 standard might discuss
13 or at least envision read leveling?

14 MR. CHANDLER: Objection. Form.

15 THE WITNESS: No. I believe it's -- it's
16 very different. Hiraishi is focusing on when to
17 turn on the input buffers I believe, in part, at
18 least, to save power consumption.

19 BY MR. LINDSAY:

20 Q. If you could turn to paragraph 110.

21 A. Okay. I'm there.

22 Q. Can you describe what Hiraishi's write
23 leveling operation is about generally?

24 MR. CHANDLER: Objection. Form.

25 THE WITNESS: So I say:

1 Hiraishi's S4 write leveling accounts for
2 mismatches between the time of receipt of a clock
3 signal and the data strobe DQS at the memory
4 chip.

5 BY MR. LINDSAY:

6 Q. With that in mind, do you recall earlier
7 today testifying about write leveling in the context
8 of DDR3 memory and it being used to address control
9 and clock address control and clock signals skew in
10 order to allow the operation of the module to be
11 accurate?

12 A. Yes, I recall that discussion.

13 Q. Is Hiraishi's write leveling operation
14 different than write leveling in the context of DDR3?

15 MR. CHANDLER: Objection. Form.

16 THE WITNESS: Yes, it is different.

17 BY MR. LINDSAY:

18 Q. For example, does Hiraishi's write
19 leveling affect the timing or skew of address and
20 control signals at all?

21 MR. CHANDLER: Object to form.

22 THE WITNESS: I don't believe so, no.

23 BY MR. LINDSAY:

24 Q. Can you pull up the Exhibit 1080? It was
25 introduced as 1080.

1 A. Yes, I have it in front of me.

2 Q. Do you recall testifying about these
3 figures from the '608 patent and the annotations that
4 were added?

5 A. Yes, I do.

6 Q. On page 2, the element 1520, which is
7 referred to as light strobe receiver, receives a
8 clock signal.

9 Is that -- am I saying that correctly?

10 A. Yes, that's correct.

11 Q. Do you recall earlier today discussing
12 whether that clock signal could be used to delay the
13 DQS signal?

14 A. Yes, I do.

15 Q. Is it inherent that the clock signal
16 would cause a delay to the DQS signal?

17 A. No. In fact, a delay to the clock signal
18 could introduce sending out the DQS signal earlier.

19 Q. Are there reasons why you would want to
20 avoid using the clock signal in the context of that
21 embodiment in a way that causes a delay?

22 MR. CHANDLER: Objection. Form.

23 THE WITNESS: Yes. I'm not familiar with
24 anybody using a clock signal in quite this way
25 to intentionally introduce a delay. Usually,

1 the delay control is done using other methods.

2 BY MR. LINDSAY:

3 Q. With reference to the '608 patent,
4 Exhibit 1001, do you recall earlier today discussing
5 Figure 19 and the passage at the top of column 19?

6 A. Yes, I do.

7 Q. So in the embodiment of Figure 19, can
8 you describe for me what your understanding is of
9 that embodiment as it's described in the top of 19?

10 A. Sure. My understanding is that the
11 embodiment in Figure 19 corresponds to an embodiment
12 where the module has no -- receives no clock signal.
13 And so it's regenerating a clock signal and then
14 making use of that clock signal for other parts of
15 the system, which is I don't believe any --
16 corresponds to any claims in the patent.

17 Q. Right.

18 So if you could look at column 18,
19 line 65.

20 A. Yes.

21 Q. Where it refers to:

22 In certain embodiments, especially the
23 embodiments shown in Figure 2D.

24 Do you see that?

25 A. Yes, I do.

1 Q. 2D -- Figure 2D is discussed in column 8.
2 Can you turn there so we can discuss that?

3 A. Okay.

4 Q. On line 61, the '608 patent says that,
5 referring to the embodiment of Figure 2D:

6 The memory devices 112 do not receive the
7 module control [sic] signal from the control
8 circuit 116. Instead, each data buffer 118
9 regenerates the clock that is used by the
10 respective set of memory devices 112.

11 Did I read that correctly?

12 A. Yes, you did. I see that.

13 Q. Is that consistent with your
14 understanding of the embodiment of Figure 19?

15 A. Yes, it is.

16 Q. In claimed invention, if you could look
17 at column 19, claim 1.

18 A. Okay.

19 Q. Do you see the second element, a module
20 control device?

21 A. Yes, I do.

22 Q. And the last clause, is the module
23 controlled device outputting a module clock signal?

24 A. Yes, I see that.

25 Q. In the next element, the memory devices

1 element.

2 A. Okay.

3 Q. Does the claimed invention require the
4 memory devices to receive the module clock signal
5 that is output by the module control device?

6 A. Yes, it does.

7 Q. So can that possibly be the embodiment of
8 Figure 19 and Figure 2D?

9 MR. CHANDLER: Objection. Form.

10 Leading.

11 THE WITNESS: I don't believe it could
12 possibly be that.

13 BY MR. LINDSAY:

14 Q. If you look at Exhibit 1029, the Butt
15 reference.

16 A. Okay.

17 Q. Do you recall earlier today discussing
18 paragraph 19 with Mr. Chandler?

19 A. Yes, I do.

20 Q. And there's a sentence in the middle of
21 that paragraph in particular that you discussed with
22 him that talks about writing data to FIFOs 112 in
23 response to, e.g., clocked by, the signals PDQS_out
24 and NDQS_out, respectively.

25 Do you recall that?

1 A. Yes.

2 Q. Paragraph right above that, can you read
3 the last sentence of that paragraph 118 [sic] for the
4 record?

5 MR. CHANDLER: Objection. Form.
6 Leading.

7 THE WITNESS: So it says:

8 Each of the DPs 114 may be configured to
9 present the DQ data to a respective asynchronous
10 FIFO 112 via the signals DR_PDQ_out and
11 DR_NDQ_out after the data is sampled using the
12 delayed read strobe signals DQS.

13 BY MR. LINDSAY:

14 Q. And then in paragraph 20 right after
15 that, does that also discuss sampling read data with
16 a read data strobe signal DQS before passing it to
17 the memory controller?

18 A. Yes, indeed.

19 MR. CHANDLER: Objection. Form. And
20 leading.

21 BY MR. LINDSAY:

22 Q. So in the context of both surrounding
23 paragraphs, what is your understanding of what it
24 means when Butt says that read data generally written
25 to the FIFOs 112 in response to, e.g., clocked by,

1 the identified DQS signals?

2 A. It's my understanding that he means the
3 FIFO samples, the data based on the DQS signals.

4 MR. LINDSAY: Thank you. I don't have
5 any further questions.

6 MR. CHANDLER: Let's take a short break,
7 maybe ten minutes.

8 THE VIDEOGRAPHER: Off the record at
9 5:55 p.m. Pacific time.

10 (Off the video record, following
11 discussion was held.)

12 MR. LINDSAY: Regular delivery, no rough.
13 Will handle read and sign.

14 (A recess was taken.)

15 THE VIDEOGRAPHER: On the record. It's
16 6:10 p.m. Pacific time.

17 EXAMINATION

18 BY MR. CHANDLER:

19 Q. Dr. Mangione-Smith, you were asked some
20 questions about horizontal flight time delays of more
21 than one clock cycle, correct?

22 A. Yes.

23 Q. And I want to follow up on those
24 questions. And for clarity, I want to use
25 Exhibit 1078, page 2, which has some clocks to help

1 illustrate the concept.

2 So could you pull that up and let me know
3 when you have it in front of you?

4 A. Yes, I have it.

5 Q. And the concept of a signal, you know,
6 traveling 8 centimeters or 15 centimeters at
7 800 megahertz or 1600 megahertz, et cetera, that's
8 not a concept that Netlist invented, correct?

9 A. That's correct. If I understand the
10 question, it's just a matter of physics.

11 Q. That's what I was going to get at.

12 So it's sort of just a matter of physics
13 that as the DDR3 clock speeds get faster and faster,
14 you know, then you go into DDR4, which can be even
15 faster, and I'm sure there's a DDR5 and a DDR6 where
16 they're trying to get even faster clock speeds, it's
17 a matter of physics that the distance that the
18 signals are going to travel in a single clock period,
19 in general, are going to get shorter and shorter.

20 And so it's essentially a matter of
21 physics where you have this tipping point where the
22 distance that the signals travel within one clock
23 period, suddenly it's such a short distance that it
24 happens within the horizontal width of the memory
25 module; is that fair?

1 A. I guess it depends on how you route the
2 signals. However, I would agree, in general, if --
3 there will be a certain distance that the signal will
4 be able to travel in a clock cycle.

5 And you are likely -- we have faced for a
6 long time the option of trying to route such signals
7 over wires that are longer than that distance.

8 Q. And so to be clear, Netlist did not
9 invent two clock signals going in the horizontal
10 direction on a memory module at the same time;
11 instead, that is a consequence of the physics of
12 clock signals as they get faster and faster as
13 standardized by JEDEC; is that fair?

14 MR. LINDSAY: Objection. Form.

15 THE WITNESS: It's a consequence of the
16 signals getting faster and faster, and then
17 whatever trace length the signals are being
18 communicated over.

19 BY MR. CHANDLER:

20 Q. And I think you said that Hiraishi,
21 marked as Exhibit 1005, you don't believe addressed
22 the problem of a clock period that's so short that
23 there could be two clock signals going in the
24 horizontal direction on the memory module at the same
25 time; is that fair?

1 MR. LINDSAY: Objection. Form.

2 THE WITNESS: That's right. I don't
3 recall seeing anything in Hiraishi discussing
4 how to adapt to the problems introduced by what
5 I've referred to as wire pipelining.

6 BY MR. CHANDLER:

7 Q. And as shown on Exhibit 1005, Hiraishi
8 was published in 2010, correct?

9 A. Yes.

10 Q. And as we discussed at the very beginning
11 in this IPR, our person of ordinary skill in the art
12 exists as of July 2012; is that fair?

13 A. Yes.

14 Q. And would it be fair to say that by July
15 of 2012, a person of ordinary skill in the art would
16 recognize, given the clock speeds for DDR3 memory
17 devices getting faster and faster, that there would
18 be this potential problem on memory modules that in
19 the horizontal direction you could have multiple
20 clock signals on the wire at the same time, which you
21 describe using the catch phrase "wire pipelining,"
22 correct?

23 MR. LINDSAY: Objection. Form.

24 THE WITNESS: Yes, I did -- that is the
25 phrase that I've heard and makes sense to me.

1 BY MR. CHANDLER:

2 Q. And it would be fair to say that by July
3 of 2012, a person of ordinary skill in the art would
4 see the writing on the wall that the clock speeds for
5 these DDR3 and subsequent memory devices are getting
6 faster and faster, and that there exists this
7 situation where there can be two clock signals in the
8 horizontal direction on the memory module at the same
9 time; is that fair?

10 MR. LINDSAY: Objection. Form.

11 THE WITNESS: I would not say that, no.

12 BY MR. CHANDLER:

13 Q. That's -- that timing as we discussed is
14 a matter of physics, right?

15 A. Yes.

16 Q. And Netlist was not the first person to
17 recognize that matter of physics and the timing issue
18 as you get faster and faster and the potential for
19 wire pipelining, correct?

20 A. Netlist was not the first party to
21 recognize that fact of physics, no.

22 Q. And we don't need to go into it in
23 detail, but Dr. Wedig did discuss that there were
24 people that had recognized this problem other than
25 Netlist before the '608 patent.

1 You're not contesting that, are you?

2 A. No. I'm just saying that I wouldn't say
3 that a person of ordinary skill in the art would have
4 recognized it in 2012, particularly the use of wire
5 pipelining.

6 In my experience, there are two circuit
7 design techniques that no engineer ever wants to use
8 unless they absolutely have to, and one of those is
9 wire pipelining. It for decades has just been viewed
10 as problematic. It's cool when it works. It's
11 difficult to get working right. It takes very good
12 engineers.

13 Q. Do you think the '608 patent teaches a
14 solution to wire pipelining?

15 A. I don't know. I haven't voiced an
16 opinion on that.

17 Q. You were asked some questions about
18 Hiraishi and S4 read leveling and S4 write leveling,
19 correct?

20 (The Court Reporter requested
21 clarification.)

22 BY MR. CHANDLER:

23 Q. You were asked some questions on redirect
24 about Hiraishi and its S4 read leveling and write
25 leveling, correct?

1 A. Yes, I recall that.

2 Q. And as you may have noticed, I prefer
3 pictures. So let me just put in the chat
4 Exhibit 1069, which was used previously with
5 Dr. Wedig. It's just a simple picture of Hiraishi.
6 And let me know when you have it.

7 (Exhibit 1069 was identified.)

8 A. Okay. I have it open.

9 Q. So in Exhibit 1069, there's Figure 5 of
10 Hiraishi in the middle, and then on the right in
11 green there's a representation of a memory chip, and
12 then on the left there's a black rectangle
13 representing a system memory controller on the host
14 computer.

15 Does that generally make sense to you?

16 A. Yes, it does.

17 Q. And so on redirect you were being asked
18 questions about S4 read and write leveling in
19 Hiraishi, which is between the memory chip as shown
20 on the right of Exhibit 1069 and Hiraishi's data
21 buffer as shown in Figure 5 in the middle of
22 Exhibit 1069; is that fair?

23 A. Yes, that's fair.

24 Q. And I believe the gist of your testimony
25 was that there was DDR3 read leveling and write

1 leveling that existed in the prior art, but that in
2 your opinion, it differed from Hiraishi's S4 read
3 leveling and write leveling; is that fair?

4 MR. LINDSAY: Objection. Form.

5 THE WITNESS: Yes, I think that's fair.

6 BY MR. CHANDLER:

7 Q. And what you were not asked about and
8 what you did not testify about in redirect was S5
9 read leveling and write leveling in Hiraishi between
10 the system memory controller and the data buffer,
11 correct?

12 A. I think that that's correct.

13 Q. And in S5 read leveling and write
14 leveling in Hiraishi, the system memory controller
15 has the read leveling circuit and the write leveling
16 circuit that is used for read and write leveling, in
17 contrast to S4 read and write levels where it's the
18 data buffer that has the read leveling and write
19 leveling circuit, correct?

20 MR. LINDSAY: Objection. Outside the
21 scope of redirect. And form.

22 THE WITNESS: So pardon me, are you
23 talking about Hiraishi -- you're talking about
24 Hiraishi, not DDR3 specifically?

25

1 BY MR. CHANDLER:

2 Q. Correct. So, although -- I mean, I guess
3 we should be clear. So why don't you go ahead and
4 answer the question with respect to Hiraishi.

5 A. Yeah, I focused on the S4 leveling
6 because I believe that was the focus of Dr. Wedig's
7 arguments and analysis because the S4 leveling
8 takes -- is -- what he calls -- what's called S4
9 leveling here is arguably relevant to the delays in
10 the claims, which is what he was -- ultimately, the
11 root of his analysis.

12 I don't recall S5 leveling being relevant
13 to that, but maybe it was and I'm just misremembering
14 at the end of the day.

15 Q. And in the DDR3 read leveling and write
16 leveling, it would be the -- common for the memory
17 controller to be performing the read leveling and
18 write leveling, correct?

19 The DDR3 standard didn't standardize a
20 data buffer performing the read leveling and write
21 leveling. When the DDR3 standard refers to read
22 leveling and write leveling, the common way at that
23 time was for the memory controller to perform the
24 read leveling and write leveling; is that fair?

25 MR. LINDSAY: Objection. Form.

1 THE WITNESS: That's fair.

2 BY MR. CHANDLER:

3 Q. And that's part of the difference that
4 I believe you were trying to point out between the
5 DDR3 standard approach to read and write leveling and
6 Hiraishi's approach to S4 read leveling and write
7 leveling; is that fair?

8 A. Yes, that's part of the differences that
9 I was trying to point out.

10 Q. And in particular, focusing now on the
11 sort of standardized DDR3 approach to read leveling
12 and write leveling, that approach focused on leveling
13 directly with the memory devices as opposed to
14 leveling with the data buffer; is that fair?

15 A. I think that that's fair.

16 MR. CHANDLER: All right. No more
17 questions, hence, concludes this deposition.

18 THE VIDEOGRAPHER: Would you like me to
19 conclude the video deposition at this time?

20 MR. CHANDLER: Yes, please.

21 THE VIDEOGRAPHER: Before I do, I just
22 need to ask if anyone needs a copy of the video.

23 MR. CHANDLER: Yes, we'll take a copy of
24 the video. No particular rush on the video. We
25 will take it, though. And then, as I think the

1 court reporter knows, for the deposition
2 transcript we'd like a final by Friday,
3 June 7th, in three business days.

4 THE VIDEOGRAPHER: Thank you.

5 And, Mr. Lindsay, sir, do you need a copy
6 of video?

7 MR. LINDSAY: No, I don't. Thank you.

8 THE VIDEOGRAPHER: Perfect. Thank you
9 very much.

10 THE COURT REPORTER: We do have an order
11 for a rough, Mr. Chandler.

12 MR. CHANDLER: I don't need a rough if we
13 get the final on Friday. I mean, the real-time
14 during the deposition was most important. And
15 now that we're done, I don't need a rough
16 anymore.

17 THE VIDEOGRAPHER: Thank you.

18 This concludes today's deposition of
19 Dr. William Mangione-Smith. We're off the video
20 record at 6:28 p.m. Pacific time on June 4th,
21 2024.

22 (The deposition of DR. WILLIAM
23 MANGIONE-SMITH concluded at 6:28 p.m.)

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DEPOSITION ERRATA SHEET

Our Assignment No. J11139007

Case Caption: SAMSUNG VS. NETLIST

DECLARATION UNDER PENALTY OF PERJURY

I declare under penalty of perjury that I have read the entire transcript of my deposition taken in the above-captioned matter or the same has been read to me, and the same is true and accurate, save and except for changes and/or corrections, if any, as indicated by me on the DEPOSITION ERRATA SHEET hereof, with the understanding that I offer these changes as if still under oath.

Signed on the _____ day of _____ 2024.

DR. WILLIAM MANGIONE-SMITH

Subscribed and sworn to on the ____ day of _____ 2024 before me.

Notary Public, in and for the State of _____.

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DR. WILLIAM MANGIONE-SMITH

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DR. WILLIAM MANGIONE-SMITH

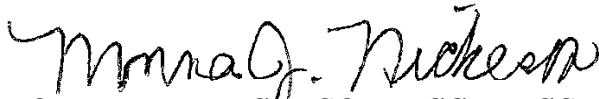
C E R T I F I C A T E

I, MONNA J. NICKESON, CCR, CSR, CLR, RPR, CRR,
the undersigned Certified Court Reporter, authorized
to administer oaths and affirmations in and for the
states of Washington (3322), Oregon (16-0441), Idaho
(1045), and California (14430), do hereby certify:

That the sworn testimony and/or
proceedings, a transcript of which is attached, was
given before me at the time and place stated therein;
that the witness was duly sworn or affirmed to
testify to the truth; that the testimony and/or
proceedings were stenographically recorded by me and
transcribed under my supervision. That the foregoing
transcript contains a full, true, and accurate record
of all the testimony and/or proceedings occurring at
the time and place stated in the transcript.

That I am in no way related to any party to
the matter, nor to any counsel, nor do I have any
financial interest in the event of the cause.

IN WITNESS WHEREOF I have set my hand on June 7, 2024



MONNA J. NICKESON, CCR, CSR, CLR, RPR, CRR