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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner,

v.

NETLIST, INC.,
Patent Owner

IPR2023-00847
Patent 10,268,608 B2

Record of Oral Hearing
Held: September 5, 2024

Before JON M. JURGOVAN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

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The above-entitled matter came on for hearing on September 5, 2024, commencing at 1:00 p.m., via video teleconference.

P R O C E E D I N G S

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JUDGE MCSHANE: Good afternoon. We're here to conduct a hearing in Samsung Electronics Co., LTD v. Netlist, Inc. This is IPR2023-00847. Can we have appearances, please? Who do we have from Petitioner?

MR. CHANDLER: Good morning, Your Honor. This is Ted Chandler from Baker Botts on behalf of the Petitioner, Samsung Electronics Co., LTD. And with me is lead counsel, Eliot Williams. I will be presenting arguments this morning.

JUDGE MCSHANE: Okay. Thank you, Mr. Chandler. And who do we have from Patent Owner, please?

MR. BEMBEN: Thank you, Your Honor. This is Richard Bemben with Patent Owner from Sterne Kessler. And with me in the room is in-house counsel at Patent Owner Netlist, Tobin Hobbs.

JUDGE MCSHANE: Okay. And Mr. Bemben, you're going to be presenting today?

MR. BEMBEN: I will be presenting, yes, Your Honor.

JUDGE MCSHANE: Thank you. All right. Very briefly, I'm going to give some general guidance. If at any time during the proceeding you encounter technical difficulties or audio problems, please let us know or contact some of the other team members who provided you with connection information. We have the entire record, including demonstratives. So, when referring to the demonstratives, exhibits, papers, and the like, just try to identify them in some manner so that we get a clear record, that's important.

And also, you may run your own slide deck if you prefer, or we have it here too as well. If you call out the slide numbers, we can follow along too as well, whatever you prefer. The hearing will be conducted as we identified in the oral hearing order. Each side has 60 minutes of argument time. Petitioner will go first and may reserve rebuttal time. Patent Owner may present its response and you may reserve surrebuttal time. And with that, that's the end of the brief directions here. And does anybody have any questions? No, not hearing anything, we will commence. So, Petitioner, you may proceed.

MR. CHANDLER: Thank you. I have some slides I'd like to share. So, Judge McShane, are you able to see the demonstratives, Exhibit 1089, that are on the screen, and are you able to hear my voice okay?

JUDGE MCSHANE: Yeah, everything's good. And also, I just forgot to ask you, do you want to reserve rebuttal time?

MR. CHANDLER: Yes, 15 minutes, please.

JUDGE MCSHANE: Thank you.

MR. CHANDLER: Thank you. And may it please the Board. Starting with slide 5. Slide 5 provides an overview of the '608 patent. As shown on the left in yellow, the '608 patent is a continuation of the '035 patent, which as I will discuss later was the subject of a final written decision by the Board that we contend gives rise to collateral estoppel. Also on the left in yellow is the provisional filing date of July 27th, 2012, which for purposes of this IPR is what both sides have assumed is the effective date of the challenged claim, given that the prior art is well before that date. As shown in blue, the '608 patent concerns distributed data buffers and specifically how those data buffers control the timing of signals going

through those data buffers. Slide 6 shows Figure 2C of the '608 patent, which shows the memory module. The green boxes are the memory devices on the memory module. Below the memory devices are the data buffers highlighted in blue. The patent sometimes refers to those blue data buffers as isolation devices or load reduction devices. And in the center in red is the module controller, which sends signals horizontally out to the left and to the right to control the data buffers in blue, and also the memory devices in green.

JUDGE MCSHANE: Mr. Chandler, two things. Number one, on the previous slide you had the claim, and I think I at least am interested in how or -- there we go -- how the claim term data path is -- should be interpreted in light of the claim. So, that's one thing. And then also, you were talking about signals going horizontally and vertically and you used that terminology I believe in the reply. And when you're using that terminology, what exactly do you mean? So, anyway, however you'd want to address those questions is fine.

MR. CHANDLER: Yeah, those -- I think it'll be easy to address those questions after I go through some introduction and those are two questions that'll be addressed very, very quickly. So, turning to slide 9, the Instituted Grounds. As shown on the bottom left after the petition was filed, Netlist disclaims Claims 6 through 12 which mooted Grounds 4 and 5. And then as shown on the upper right after the petition was filed, the Board issued its final written decision in IPR2022-00236, which invalidated Claims 1, 10 through 13, and 21 through 22 of the related '035 patent. That decision was not appealed, and those claims have now been canceled. That decision relied on a reference called Osanai, but the parties in this IPR agree that the

Osanai reference is identical in all relevant respects to the Hiraishi reference in Grounds 1 through 3, which is why we contend that there's collaborative estoppel, as I will discuss later. And that issue of collateral estoppel, Judge McShane, is also relevant to your question about the meaning of data paths. And so, I'll pick up on that when we get to that point.

For Ground 3, Netlist only relies on its arguments concerning Grounds 1 and 2. So, my presentation today will only focus on Grounds 1 and 2.

Slide 11 shows the level of skill in the art, which is undisputed. As shown in yellow, a person of ordinary skill in the art would have been familiar with the JEDEC industry standards. Those standards govern many aspects of memory devices and memory modules, and thus they are relevant to understanding the prior art, as I will discuss in the next few slides.

So, slide 12, Judge McShane, gets to your question about horizontal versus vertical. So, slide 12 shows the general layout for a memory module with DRAM memory devices shown as the black boxes all in a row. As shown by the horizontal red arrows at the top, the address, command, and clock signals travel horizontally across the DRAM memory devices. So, they physically go in the horizontal direction. Meanwhile, as shown left by the vertical orange arrows, the data and strobe signals travel vertically to and from the DRAM memory devices. Now, the fact that the data and strobe signals travel vertically while the clock signal travels horizontally is important to keep in mind because those signals need to intersect and align with each other at the right time at each DRAM memory device. Now, it is unlikely that those signals will be properly aligned by pure chance, given the different distances that the vertical and horizontal

signals must travel, which is why it was well known in the art that timing adjustments may be required for a memory module to work properly.

So, let me pause there. Judge McShane, are there follow up questions on the horizontal versus vertical concept?

JUDGE MCSHANE: But vertically, are you suggesting that they're in different layers, if you will, physical layers? I mean, you're saying it's physical, so I'm getting that, but, you know, you have the RAMs, and you have the memory controller, and they're, you know, vertically means, you know, a layer on top of each other, for instance.

MR. CHANDLER: Yeah.

JUDGE MCSHANE: Is that what you're suggesting?

MR. CHANDLER: There is a little bit of aspects of what you're just saying, but really vertically is I was assuming just a two-dimensional, what's shown on here on slide 12, just focused on the two-dimensional aspects. So, you've got to assume a flat printed circuit board. So, don't worry about the Z dimension coming out to you from the page. Just imagine just a flat X by Y. So, that's what I was trying to get at here, is that the data and strobe signals in orange, they're literally going vertically just in the two-dimension space.

JUDGE MCSHANE: Okay. It's just the configuration is what -- your physical configuration, that's what you're referring to in the X, Y. I got that now. You know, you brought up -- the only time I started seeing that terminology was when I was reading your reply, so I was just a little confused there. Thank you.

MR. CHANDLER: All right. It came up also in the preliminary response and, you know, here at UC -- sometime in the -- here the UC

reference refers to the X direction and the Y direction. So, that's -- it also comes up in Hiraishi in that context.

So, moving on to slide 13, slide 13 shows a timing diagram from the JEDEC standard for DDR3 memory devices. DDR3 memory devices were common in the market in 2012, and they are the type of memory devices most relevant to the '608 patent, as well as our primary reference, Hiraishi. As shown by the vertical red line that we have added to this timing diagram, the JEDEC standard teaches that you should align the clock signal CK, the strobe signal DQS, and the data signal DQ.

Slide 14 shows a slight nuance from the JEDEC standard that's not disputed, which is that the alignment is slightly different depending on whether you are reading data or you are writing data. If you're reading data, then the edge of all three signals should be aligned. But if you are writing data, then the center of the data signal should be aligned with the edge of the strobe signal. In both cases, the DQS strobe signal has a preamble that lasts for one clock cycle, as shown to the left of the vertical red lines. And when that DQS strobe signal transitions from low to high, which first happens at the vertical red line, that is when the strobe needs to be aligned with the clock signal and with the data signal.

Slide 15 shows something pretty amazing and something that's a big reason why we're able to hold this hearing remotely, which is that by 2012 the standard clock speed for DDR3 memory devices was about one billionth of a second, also known as a nanosecond. Now, that was the standard speed, not the cutting-edge speed. That was the speed that people of ordinary skill in the art dealt with every day. And at those high speeds, it was known in the art that it was important to keep the strobe signal, the data

signal, and the clock signal properly aligned.

Slide 16 shows an overview of Hiraishi, which is our primary reference for Grounds 1 to 3. The left side shows Figure 1 of Hiraishi with the memory devices in green, data buffers in blue, and a module controller in the center highlighted in red. The right side shows Figure 7 of Hiraishi, which is similar to Figure 1, but it provides a little more detail.

Slide 17 compares Hiraishi on the left to the '608 pattern on the right. As you can see, they're very similar in layout with blue distributed data buffers underneath green memory devices, and a red module controller in the middle. One other thing to notice is that on the bottom right, the '608 patent has a blow up of one of the data buffers in blue. And you can see that there's one orange arrow at the bottom of the data buffer and two orange arrows at the top of the data buffer. That is sometimes referred to by the parties as a “fork in the road” layout. And Hiraishi on the left has the same fork in the road layout through its data buffers. So again, Hiraishi and the '608 patent are very similar to each other.

Slide 19 shows a blow up on the left of part of Hiraishi's memory module. And the bottom right shows a blow up of the data buffer in blue, which we've rotated to match the orientation of the other figures. And on both the left and the bottom right, you can see the fork in the road layout through the data buffer. On the left, you can also see that one fork connects to a longer path labeled L1. And the other fork connects to a shorter path labeled L2. And this difference in length between L1 and L2 is very important to Ground 1 because it takes a longer time for the data and strobe signals to travel on the longer data path L1 than on the shorter path L2. And what Hiraishi teaches is that the data buffer in blue should make timing

adjustments to both the data and the strobe signals to account for the different vertical flight time delays on L1 and L2. And again, Judge McShane, by vertical, I just mean from the bottom of the memory module up to the top where the green memory devices are located.

Slide 20 shows that Hiraishi's data buffer uses a two-step process to delay the DQ data and DQS strobe signals. First, on the left, during initialization, Hiraishi's data buffer performs S4 read and write leveling, which measures the vertical flight time delay on L1 and L2, and then stores the amount of delay needed to account for those different vertical delays. Second, on the right, during normal read and write operations, the data buffer uses the previously stored delays to adjust the timing of both the DQ data signal and the DQS strobe signal. This is shown in detail in Figures 11 and 12 on the right, and it is explained in paragraphs 130 and 135 in the middle. This two-step process is important to understanding Ground 1. So, I'll go through these two steps in more detail in the next few slides.

Slide 21 provides more detail about the first step of the process. Starting on the bottom left, there's a purple line going up to the memory module, and that purple line represents the mode register set command, which is the standard JEDEC command used to start the initialization process for a memory module. The mode register set command is often abbreviated MRS, which looks like Mrs., but it's typically pronounced MRS. The MRS mode register set command goes to the red module controller in the middle of the module. And then as shown on the right side of the slide, the red module controller in response to the purple MRS command uses the brown DRC line to send a module control signal to the blue data buffers to tell the data buffers to perform S4 read and write leveling.

Slide 22 shows that during this first step where S4 read and write leveling is being performed by the data buffers, those data buffers measure and store the vertical flight time delays. On the bottom right is paragraph 151 of Hiraishi, which explains the process. And in the middle is Figure 15, which shows, for example, that the vertical flight time delay on the shorter path L2 is about 0.3 clock cycles. And we've added in the middle red text that says 0.3 CLK. And to the left of that, you can see in black, it says flight time, and that measurement is about 0.3 clock cycles from about T5 to about T5.3.

JUDGE MCSHANE: Ms. Chandler, I hate to interrupt, but, you know, what we're looking at, as I kind of suggested earlier, is we're looking at the claim, and in particular, we're looking at the, you know, whether the prior art teaches the claims, right? And so, you know, we appreciate all this background, but, you know, and you can use your time as you wish, but we frankly would find it a little bit more helpful if we started to focus on the issues in the case directly.

MR. CHANDLER: Thank you, Your Honor. So, the general point is, in the second step, as shown in slide 24, Hiraishi's FIFO data, FIFO 302 in the data buffer provides a variable amount of delay, and that satisfies the delay circuit on the data path, even under Netlist's narrow claim construction that only focuses on the DQ data signal line. So, just the FIFO alone is sufficient under Netlist's claim construction to satisfy the claim requirement of delaying a signal through the data path, even if you limit the construction of data path to the -- only the DQ data signal line, even if you ignore the DQS strobe line for purposes of the claim term of data paths.

And Netlist has suggested that somehow in our reply brief that

we're not permitted to respond to that. And the Federal Circuit has rejected to that in the *Axonics v. Medtronic* case, 75 F.4th 1374 at page 1384 where the Federal Circuit held, "We hold that where a Patent Owner in an IPR first proposes a claim construction in a Patent Owner response, a Petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction, at least where it relies on the same embodiments for each included ground as were relied on in the petition."

And that's the situation we have here where we are relying on the same embodiment of Hiraishi, Figure 5, and we're relying on S4 read and write leveling both in the petition and the reply. And so, our primary argument for today is that the Board does not need to resolve the claim construction dispute about whether the data path is limited to just the DQ data signal as proposed by Netlist, or whether it includes both the DQ data signal and the DQS strobe signal, as we suggested in the petition, because either way, the FIFO in blue, as shown on slide 24 and on slide 25, delays the data signal through the data path. And something important to notice here on slide 25 is that Hiraishi's FIFO does not simply delay the data by one clock cycle and does not simply output the data at time T6. Netlist argued that Hiraishi's data buffer doesn't measure the delay and simply waits until T6 to output the data. But that's completely wrong, as shown, for example, by this slide 25. Sometimes Hiraishi's data buffer may output the data at T4.05. Sometimes it may output at T4.45. It does not always output at T6. Again, Hiraishi has this two-step process where first Hiraishi measures and stores the necessary delays as part of S4 read and write leveling. And then the second step is shown, for example, here on slide 25, which is during a

normal read or write operation. Hiraishi's FIFO in blue applies the appropriate amount of delay to the data signal depending on whether that data is going to be traveling on L1 or L2, which have different vertical flight time delays.

JUDGE MCSHANE: Mr. Chandler, you know, here's the deal. So, looking -- all right, if we can go back to that slide you were just on, please.

MR. CHANDLER: Yeah.

JUDGE MCSHANE: Yeah. So, you know, we see this slide up above, right? And it's got all the yellow, you know, the signals and the strobe signals and so on and so forth, and the trail signals, what have you. But, you know, it is fair to say that your position from the time of the petition to what you're proposing now is a significant change. Isn't that a fair statement?

MR. CHANDLER: No, Your Honor.

JUDGE MCSHANE: And please go back to that slide, please.

MR. CHANDLER: Sure. I mean, I was trying to address the question, but yeah, go ahead.

JUDGE MCSHANE: Okay. Yeah. No, no, but let's stay on this one. That's just the question right now. So, you know, isn't that a fair statement?

MR. CHANDLER: No, we would not consider it a significant change because it's the exact same embodiment of Hiraishi. And I mean, a number of responses. I mean, it's the same embodiment. So, we don't think it's a significant change.

The second is shown in slide 31. We weren't the ones that

changed. It was Netlist that changed. So, before we filed the petition, Netlist sued us. And slide 31 shows what Netlist put in its complaint. And Netlist specifically identified in its complaint against us what it alleged to be the delay circuit in the data path. And as shown by the yellow highlighting, Netlist specifically identified the DQS strobe signal as being in the delay circuit in the data path. So, when we filed the petition, we looked at what they had identified. And that is what we mapped the claims to be consistent with how they had mapped the claims when they sued us. And the mapping that we use, which is that the data path includes both the strobe signal and the data signal through the data path, is consistent with the Board's final written decision in IPR2022-00236, where the Board also mapped the data path to include both the strobe signal and the data signal.

We don't think it's a significant change because it's the same embodiment. And the FIFO was identified in the petition, as shown, for example, on slide 33, we specifically identified the FIFO in the petition as the delay circuit for read operations, as shown on slide 33 in the upper left. That's petition page 51. And then on slide 34, the petition at page 47 identified the right FIFO as the delay circuit for write operations. So, we don't -- I would push back on the idea that it's a significant change, but my primary pitch is that the Board does not need to resolve the claim construction, because even under Netlist's narrow claim construction, the FIFO still satisfies Netlist's definition of a delay circuit in the data path.

JUDGE MCSHANE: Yeah. Mr. Chandler, can you go back to slide 31?

MR. CHANDLER: Yes.

JUDGE MCSHANE: So, I see this argument about what the

Patent Owner is arguing. I see it in the, I think it's your opposition to Patent Owner's argument, or rather Patent Owner's motion to file supplemental information. That's the first time I think I've seen that figure. If you have cited it elsewhere, let me know.

MR. CHANDLER: Yes, Your Honor. As shown on slide 31, this figure was cited in our reply brief, Figure 23 on page 16. And as we specifically quoted on page 16, this figure was a, quote, example of a -- I'll get the quote here -- example of a delay circuit. So, right?

JUDGE MCSHANE: Yeah, but you didn't really present the argument there. You didn't present this argument there. You were arguing something else in that -- in the reply, I think.

MR. CHANDLER: Well, we were trying to be -- we were arguing about claim construction, and we were showing that Netlist's own claim construction in the beginning was consistent with the claim construction presented in the petition. So, but the point is that Netlist is the one that has shifted claim construction, not us. We were consistent with Netlist's claim construction, and in the reply brief shows that even under Netlist's new claim construction, the claim is still obvious. And again, the Federal Circuit's decision in *Axonics* allows us to respond to their new claim construction to show why the FIFO satisfies even Netlist's new claim construction. And the Federal Circuit said that that's both proper and also it's necessary for that argument to be considered.

JUDGE MCSHANE: Well, yeah. Well, let's go back. Let's not call it claim construction just for the sake of argument. We're going to call it claim interpretation because it's really what we're -- what I think is going on anyway is that we're looking at the claims and interpreting the claims. So, if

we could go to that, go looking at the claim language, and if you could go to that issue it would be appreciated.

MR. CHANDLER: Okay. So, again, our primary argument is claim construction is not required, but if we were to construe the claims, our slides, starting at slide 54, talk about claim construction and explain why the proper construction for data paths includes both the data and the strobe signals. And the Board in the institution decision, as shown on slide 55, preliminary agreed with our proposed interpretation and adopted that the data path would include both the strobe and the data signals. Slide 56 is very important because the Board resolved this issue against Netlist, and actually I should probably back up. The same slide is shown on 46. So, slide 46 is important because in IPR2022-236, the Board specifically resolved this issue against Netlist about whether Hiraishi delays data and strobe signals on the data path and agreed that Hiraishi does delay both the data and the strobe signals on the data path, and as shown on the bottom left, the Board specifically agreed that the data path in question was from L0 to L1 and L2, which is the same data path that our petition pointed to is L0 to L1 and L2 and that's what creates the fork in the road. And as shown on slide 48 in the *Mobile Tech* case, the Board held that collateral estoppel applies in the context of a non-appeal case. That's what we have here. IPR2022-236 was not appealed, and the claims are canceled as shown on the bottom left in Exhibit 1088. And then the next quote from *Mobile Tech* is very important, which is, "That a party may be bound not simply by the ultimate conclusion, e.g., unpatentability of a claim, but by any subsidiary factual determinations that were actually litigated and essential to judgment." And so that's what we have here in IPR2022-00236. This

question of does Hiraishi delay strobe and data signals on the data path was actually litigated and that was resolved against Netlist, as shown for example, on slide 46. And so, that's relevant both as a legal matter as to, you know, what does the term data path mean? And it's also relevant as a factual matter, which is does Hiraishi's S4 read and write leveling delay strobe signals and data signals on the data path from L0 to L1 and L2. And the Board found that, yes, Hiraishi does control the timing of the data and the strobe signals on the data path. And so, from our perspective, that's dispositive regardless of whether you construe data paths to be broad enough to cover both the strobe and data signals, or whether we just focused on the data signal alone. Either way, the Board has already resolved this issue against Netlist and held that Hiraishi does delay the data signal.

There is an addition --

JUDGE MCSHANE: Yeah, Mr. Chandler, on that issue, I know I'm sure Patent Owner is going to address this. But the claim, the independent claim at issue here, I think, the language is different. And if you want to address that issue, go ahead.

MR. CHANDLER: But again, that's exactly what the point is on 48, on slide 48, which is even if the claim language is different, that does not remove collateral estoppel because collateral estoppel also applies to any subsidiary factual determinations that were actually litigated and essential to the judgment. Now, we believe that the claim is materially identical, as shown on slide 49. During prosecution, the examiner agreed that the claims are not patently distinct, distinct as between the '608 patent and the '035 patent. And the distinctions that Netlist has raised don't change any of the analysis. So, for example, slide 50 compares the '035 claim language in the

middle, and the '608 claim language on the right, and it's a little easier. I see on slide 51, '035 says control the timing, whereas '608 says control of the data path to delay a signal through the data path. It's not a materially different claim language because either way, the Board has already determined, as shown on the left side, that Hiraishi delays the data and strobe signals, the DQ data and the DQS strobe signals, going through the data path. So, the yellow and blue highlighting is correlating how the different claim language in '035 matches up to '608. So, you know, it's sort of in a different order, where 1J in '035 corresponds to the end of 1F in '608, and 1E in the beginning of 1F in '608 corresponds to the end of 1J in '035.

But as a practical matter, the claim language is not materially different, as shown, again, during prosecution. And also, in slide 48 on the bottom right, the test is that the claim language doesn't need to be identical. Instead, the test is that collateral estoppel can apply so long as the differences between the unadjudicated patent claim and the adjudicated claim do not materially alter the question of invalidity. So, you know, what -- is there something materially different in the '035 or '608 claim language that materially alters the question of invalidity, and our answer is no, because Hiraishi, as for read and write leveling, is the exact same thing that we're pointing to in both, the exact same thing that the Board previously relied on, the same thing that we're pointing to here, and it matches up both with what the '035 claim language was talking about, as well as what the '608 claim language is talking about.

JUDGE MCSHANE: Mr. Chandler, and I apologize because I seem to keep dragging you back and forth between your slides, but we're going back to slide 49. Okay? And this is the -- this is the argument you are

making here related to the prosecution history. I didn't see -- I saw a reference to this, you know, a general statement here about the -- it was an -- I guess it was an obviousness of patenting rejection and the claims weren't patentably distinct over each other. But this is the first time I kind of am hearing a more fleshed out argument that this is directly relevant to how we should interpret the claim in our case and for this patent. And so, I don't recall seeing that in your papers and any place else. Maybe I'm wrong. So, if you just point me to where you do that.

MR. CHANDLER: Well, again, this is in the reply brief. The final written decision didn't exist at the time of the petition. So, it's not in the petition, obviously. But in the reply brief, our first argument was that the claim of the '035 patent on the left here on page 1 of the reply brief, is not materially different from claim 1 of the '608 patent. And then, you know, we go through and we talk about how this petition has pointed to the same thing that the Board was talking about in IPR2022-00236. And then we go on the cite the *Google* case and the *Mobile Tech* case as to why there should be preclusion. And then we -- this isn't the only point we talk about. I mean we talked about repeatedly as we go through the decision -- or through the reply brief. So, you know, it's Exhibit 1066 is the previous decision. So, you can see all the places that we keep pointing to Exhibit 1066 about how issues had already been decided for example, on page 13, page 17 in the reply, page 32 of the reply, page 33 of the reply twice, page 34 of the reply twice, page 38. So, it was something we talked about a lot in the reply about how the issues that were raised and decided in IPR2022-00236 resolve the issues that Netlist is trying to relitigate in this case.

JUDGE MCSHANE: Yeah, yeah, I was kind of referring to the

implications of the prosecution history, that and that alone. So, in any event, you know, please proceed.

MR. CHANDLER: All right. I'll touch, again, on claim construction. We really don't think the Board needs to resolve it because the FIFO alone is sufficient. And I'll talk about it briefly since it seems like you're interested in it. Slide 59 shows that again Netlist admitted in its original complaint that the strobe signals were part of the data path, which is the red box. And this red box was Netlist's red box. And furthermore, Netlist admitted that those strobe signals are corresponding to each data signal line. And that's the claim language of Claim 1.

So, let me go to slide 64. So, slide 64 shows the language of Claim 1 on the left, and then it shows Figure 2C in the middle, and it has some quotes from the specification in the middle. And it shows Figure 1 on the right. And it's interesting because Netlist has basically backed away from its Patent Owner response argument, which was in the Patent Owner response, Netlist is trying to say that the claim term data path by itself excludes the strobe signal. In the sur-reply Netlist realizes that's not going to work because in the '035 patent, Claim 1 makes clear a data path to have a strobe signal. Dependent Claim 10 makes clear that the data path can have a strobe signal. And Netlist's expert admitted the data path can have a strobe signal. Also, both Hiraishi and Butt, those are both now intrinsic evidence, because they're both part of prosecution in the family of patents as a result of the previous final written decisions against Netlist. Both Hiraishi and Butt use the term data path to include both strobe and data signal.

So, Netlist has basically abandoned the idea that the word data path by itself excludes the strobe signal. And now, Netlist's new argument, in

their sur-reply, is that it's really the word corresponding. So, if you look at the claim language in the bottom left here, it says a data path, and then it says corresponding to each data signal line in the respective set of data strobe signal lines. So, now Netlist is arguing, all right, well, it's not data path. We can't say that the word data path is what excludes the strobe signal. So now, Netlist is saying, all right, it's really this other language, corresponding to each data signal line. What Netlist is trying to do is say that when the claim says corresponding to each data signal line, that there must be a one-to-one correspondence between each data signal line and each data path, making the data path just an extension of the data signal line. That is Netlist's new argument. But Claim 1 does not require a one-to-one correspondence between each data path and each data signal line. And Figure 2C expressly teaches that there's not a one-to-one correspondence. Figure 2C shows there's a fork in the road through the data path -- or through the data buffer, which means that there are multiple lines going through the data buffer that correspond to each data signal line coming into the bottom of the data buffer. And that's entirely consistent with our position that you can have multiple lines, such as a DQ strobe signal and a DQ data signal that are in the data path through the data buffer. And that both of those signals will correspond to each data signal line coming in at the bottom of the data buffer.

There's nothing in the patent or the claims that requires a one-to-one correspondence, as suggested by Netlist, to contrast both Claim 1 in the specification of the '608 patent is consistent with multiple signals in the data path corresponding with each data signal line. And we know as a technical matter that the DQS strobe signal must travel with the DQ data signal and

thus correspond with that DQ data signal, which is entirely consistent with the language in Claim 1 of the '608 patent requiring that the signals in the data path correspond to each data signal line that comes into the bottom of the data buffer. And this idea of the strobe signal and the data signal corresponding to each other is shown, for example, on slide 60 where Netlist admitted -- and this is an annotation that Netlist provided where Netlist admitted that the DQS strobe signal must travel with the DQ data signal to ensure accurate data transmission. This is taught by Hiraishi, the figure that's shown here on the screen with Netlist's annotations, is Hiraishi's figure which again shows the strobe signal, and the data signal aligned with each other. It's taught by JEDEC. When I started the presentation today, I showed how JEDEC requires that the strobe and the data signal are aligned with each other. It's also admitted by Netlist's expert on slide 61 where he admitted that JEDEC requires the DQS strobe signal to travel with the DQ data signal within a very tight tolerance.

So, as a technical matter when we get back to slide 64, we know that every time that there's a data signal going through the data buffer there is a corresponding strobe signal that travels with it in a very tight alignment. And so, as a matter of claim construction, it makes sense to say that the strobe signal, in addition to the data signal going through the data buffer, corresponds to each data signal line that's coming up into the bottom of the data buffer.

JUDGE MCSHANE: Yeah, Mr. Chandler, on this, and I'll just try to, as best I can, I'm sure a Patent Owner's counsel will correct me if they find an error with what I say. But I think their position, I think what Patent Owner is trying to say, is that the data path is a data path, okay. It can carry

all different kinds of data, you know, it's just a general term. But let me suggest that we're not talking about claim construction here, we're not talking about claim construction of the term data path, *per se*. What we're doing is we're interpreting the claim to figure out what signals are being claimed to be sent on the data path, okay? So, that's what we're -- I think that's what we're doing, and that's what I think Patent Owner's position is. And Patent Owner points us to some embodiments in the patent that show that there is a disclosure of only data signals being sent on a data path. So, what do you say to that?

MR. CHANDLER: I disagree that those are embodiments where the patent has limited that embodiment to a, quote, data path. And the patent is quite emphatic about this issue where the patent says at column 10, line 25, "It should be strongly noted that the following information is set for illustrative purposes and should not be construed as limiting in any manner." And then it goes right into Figure 3, which is one of the figures that Patent Owner is pointing to. So, those figures are not limiting as to what is a data path. The discussion of Figure 3 never says that the data path is only the data signal line. And with respect to Figures 15 and 16 as shown on slide 68, the term I can -- it's is also shown on slide 67. So, there's the term first right strobe path, first right data path, second right strobe path, second right data path, etcetera. Those terms reinforce our position that all of those signals correspond to each other. They're all going through the data buffer together, and as shown on slide 68, as a legal matter, the Federal Circuit has told us on the bottom left in the *Weber* case, 492 F.4th at the 1070, "We've repeatedly warned against confining the claims to the specific embodiments." So, we think it'd be erroneous to limit the, quote, data path

to just Figure 16 which is at shown at the top, while ignoring the corresponding signal that travels along with the data signal, which is the strobe signal, and that together the strobe signal and the data signal are broad enough to fit within the broader definition of the claim data path.

I do want to get back through to the point which is my primary point which is that the Board doesn't need to resolve the construction, or as you put it, the claim interpretation, because regardless of how you try to say what is the data path, Hiraishi's embodiment, the same embodiment that we rely on in the petition as shown, for example, on slide 32, it matches up precisely with the preferred embodiment that Netlist is pointing to -- to try to interpret the data path which is Figure 16. So, on slide 32 I've got Hiraishi's Figure 5 on the left with the FIFO highlighted in blue, and that FIFO directly corresponds to what Netlist is claiming is the delay circuit through the data path which is again highlighted in blue on the right side of Figure 32. And so, I agree that the, you know, you don't have to call it claim construction, you can call it claim interpretation. But either way the Board doesn't need to resolve whether the proper claim construction or the proper claim interpretation is that the data path is broad enough to include both the strobe signal and the data signal, or whether it's narrower, as Netlist is trying to suggest with these dashed red lines that we've added on slide 32 where Netlist is suggesting that the data path is just the data signal because Hiraishi matches up precisely with Figure 16 of the '608 patent, and Hiraishi's teaching that you delay both the strobe signal and the data signal. And we know that you got to delay both of them because the only thing -- the only way anything works is if the strobe signal and the delay signal travel together. If you delay one of those signals you're going to have to delay the

other signal so that everything works properly. So, I mean it's honestly kind of red herring to say, well, you know, are you delaying the strobe signal or just the data signal, you're always going to be delaying both of them because they need to stay in alignment for anything to work properly.

Slide 33 and 34 is what I talked about earlier that the petition pointed to the FIFO, so there's no change in the in the embodiment that we're pointing to. And I want to talk about slide 35 because again it was --

JUDGE MCSHANE: Mr. Chandler, just a real quick one. You're pretty much, the time that you allocated for your opening, it's pretty much timed out here and you're getting into your rebuttal time. So, sorry, I didn't give you a warning, but (CROSSTALK) --

MR. CHANDLER: (CROSSTALK) Yeah, I'll say a few more words and then I'll wrap up for now.

Slide 35 compares Hiraishi's Figure 5 on the left to Figure 16 and 15 of the '608 patent in the middle, and all of the green boxes. The point of the green boxes is to show that when Netlist tries to say that, and it's, you know, for the first time in its Patent Owner response that the data path is limited to just the solid orange data signals. What that does that excludes all of these components highlighted in green that affects the component in blue, such as the signals that are used to time that component in blue. But that's true for both Hiraishi on the left and the '608 patent on the right. So, it doesn't change the analysis. It's still an apples-to-apples comparison, whether you construe the data path very narrowly to just include the blue circuitry, which in Hiraishi is the FIFO, or whether you zoom out and say, no, really the data path and the delay circuit are all the components that have some impact on the timing of the signaling, which would include all of these

green components. Either way, depending, you know, whether you zoom out or you zoom in, Hiraishi matches up and is doing the same thing as the '608 patent. And what it's doing is this delaying both the strobe signal and the data signal.

I guess I will save the rest of my time for rebuttal.

JUDGE MCSHANE: Okay. Thank you, Mr. Chandler. You have about 13 minutes left for rebuttal. Mr. Bemben, are you ready to proceed?

MR. BEMBEN: I am. Thank you, Your Honor. I'm going to share my slides.

JUDGE MCSHANE: And how much time do you wish to reserve for surrebuttal?

MR. BEMBEN: I would like to say -- to reserve 15 minutes as well.

JUDGE MCSHANE: Thank you.

MR. BEMBEN: Now, can you see my slides and can you hear me well?

JUDGE MCSHANE: Yes, to both.

MR. BEMBEN: Okay. Thank you, Your Honors. And again, Richard Bemben on behalf of the Patent Owner, Netlist. Samsung has failed to demonstrate that Claims 1 through 5 are unpatentable. And I'm going to jump right to Judge McShane, your questions about claim construction, because I disagree with Mr. Chandler that they are not dispositive. They are dispositive to Samsung's original positions with respect to Ground 1. And then they're also dispositive with respect to Ground 2, in which Samsung has proposed moving a delay circuit from the Tokuhiro reference into Figure 5 of Hiraishi at a location that is not on the data path corresponding to a data

signal line. And so, I'm going to go right to Claim 10, which is the claim language. The one thing I want to point out about Mr. Chandler's presentation is when you asked him about the claims, he went to the extrinsic evidence, the complaint, what the Board said in the '035 final written decision. There the claims were very different and they're different in a material way. What I want to focus on with respect to Claim 10 is the claim language and -- I'm sorry, slide 10, Claim 1 on the left hand side. And it shows the claim language and the operative language is that the data path corresponds to each data signal line in the respective set of data strobe signal lines. Netlist's construction or interpretation of this entire phrase, not just the term data path, is that Claim 1's data paths do not include strobe signal lines. Samsung had taken the opposite construction, as you heard today from Mr. Chandler, that includes both data signal lines and strobe signal lines. And as you pointed out, Your Honor, that is inconsistent with the plain language of the claim. We're not just asking you to analyze or to construe data path in isolation. That would be incorrect. That's not how we do claim construction according to the Federal Circuit. But what we do is we look at the way that that term is used in the context of the claims, including the surrounding claim language. And here it is clear that that data path, the Court specifically says corresponding to each data signal line in the respective set of data strobe signal lines. That's the claim language itself. And then if we look at the specification, that's also supported in the specification.

I'm going to move to slide 11, which shows on the left hand side, the operative language from the text of the patent. And on the right hand side, Figure 3. And what we see is that there are -- are these data signal

lines, DQ signal lines 322, shown in blue, and those correspond to the data signal lines that go into the circuits 320, which are DQ routing circuits or data routing circuits. By contrast, we have the strobe signal line, which is shown DQS, that feeds into the ID control circuit, which is on the bottom of Figure 3. So, there's data lines -- or I'm sorry, data signal lines that have data paths. And there are different strobe lines that have strobe paths. And that's also consistent with -- I'm going to move to slide 12. It's consistent with Samsung's District Court expert, some of his recent testimony. This was the subject of the recent motion for supplemental information. And this is extrinsic evidence, but it is consistent with the intrinsic record.

JUDGE MCSHANE: Yeah. Let me just interrupt on that one, if you don't mind, Mr. Bemben. On that one, we have a pending motion from you to file the supplemental, this stuff as supplemental evidence. And that motion is still pending. So, I just want to note that for the record. And also, here's a question though. What do you say about Petitioner's contention that in the District Court, what you're contending is that the data path includes both the strobe signal and the data signal?

MR. BEMBEN: So, yes, Your Honor. So, a few points on that. The first is that the District Court complaint is extrinsic evidence. It's not intrinsic evidence to the record. The intrinsic evidence trumps the extrinsic record. And what the intrinsic record is, is the claims in the specification. Those all support our construction. The second point I want to make is that it's a complaint. The purpose of the complaint is to provide notice. It's not a claim construction brief. It's not a Markman here. It's not a Markman order. It's none of those things. It's preliminary, and it doesn't dictate claim construction positions. If you go and look at what they've cited to, and even

on their slides, there's no express claim construction positions taken there. It's -- a complaint is to provide notice. And I believe other Board panels, at least in institution decisions, have recognized that a complaint is preliminary. It's not sufficient for making claim constructions. When you have to make a claim construction, you look at what the patent says and what the specifications of the claims say, what the specification says, and what the prosecution history says first. And here, the intrinsic record is clear that it's consistent with our construction. And so --

JUDGE MCSHANE: Well, nevertheless, Mr. Bemben, not to be argumentative, but it is -- you're representing the Patent Owner. It is their patent. So, presumably they have an understanding of the claims and what they mean, and what the, well, what's called the interpretation of the claim should be. Am I correct?

MR. BEMBEN: So, that is correct, I would say. But again, it's -- the purpose of a complaint is to provide notice. It's not a claim construction position or a claim construction briefing. And so, to the extent that it is different or inconsistent with what the specification, with claims say, the specification in the claims trump. And that's how we get to interpret the claim in this proceeding. That's how the claim should be interpreted based on what the claim says.

JUDGE MCSHANE: Right. So --

JUDGE SZPONDOWSKI: So, Counsel, but it is the -- is the position that was taken in the complaint different from the position that's being taken here?

MR. BEMBEN: I will get back to you on that. Let me put a pin in that and get back to you on surrebuttal if you don't mind. I'd like to take a

look and consult with my co-counsel here. But I believe, I think I can answer your question just that if there is any inconsistency, it was -- it was a preliminary position. And it was before any Markman hearing, it was before any Markman briefing was filed in that case. And that is the type of thing that we would need to look to with respect to Patent Owners' positions on what they thought certain claim terms meant. We don't have that here, but what we do have in our case is the claim language itself, as well as the specification and prosecution history, all of which supports our position.

And so, getting to that point, if we look at slide 13, this is additional support in the specification for Netlist's claim construction position. And so, on the left hand side, we have some language from the patent itself. And the point of this slide is that Figure 16 in the patent, it shows the DQ routing circuit. That's the data routing circuit that is fed by the data signal lines. And what the patent describes the circuit and describes the data signal lines, it describes data paths. By contrast, if we go to slide 14, slide 14 shows Figure 15 of the patent and some of the operative language from the specification. And here, this is showing the strobe path. And the strobe path, again, if we look at the small Figure 3 in the top righthand corner of the slide, that is in the ID control circuit. And that's for the strobe signal line. And when the specification refers to the strobe signal line, it refers to strobe path, which is, again, in contrast to Figure 16, when it's referring to data signal lines, it refers to data paths. So again, it’s additional support for our position that the data paths that are recited in Claim 1 correspond to the data signal lines expressly said in the claim, and not the strobe signals.

Now, Mr. Chandler talked about -- I'm turning to slide 16, about

collateral estoppel, and I just want to briefly touch on some of the differences between Claim 1 of the '608 patent, which is shown on the left hand side of figures -- claim -- I'm sorry, slide 16, and '035 patent, Claim 1 on the righthand side. And so, the language is materially different. The first thing is that in the '608 patent, Claim 1, the data path specifically in the claim, it says that it's corresponding to each data signal line in the respective set of data strobe signal lines. By contrast, the '035, Claim 1, it recites that the data paths are for transmitting respective data in strobe signals. That's different. That's expressly saying that the data paths there are for data in strobe. By contrast, Claim 1 of the '608 does not have that language, has different language, narrower language in some respects that the data path just corresponds to the data signal lines. Now, that's one material distinction. Another material distinction is when we get to the data path itself, and that's shown at the bottom of the claim highlighted in yellow. The data path must include a tristate buffer that's controlled by the expand processing circuit and a delay circuit that is configured to delay the signal through the data path and so on. So, a tristate buffer and a delay circuit in the data path. None of those limitations show up in the '035 patent Claim 1. By contrast, you see it's broader in a lot of respects. It says to control timing of the respective data and strobe signals on the data path. And so, those are material distinctions or material differences between the claim language, and those material differences also led to different ways that Samsung has tried to apply the prior art to the claims and then try to interpret prior art differently. So, what this shows is that the claims are materially different, and it actually supports our position that when Netlist wanted to recite a data path that transmitted both data and strobe signals or data paths that

transmitted both, it said it. And you see that in Claim 1 of the '035 patent. By contrast, Netlist also knew how to claim a data path that just corresponded to the data signal lines, and that's shown in the '608 patent, the patent that we're here to talk about today.

And so finally, I just want to point out that if you agree with Samsung's construction, what they're essentially doing is they're completely reading out each data signal line. And you see that here. They're rendering that language superfluous, which we know is incorrect, because you could read it, and you see on the bottom this is the way that they originally interpreted the data path with respect to Hiraishi. You could read that as just the data path corresponds to their respective set of data strobe signal lines. That's how they were interpreting it. They weren't interpreting it to include the language each data signal line -- or I'm sorry, corresponding to each data signal line. And so, they're rendering that language superfluous and that it, our contention is that that is incorrect from a claim construction position. It's also just inconsistent with the claim language of the claims and the specification.

So, unless there are any questions about claim construction, I just want to kind of take a step back and just kind of explain and try to frame our --

JUDGE MCSHANE: Yes, Mr. Bemben, I do have a quick question. There was a -- Petitioner had in its slide deck this argument about the prosecution history. Do you have any response to that? Is that --

MR. BEMBEN: Absolutely. So --

JUDGE MCSHANE: -- is that dispositive as to how we should interpret the claims, and why or why not?

MR. BEMBEN: It is not dispositive, Your Honors. And the first thing is I completely agree with you that this was not an argument that they developed in the papers at all. When you ask Mr. Chandler to show you he went through and pointed you to the '035 final written decision. Not where they argued that there was a terminal disclaimer and that that means we should be collaterally estopped. The second thing is -- is that terminal disclaimers they are prosecution conveniences and prosecution to get over – to -- to get over obviousness this type double patent rejections. They are not admissions that the patents -- the patent claims are not at least distinct for the purpose of collateral estoppel. When we look at collateral estoppel we need to look at, I'm going to go to slide 6 real quick. These are the factors for collateral estoppel, and the first one that Samsung needs to prove is that the issues are identical. And one of those things -- identity of issues includes material differences between the claims. And they simply haven't shown that, and a terminal disclaimer is not dispositive with respect to that. There's no admission with the terminal disclaimer that the claims are not patently distinct.

JUDGE MCSHANE: Thank you.

MR. BEMBEN: So, just like I said, I wanted to just take a step back and just kind of level set on this case. And it's our position, of course, that Samsung has failed to demonstrate the Claims 1 through 5 are unpatentable. We believe that Samsung has made two fundamental errors and misunderstood the claim which we just talked about. But they also misunderstood key teachings in the Hiraishi reference. When we pointed out these errors Samsung has taken a two-prong approach. The first thing that they did is they presented new theories and they distanced themselves

from their own expert. Samsung's reply, we believe and I believe it's consistent with some of the questions you asked, Your Honor, it has significantly changed their invalidity theory and it's presented new interpretations of Hiraishi. They've essentially attempted to rewrite the Hiraishi reference to meet their new theories. That's improper. But very importantly for this case, Your Honor, is that Samsung did not provide a reply declaration from their expert to support their new theories. And so, what we have now is Samsung's positions are based on unsupported attorney arguments, not on evidence.

The second way that Samsung responded when we pointed out the errors was to take a scorched earth approach to try to prevent the panel from considering arguments and evidence that proves that Samsung's positions are wrong. You saw that today in Mr. Chandler's opening. They're trying to evoke collateral estoppel to avoid our arguments, even though the claims and the issues were very different with respect to the '035 final written decision. They're trying to exclude Dr. Wedig's testimony from a related IPR in which he explained his understanding of Hiraishi in a way that's consistent with Netlist's positions. Also, tried to prevent the panel from considering testimony from their District Court expert, which we just talked about. And in fact, when they file their opposition that we mentioned, that totals 266 pages and includes a new declaration and attachments A through L, none of which was authorized by the panel. If you -- excuse me. Can I just, one second, Your Honor, there's some background noise that we're getting. I just want to make sure that you guys can hear.

JUDGE JURGOVAN: Hold on, okay.

JUDGE MCSHANE: Okay.

MR. BEMBEN: My sincere apologies, Your Honor. Your Honor, you were about to ask a question, I believe.

JUDGE SZPONDOWSKI: Yeah, so my question is that, you know, Petitioner is allowed to respond to arguments that are made in the Patent Owner's response. And isn't that all that they're doing here? Like, if the Patent Owner came up with a claim interpretation, a data path that perhaps Petitioner didn't anticipate, so they say, okay, well, you know, under that construction, here's our position, we're using the same embodiment of the reference that we relied on in the Petition. And so, I mean, what's your response to that? I mean, aren't they allowed to respond to your arguments?

MR. BEMBEN: So, Your Honor, they are allowed to respond to our arguments, of course, that's what the reply is for. However, Mr. Chandler talked about the *Axonics* case. I'm familiar with that case as well. There, that case is distinguishable for a few reasons. Here, it's not the situation where we have taken the claim construction position that they couldn't have -- that they couldn't have anticipated. In fact, Judge McShane, you have kind of described it as claim interpretation as opposed to claim construction because really we're just looking at the claim language of the claims, what the claims say. And so, for that reason alone, we think that this is distinguishable from *Axonics*. They should have seen the plain language of the claims to understood what they meant. But even I think another point (CROSSTALK) --

JUDGE SZPONDOWSKI: (CROSSTALK) Petitioner relies on your complaint though, and I think their position is that, hey, in the complaint this interpretation, construction, or interpretation, or -- or whatever of data paths. So, this is what we're relying on here in the

complaint. So, and I look forward to your answer about whether or not that position is or isn't consistent with the position here, but they certainly seem to think that it is.

MR. BEMBEN: So, and that's exactly what Mr. Chandler said. He said when you asked him, he said that the claim construction, or the -- the positions in the petition, the mapping was based on what was said in the complaint. And what I have to say about that that's an incorrect way to do and analyze claims. You have to look at what the specification, what the claims say and what the specification says. That's the correct way to approach a petition in claim construction, not just look at a complaint. And again, for the reasons that I provided, even if it is inconsistent, it's the complaint, the purpose of the complaint is just to provide notice. It's not a claim construction position.

JUDGE JURGOVAN: Counsel, I'd like to ask a question.

MR. BEMBEN: Yes, Your Honor.

JUDGE JURGOVAN: That is, it sounds like, let's assume you're correct about this claim construction argument. It sounds like Petitioner has a fallback that is reading the delay circuit on Hiraishi's FIFO. Is the FIFO a delay circuit?

MR. BEMBEN: So, the FIFO is not the delay circuit that's recited in Claim 1. No, it's not. It doesn't --

JUDGE JURGOVAN: Why not?

MR. BEMBEN: Sure. Let me just get right to that, Your Honor. Okay, so I think I'm just going to start by turning to our slide 26 and just walking you through this figure on the righthand side. And so, with the figure on the righthand side, this is the figure directly from Samsung's reply,

page 14, okay? In the reply, they juxtaposed Figure 5 of Hiraishi, and Figure 16 of our patent below to try to show the similarities between the data paths. Now, what it actually shows is the differences, okay? Because what we have in Hiraishi on the top, and this is in the redirection, so on the righthand side would be the memory itself. The buffer of Hiraishi is in the middle. On the lefthand side is the memory controller that's off-chip. And so, going from right to left, we have signals coming in, data signals coming in, going to a selector, which is like a multiplexer. It's flexed between lines, L1 or L2, and it goes to the FIFO. The FIFO receives a strobe signal to let it know, sample the data now, and it's clocked out by the local clock signal, goes to a buffer, and then to the output pin. By contrast, if you look at ours, there are some similarities. For example, coming from right to left, there's a multiplexer that decides between lines YA and YB. But there's a key difference, and that key difference is that we have a delay circuit in the delay path. That's 1660. You see that being fed by a clock and by a delay signal that is computed. There's an amount of delay that's computed, and it's fed to that delay circuit to tell the delay circuit how much to delay the data signal. And then it goes to a sampler that's clocked by the, or that's, I'm sorry, that receives a strobe signal for sampling to the buffer and then out to the pin. And so, that FIFO in Hiraishi is not described as the delay circuit of Claim 1 in any way. There's no express disclosure of that. And because there's no express disclosure, what Samsung needs is they need evidence demonstrating that a person of skill in the art would have understood Hiraishi's FIFOs to satisfy that claim element. They don't have that. Again, they failed to do it because they didn't provide a reply declaration from their expert. Dr. Wedig's positions in his original declaration, they're inconsistent

with this new theory. He did provide some testimony about the FIFO in his original declaration. And what he said is that it offers data and that it outputs based on the local clock. That is how Hiraishi describes it, and that's what it does. It doesn't satisfy the delay circuit of Claim 1.

JUDGE JURGOVAN: All right. Okay. But I mean, you know, as the data is being clocked through the FIFO buffer, is it not being delayed in a sense?

MR. BEMBEN: No, that's not what Hiraishi teaches at all. Hiraishi teaches that it's buffered and that it moves through based on the local clock signal. There's nothing like a delay circuit in the delay path receiving a delay signal that tells it how much an amount to delay, which is recited in our claims. It's not. They haven't proven that point, and that's not how Hiraishi describes the FIFO. And so, --

JUDGE JURGOVAN: I mean, if it's called FIFO, right, that's first in, first out, right? So, it's receiving data serially and it's clocking it in and clocking it out of the buffer.

MR. BEMBEN: That's right.

JUDGE JURGOVAN: So, wouldn't any data going through that buffer necessarily be delayed?

MR. BEMBEN: That's not, yeah. So, that's not what's required by the claim. It's not just is it delayed by some amount that is inherent in a signal passing through a line. The claim requires that it's delayed by a specific amount that's determined by the command processing circuit. And that's what we see in our Figure 16. There's the DS signal that's being fed to the delay circuit, telling it it's a specific amount. It's not just some inherent delay because there's data passing through to that circuit.

JUDGE JURGOVAN: Okay. But Hiraishi is showing that this LCLKW signal is coming from what I see in Petitioners saying the command processing unit, and it's going to the FIFO read circuit to adjust its timing.

MR. BEMBEN: So, the DLL is just a delay lock clock.

JUDGE JURGOVAN: Right. It's generating a clock signal.

MR. BEMBEN: It's taking the clock, that's right. It's taking the clock from that buffer in the center of the chip and then generating its own local clock. That's not a delay, and that's also not determining a delay amount, which is what our claims require.

JUDGE JURGOVAN: Got it.

MR. BEMBEN: There has to be that delay amount that's determined. And the important -- and we see that in the figure as well because that delay signal is going to the data path, and that delay signal is telling it how much do you delay this, delay the signal through the path?

JUDGE JURGOVAN: Thank you. I understand your argument.

MR. BEMBEN: Thank you. And so, what I will say is that, you know, Hiraishi describes the FIFO just as buffering data and being clocked out by the clock. It doesn't describe it as a delay circuit that satisfies Claim 1. And so, as I was mentioning, what they need, Samsung needs evidence, some sort of evidence to prove that that's how a person of ordinary skill in the art would have understood it. They haven't done that, and again, their own expert described it as simply a circuit that buffers the data, and it uses a local clock to output the data. What he said, and I'm going to go to slide 23, his testimony was that it was the combination of all of the various elements that Samsung initially pointed to that made up the delay circuit. And you

can see the testimony here. He says, I mean, they all work together to implement the delay circuit. He didn't say that that FIFO alone satisfied the delay element of Claim 1. And this is his testimony, his deposition transcript, 2012, page 17, line 23 through 18, 5.

Now, so because they don't have evidence, they don't have a reply declaration, they don't have anything supporting this notion that the FIFO meets the delay circuit of Claim 1. That's a failure of proof, and that's dispositive in this case. You could rule on that, and that should end consideration. However, we have also prepared and provided a number of additional reasons why that FIFO does not satisfy the delay circuit of Claim 1. We have those in our papers, and right now, I want to focus kind of just on the first one, because it's very easy to see. So, the FIFO's, they've do not operate in response to a module control signal. Their output is timed by the local clock signals, which we just discussed. And I'm going to go to slide 28, which shows just that.

So, on slide 28 on the left hand side is paragraph 87 of Hiraishi explaining that the clock signal CK, which is shown in red, that's generated by the command address control register buffer 400, fed into Figure 5. And it generates the two local clock signals shown in blue and yellow, respectively. That's how it operates. Now, Petitioner maps that clock signal to the module clock signal, which is different. It's not the same. It's a different -- it's a distinct claim limitation. It's not the module control signal that is relevant to the delay circuit that's recited in Claim 1.

Now, I wanted to also mention, so this is one reason why Samsung's Ground 1 positions fail. But just jumping up to our roadmap, what I want to point out is that there's a second independent reason why

Samsung's Ground 1 position fails, and it's because they are incorrect and they haven't shown that the combination of Hiraishi and Butt disclose that determining the amount to delay the signal through the data path. And so, I want to get to that. I'm going to go to slide 33. And what you heard Mr. Chandler say, and I can actually just turn to slide 20 of Samsung's demonstrative here to ensure that this is fresh in your mind, their position is that for determining the amount, they have this two-step approach. The first step, according to them, is that delays are measured during the S4 read-write leveling operations in Hiraishi. Those delays, now first of all they're wrong about, those delays are not for delaying the signal through the data path, and I'll get to that, but that's the first step. So, delays in the S4 leveling, and then the second step, they say that Hiraishi teaches those delays from the first step are used during re-timing. That is incorrect. And that's incorrect for two reasons. First, they're fundamentally misunderstanding the S4 leveling operations that are described in Hiraishi. And the second reason is that Hiraishi simply doesn't teach that the re-timing is based on the S4 leveling. So, I'm going to start with the first one though, that they're just fundamentally misunderstanding how the S4 leveling operations are performed and what their purpose is.

I'll start with slide 19. This is Samsung slide 19. And this is something that Mr. Chandler showed you. And what he explained to you was that the S4 for leveling operations were to account for these delays between L1 and L2, those data paths. That's not what Hiraishi actually states. And what I'll say is that Mr. Chandler's position it's repeated in their reply. In their reply, page 20, they said that the leveling operations are needed because data line L1 to the upper memory chip is longer than data

line L2 to the lower memory chip, resulting in longer flight time delays. That's not what Hiraishi teaches. And so, I'll go to slide 34, our slide 34. I'm sorry. So, what Hiraishi teaches is that the clock signal is coming from the command address buffer 400 in the center of the chip. And the strobe signals are coming from the buffer circuits. And the write leveling operation is to align the strobe and the clock, which are coming from different locations to the memory chip. And we see that. That's described expressly in Hiraishi in paragraphs 143, 145, and 146. It's also shown in his figures. If you look at Figure 14 on the righthand side of slide 34, what he's showing in Figure 14B on the righthand side, and we have it circled in red, is that the result of the write leveling operation is that the clock signal coming from the command address control register 400 is going to be aligned with the data, that the data strobe signal that's coming from the buffer circuit when they reach the memory module. That's the purpose of Hiraishi's write leveling. It's not to determine delays in the data signal lines, it's delay of data signal lines. It affects the strobe signal.

Similarly, with respect to read leveling, I'm going to move to slide 37 of our presentation, and this is the read leveling. And this is Hiraishi describes expressly, it's not about the L1, L2 differences in the data lines. It's because data is coming, now data is coming from the memory chip to the buffer now. So, data is coming from the memory chip to the buffer, and then the clock signal is coming from the command address control register to the buffer. And because of those two, the difference in the timing of those two signals being received by the buffer circuit, there is some adjustment. And what the adjustment is doing though, it's determining when to turn on the input buffer, input B. That's what it's deciding what to do. When do I

turn on the input buffer B? And let me show you a slide to -- I'll just go.

So, going back to slide 20, this is slide 20, and what this is showing is Figure 5, and the input buffers are shown in green. Now importantly, those input buffers are not being mapped. Samsung is not mapping them to the delay circuit. They map them to the tristate buffer. We see that the left hand side is from their petition and that was also confirmed by Dr. Wedig in his testimony. So, read leveling is not effecting, it's not about the delay circuit, it's about when do you turn on the timing of those input buffers to start receiving data. That's it.

And so, the second thing that they're misunderstanding is that these, the leveling operations are not the basis of the retiming operations. And so, now if I'm going to move to the retiming operations, the retiming operations in Hiraishi, he discloses that they occur during normal memory operations, so entering a normal read or normal write. By contrast, the S4 leveling those are initialization or calibration procedures that happen before the normal operations. And so, the re-timing with this slide 35 shows is the re-timing in the right direction. And this is coming directly from our own expert. What he says is that Hiraishi resets the internal latency to the next highest clock cycle, which avoids the tedious process of having the buffer circuit compute individual delays. And we see that. The WL four clock cycles, the write latency, that's a known parameter of the system. Hiraishi just simply resets that to five. And because Hiraishi assumes that the differences in fly-by delays is less than one clock cycle, Hiraishi simply sets the buffer latency to the next higher clock cycle to adequately address all expected delays. That's Exhibit 2013, paragraph 125, our expert's testimony on this point. So, that's all that it's doing. There's no disclosure in Hiraishi

that you take the delays that are used in the S4, which are not even for delaying data signals, and then move them or use them for some reason in the re-timing. And we can see that nicely also in the figures. So, Figure -- slide 36 shows Figure 12 of Hiraishi. This is a normal re-operation. And what you see is, you see the re-timing shown in green, where it's re-timing from four to five clock cycles. And you also see in red on the memory chip side, again, the leveling operation in the right direction is so that the clock in and the strobe signal are aligned, and you see that. These are two separate operations. They're not being used together. And in the redirection, it's even more apparent because if we look at slide 39, for example, what we have is that we have on the left hand side, again, this is Hiraishi Figure 5. And, as I mentioned, the write, I'm sorry, the read leveling, the S4 read leveling is for determining when do you activate those buffers. That's it. And what we have on the right hand side is we have the retiming in the right direction. And again, it's just moving from this one is a five, is the known parameter, and it's moving the latency to six. That's all. These are separate operations affecting different things. Are there any points -- any questions on this point? Because we think that this is an independent reason that Samsung's position fails on Ground 1. Again, they have taken this position that there's this two-step approach. You use the S4 leveling -- S4 read and write leveling delays, move them into the retiming. There's no support for this. Again, their expert did not provide a reply declaration on this point. And what we see in their reply is a lot of figures, a lot of color, and a lot of attorney argument trying to make this case, trying to show that you use those S4 leveling delays in the retiming. It simply isn't the case. It's not disclosed in the reference. The only thing that they have is a bunch of

figures that their attorneys made in color coded.

Now, I will get to Ground 2 briefly. So, in Ground 2, and I'm going to turn to slide 41. As I mentioned before, on the left hand side is the proposed combination. And what they have proposed is you see the purple DR1, that is a delay circuit from the Tokuhiro reference. And they proposed moving it next to, or on top of, the strobe generating circuit that's shown in Figure 5 of Hiraishi. Now, this fails facially because that's a delay circuit, even if you could do it, it's not in the data path. And so, again, this is our construction on this. The construction on data path is dispositive for this, for Ground 2. Even if you want to entertain this argument for a little bit, there's other reasons why this combination would fail. And so, what slide 43 shows is testimony from Dr. Wedig. What he said was that, and this is a little bit in the weeds, but what he said is that you would, that circuit that he's coming out of 376, this circuit that they created by putting the delay circuit from Tokuhiro into the strobe generating circuit. What that would do is it would take the local clock signal and then generate a delayed strobe. And that delayed strobe would be sent both output on the line L0, but that delayed strobe would then be fed to the FIFO and will be used to output the FIFO. That's what he said. Now, that theory is wrong. It doesn't make any sense. First of all, it's inconsistent, I'm moving to slide 44. It's inconsistent with what Hiraishi teaches. Hiraishi teaches plainly that the FIFO is a synchronous FIFO. It operates in response to the clock signal, not a strobe signal. The other thing I want to point out is that if you, or if you kind of entertain the combination there, that FIFO is not receiving two strobe signals. It would be receiving this strobe signal from the combination of Hiraishi and Tokuhiro that they've made up. But it's also receiving a strobe

signal that's highlighted in the red box on the righthand side. Samsung hasn't explained how that FIFO would operate when it receives two strobe signals, nor would it. And the reason, we can go to slide 45, strobe signals are different than clock signals. Strobe signals are intermittent signals, they're like any other command. Clocks are continuous signals. They are continuously being pumped into the FIFO. It's very different. They haven't explained how you would clock out the FIFO with a strobe signal. Another problem that's shown on this slide, 45, is that the strobe signal, it has additional data. It has a preamble and a post amble that would interrupt or interfere with any type of, or any attempt to clock out that FIFO. It simply wouldn't work, and they haven't accounted for that. And just on this point, again, there is no expert testimony. There is nothing to support them on these points other than their attorney argument.

Unless there are any questions, I will reserve my remaining time for rebuttal, Your Honors.

JUDGE MCSHANE: Okay. Thank you. And just give me a minute, and I will figure out how much time you have remaining for -- oh, actually, I do have a question.

MR. BEMBEN: Yes, Your Honor.

JUDGE MCSHANE: Let me ask you a question real quick. In your sur-reply, I noticed that you did address issues, and in this discussion today, you did address issues related to the supplemental evidence, which as I indicated, that motion to be allowed to file that supplemental evidence is still pending. So, it's not in the record, officially. Anything, any arguments you want to add here on the record, on that evidence, if we were to grant that motion, and it would be allowed in the record. Anything else you want to

say about it at this point?

MR. BEMBEN: Yes. Just to make sure that I'm understanding your question, Judge McShane, you're talking about the Samsung's District Court expert's testimony with respect to the data path?

JUDGE MCSHANE: Yes, exactly. I'm sorry, I mangled the question, but I'm from Brooklyn, so there you go.

MR. BEMBEN: No problem.

JUDGE MCSHANE: It goes with the territory.

MR. BEMBEN: The only point that I'd like to reiterate there is that it's consistent with our positions, and more importantly, it's consistent with the intrinsic evidence that you don't necessarily need to turn to the extrinsic evidence here. And in fact, you know, one of the things that Samsung said, so, so, you know, they're fighting to keep this evidence out. And they go through and try and keep this evidence out. One of the things they say, and this is in their own paper, 37 at page five, they say, thus, the Board need not resort to extrinsic evidence to determine the construction of data path. I completely agree. Look at the intrinsic evidence. It is telling that the claim language, and the specification supports our position. I will also say, just, just since we're talking about claim construction again, and there's been a lot of allegations that we have changed our claim construction positions. What I want to say is that's not true. And one of the reasons that that's not true is because in our Patent Owner preliminary response or POPR, we did include a footnote about this issue. This is on page 10, footnote 2 of the Patent Owner preliminary response, paper 6. Of course, it's not a fully fleshed out claim construction position. But what we did say is that with respect to this specific limitation that we're talking about today, that

Petitioner's analysis was conflating the data in the strobe signals and that it didn't show that the data was being delayed. And so, we see that in two. And Samsung did have an opportunity to respond. They were granted a reply to our Patent Owner preliminary response. They did not address this issue at all. And so, we have been consistent in this proceeding about the way that we are interpreting this claim limitation. And I'll leave it at that.

JUDGE MCSHANE: Okay. Thank you. You're going to have 18 minutes for sur-rebuttal, and I'll turn it over back to Mr. Chandler, and you have 13 minutes for rebuttal.

MR. CHANDLER: Thank you, Your Honor. The last argument by Counsel was directly refuted by the institution decision, paper 13, page 16, where the Board specifically held Patent Owner does not present any proposed claim constructions. And that was both after the preliminary response and the preliminary reply. So, Patent Owner clearly changed its theories. This is addressed on our slides, 58 and 59, where in the complaints against Samsung, they very clearly drew a dashed red box that included the strobe signal as part of the delay search in the data -- in the data path. And then as shown in our slide 59, they specifically said that that data path, and they put a red box around it, and that red box includes DQS strobe signals, as well as multiple DQ data signals. They said that data path, the red box, corresponds to each data signal line. That's the exact claim language. So, they changed their construction from the time of the petition, so the Patent Owner response, and as Judge Szpondowski noted, it is appropriate for us under the *Axonics* case to respond to their change in claim construction.

I thought their argument was pretty remarkable in what they were doing because they literally are trying to challenge every single issue that

this Board already determined in a final written decision against Netlist, including Ground 2. The argument, the second to last argument by counsel for Netlist was trying to challenge Ground 2's combination. The Board specifically held, as shown in our slide 112, that there was a motivation to combine Tokuhiro with Hiraishi with a reasonable expectation of success. And the Board specifically rejected the same arguments that Netlist is trying to raise now about how there would have been some differences, and the Board said that's just a bodily incorporation argument.

Same thing with Ground 1. Again, the test for collateral estoppel is not only -- it's not simply whether the claim is the same. That would be a claim preclusion argument. Issue preclusion also applies and that is that the issue is the same. The Board held in *Mobile Tech v. InVue* that a party is bound by any subsidiary factual determinations. And so, if we look at that final written decision, Exhibit 1066 at the top of page 34, you can see the arguments that Netlist made to this very Board, and they were all rejected. Netlist argued that Osanai, which is the same as Hiraishi, doesn't control the timing of the data in strobe signals on the data paths in accordance with time information. So, all the arguments you just heard from counsel for Netlist, same arguments that were being presented in the previous final written decision in IPR2022-00236, the Board rejected them. The Board correctly concluded that S4 read and write leveling does change the timing of both the strobe and the data signals. And that's the same theory that we're relying on here. It doesn't matter if you zoom out and look at the entire data buffer, if you just zoom in and look at the FIFO on the data line, the result is the same, which same environment is that Hiraishi delays the data signals.

I wanted to respond to the argument about write leveling where

counsel for Netlist was pointing to Figure 14 of Hiraishi. Figure 14 of Hiraishi is how the write leveling measures the delays on the vertical delays L1 and L2. And to make that measurement, you only need to measure the delay of the strobe signal because you know that the data signal is going to travel along with the strobe signal. So, you don't need to make two measurements because those two measurements are going to be the same. Instead, you just make one measurement using the strobe signal. But here's the key point. It's expressly described in the petition on pages 45 to 46, which is after you have measured that delay as part of write leveling, you know now what that vertical delay was on L1 and L2. You then apply that delay to both the data signal and the strobe signal during a write operation. That's how it works and that's explicitly shown in Figure 12 of Hiraishi. From Figure 12 of Hiraishi shows that after write leveling, both the DQS strobe signal and the DQ data signal are both delayed by the amount shown in this blue box called retiming, which is about 0.7 clock cycles. So, in this example the vertical flight time delay on L2 was about 0.3 clock cycles. Hiraishi teaches displaying both the strobe signal and the data signal by 0.7 clock cycles. And you can see that if you compare DQS in, that's the strobe signal coming into the blue data buffer as compared to DQS out. DQS in versus DQS out is a difference of 0.7 clock cycles if you look at the timing diagram. And similarly, the difference between DQ in and DQ out is a difference of 0.7 clock cycles. So, Netlist's suggestion that write leveling is only about the strobe signal is completely wrong and is completely contradicted by what we said in the petition when we explained, which is that Figure 12 of Hiraishi expressly teaches that you delay both the data signal and the strobe signal. And that's exactly what the Board held in

IPR2022-00236 is that S4 read and write leveling both delay the timing of both the data signal and the strobe signal. So, it's completely improper for Netlist to keep relitigating issues that it already lost.

There was some more arguments about why Hiraishi's FIFO is not a delay circuit. And let me just put up a slide that summarizes the three arguments that was Netlist's slide 27. So, Netlist had three arguments for why the FIFO is not a delay circuit, even under our theory. And I want to just respond to I think the first argument, which is the one that Netlist focused on was about how FIFO, Hiraishi's FIFO, supposedly does not operate in response to a module control signal. And it just uses a local clock signal. That's incorrect. And we addressed this on our slide 37. So, our slide 37 shows the way that Hiraishi's data buffer works, and again, this two-step process where the first step is a mode register set command issued during initialization. So, when you boot up your computer in the morning, the first thing that happens is everything gets initialized, and that's all done in response to this mode register set command. That mode register set command satisfies claim limitation 1[b] of a system command signal that goes to the module. And then what happens is the red module controller, in response to that mode register set command, will issue over the DRC line the module control signal in response to the system command signal that tells the blue data buffers to perform the S4 read and write leveling. And then as shown on slide 40, for example, during the S4 read and write leveling, the data buffers, they measure and store the amount of delay. And this is done in response to that brown DRC module control signal as part of the S4 read and write leveling. Figures 14A and 14B on the top are the measurements done for write leveling. And then Figure 15 are the

measurements done for read leveling. So, those measurements are both done during initialization. Everything's calculated and stored. And then initialization is finished. And then slide 41 shows, okay, now we're done with initialization. Now we're up and running. The computer's running normally. And now, when there is a normal read or write command in purple, that is a system command signal that satisfies claim limitation 1[b]. And this time, the red module controller will issue a signal over DRC, which is a module control signal in response to the normal read or write command. And then DRC will cause all of these delays to happen that we talked about. Those delays were stored in the upper right of Figure 5 in the data register control circuit. And those delays are what caused the FIFO to delay by the appropriate amount. And that was discussed in paragraph 135 with respect to Figure 12, which is in the right direction, when you're writing data. And then paragraph 130 does it for Figure 11 in the read direction. And it's the FIFO that does it. And that's expressly stated in paragraph 130 and 135. The FIFO does the retiming. And the way it works, let me see if I've got, I'll stick with this slide. The way it works is there are two signals to the FIFO. You can see the signal on the right, this input signal on the right that's a hash orange, that times when the FIFO takes in the data signal, and then there's a second signal, which here is red, and that times when the data goes out of the FIFO. And so, the difference between the timing of the input signal and the timing of the output signal will vary depending on how long the FIFO needs to delay the data. And that is how the FIFO is able to provide a variable amount of delay, and this is summarized at the beginning with these big arrows on slide 76, summarizes the delay in the right direction where the FIFO can do a variable delay of 0.3 clock cycles. If the data is going onto

L1, which has that longer vertical flight time delay, or the FIFO can delay it by 0.7 clock cycles if the data is going on the shorter L2 which has a shorter vertical flight time delay of 0.3 clock cycles. So, the FIFO satisfies even Netlist's narrow claim construction, and that's why our position is that the Board doesn't need to resolve exactly whether the claim should be interpreted or construed or whatever word you want to use the way that Netlist contends, or whether the way that we contend, because the FIFO satisfies even Netlist's narrowest construction, and the FIFO not only satisfies that construction it matches up with the preferred embodiment in Figure 16 of the '608 patent.

There's some more I can say. Are there questions the Board would like me to respond to before I run out of time?

JUDGE MCSHANE: Yes. Mr. Chandler, I'm just going to repeat the question that I had for your colleague. We do have that pending motion to file the supplemental evidence. If that motion was granted is there anything that you want to add on the record here as to that evidence?

MR. CHANDLER: Oh, no. I mean I think our paper suggested quite clearly and then slides 141 through 144 respond to it. 141, there's no way they can get over the requirement that the reason we could not have obtained it earlier, and in 142, I mean if it comes in it doesn't change anything because the witness was testifying under Netlist's apparent view of the claim scope. Claim construction was not an issue in District Court. Neither party proposed any claim construction in District Court, and Samsung's expert, who is not the same expert here, and we had no notice of this deposition, he stated that he was just providing opinions under Netlist's apparent view. So, not only is it extrinsic evidence, it's extrinsic evidence of

what Netlist's apparent view was, not what Samsung's claim construction position was.

JUDGE MCSHANE: Okay. Thank you. Any other questions, Judges?

MR. CHANDLER: I mean, there's more, you know, there's more if I have more time that I can.

JUDGE MCSHANE: Oh, yeah, yeah, you can wrap up. We'll give you a minute here or two to wrap up.

MR. CHANDLER: All right. So, I'll end again on slide 76, which is, you know, the Board already determined in IPR2022-236 the way that Hiraishi works and the (INDISCERNIBLE) for read and write leveling does delay the data signal through the data path. And slide 76 is really important because it rebuts Netlist's primary two arguments, which is the FIFO does not simply add one clock cycle of delays. That it adds a variable amount of delay based on what it previously measured and stored. And in the example here, that delay is either 0.3 clock cycles, or 0.7 clock cycles. And it also rebuts Netlist's argument that Hiraishi just simply waits until the next clock cycle, and then again, you can see that's not what happens. The data comes out at T4.05, which is not the next clock cycle, or it comes out at T4.45, which is not the next clock cycle. So, both of the Boards has already determined, as well as what Hiraishi clearly teaches, the FIFO delays in response to the amount that was previously measured and stored, and that satisfies Claim 1's requirement of delaying a data signal in the data path by the amount that was determined.

Any other questions the Board would like me to address?

JUDGE MCSHANE: Yes. I'm not hearing any -- any other

questions. And with that, thank you, Mr. Chandler. And we turn it back to Mr. Bemben. And you have 18 minutes for surrebuttal, sir.

MR. BEMBEN: Thank you, Your Honor. And to address a question that Judge Szpondowski asked, you asked with respect to did we make a different claim construction or is the complaint inconsistent with what we're saying here about the data path? The answer is no, it's consistent. We will direct you to 58 through 60 of the complaint. And what I want to show is Samsung's slide 31. And they focused on the orange box here. That orange box is not in the complaint. It's an annotation by Samsung themselves. It's one of the things that they pointed to -- to show that the claim construction positions were inconsistent. And my co-counsel even mentioned that Netlist offered to put our position in a report to Samsung and they refused that offer. And so, our position is that the positions that we've taken with respect to the claims in the complaint, as well as in this IPR, are consistent.

Now, to address Mr. Chandler, again, Samsung is relying heavily on collateral estoppel, and we are simply not estopped in this case. I'm going to go back up to the difference in the claim language. This is our slide 7 and we have significant differences in claim language which drove also the mapping of the prior art. The prior art that were used in the two proceedings, the one for the '608 and the '035 are the same or largely the same, but that doesn't end the inquiry. That's not sufficient. We have to look at the claims. The claims are very different. There's a data path that corresponds to the data signal lines in the '608, and that data path is even further narrowed because it has a tristate buffer and the delay circuit. That's not in the other claims, the claims of the '035 patent. And because we have a

specific delay circuit in the data path of the '608 patent, Samsung had to make this combination, or tried to make this combination, to move the Tokuhiro delay circuit DR1. I'll show you. Slide 41. They moved that into Figure 5 of Hiraishi for this, in this IPR. They didn't make those arguments in the previous IPR. And so, just to say that, yeah, there was a motivation to combine argument that the Board accepted for broader claims doesn't mean that there's motivation to combine arguments in the specific combination that they presented in this IPR, that that is supported, and that that is something that we should be collaterally estopped from you sharing our arguments on.

Now, Mr. Chandler also talked about the leveling operations in Hiraishi and showed you some slides. I encourage the panel to go back and look at Hiraishi. Hiraishi never says that the S4 leveling operations are then used, later used, in the retiming operations. It simply doesn't say that. And if you go back and you look at what Samsung is pointing to when they're making those arguments, it's their own petition. It's their own figures that they made up to try to prove this point. Let me show you slide 24 of Samsung's presentation. This is one that Mr. Chandler showed. It talks about --

JUDGE MCSHANE: Mr. Bemben, you're not running, or we can't see your slides, I don't think, but we can refer to them as well. We have them on our desktop.

MR. BEMBEN: My apologies, Your Honor. I'll choose. Let me just share that. So, this is, again, Samsung's slide 24, and this is something that he showed today. He made this argument that there's the retiming is the, I'm sorry, the leveling is the delays are then used in the retiming, and he

showed this figure, and he showed these arrows in yellow and in blue. Those are things that they made up. And then what he's pointing to as support is the petition. This is not in Hiraishi. And there's also no support from their expert that explains that this is the way that this works because their expert did not provide a reply declaration.

Now, Mr. Chandler also made a statement about the, about the command, let me go to Samsung's slide 38, the MRS command. And now, this is going back to the FIFO. So, let me just reset for a second. This is going back to the FIFO. Still our position that if you consider this new argument that the FIFO satisfies Claim 1's buffer circuit, that they don't have any expert testimony, they don't have anything to support that. And so, that's a failure of proof and we should prevail there. But there is additional arguments that we pointed out to why that FIFO does not satisfy Claim 1's delay circuit. And one of them is this argument that the delay circuit in Claim 1 it operates in response to module control signals, which have to come from system command signals. Okay. There's no dispute on that point.

And Samsung's mapping is shown here. It's shown on their own slide 38. They're alleging that Hiraishi teaches the S4 read and write leveling. It's performed in response to the MRS command. Now, that's incorrect. Now, what Hiraishi teaches, and this is shown in their own slide, if you look at the bottom here, it has reproductions of paragraphs 139 and 140 of Hiraishi. If there is an MRS command, which Hiraishi doesn't teach, Hiraishi teaches set mode registers in step S3. And what he says is that upon completion of mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed. So, any

MRS command, if there was one, it would be used in step three, not in the S4 leveling. And that's consistent with our own expert said. We have a picture of their expert here on the righthand side and look at this language carefully. What he said is, a skilled artisan would have understood from the disclosure that the system memory controller instructs the command address control register buffer of Hiraishi's module to perform the S4 read write leveling using a first set of command signals similar to the mode switching commands and the mode register set commands. He doesn't say that they use the MRS command. He's speculating that there would be some other command, which he has not identified, that would be similar to those commands that Hiraishi would use in S4 leveling. His testimony is not consistent with what they're saying on this slide, that Hiraishi's S4 write leveling is performed in response to the MRS command. If there is an MRS command, Hiraishi teaches that that would be used in S3, not in S4.

Now, I just want to go back to what we originally said. We heard today there was a lot about, a lot of figures, a lot of annotations, all of that, but if we just return to the fundamentals of patent law and we think about what did the claims say and what did the prior actually teaches, we should prevail on that. The data path, our construction of the entire term is consistent with the specification, it's consistent with the intrinsic record and the claim language, and that is dispositive to a lot of the issues and dispute here today.

Now, what we talked about today also was just Claim 1. Of course, Claims 2 through 5 are also at issue in this proceeding, and Petitioner carries the burden on those to prove that those are invalid, and that burden never shifts to the Patent Owner. There has been no record development

with respect to claim, Dependent Claims 2 through 5, and I just want to point that out. You know, the Patent Owner carries no obligation to raising objections to those, but the Petitioner still has to meet their burden. Here, they've shifted their theory with respect to the FIFO and the delay circuit, and they never come back and address how they're under their new theory, Dependent Claims 2 through 5, which supposedly are still the same or still good. And so, it's our position, of course, that they have failed to meet their burdens for multiple reasons on Claim 1, but they have done nothing to develop the record with respect to Dependent Claims 2 through 5, which is their burden.

With that, if there are any questions, I'd be happy to entertain them.

JUDGE MCSHANE: Okay. I'm not hearing any questions. And with that, the case is submitted and taken under advisement. We would like to thank counsel very much for their preparation and the presentation of arguments today and answering our questions. It really has been very helpful, and we really do appreciate it. We know how much time you folks put into this. It's pretty dense to put it mildly, and, you know, you really have, you know all the details, and we appreciate that.

If the parties could just stay, counsel could stay on the line after the Judges drop off, we'd appreciate it, just in case the court reporter has any questions for you. And with that, we're off the record, and thank you very much.

(Whereupon the above-entitled matter went off the record at 2:57 p.m.)

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