

I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300

member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

5. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (<https://www.jedec.org>), where they are cataloged and indexed by keyword and technological subject matter. By 2000, the JEDEC website was publicly available and commonly used by manufactures, companies in the microelectronics industry, and other interested parties to access and obtain standards information pertaining to that industry. Anyone interested can join JEDEC online, at JEDEC.org.

6. This declaration concerns JEDEC Standard No. 21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002), Page 4.20.4-1 to -82 (hereinafter, "JESD21-C"). The copy of JESD21-C attached to this declaration as Exhibit A is identical to the copy of JESD21-C in JEDEC's files.

7. The following statements on the public availability of JESD21-C as of January 2002 and October 2003 are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the

date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and posted to the website. For JESD21-C, the date on the cover is January 2002. However, JESD21-C was part of JEDEC Standard No. 21-C, for which JEDEC provided an update service where specific pages could be updated as part of a periodic "Release." In the copy of JESD21-C attached as Exhibit A, most pages (like the cover page dated January 2002) were published in January 2002. A few pages were updated as part of Release 12, *see* Exhibit A at pages 4.20.4-6 to -9, -22, and one page was updated as part of Release 13 in October 2003, *see* Exhibit A at page 4.20.4-71.

8. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication, and seeks final review and approval to publish from the JEDEC legal department. Once legal approval is received, the JEDEC publications department uploads the approved document to the JEDEC website with a brief description. An email announcement is then sent to the sponsoring committee and any approved resellers. By 2000, JEDEC made its published standards available for download from www.jedec.org, as mentioned above.

9. Based on my personal knowledge of JEDEC's policies, most of the pages of the copy of JESD21-C attached as Exhibit A were made publicly

available in January 2002 and all of the pages of the copy of JESD21-C attached as Exhibit A were made publicly available by October 2003. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's typical practice was not followed. I have no reason to believe that JESD21-C was not made publicly accessible in January 2002 in October 2003 as described above.

10. To further confirm my statements above regarding JESD21-C, I have visited the Internet Archive to look at the first capture of the online catalog at www.jedec.org after January 2002, which occurred on November 5, 2002: <http://web.archive.org/web/20021105112938/http://www.jedec.org/Catalog/display.cfm>>. A printout of this capture is attached as Exhibit B and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on November 5, 2002, the JEDEC Standard No. 21-C was cataloged, indexed with the title "CONFIGURATIONS FOR SOLID STATE MEMORIES" and the keyword "21-C," and was available to the public by that date, consistent with my statements above. See Exhibit B at pages 6, 43, 66. The JEDEC website explained, "JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council

from September 1989. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication.” *See* Exhibit B at page 6. In addition, the JEDEC website offered an “ANNUAL UPDATING SERVICE” for the JEDEC Standard No. 21-C: “The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication.” *See* Exhibit B at page 6. As explained above, JESD21-C attached as Exhibit A was part of JEDEC Standard No. 21-C, for which JEDEC provided an update service where specific pages could be updated as part of a periodic “Release.” The capture on November 5, 2002, attached as Exhibit B included a link to the Table of Contents for the current Release of the JEDEC Standard No. 21-C. *See* Exhibit B at page 66. I have visited the Internet Archive to look at the first capture of that Table of Contents after January 2002, which occurred on April 21, 2003:

http://web.archive.org/web/20021105112938/http://www.jedec.org/download/search/21C_TOCR11b.pdf>. A printout of this capture is attached as Exhibit C and is consistent with my personal recollection of the JEDEC website and the JEDEC Standard No. 21-C. As can be seen from this Table of Contents attached as Exhibit C, “4.20.4 — 184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Specification” was included as part of “Release 11” to the JEDEC Standard No.

21-C and made available to the public, consistent with my statements above about JESD21-C attached as Exhibit A. See Exhibit C at page xxi.

11. Exhibit D is a printout of https://web.archive.org/web/20031208154552/http://www.jedec.org:80/service_members/New_Members/memberco.cfm, which is a capture on December 8, 2003. Exhibit D shows the list of member companies on JEDEC's website as of that date, which is consistent with my personal recollection of JEDEC's membership. All of those member companies would have had access to JESD21-C attached as Exhibit A no later than that date.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 2021/09/16

Julie D. Carlson

Julie D. Carlson

Exhibit A

PC2100 and PC1600 DDR SDRAM Registered DIMM

Design Specification

Revision 1.3

January 2002

DDR SDRAM Registered DIMM Design Specification

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Product Description

This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC1600/PC2100 refers to the JEDEC standard DIMM naming convention in which PC1600 indicates a 184-pin DIMM running at 100 MHz clock speed and offering 1600MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC1600/PC2100 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Registered DDR SDRAM DIMM product (refer to JEDEC Standards Manual 21-C, at <http://www.jedec.org>).

Product Family Attributes

DIMM organization	x72 ECC, x64
DIMM dimensions (nominal)	5.25" x 1.2"/1.7"
Pin count	184
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb, 1Gb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB
Serial PD	Consistent with JC 42.5 Rev 0
Voltage options	2.5 volt (V_{DD}/V_{DDQ})
Interface	SSTL_2

Environmental Requirements

DDR SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating temperature (ambient)	0 to +55	°C	1
H _{OPR}	Operating humidity (relative)	10 to 90	%	1
T _{STG}	Storage temperature	-50 to +100	°C	1
H _{STG}	Storage humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Up to 9850 ft.

Architecture

Pin Description

Pin Name	Description	Pin Name	Description
A0 - A15	SDRAM address bus	CK0	SDRAM clock (positive line of differential pair)
BA0 - BA1	SDRAM bank select	$\overline{\text{CK0}}$	SDRAM clock (negative line of differential pair)
DQ0 - DQ63	DIMM memory data bus	SCL	IIC serial bus clock for EEPROM
CB0 - CB7	DIMM ECC check bits	SDA	IIC serial bus data line for EEPROM
$\overline{\text{RAS}}$	SDRAM row address strobe	SA0 - SA2	IIC slave address select for EEPROM
$\overline{\text{CAS}}$	SDRAM column address strobe	V _{DD}	SDRAM positive power supply
$\overline{\text{WE}}$	SDRAM write strobe	V _{DDQ}	SDRAM I/O Driver positive power supply
$\overline{\text{S0}} - \overline{\text{S3}}$	SDRAM chip select lines (Physical. banks 0, 1, 2, and 3)	V _{REF}	SDRAM I/O reference supply
CKE0 - CKE1	SDRAM clock enable lines	V _{SS}	Power supply return (ground)
DQS0 - DQS8	SDRAM low data strobes	V _{DDSPD}	Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation)
DM(0-8)/DQS(9-17)	SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs)	NC	Spare Pins (no connect)
V _{DDID}	V _{DD} Identification Flag	$\overline{\text{RESET}}$	Reset pin (forces register inputs low)
Test	Used by memory bus analysis tools (unused on memory DIMMs)		

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	SSTL	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. (All DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.)
$\overline{\text{CK0}}$	SSTL	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0, CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}, \overline{\text{S2}}, \overline{\text{S3}}$	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	SSTL	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0,BA1	SSTL	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11 A10/AP, A12- A15	SSTL	—	During a Bank Activate command cycle, A0-A15 defines the row address (RA0-RA15) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	SSTL	—	Data and Check Bit Input/Output pins
DM0-DM8	SSTL	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
$V_{\text{DD}}, V_{\text{SS}}$	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0-DQS8	SSTL	Negative and Positive Edge	Data strobe for input and output data.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation).
$\overline{\text{RESET}}$	LV-CMOS	Active Low	This signal is asynchronous and driven low to the register to guarantee that the register outputs are low.

184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
1	V _{REF}	V _{REF}	93	V _{SS}	V _{SS}	48	A0	A0	140	NC	DM8,DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10	A10
3	V _{SS}	V _{SS}	95	DQ5	DQ5	50	V _{SS}	V _{SS}	142	NC	CB6
4	DQ1	DQ1	96	V _{DDQ}	V _{DDQ}	51	NC	CB3	143	V _{DDQ}	V _{DDQ}
5	DQS0	DQS0	97	DM0,DQS9	DM0,DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	V _{DD}	V _{DD}	99	DQ7	DQ7	53	DQ32	DQ32	145	V _{SS}	V _{SS}
8	DQ3	DQ3	100	V _{SS}	V _{SS}	54	V _{DDQ}	V _{DDQ}	146	DQ36	DQ36
9	NC,A15	NC,A15	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	102	NC,TEST	NC,TEST	56	DQS4	DQS4	148	V _{DD}	V _{DD}
11	V _{SS}	V _{SS}	103	NC	NC	57	DQ34	DQ34	149	DM4,DQS13	DM4,DQS13
12	DQ8	DQ8	104	V _{DDQ}	V _{DDQ}	58	V _{SS}	V _{SS}	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	V _{SS}	V _{SS}
15	V _{DDQ}	V _{DDQ}	107	DM1,DQS10	DM1,DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	NC (CK1) ¹	NC (CK1) ¹	108	V _{DD}	V _{DD}	62	V _{DDQ}	V _{DDQ}	154	$\overline{\text{RAS}}$	$\overline{\text{RAS}}$
17	NC ($\overline{\text{CK1}}$) ¹	NC ($\overline{\text{CK1}}$) ¹	109	DQ14	DQ14	63	$\overline{\text{WE}}$	$\overline{\text{WE}}$	155	DQ45	DQ45
18	V _{SS}	V _{SS}	110	DQ15	DQ15	64	DQ41	DQ41	156	V _{DDQ}	V _{DDQ}
19	DQ10	DQ10	111	CKE1	CKE1	65	$\overline{\text{CAS}}$	$\overline{\text{CAS}}$	157	$\overline{\text{S0}}$	$\overline{\text{S0}}$
20	DQ11	DQ11	112	V _{DDQ}	V _{DDQ}	66	V _{SS}	V _{SS}	158	$\overline{\text{S1}}$	$\overline{\text{S1}}$
21	CKE0	CKE0	113	NC(BA2)	NC(BA2)	67	DQS5	DQS5	159	DM5,DQS14	DM5,DQS14
22	V _{DDQ}	V _{DDQ}	114	DQ20	DQ20	68	DQ42	DQ42	160	V _{SS}	V _{SS}
23	DQ16	DQ16	115	A12,NC	A12,NC	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	V _{SS}	V _{SS}	70	V _{DD}	V _{DD}	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, $\overline{\text{S2}}$	NC, $\overline{\text{S2}}$	163	NC, $\overline{\text{S3}}$	NC, $\overline{\text{S3}}$
26	V _{SS}	V _{SS}	118	A11	A11	72	DQ48	DQ48	164	V _{DDQ}	V _{DDQ}
27	A9	A9	119	DM2,DQS11	DM2,DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	V _{DD}	V _{DD}	74	V _{SS}	V _{SS}	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	NC ($\overline{\text{CK2}}$) ¹	NC ($\overline{\text{CK2}}$) ¹	167	A13,NC	A13,NC
30	V _{DDQ}	V _{DDQ}	122	A8	A8	76	NC (CK2) ¹	NC (CK2) ¹	168	V _{DD}	V _{DD}
31	DQ19	DQ19	123	DQ23	DQ23	77	V _{DDQ}	V _{DDQ}	169	DM6,DQS15	DM6,DQS15
32	A5	A5	124	V _{SS}	V _{SS}	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	V _{SS}	V _{SS}	126	DQ28	DQ28	80	DQ51	DQ51	172	V _{DDQ}	V _{DDQ}

NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins reserved for unbuffered DDR DIMMs. Systems supporting both unbuffered and registered DIMMs may be connected to an active signal on the baseboard.
2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)

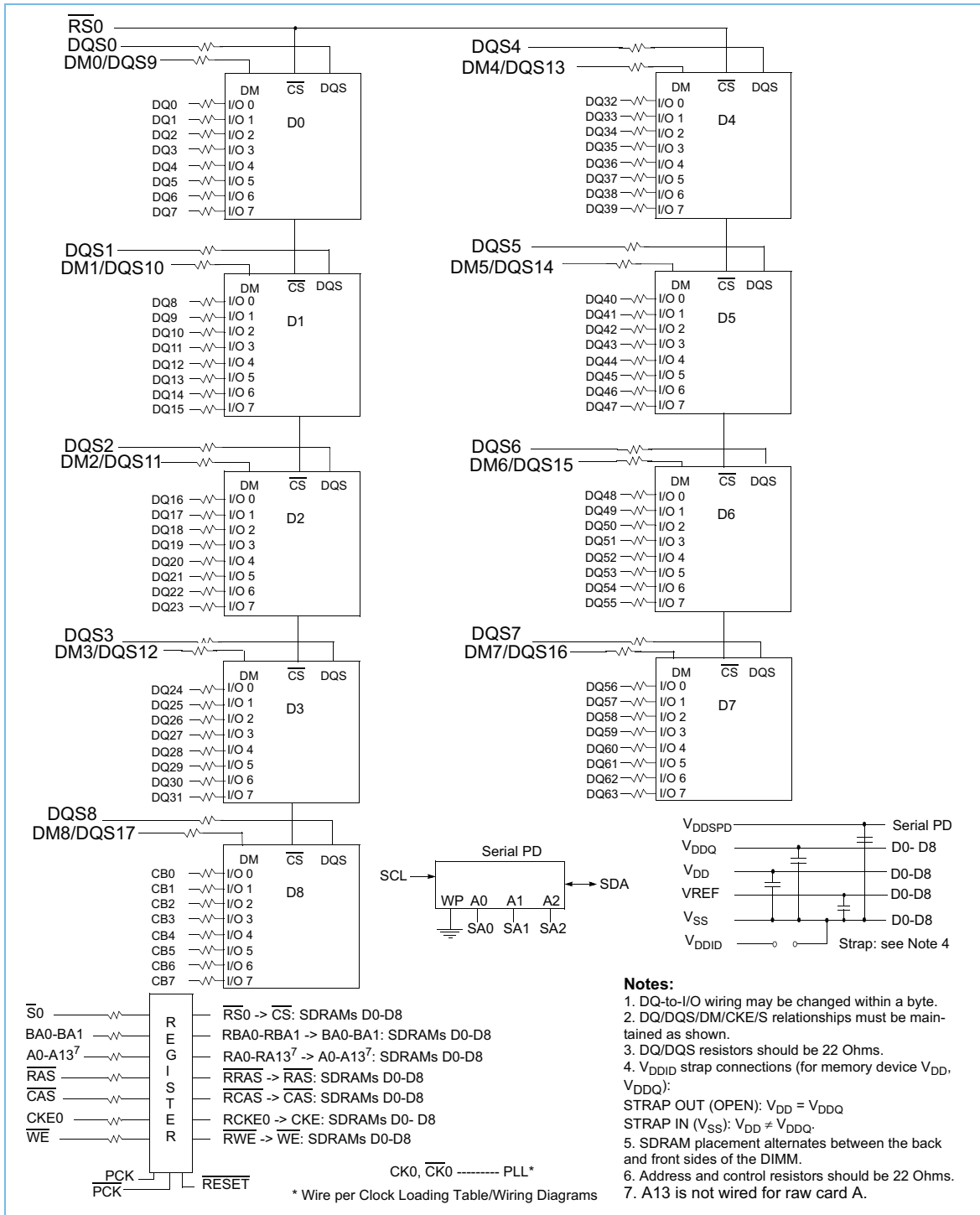
184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
35	DQ25	DQ25	127	DQ29	DQ29	81	V _{SS}	V _{SS}	173	NC,A14	NC,A14
36	DQS3	DQS3	128	V _{DDQ}	V _{DDQ}	82	V _{DDID}	V _{DDID}	174	DQ60	DQ60
37	A4	A4	129	DM3,DQS12	DM3,DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	V _{DD}	V _{DD}	130	A3	A3	84	DQ57	DQ57	176	V _{SS}	V _{SS}
39	DQ26	DQ26	131	DQ30	DQ30	85	V _{DD}	V _{DD}	177	DM7,DQS16	DM7,DQS16
40	DQ27	DQ27	132	V _{SS}	V _{SS}	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	V _{SS}	V _{SS}	134	NC	CB4	88	DQ59	DQ59	180	V _{DDQ}	V _{DDQ}
43	A1	A1	135	NC	CB5	89	V _{SS}	V _{SS}	181	SA0	SA0
44	NC	CB0	136	V _{DDQ}	V _{DDQ}	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	V _{DD}	V _{DD}	138	$\overline{CK0}$	$\overline{CK0}$	92	SCL	SCL	184	V _{DDSPD}	V _{DDSPD}
47	NC	DQS8	139	V _{SS}	V _{SS}						

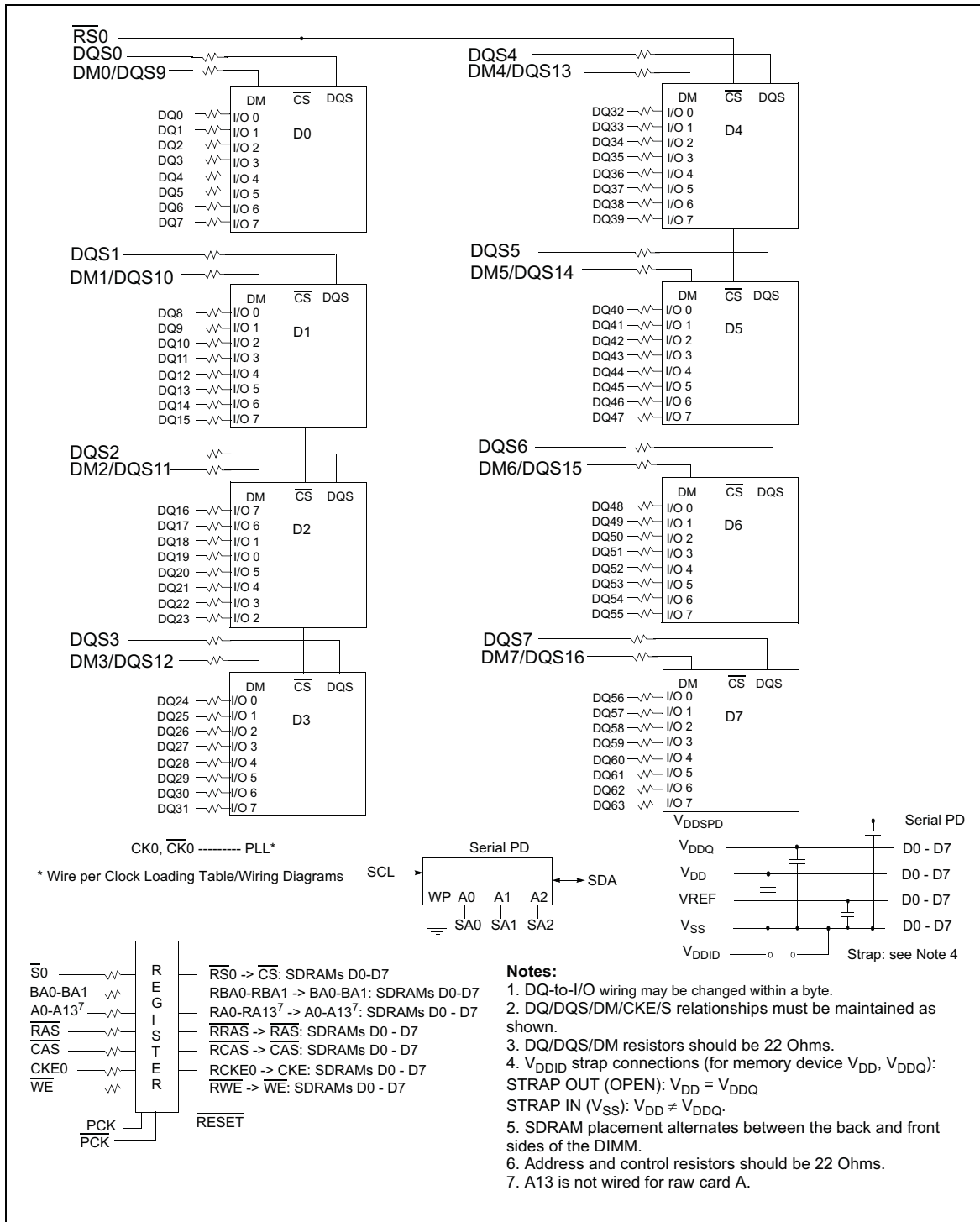
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2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)

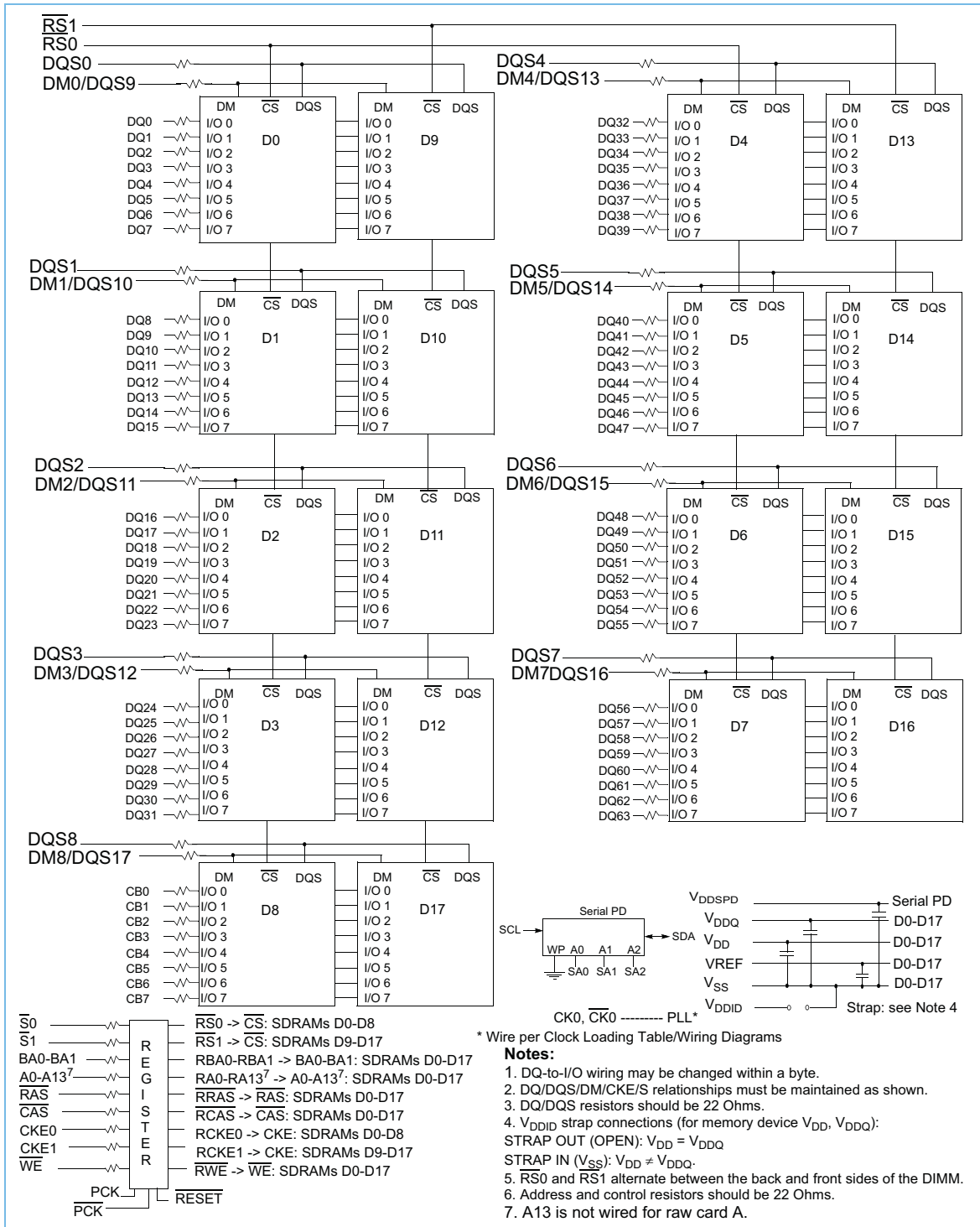
Block Diagram: Raw Card Version A/L (x72 DIMM, populated as one physical bank of x8 DDR SDRAMs)



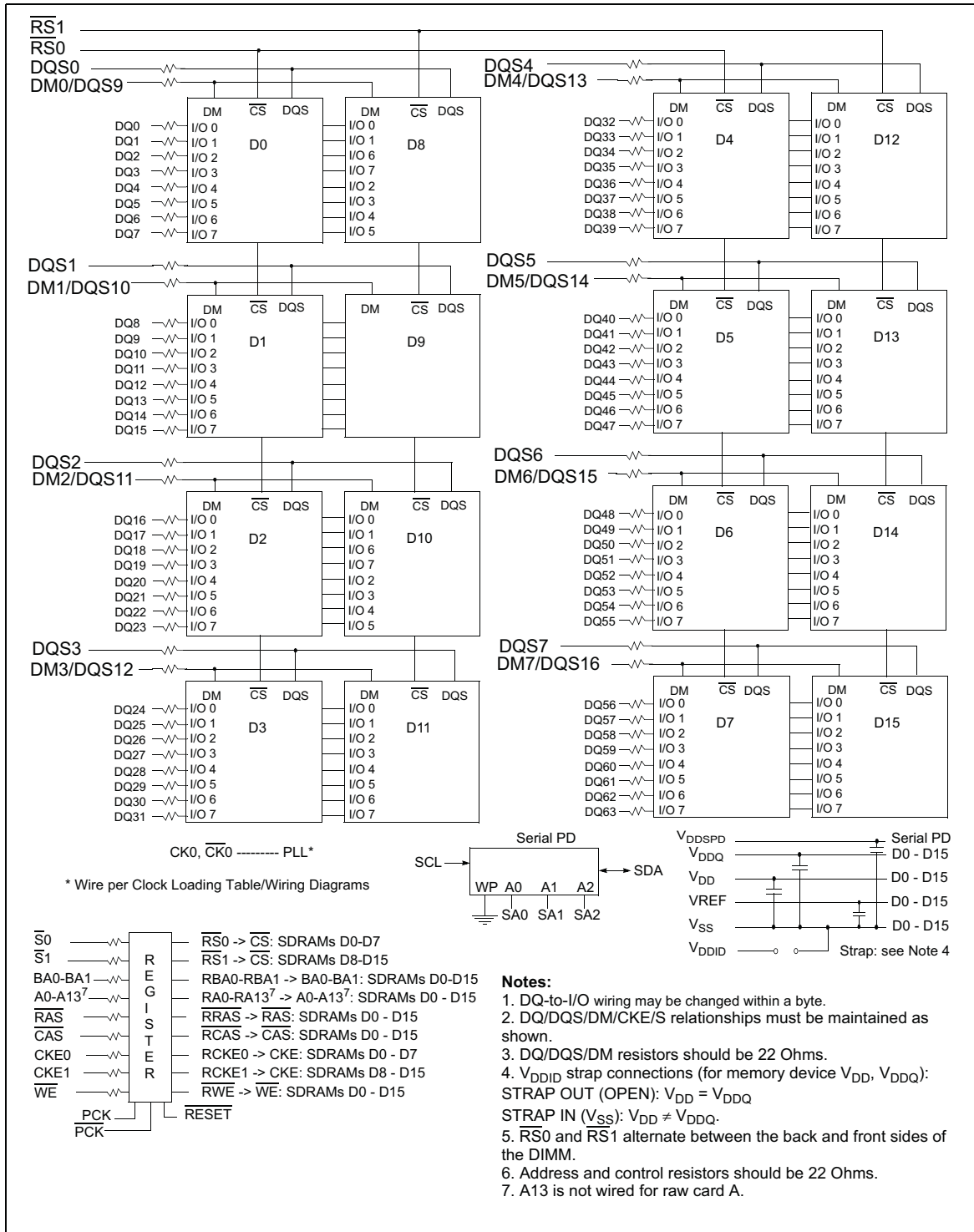
Block Diagram: Raw Card Version A/L (x64 DIMM, populated as one physical bank of x8 DDR SDRAMs)



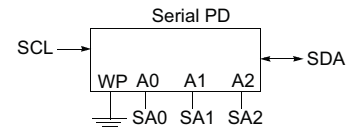
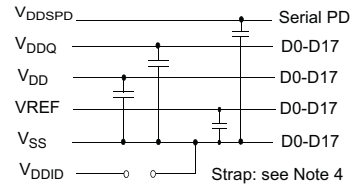
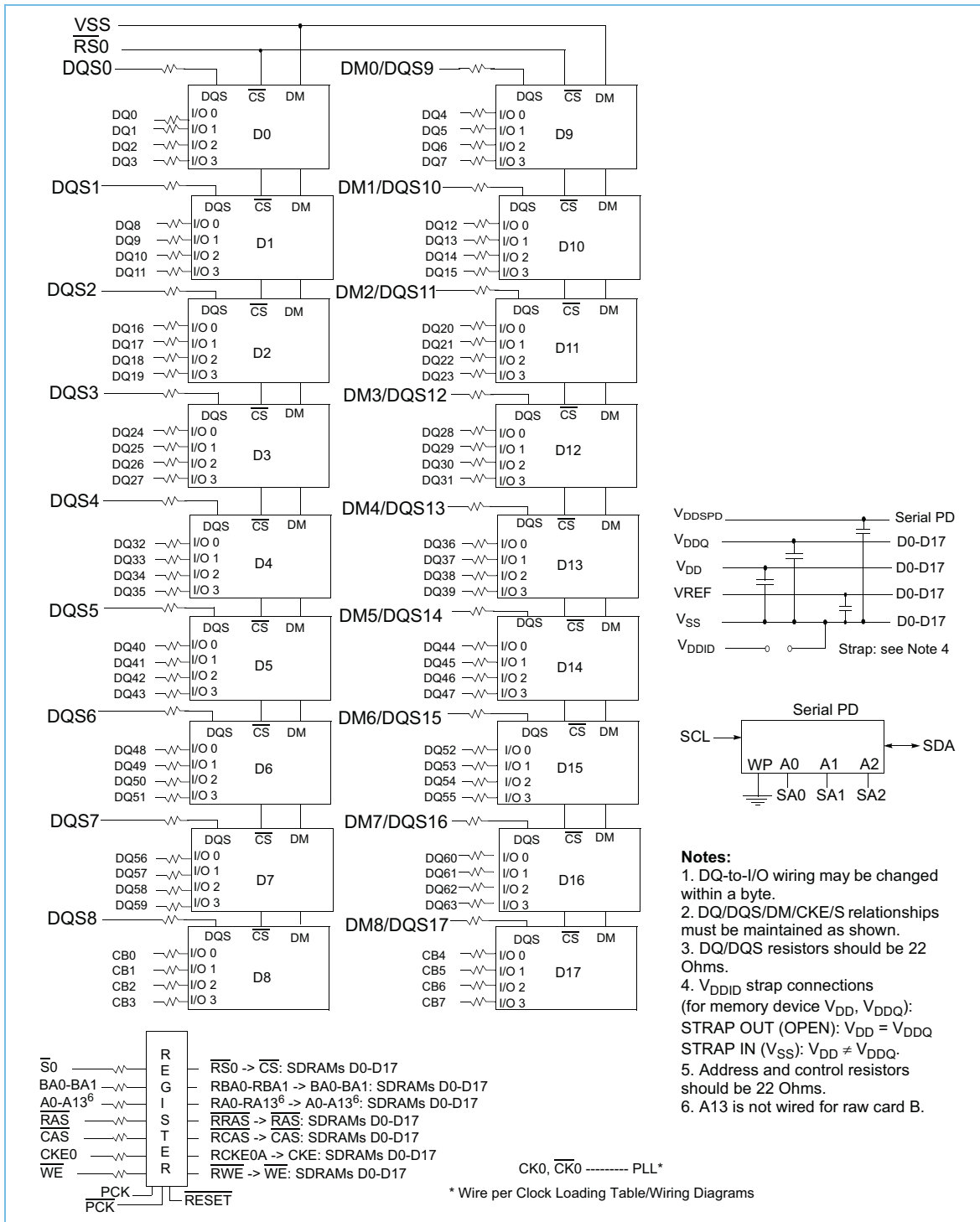
Block Diagram: Raw Card Version A/L (x72 DIMM, populated as two physical banks of x8 DDR SDRAMs)



Block Diagram: Raw Card Version A/L (x64 DIMM, populated as two physical banks of x8 DDR SDRAMs)

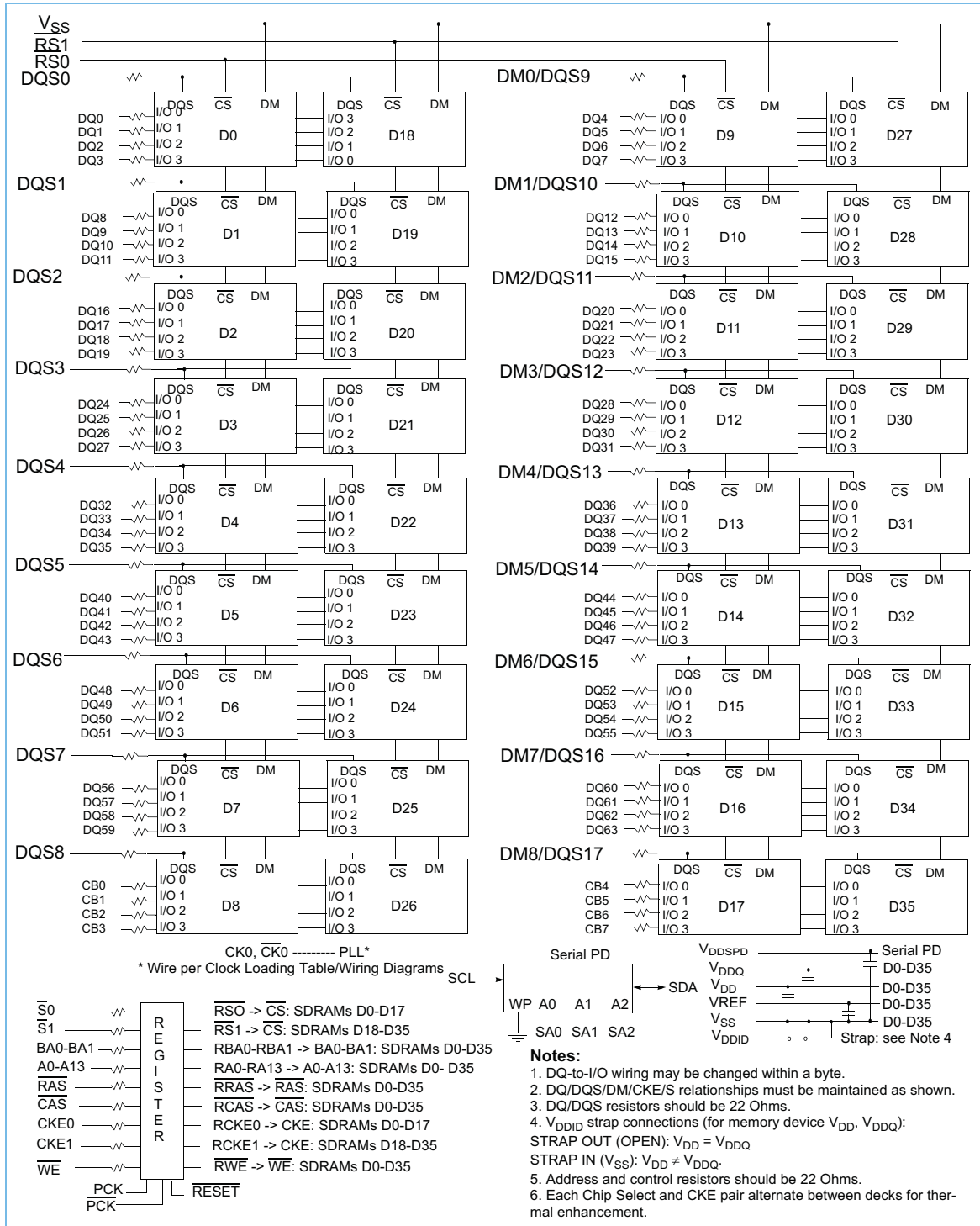


Block Diagram: Raw Card Version B/M (Populated as one physical bank of x4 DDR SDRAMs)

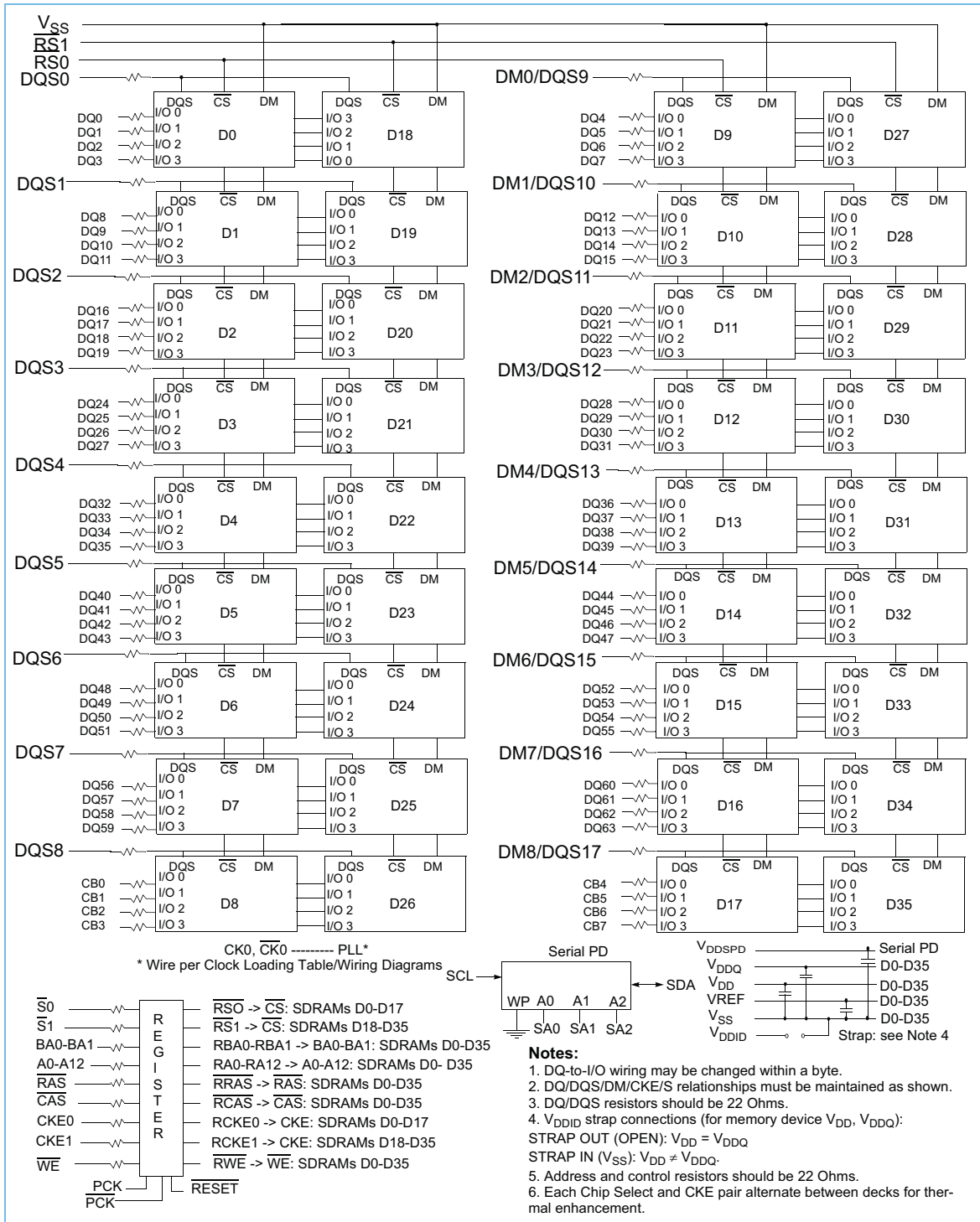


- Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. DQ/DQS resistors should be 22 Ohms.
 4. V_{DDID} strap connections (for memory device V_{DD} , V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$; STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
 5. Address and control resistors should be 22 Ohms.
 6. A13 is not wired for raw card B.

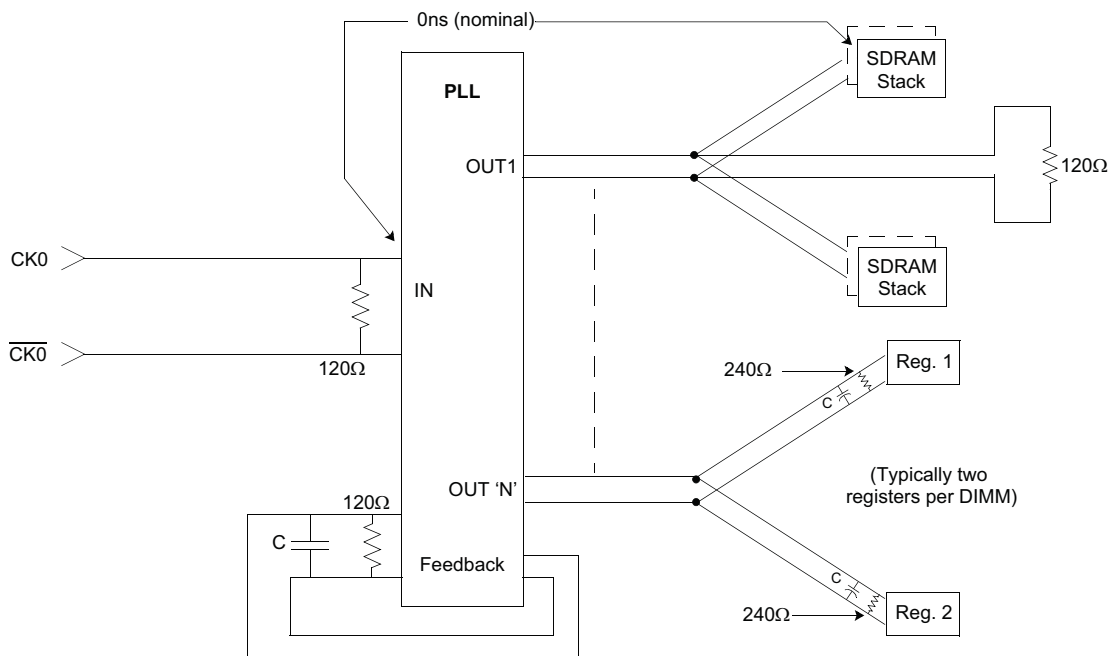
Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



Block Diagram: Raw Card Version C/E (Populated as two physical banks of x4 DDR SDRAMs)



Differential Clock Net Wiring (CK0, $\overline{\text{CK0}}$)



1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal). See "Clocking Timing Methodology" on page 74.
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.

Register Functional Assignments

Raw Card Versions A, B, and L (Two SSTV16857 1:1 Registers)				Raw Card Versions C and E (Two SSTV16859 1:2 Registers)			
Register 1		Register 2		Register 1		Register 2	
In	Out	In	Out	In	Out	In	Out
A1	RA1	A0	RA0	A1	RA1A	A0	RA0A
A2	RA2	A10	RA10		RA1B		RA0B
A3	RA3	$\overline{S0}$	$\overline{RS0}$	A2	RA2A	A10	RA10A
A4	RA4	$\overline{S1}$	$\overline{RS1}$		RA2B		RA10B
A5	RA5	\overline{CAS}	\overline{RCAS}	A3	RA3A	$\overline{S0}$	$\overline{RS0A}$
A6	RA6	\overline{RAS}	\overline{RRAS}		RA3B		$\overline{RS0B}$
A7	RA7	BA0	RBA0	A4	RA4A	$\overline{S1}$	$\overline{RS1A}$
A8	RA8	BA1	RBA1		RA4B		$\overline{RS1B}$
A9	RA9	\overline{WE}	\overline{RWE}	A5	RA5A	\overline{CAS}	\overline{RCASA}
A11	RA11				RA5B		\overline{RCASB}
A12 ¹	RA12			A6	RA6A	\overline{RAS}	\overline{RRASA}
A13 ²	RA13				RA6B		\overline{RRASB}
CKE0	RCKE0			A7	RA7A	BA0	RBA0A
CKE1	RCKE1				RA7B		RBA0B
				A8	RA8A	BA1	RBA1A
					RA8B		RBA1B
				A9	RA9A	\overline{WE}	\overline{RWEA}
					RA9B		\overline{RWEB}
				A11	RA11A		
					RA11B		
				A12 ¹	RA12A		
					RA12B		
				CKE0	RCKE0A		
					RCKE0B		
				CKE1	RCKE1A		
					RCKE1B		

1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs.

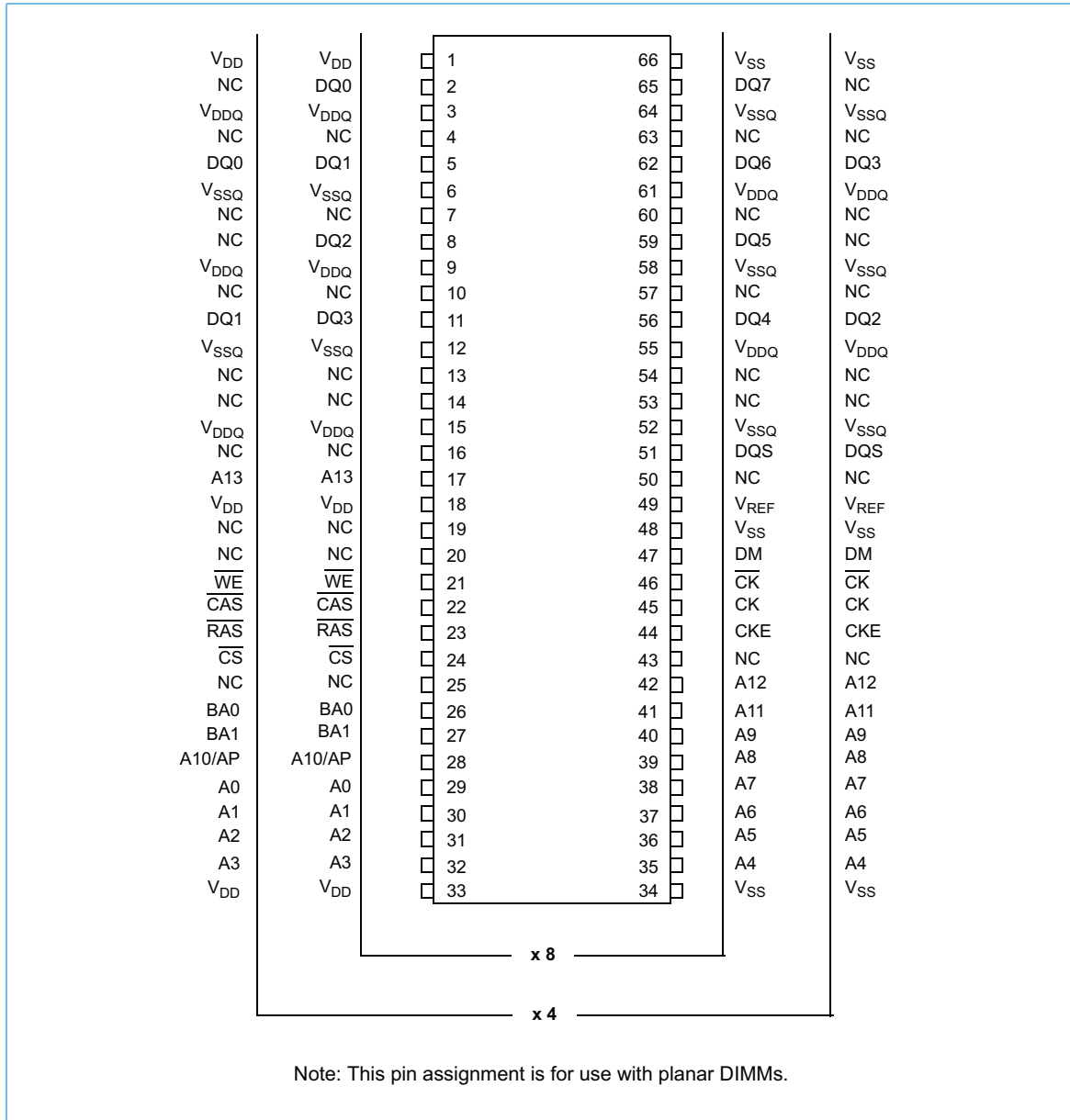
Register Functional Assignments

Raw Card Versions M (Two SSTV16857 1:1 Registers)				Raw Card Versions N (One SSTV32852 ³ 1:2 Registers)			
Register 1		Register 2		Register 1			
In	Out	In	Out	In	Out	In	Out
A2	RA2	A0	RA0	A1	RA1A	CKE0	RCKE0A
A3	RA3	A1	RA1		RA1B		RCKE0B
A4	RA4	A10	RA10	A2	RA2A	CKE1	RCKE1A
A5	RA5	S0	R \bar{S} 0		RA2B		RCKE1B
A6	RA6	$\overline{\text{CAS}}$	$\overline{\text{RCAS}}$	A3	RA3A	A0	RA0A
A7	RA7	$\overline{\text{RAS}}$	$\overline{\text{RRAS}}$		RA3B		RA0B
A8	RA8	BA0	RBA0	A4	RA4A	A10	RA10A
A9	RA9	BA1	RBA1		RA4B		RA10B
A11	RA11	$\overline{\text{WE}}$	$\overline{\text{RWE}}$	A5	RA5A	\bar{S} 0	$\overline{\text{RS0A}}$
A12 ¹	RA12				RA5B		$\overline{\text{RS0B}}$
A13 ²	RA13			A6	RA6A	\bar{S} 1	$\overline{\text{RS1A}}$
CKE0	RCKE0				RA6B		$\overline{\text{RS1B}}$
				A7	RA7A	$\overline{\text{CAS}}$	$\overline{\text{RCASA}}$
					RA7B		$\overline{\text{RCASB}}$
				A8	RA8A	$\overline{\text{RAS}}$	$\overline{\text{RRASA}}$
					RA8B		$\overline{\text{RRASB}}$
				A9	RA9A	BA0	RBA0A
					RA9B		RBA0B
				A11	RA11A	BA1	RBA1A
					RA11B		RBA1B
				A12 ¹	RA12A	$\overline{\text{WE}}$	$\overline{\text{RWEA}}$
					RA12B		$\overline{\text{RWEB}}$
				A13 ²	RA13A		
					RA13B		

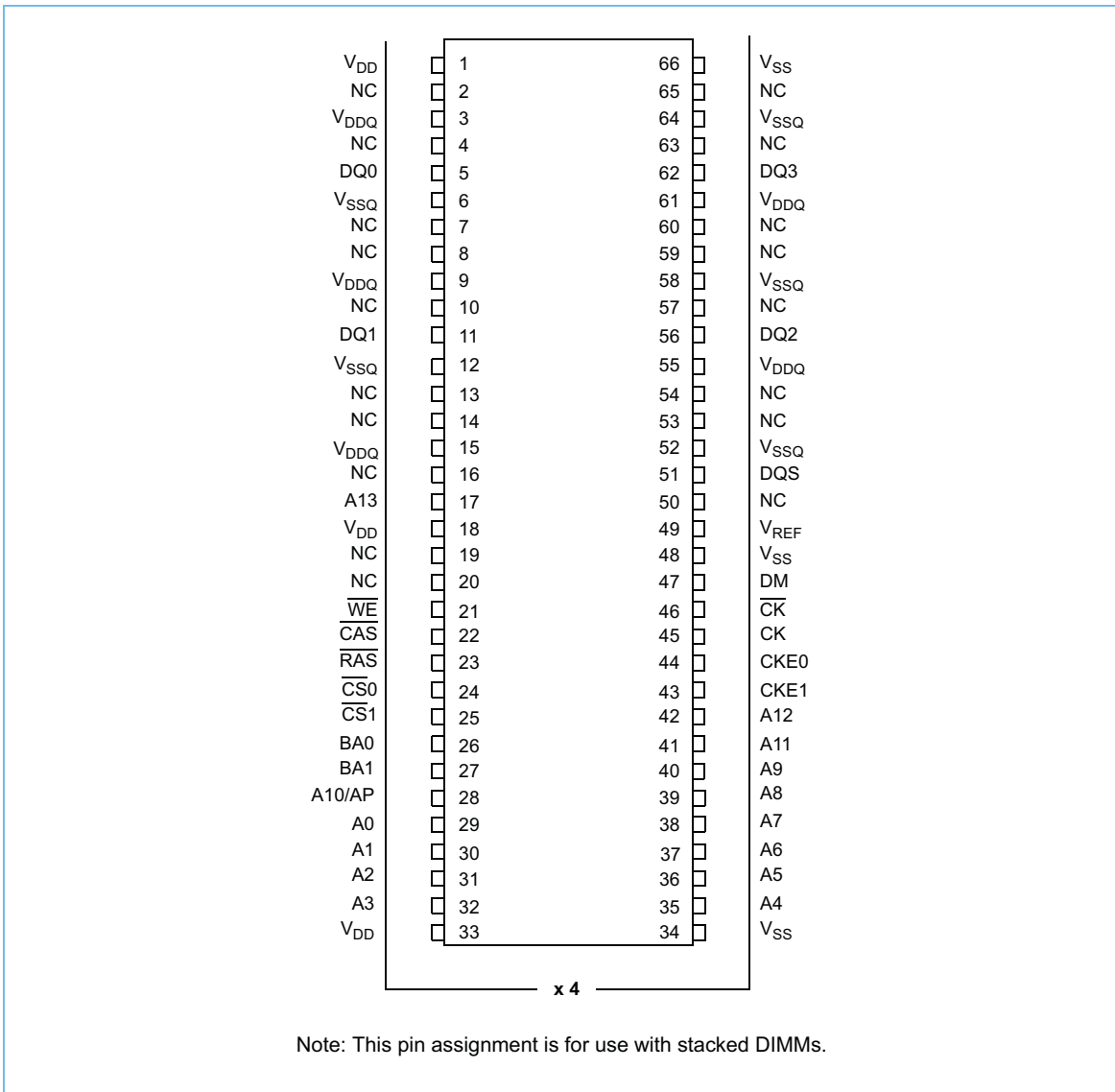
1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs
3. Reference to the JC40 nomenclature and ballots for support chips (Registers and PLLs)

Component Details

Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM Planar Components (Top View)



Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM 2-High Stack Package (Top View)



DDR SDRAM Component Specifications

The DDR SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC standard JESD79. DDR SDRAM component specification violations also violate the DDR SDRAM Registered DIMM specifications.

Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which registers should be used on each DIMM type.

DIMM Register Use

Raw Card Version	# of Banks	# of SDRAMs per output	Register Type	Package	Quantity
A/L	1	9	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
	2	18	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
B/M	1	18	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
N	2	18	SSTV32852 (1:2 24-bit SSTL)	BGA	1
C/E	2	18	SSTV16859 (1:2 13-bit SSTL)	TSSOP	2

The following specifications for the register are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on both the 1:1 and 1:2 registers, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

Critical Register Specifications

Register	Symbol	Parameter	Conditions	$T_A = 0-70^\circ \text{C}$ $V_{DD} = 2.5V \pm 0.2V$		Units	Notes
				Min	Max		
SSTV16857 (1:1 14-bit) and SSTV16859 (1:2 13-bit) and SSTV32852 (1:2 24-bit)	t_{CK}	Clock Frequency		60	170	MHz	
	t_{PD}	Clock to Output Time	30pF to GND and 50 Ohms to V_{TT}	1.1	2.8	ns	4
	t_{RST}	Reset to Output Time		—	5	ns	
	t_{SL}	Output Slew Rate	30pF to GND and 50 Ohms to $V_{TT}/2$	0.5	4	V/ns	
	t_{su}	Setup time, fast slew rate (see Notes 1 and 3)		0.75	—	ns	1, 3
			Setup time, slow slew rate (see Notes 2 and 3)	0.9	—	ns	2, 3
	t_h	Hold time, fast slew rate (see Notes 1 and 3)		0.75	—		1, 3
			Hold time, slow slew rate (see Notes 2 and 3)	0.9	—		2, 3
	$C_{IN(CK)}$	Clock Input Capacitance		2.5	3.5	pF	
$C_{IN(data)}$	Data Input Capacitance		2.5	3.5	pF		
<ol style="list-style-type: none"> For data signal, input slew rate ≥ 1 V/ns. For data signal, input slew rate ≥ 0.5 V/ns and < 1 V/ns. For CLK and $\overline{\text{CLK}}$ signals, input slew rates are ≥ 1 V/ns. For the SSTV32852, t_{PD} is 3.1ns max 							

Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly designed DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of both the 1:1 and 1:2 registers have been standardized at JEDEC in JC-40, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

DIMM PLL Use

Raw Card Version	# of Banks	# of SDRAMs per output	PLL Type	Package	Quantity
A/L	1	2 ¹	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
	2	2	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
B/M	1	2	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
N	2	4	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
C/E	2	4	CDCV857 (1:10, 2.5 Volt)	TSSOP	1

1. In the case of the One-Bank A/L Card, a padding capacitor is added across each SDRAM clock and $\overline{\text{clock}}$ pair to ensure that timing is the same for One and Two-Bank DIMMs. Also, on X64 A cards, a padding capacitor is used across the clock pair for the depopulated ninth SDRAM(s) position(s).

The following specifications for the PLL are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on this part, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as CDCV857 (Item #25).

Critical PLL Specifications

Device	Symbol	Parameter	Conditions	$T_A = 0-70^\circ\text{C}$ $V_{DD} = 2.5V \pm 0.2V$		Units	Notes
				Min	Max		
CDCV857 (1:10, 2.5 Volt)	f_{CK}	Operating Clock Frequency		60	170	MHz	1
	f_{CK}	Application Clock Frequency		95	170	MHz	1
	t_{SPE}	Static Phase Error	Application Load	-50	50	ps	2
	t_{SK}	Output Clock Skew	Application Load	—	100	ps	2
	t_{SL}	Output Slew Rate		1	3	V/ns	2
	$t_{jit(per)}$	Period		-75	75	ps	3, 4
	$t_{jit(cc)}$	Cycle-to-Cycle					4
	$t_{jit(hper)}$	Half-period		-100	100		4
	t_{STAB}	PLL Stabilization Time			100	μs	
C_{IN}	Input Capacitance		2.5	3.5	pF		

1. The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Frequency of 30 to 50KHz and a Clock Frequency Deviation of -0.5%. PLL designs should target the following values:

- Greater than 2MHz PLL loop bandwidth
- Less than -0.031 degrees of phase angle

2. The application load is defined in *Differential Clock Net Structures* on page 38.

3. Period jitter defines the largest variation in clock period, around a nominal clock period.

4. Period jitter and half-period jitter are independent from each other.

PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM Registered DIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of this part have been standardized at JEDEC in JC-40, as CDCV857 (Item #25).

Registered DIMM Details

DDR SDRAM Module Configurations (Reference Designs) (Part 1 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
A	64MB	8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9	No
	128MB	16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10	No
	512MB	64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11	No
	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	No
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	No
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	No
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	No
	64MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9	No
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10	No
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10	No
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11	No
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	No
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	No
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	No
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	No

DDR SDRAM Module Configurations (Reference Designs) (Part 2 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
L	64MB	8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9	No
	128MB	16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10	No
	512MB	64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	1Gb	128Mx8	9	66 lead TSOP	1	4	14/11	No
	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	No
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	No
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	No
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	No
	2GB	256Mx72	1Gb	128Mx8	18	66 lead TSOP	2	4	14/11	No
	64MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9	No
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10	No
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10	No
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11	No
	1GB	128Mx64	1Gb	128Mx8	8	66 lead TSOP	1	4	14/11	No
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	No
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	No
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	No
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	No
	2GB	256Mx64	1Gb	128Mx8	16	66 lead TSOP	2	4	14/11	No
B	128MB	16Mx72	64Mbit	16Mx4	18	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	128Mbit	32Mx4	18	66 lead TSOP	1	4	12/11	No
	512MB	64Mx72	256Mbit	64Mx4	18	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	512Mbit	128Mx4	18	66 lead TSOP	1	4	13/12	No
M	128MB	16Mx72	64Mbit	16Mx4	18	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	128Mbit	32Mx4	18	66 lead TSOP	1	4	12/11	No
	512MB	64Mx72	256Mbit	64Mx4	18	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	512Mbit	128Mx4	18	66 lead TSOP	1	4	13/12	No
	2GB	256Mx72	1Gb	256Mx4	18	66 lead TSOP	1	4	14/12	No
C	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	No

DDR SDRAM Module Configurations (Reference Designs) (Part 3 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
N	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	No
	4GB	512Mx72	1Gb	256Mx4	36	66 lead stacked TSOP	2	4	14/12	No
E	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOJ	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOJ	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOJ	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOJ	2	4	13/12	No

Input Loading Matrix

Signal Names	Input Device	Raw Card Version		
		A/L	B/M	C/E/N
Clock (CK0)	PLL	1	1	1
CKE0	Register	1	1	1
CKE1	Register	1 or 0	N/A	1
Addr/RAS/CAS/BA/WE	Register	1	1	1
Chip Selects	Register	1	1	1
DQ/DQS	DDR SDRAM	1 or 2	1	2
DM	DDR SDRAM	1 or 2	N/A	N/A
SCL/SDA/SA	EEPROM	1	1	1

DDR Registered Design File Releases

'Reference' Design file updates will be released as needed. This Registered DIMM specification will reflect the most recent Design files, but may also be updated to reflect clarifications to the specification only; in these cases the Design files will not be updated. The following table outlines the most recent Design file releases.

Note: Future Design file releases will include both a date and a revision label. All changes to the Design file are also documented in detail within the 'read-me' file.

Raw Card Version	Specification Revision	Applicable Design File	Notes
A	0.6	A0	Release on 12/15/99
	1.0	A1	Release on 03/31/00
B	0.6	B1	Release on 11/26/99
	1.0	B2	Release on 03/31/00
C	0.9 ¹	C1	Release on 02/25/00
	0.95 (JEDEC ballot)	C2 ²	Release on 06/23/00
	1.0	C3 ²	Release on 08/01/00
E	1.0	TBD	Original Release
L	1.2	1.0	Release on 10/05/01
M	1.2	1.0	Release on 10/05/01
N	1.3	N0	Release on 11/30/01

1. With exception of the cross section which utilized Revision 0.6.

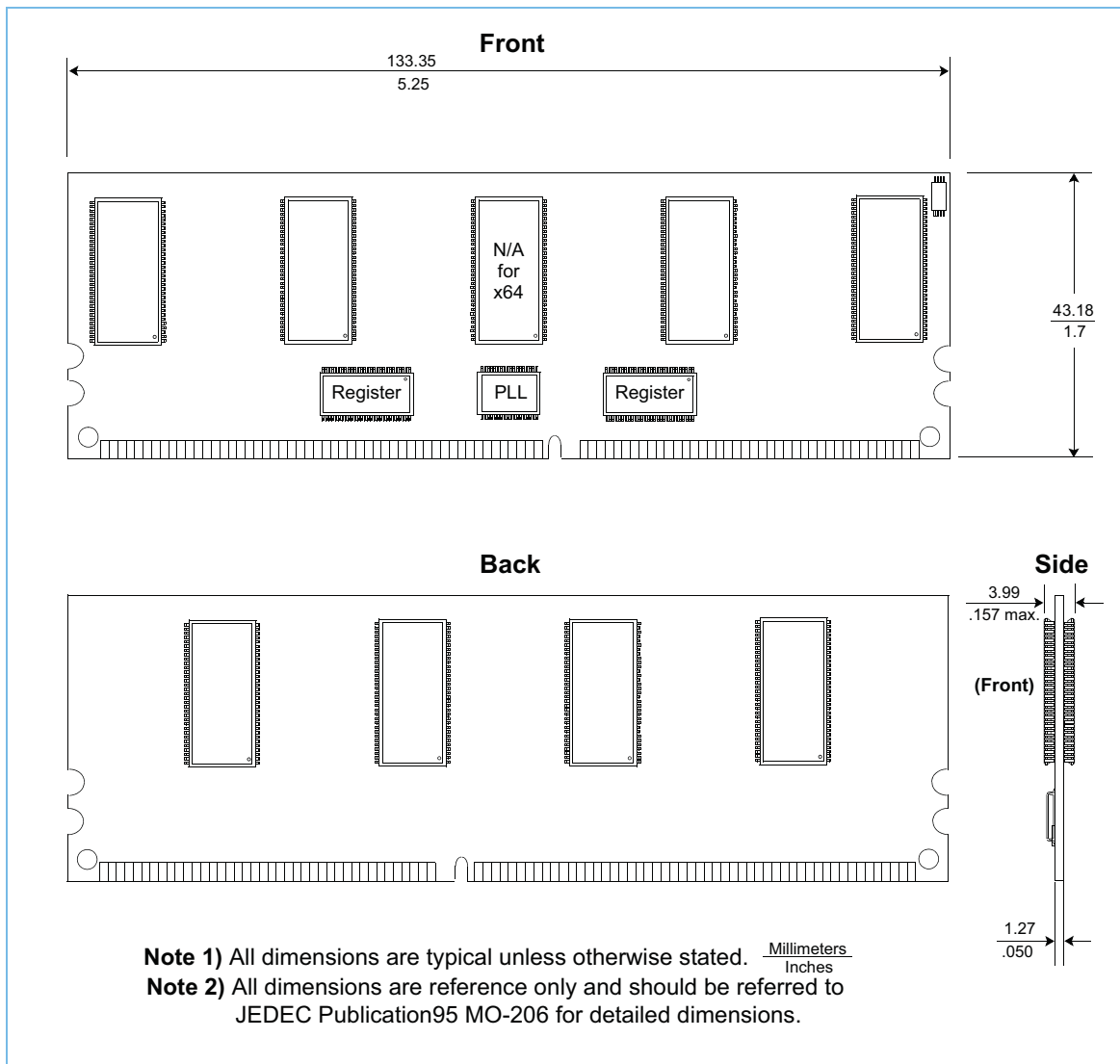
2. The C2 release is missing the gnd via connection for impedance coupons. The C3 release corrects this error. This omission has no bearing on the use of this design level in system applications.

Component Types and Placement

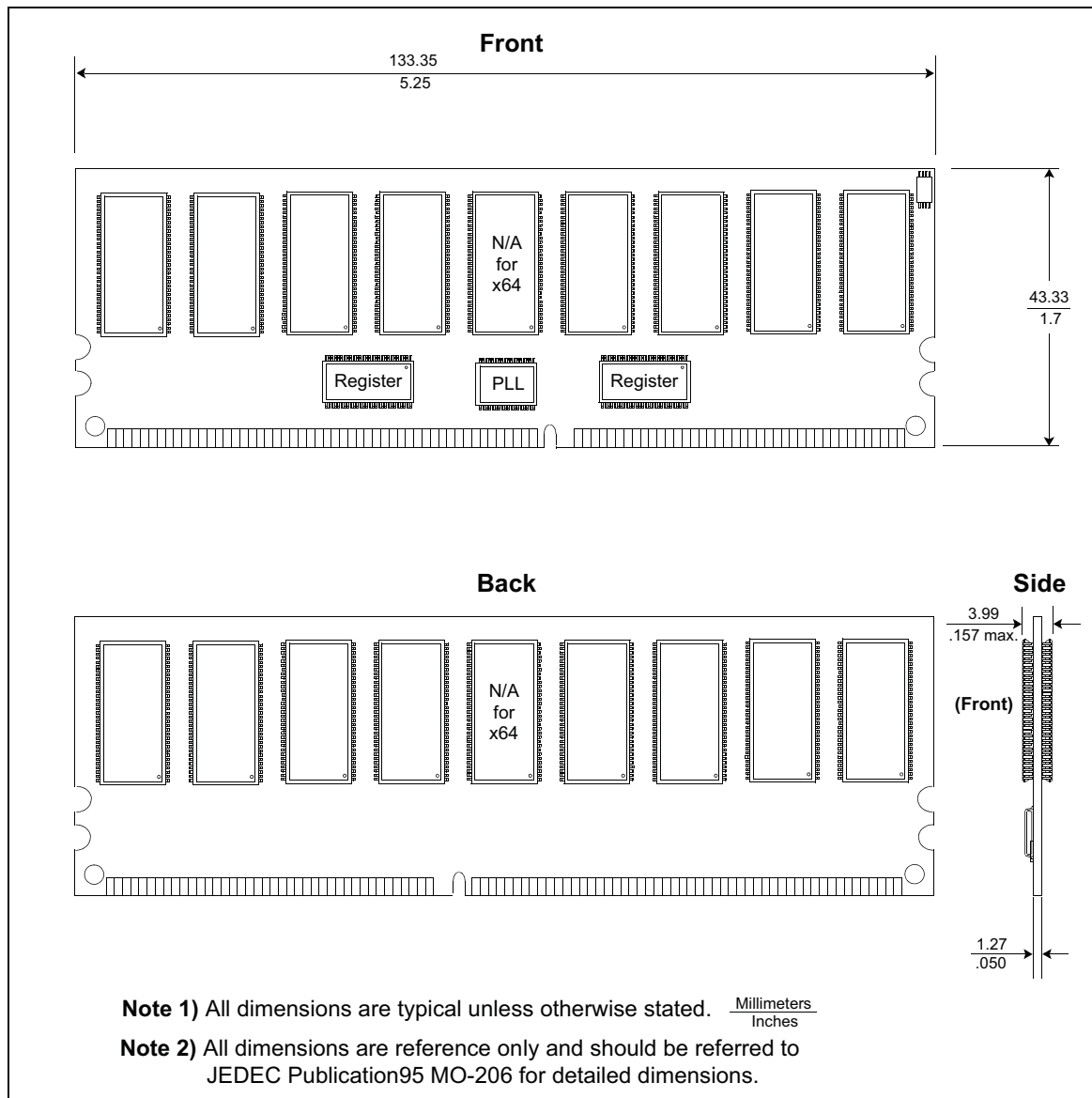
Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. In two-bank, x4 based DDR SDRAM designs, the second DDR SDRAM bank devices will be stacked on the first DDR SDRAM bank devices.

The following layouts suggest placement for the Raw Card Versions A, B, C, E, L, M and N. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

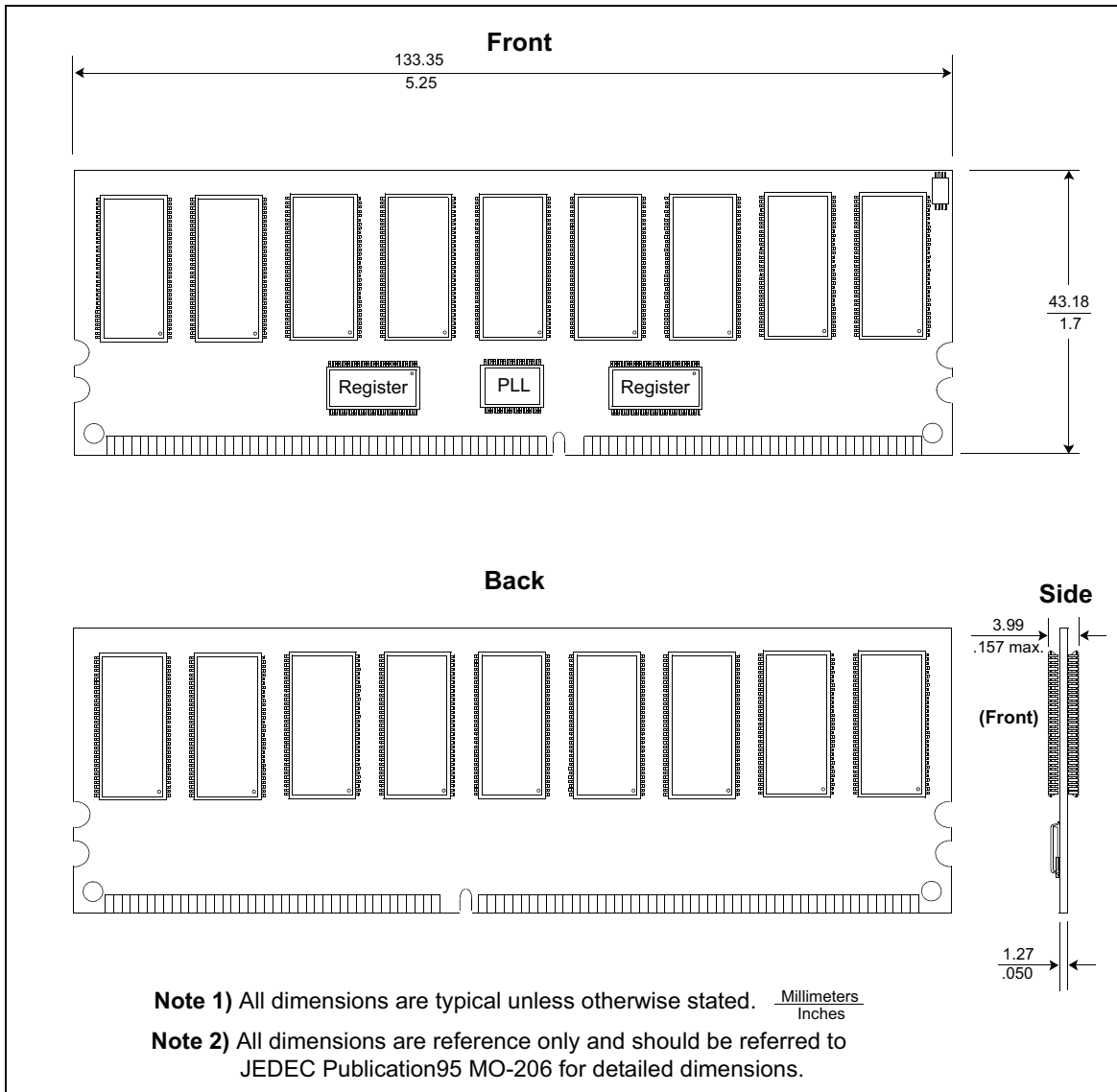
Example Raw Card Versions A (1 Physical Bank) Component Placement



Example Raw Card Versions A (2 Physical Banks) Component Placement



Example Raw Card Version B Component Placement



Example Raw Card Version C/E Component Placement

