

No. 2025-1378

**United States Court of Appeals
for the Federal Circuit**

SAMSUNG ELECTRONICS CO., LTD.,

Appellant,

v.

NETLIST, INC.,

Appellee.

On Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in IPR2023-00847

NETLIST'S RESPONSE BRIEF

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EXEMPLARY PATENT CLAIM

1. [pre] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

[a] a module board having edge connections for coupling to respective signal lines in the memory bus;

[b] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

[c] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

[d] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,

[e] wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,

[f] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

CERTIFICATE OF INTEREST

Case Number 2025-1378

Short Case Caption Samsung Electronics Co., Ltd. v. Netlist, Inc.

Filing Party/Entity Netlist, Inc.

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<p>Netlist, Inc.</p>		

Additional pages attached

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

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STATEMENT OF RELATED CASES

No appeal in or from the same Board proceeding was previously before this or any other appellate court. Netlist has asserted the '608 patent at issue here in the following proceedings: *Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:22-cv-00293-JRG (E.D. Tex.); *Netlist, Inc. v. Micron Tech., Inc.*, No. 1:22-cv-00136 (W.D. Tex.) (currently stayed). The Court's decision in this appeal will directly affect those cases.

INTRODUCTION

In a nutshell, Samsung lost this IPR because it fundamentally misread the '608 patent claims. The claims recite a memory module having a “set of data/strobe signal lines” and multiple “buffer circuits.” Each buffer circuit includes “a data path corresponding to each data signal line in the respective set of data/strobe signal lines.” The claims further require that the “data path corresponding to each data signal line include[] ... a delay circuit configured to delay a signal through the data path.” Samsung’s petition mapped the claimed delay circuit to a hodgepodge of components in the Hiraishi reference, many of which are not in a data path and some of which are not even in a strobe path. This mapping—as Netlist pointed out in response—does not work. Based on the plain language of the claims, the delay circuit must be in a path “corresponding to” a *data* signal line. Samsung’s alleged delay circuit in Hiraishi was not.

With its petition’s obviousness theory exposed as flatly inconsistent with the claim language, Samsung tried to fix its mistake in reply with a bevy of scattershot and underdeveloped arguments. *First*, Samsung proposed a construction permitting the claimed “data path” to accommodate strobe signals, even though the claims refer specifically to a data path “corresponding to” a *data* signal line from among the “set of data/strobe signal lines.” *Second*, Samsung argued that its construction was somehow required based on the Board’s decision in IPR2022-00236 (“the 236

IPR”), which involved a different Netlist patent, No. 9,824,035. *Third*, Samsung—relying solely on attorney argument and language from the prior Board ruling—introduced a brand-new obviousness theory, contending that the “delay circuit” in Hiraishi is actually a single component (the FIFO) rather than a collection of components as Samsung had argued in the petition.

The Board rejected Samsung’s arguments, and this Court should too.

As an initial matter, the obviousness theory in Samsung’s petition fails even under Samsung’s construction of “data path” because the alleged delay circuit includes components that are not in a data *or* strobe path. Samsung’s claim-construction argument is therefore immaterial. It also violates basic claim-construction principles, as it reads the words “each data signal line” out of the “corresponding to” clause of the claim. So Samsung’s petition’s theory fails on multiple levels.

The Board was on equally solid ground in rejecting Samsung’s new reply theory. The Board correctly rejected Samsung’s collateral-estoppel argument about Hiraishi’s FIFO because the 236 IPR involved substantially different claims, which led to substantially different issues being litigated across the two proceedings. On top of that, Samsung forfeited many of the specific estoppel contentions advanced in its brief by failing to raise them below.

Samsung's remaining challenges to the Board's rejection of its new reply theory are purely factual, but Samsung does not and cannot surmount the demanding substantial-evidence standard of review. Indeed, the record on these issues is one-sided in *Netlist's* favor given Samsung's failure to adduce any evidence—expert testimony or otherwise—supporting its new argument that Hiraishi's FIFO alone constitutes the claimed delay circuit. In fact, Samsung's expert testimony fatally *undermines* Samsung's new theory; the expert was quite clear that *multiple* Hiraishi components working together were required to satisfy the delay-circuit element.

This Court should affirm.

STATEMENT OF THE ISSUES

1. Whether the Court should affirm the Board's finding that Samsung's *petition* failed to show that the prior art discloses a "data path corresponding to each data signal line" that "includes ... a delay circuit configured to delay a signal through the data path," where:

(a) the Board's undisputed factual findings demonstrate that Samsung's *petition's* prior-art combinations in Grounds 1 and 2 do not disclose the claimed "delay circuit" even under Samsung's construction of "data path";

(b) in any event, the Board correctly construed "data path corresponding to each data signal line" as requiring the path to accommodate only data signals

(and not strobe signals), in accordance with the plain meaning of the claim language and specification;

(c) the petition's Ground 1 and 2 obviousness theories undisputedly fail under the Board's construction; and

(d) Samsung forfeited reliance on its supposed "alternative" theory embedded within Ground 2 by failing to sufficiently develop it below and, in any event, the Board did not abuse its discretion in finding that this theory rises or falls with Samsung's other theories.

2. Whether the Court should affirm the Board's finding that Samsung's *reply* theory failed to show that the prior art discloses the claimed "data path," where:

(a) the Board correctly concluded that its findings in the 236 IPR did not have preclusive effect in light of material differences between the claims and disputed issues across the two proceedings; and

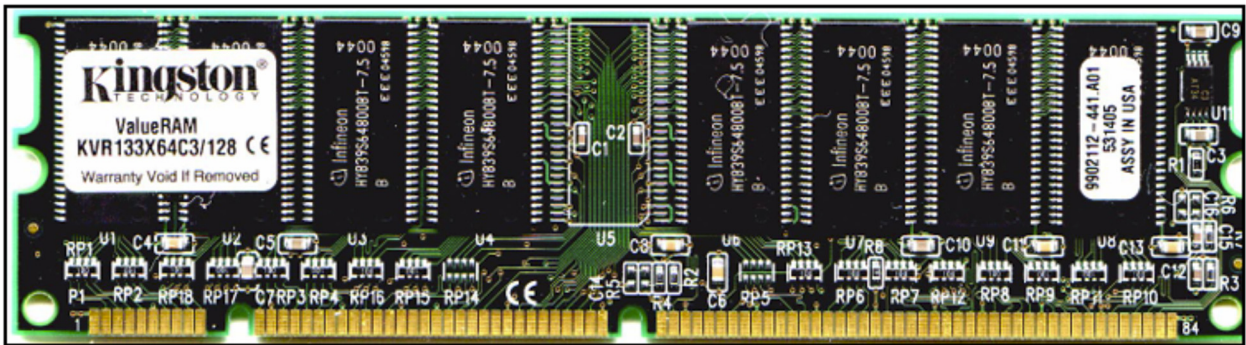
(b) substantial evidence supports the Board's factual findings regarding Hiraishi.

STATEMENT OF THE CASE

A. Netlist's '608 patent

1. Prior-art difficulties with synchronizing signals in memory modules

Netlist's '608 patent concerns an innovative design for a “memory module”—a form of dynamic memory used in computer systems. A memory module includes a set of memory chips (black below) and associated circuitry attached to a piece of printed circuit board (green):



See Appx3397; Appx7217(¶17). Once a module is plugged into a computer’s motherboard, the computer may store (“write”) data to or access (“read”) data from the memory chips. Appx3399. The computer does so using a “memory controller,” which routes signals between the module and other parts of the computer. The signals include data signals (signals that carry data—abbreviated “DQ”) and command signals (signals that tell the memory devices what to do). *E.g.*, Appx3400; Appx3414; Appx3511-3512. These different types of signals are transmitted on different individual pieces of wire, referred to as “signal lines.”

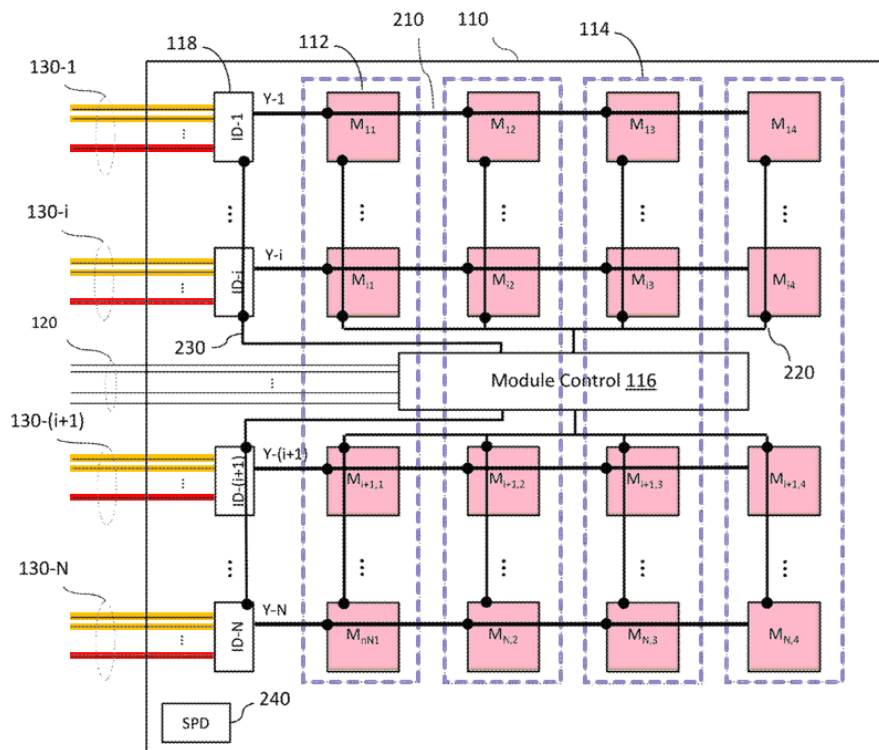
Appx7055(54:3-12).

The memory chips on which data are stored are called DRAM chips (or “DRAMs”). Appx3398. DRAM stands for Dynamic Random Access Memory. The most common type of DRAM is “synchronous DRAM,” or SDRAM, which uses a system-level clock to time transmissions of data and command signals. Appx3404. The clock functions like a metronome or “heartbeat,” keeping the various parts of the memory system in sync with one another. Appx3404. Most modern SDRAM is “Double Data Rate,” or DDR, memory, meaning two bits of data can be communicated on each data line in one clock cycle. Appx3411-3412; Appx3415-3416; *see* Appx7217-7219(¶¶18-20).

DDR SDRAM uses a special type of signal called a “strobe” signal (abbreviated “DQS”) to ensure accurate timing for driving and capturing data. Appx3416. A strobe signal indicates that another signal (like a data signal) is present and valid. Appx3400 n.1. Strobe signals allow the system to distinguish each data transmission accurately. Appx7219-7220(¶21). Data signals and strobe signals must be tightly correlated (in a temporal sense) for the system to accomplish this. *E.g.*, Appx8981(139:13-24). As Samsung does not dispute, however, the two types of signals are transmitted via distinct signal lines. Appx7055(54:3-12). And “the timing of strobe signals does not affect the timing of the data signals themselves, just the accuracy in capturing the data itself.”

Appx7219-7220(¶¶21).

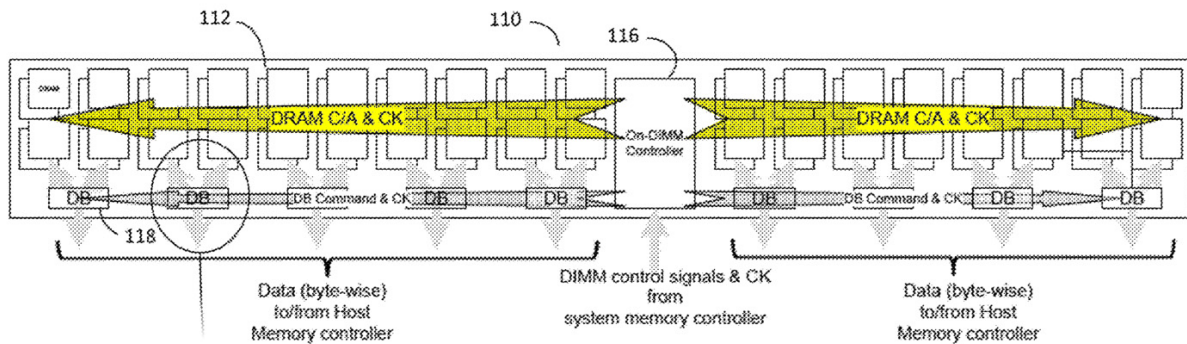
Most DDR memory modules comply with a standard issued by industry-consortium JEDEC. *See, e.g., Appx3357.* The relevant JEDEC DDR standard imposes very precise timing requirements for the strobe signal (DQS). *See Appx3487; Appx7220-7223(¶¶22-25); Appx7383.* Ensuring proper timing of signals within a memory module is made more complicated by the fact that, due to the physical layout of the module, signals must travel different distances to reach different DRAMs in the module. Figure 2A of the '608 patent depicts the basic layout:



Appx83(Fig. 2A) (annotated). The module contains DRAMs 112 (labeled M, pink) organized into multiple “ranks” 114 (outlined in purple). Appx109-111(4:65-8:21);

see Appx7223-7224(¶27). Data (orange) and strobe (red) signal lines 130 transmit data signals and strobe signals, respectively, between the system memory controller (to the left, out of picture) and the DRAMs. Module control 116 routes control signals (which tell the DRAMs what to do), address signals (which specify where in the DRAM to do it), and clock (“CK”) signals from the memory controller to the DRAMs. Appx110(5:11-26); Appx117(19:26-33); Appx7223-7227(¶¶27-32).

As shown in Figure 2C below, the C/A and CK signals coming from the module control must travel different distances to reach different DRAMs because the length of wire between the module controller and DRAMs near the inside of the module is shorter than the length of wire between the module controller and DRAMs near the outside of the module.



Appx85(Fig. 2C) (annotated). In other words, the wire lengths are “unbalanced.” Appx7227(¶33).

This difference in wire length can cause synchronization issues. See, e.g.,

Appx111(8:47-50); Appx7227(¶33). The prior art disclosed certain “leveling mechanisms” to address such issues. Appx108(2:28-32). But they proved insufficient to adequately “manag[e] read/write data timing” in newer-generation systems with higher memory operating speed and greater memory density.

Appx108(2:32-36); Appx115(15:21-23). The '608 patent is directed to solving this problem. Appx7226-7228(¶¶32-34).

2. The '608 patent invention

The '608 patent addresses these timing issues by adding “isolation devices” (also called “data buffers” or “buffer circuits”), labeled 118 in Figure 2A. *See* Appx83(Fig. 2A); Appx109(3:27-29, 4:30); Appx7227-7228(¶34); Appx7248-7249(¶70). Each isolation device includes a “data path corresponding to each data signal line,” and each data path in turn includes a tristate buffer and a delay circuit. Appx113(12:3-26); Appx117(19:43-55).

The isolation devices are responsible for providing the correct timing for data signals and control signals. Appx111-112(8:56-9:3). In particular, they “include[a] signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation.” Appx115(15:23-26). Essentially, the buffers determine how long the signals associated with a write operation take to travel to and from a given memory device and use that information to “properly time transmission” of a later read operation.

Appx115(15:45-50). The buffers can also isolate the memory devices from the rest of the module to reduce electrical load. Appx112-113(10:50-11:7).

Claim 1 is representative and recites, as relevant here, a memory module having a “plurality of sets of data/strobe signal lines” connecting the module’s memory devices to buffers, and, within each buffer, a “data path corresponding to each data signal line in the respective set of data/strobe signal lines.” Each data path, in turn, includes a “delay circuit configured to delay a signal through the data path”:

A memory module operable to communicate with a memory controller via a memory bus, the memory bus including ... a set of control/address signal lines and *a plurality of sets of data/strobe signal lines*, the memory module comprising:

- [a] a module board ... ;
- [b] a module control device ... ; ...
- [c] ... a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
- [d] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,
- [e] wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, *the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines*, and a command processing circuit configured to decode the module control signals and to

control the data path in accordance with the module control signals and the module clock signal,

[f] *wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.*

Appx117(19:14-55) (emphases added for relevant terms; reference letters used by the Board added; spacing adjusted for clarity).

B. The proceedings below

As relevant here, Samsung argued below that claims 1-5 would have been obvious over (i) Hiraishi and Butt and (ii) Hiraishi, Butt, and Tokuhiko. Appx141.

1. Samsung's petition mapped the "data path" element of limitation 1[e] to various portions of Hiraishi's buffer circuit (below). Appx173-174. The top figure depicts a read operation and the bottom figure depicts a write operation. In both figures, the system memory controller and the DRAMs would be to the left and right, respectively, of the buffer circuit 300.

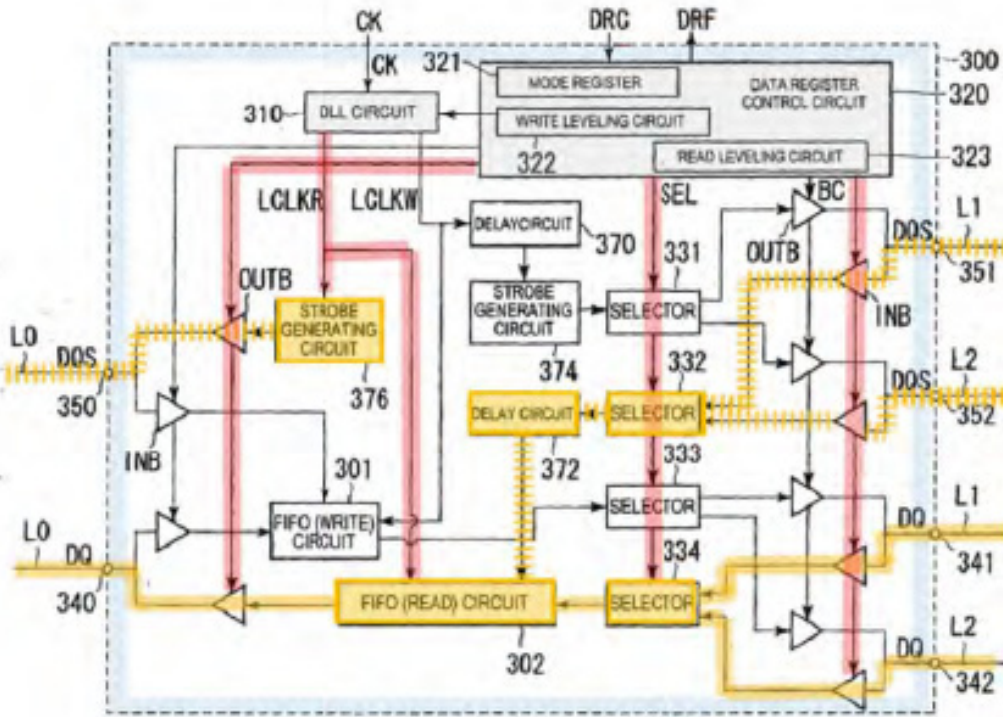


FIG.5

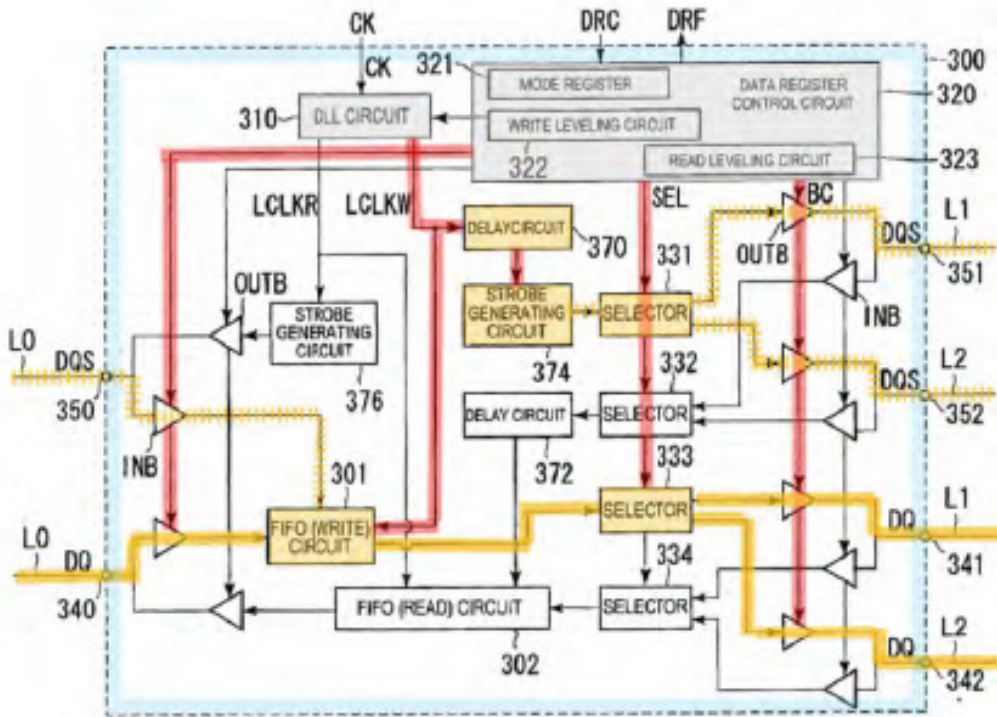


FIG.5

Appx174. The solid orange lines depict the paths traversed by data signals, while the hatched orange lines depict the paths traversed by strobe signals (the red lines depict other types of signals). Samsung argued that both the data and strobe signal lines were part of the claimed “data path.” Appx173-174.

Samsung mapped the claimed “delay circuit” to a collection of elements: Hiraishi’s “DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376.”

Appx179. Samsung argued that this alleged “delay circuit” satisfied the claims because it would determine delays based on Hiraishi’s step S4 read/write leveling and apply those delays on data and strobe signals for normal operations. Appx179-191. Samsung’s expert—in a concession that would ultimately prove fatal to Samsung’s invalidity theory—admitted that all the identified components in Hiraishi must “work together to implement the delay circuit.” Appx7018-7019(17:23-18:5).

Samsung’s second obviousness ground relied on incorporating Tokuhiko’s “delay elements DR1 and DR2” in Hiraishi’s strobe generating circuit 376, as shown below:

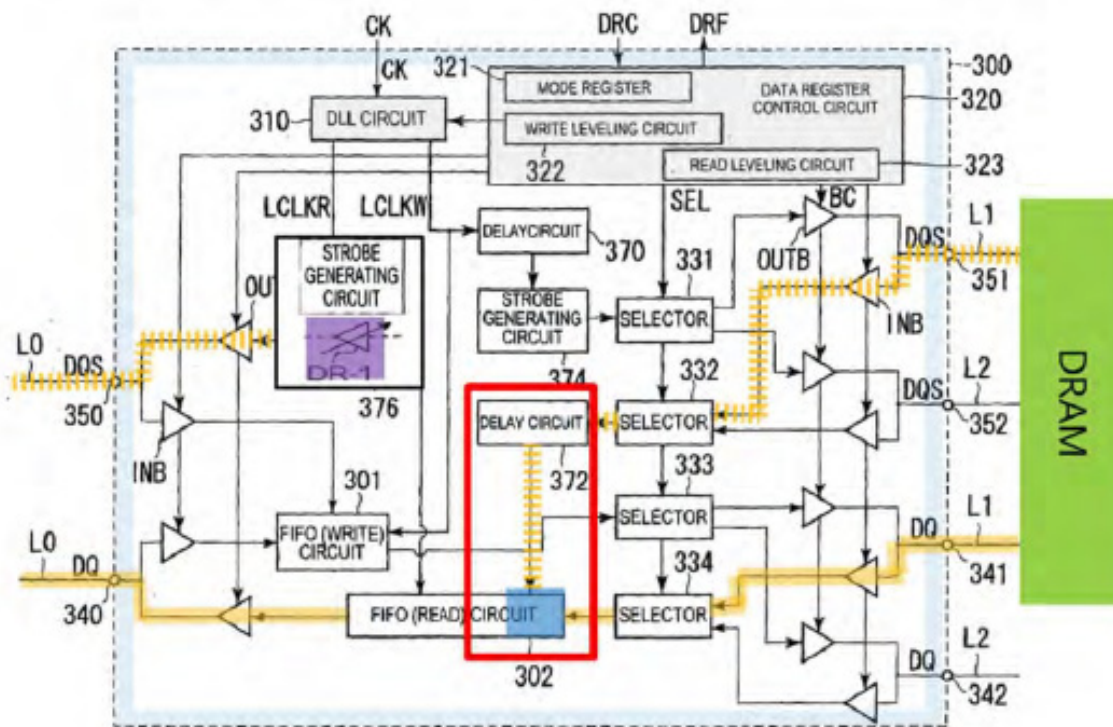


FIG.5

Appx229; see Appx222.

2. In response, Netlist argued that Samsung had misread the claims. Appx6916. Based on the plain claim language, Netlist explained, the claimed data path must “correspond to each data signal line in the respective set of data/strobe signal lines”—meaning the data path is the path that connects the *data signal lines*—not strobe signal lines or clock signal lines—through the buffer. Appx6934-6935. Furthermore, the specification consistently distinguishes the paths along which data signals travel from the paths along which strobe signals travel. Appx6935-6939. Netlist further argued that Samsung had failed to identify a delay circuit in the data path because it mapped the claimed delay circuit to components

on Hiraishi's strobe and clock signal lines. Appx6941-6943. Not only were these components not in the claimed data path, they also did not delay signals through the data path in response to module control signals, as claimed. Appx6943-6955.

Netlist also argued that Samsung misunderstood Hiraishi's S4 read and write leveling processes. The S4 write leveling process, Netlist explained, does not delay data signals but rather aligns the strobe signal DQS to the system clock signal CK. Appx6955-6967. And the S4 read leveling process adjusts the activation timing of the input buffers; it does not delay data *or* strobe signals. Appx6967-6973.

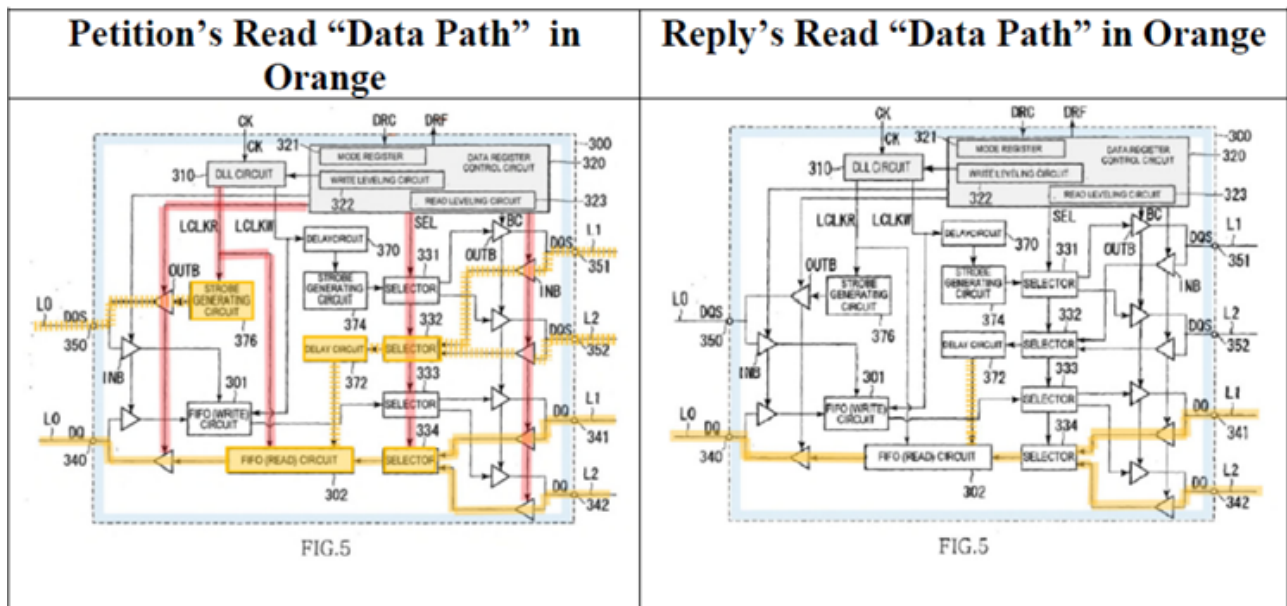
Finally, Netlist explained that the addition of Tokuhiko did not fix these flaws. Samsung proposed adding Tokuhiko's delay element in Hiraishi's "strobe generating circuit 376," but this circuit "is not on any of the DQ lines and therefore cannot satisfy" the claimed requirement of a delay circuit in the data path that is configured to delay a signal through that path. Appx6917-6919; Appx6974-6975.

In short, both of Samsung's obviousness grounds defied the claim language.

3. In reply, Samsung argued that—notwithstanding the claim language—the claimed "data path" corresponded to data *and* strobe signal lines and thus can accommodate both data signals and strobe signals. Appx10470-10481. Samsung contended, among other things, that the Board's decision in the 236 IPR, Appx6702-6765, estopped Netlist from contesting the exclusion of "strobe signal lines" from the claimed "data path." Appx10470-10473.

Samsung also made a brand-new argument. Even though Samsung’s expert Dr. Wedig had admitted that the *combination* of Hiraishi’s DLL circuit 310, FIFO circuits 301 and 302, delay circuits 370 and 372, and strobe generating circuits 374 and 376 was collectively required to implement the alleged delay circuit, Appx7018-7021(17:23-18:5, 20:10-16), Samsung’s reply argued that Hiraishi’s FIFOs *by themselves* constitute the claimed “delay circuit.” Appx10484; *see* Appx10481-10501. Samsung submitted no expert testimony supporting this contention.

The following side-by-side comparison of the alleged “data path” and “delay circuit” identified in Samsung’s petition (left) and the alleged “data path” and “delay circuit” identified in Samsung’s reply (right) demonstrates the dramatic shift in Samsung’s theory between petition and reply:



Appx9803.

C. The Board’s final written decision

The Board determined that the challenged claims are not unpatentable.

1. The Board first addressed the parties’ dispute concerning the “data path” element of claim 1. Appx10-24. The Board explained that “[t]he claim differentiates between data signal lines and strobe signal lines” and specifies that the “data path” in “limitation 1[e] ... corresponds to the data signal line in the set of data/strobe signal lines.” Appx17. In other words, “it is the path that data is transmitted on.” *Id.* The specification, too, explains that “there are different transmission lines (data paths) with separate signal transmission lines for transmitting ... data signals and a separate strobe line for transmitting ... strobe signals.” *Id.* Accordingly, the Board agreed with Netlist that the claimed “data path” “corresponds to data signal lines carrying data signals and not to strobe signal lines carrying strobe signals.” Appx24.

The Board considered but rejected Samsung’s contention that the Board’s analysis of the ’035 patent in the 236 IPR precluded adoption of Netlist’s construction. The two patents, the Board found, have materially different claim language. “Claim 1 of the ’035 patent recites ‘each respective buffer circuit including *data paths for transmitting respective data and strobe signals* associated with the first memory operation’”—that is, the claim “explicitly recites that the

data paths have data and strobe signals transmitted on them.” Appx20. “That is unlike claim 1 of the ’608 patent,” which specifies that the claimed data path “correspond[s] to *each data signal line* in the respective set of data/strobe signal lines.” Appx20-21. The Board therefore found that the 236 IPR decision did not inform the meaning of “data path” in the ’608 patent. Appx23. Samsung does not challenge this finding on appeal.

2. The Board rejected the Ground 1 obviousness theory from Samsung’s petition because it defied the claim language. Specifically, many of the components of Hiraishi that Samsung argued were part of the claimed delay circuit “are not in a ‘data path’ as claimed and do not ‘delay a signal through the data path.’” Appx37. For example, DLL circuit 310—as is plain from the figure below and as Samsung’s expert confirmed—is not in the data path (solid orange line); indeed, it is not even in the *strobe* path (hatched orange line). And it does not delay a signal through the data path. Appx40.

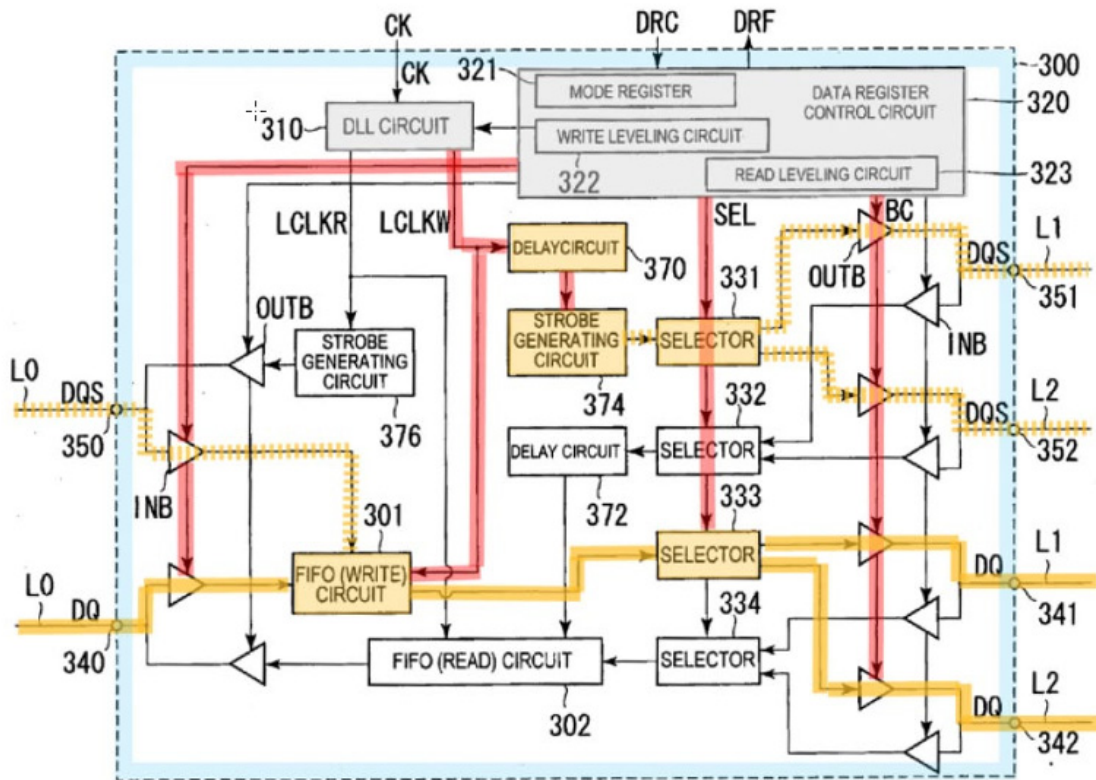


FIG. 5

Appx38. Other components of the alleged delay circuit in Hiraishi—for example, delay circuit 370 and strobe generating circuit 374—are likewise not in the data path and do not delay a signal through the data path. Appx38-43. Accordingly, the Board found that Samsung’s petition “fail[ed] to demonstrate that Hiraishi teaches or suggests the ‘delay circuit’ of claim 1.” Appx42.

3. As for Samsung’s new reply theory—namely, that Hiraishi’s read FIFO circuit and write FIFO circuit comprise the entirety of the claimed “delay circuit” for the read and write direction, respectively—the Board was skeptical that the theory was timely raised. Appx44-46. While petitioners are generally permitted

to respond to “new claim construction issues” raised post-institution, in the Board’s view, this was “a case where the language of claim 1 of the ’608 patent is dispositive.” Appx46. Nonetheless, giving Samsung the benefit of the doubt, the Board considered the “newly-raised” theory. Appx46.

The Board rejected that theory on the merits, agreeing with Netlist that Hiraishi’s FIFOs do not “delay[] a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals,” as required by claim 1. Appx48-68. The Board specifically considered and rejected Samsung’s theory that Hiraishi satisfies this claim requirement because it discloses a “two-step process” in which a “DRC signal” causes Hiraishi to perform “S4 read/write leveling,” which in turn determines and stores a delay that the FIFO circuit uses to retiming the data signal. Appx48-49 (describing Samsung’s argument). Instead, the Board credited Netlist’s arguments that Hiraishi’s write leveling aligns the clock signal and the data strobe signal, Appx56-62, while Hiraishi’s read leveling “adjusts the activation timing of the input buffers and is not related to the FIFO,” Appx64-65.

In making these findings, the Board expressly credited Netlist’s expert Dr. Mangione-Smith. *E.g.*, Appx62. “The parties,” the Board explained, “have different views on how Hiraishi operates,” Appx57—and the Board found Netlist’s and its expert’s view more credible. Appx62. The Board also noted that, because

Samsung had not submitted an expert declaration with its reply brief, there was no “expert testimony in the record” supporting Samsung’s new argument “that only Hiraishi’s FIFO circuits teach the claimed ‘delay circuit.’” Appx49.

The Board also rejected Samsung’s argument that the 236 IPR decision had preclusive effect on this issue. The 236 decision, the Board explained, was not relevant to this question because its findings concerned the function of different components of Hiraishi—namely, the selectors 331-334 and INB/OUTB buffers—none of which Samsung argued were part of the claimed delay circuit. Appx51. In other words, the 236 decision has nothing to say on the question of whether Hiraishi’s FIFOs could qualify as the ’608 patent’s claimed “delay circuit.”

4. The Board then addressed Samsung’s Ground 2 theory, which added “Tokuhiko’s read circuit DR-1” to Hiraishi’s strobe-generating circuit. Appx68-69. Ground 2, the Board concluded, failed because those components do not lie in the claimed “data path.” Appx69-70.

The Board therefore found that none of the challenged claims had been shown unpatentable. Appx72-73.

SUMMARY OF THE ARGUMENT

The Board’s decision should be affirmed.

I. Samsung’s petition failed to show that the prior art discloses a “delay circuit” in the “data path,” as required by the claims.

The claim-construction argument on which Samsung focuses its appeal—that the claimed “data path” should be construed to encompass both data and strobe signals—is both irrelevant and wrong. It is irrelevant because Samsung’s prior art does not disclose the claimed delay circuit even under Samsung’s construction: many of the components collectively comprising the alleged delay circuits in Samsung’s prior-art combinations do not lie in a data path *or* a strobe path. And it is wrong because the intrinsic evidence makes clear that the claimed data path corresponds to data signal lines only. The claim language could hardly be clearer: the “data path” at issue is the “data path corresponding to *each data signal line* in the respective set of data/strobe signal lines.”

The “alternative combination” that Samsung purportedly embedded in Ground 2 of its petition fares no better. As an initial matter, Samsung devoted one conclusory sentence to this “alternative” theory below, which was insufficient to preserve the argument for appeal. In any event, the Board reasonably interpreted the alternative theory to fail for the same reason Samsung’s primary theories failed: Samsung did not show a delay circuit in the claimed data path.

II. The Board relied on substantial evidence in rejecting Samsung's new reply theory that Hiraishi's FIFOs alone constitute the claimed delay circuit.

Collateral estoppel does not apply. As the Board correctly found, the 236 IPR that Samsung invokes involved a patent with materially different claim limitations, which led to different issues being litigated across the two IPRs.

Samsung's assertion that the Board "refused to consider factual preclusion" is false; the Board squarely addressed and correctly rejected every individual estoppel contention Samsung advanced. To the extent the Board did not address some of the estoppel arguments that Samsung makes *on appeal*, that is because Samsung is presenting them for the first time to this Court. Those arguments are therefore forfeited (and they fail on the merits in any event).

Samsung's challenges to the Board's factual findings regarding Hiraishi do not come close to surmounting the substantial-evidence standard of review. The Board expressly credited Netlist's expert's views about how Hiraishi functions. Credibility determinations of that sort are the Board's to make. Moreover, Samsung submitted *no expert testimony whatsoever* in support of its new reply theory involving Hiraishi's FIFOs and instead relied solely on attorney argument. But attorney argument is not evidence, and the record on these issues is therefore one-sided in Netlist's favor. Nor are there any inconsistencies between the findings from the 236 decision and the findings below.

STANDARDS OF REVIEW

Obviousness is a question of law with underlying questions of fact. *Elekta Ltd. v. ZAP Surgical Sys. Inc.*, 81 F.4th 1368, 1373-74 (Fed. Cir. 2023). The Board’s underlying factual findings are reviewed for substantial evidence. *Id.* “Substantial evidence is such relevant evidence as a reasonable mind might accept as adequate to support a conclusion.” *Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1001 (Fed. Cir. 2023) (cleaned up). “The possibility of drawing two inconsistent conclusions from the evidence does not prevent an administrative agency’s finding from being supported by substantial evidence.” *Id.* (citation omitted); *see also Roku, Inc. v. Universal Elecs., Inc.*, 63 F.4th 1319, 1326 (Fed. Cir. 2023). Said differently, “[t]his court does not reweigh evidence on appeal.” *In re NTP, Inc.*, 654 F.3d 1279, 1292 (Fed. Cir. 2011).

Claim construction—if the Court reaches it—“is a question of law that may be based on underlying factual findings.” *Restem, LLC v. Jadi Cell, LLC*, 130 F.4th 941, 944 (Fed. Cir. 2025). This Court “review[s] the Board’s claim construction de novo and any underlying factual findings for substantial evidence.” *Id.*

This Court reviews a lower tribunal’s application of collateral estoppel de novo. *See Ohio Willow Wood Co. v. Alps S., LLC*, 735 F.3d 1333, 1341 (Fed. Cir. 2013). “Whether the differences between the patent claims materially alter the question of patentability” for purposes of collateral estoppel “is a legal conclusion

based on underlying facts.” *Google LLC v. Hammond Dev. Int’l, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022).

The Board’s understanding of arguments raised in the proceedings below is reviewed for abuse of discretion. *See Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330 (Fed. Cir. 2019).

ARGUMENT

Samsung takes a kitchen-sink approach to this appeal, raising a complicated web of arguments with unclear relationships to one another. At bottom, though, Samsung’s appeal arguments fall into two buckets: those made in support of the obviousness theory in Samsung’s *petition* and those made in support of the obviousness theory in Samsung’s *reply*. Samsung’s claim-construction argument (BBr.33-53) and its supposed “alternative” argument based on Tokuhiro (BBr.74-76) fall into the first bucket and are addressed *infra* Section I. Samsung’s collateral-estoppel arguments (scattered throughout Sections III-IV of Samsung’s brief, BBr.53-74) and substantial-evidence arguments (BBr.62-74) fall into the second bucket and are addressed *infra* Section II. All these arguments lack merit.

I. The Court should affirm the Board’s findings that Samsung’s petition failed to show that the prior art discloses a delay circuit in the claimed data path.

Samsung frames its defense of its *petition*’s obviousness arguments as turning on the proper construction of “data path.” According to Samsung, the

claimed “data path corresponding to each data signal line” can accommodate *both* data signals *and* strobe signals. BBr.52-53.

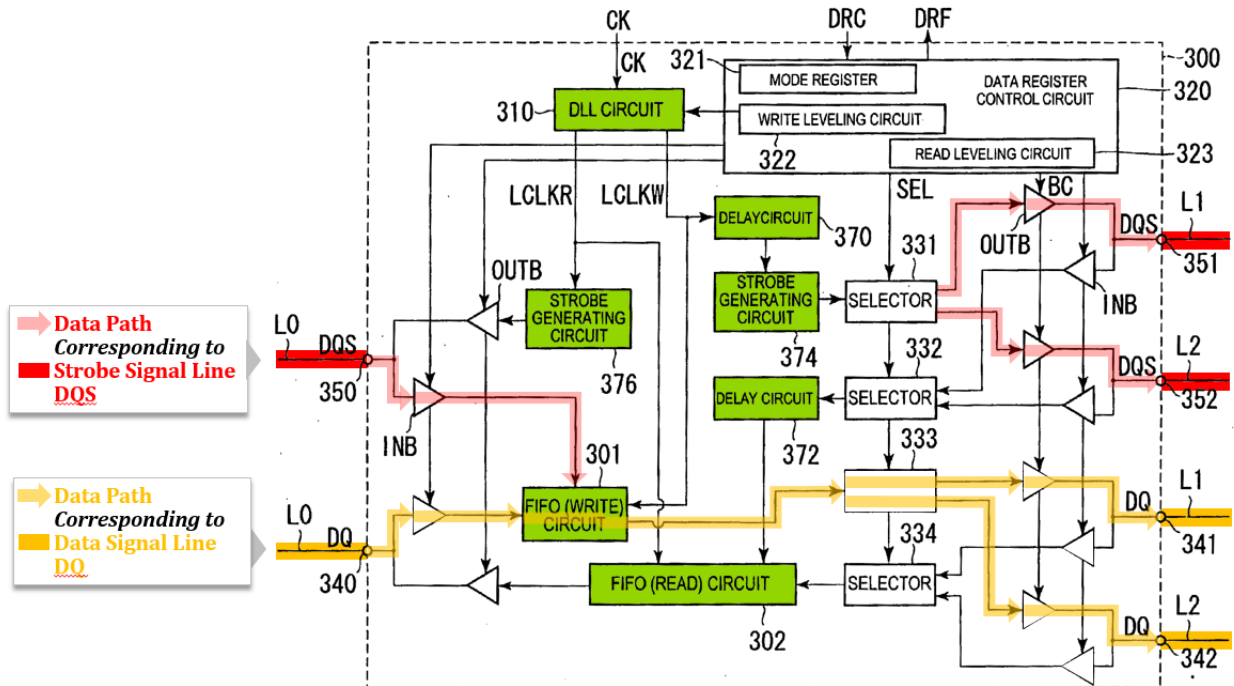
As explained *infra* Section I.B, Samsung’s claim-construction argument defies the claim language and the specification. But the Court need not even reach this argument because the petition’s obviousness theory indisputably fails even under Samsung’s construction. Some of the circuit components in Hiraishi (Ground 1) and Tokuhiko (Ground 2) that Samsung mapped onto the claimed “delay circuit” are not in the data path and do not delay signals “through” that path *even if* “path” is construed to encompass strobe paths. So, regardless of which claim construction is adopted, Samsung loses.

A. The Board’s undisputed factual findings demonstrate that the art does not disclose the required delay circuit under Samsung’s construction of “data path corresponding to each data signal line.”

Claim 1 of the ’608 patent requires that the claimed “data path” “include[] a delay circuit configured to delay a signal through the data path.” Appx117(19:49-54). As Samsung acknowledges, for the data path to “include” a delay circuit that delays signals “through” the path, the “*entire* ‘delay circuit’” must be “included in the data path” (however “data path” is construed). BBr.39 (emphasis added). If any portion of the delay circuit is not in the data path, the claim is not satisfied.

Samsung’s obviousness theories run afoul of that requirement even if “data path” is construed to accommodate strobe signals. The Board’s own findings—findings Samsung does not challenge on appeal—confirm this.

In Ground 1, Samsung pointed to Hiraishi’s “DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376” (green below) as collectively comprising the claimed delay circuit. Samsung’s expert conceded that all these components must “work together to implement the delay circuit.” Appx7018-7019(17:23-18:5). But, as shown below for write operations, some of those components do not lie in a path traversed by *either* data signals (orange arrows) *or* strobe signals (red arrows):

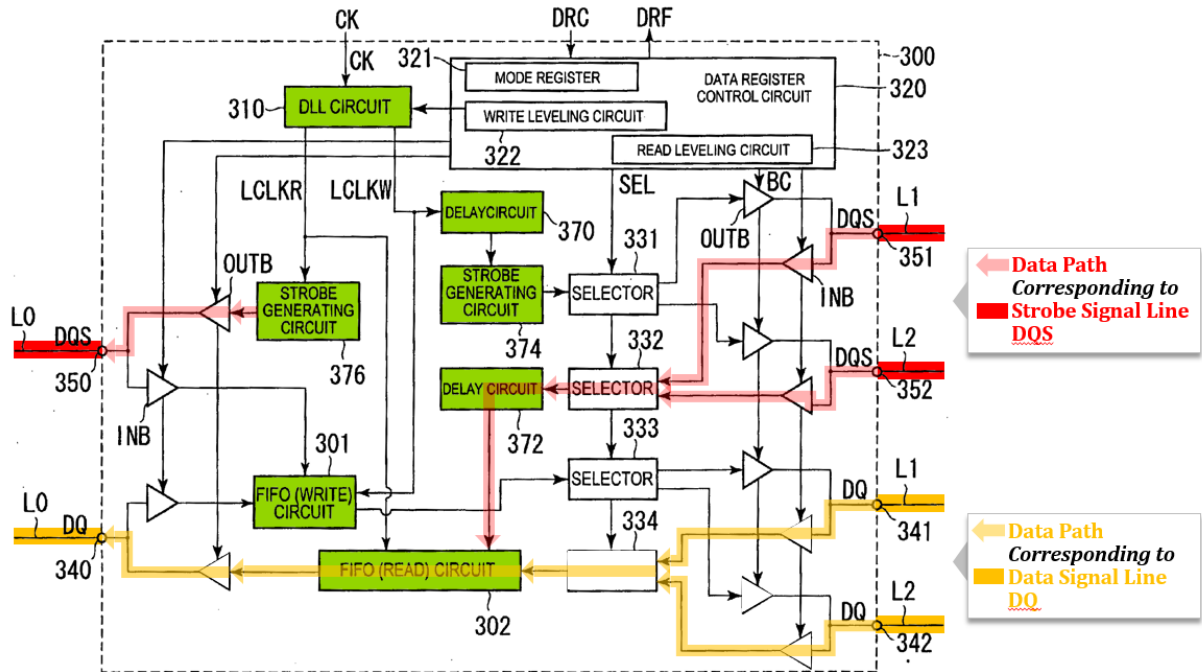


Appx174 (Samsung's petition) (re-annotated).¹

For example, delay circuit 370 receives a local clock signal (LCLKR) and outputs a delayed clock signal. Appx39. Quoting Samsung's expert, the Board found that the clock signals are "not part of the data path" through Hiraishi's data buffer. *Id.* (quoting Appx7042-7043(41:2-5, 42:1-4)). Likewise, the Board found that strobe generating circuit 374 "receives a clock signal, which is not on the 'data path' as mapped by Petitioner[.]" Appx40. Still further, the Board found—again based on Samsung's expert testimony—that Hiraishi's DLL circuit 310 "is not in the 'data path' of claim 1" and "neither the CK signal to DLL circuit [310] nor the LCLKW output are 'a signal through the data path.'" Appx40 (citing Appx7043-7044(42:24-43:1)). Even under Samsung's construction, the clock signals are not part of the claimed data path. Consequently, the components receiving or outputting those signals are not in the data path and do not delay signals through the path, as Samsung concedes is required by the claims.

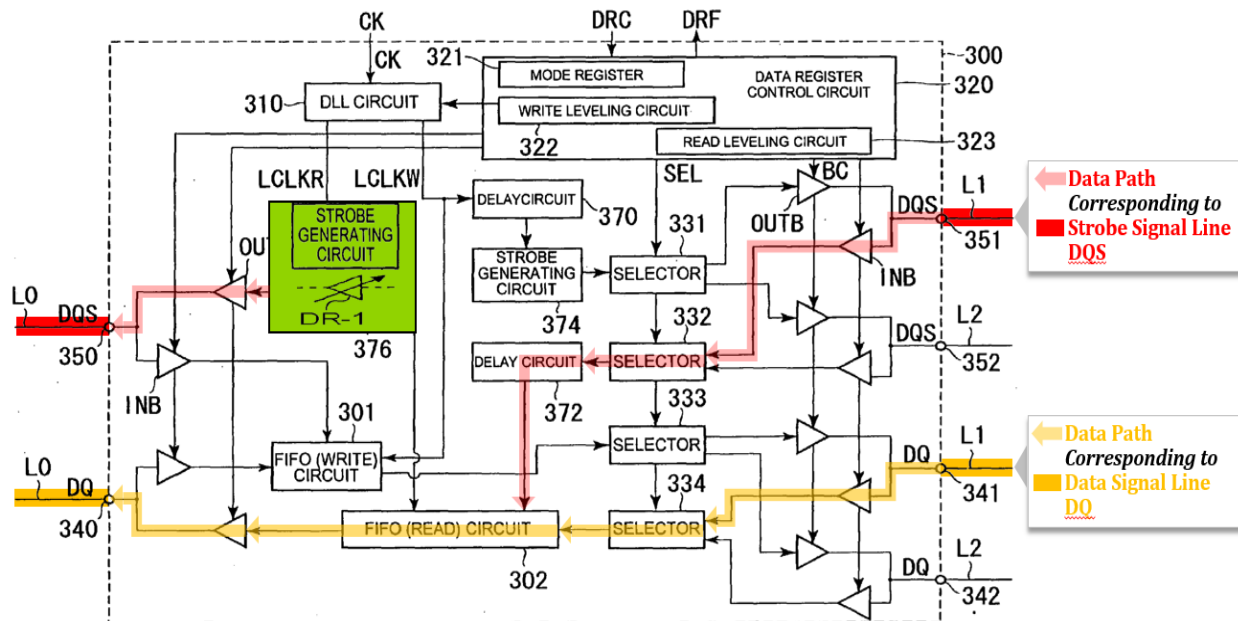
The same is true for Hiraishi's read operations:

¹ Samsung's depictions of its prior-art combinations have been re-annotated to better illustrate the relevant components and disputed issues.



Appx174 (Samsung’s petition) (re-annotated). Once again, delay circuit 370 and DLL circuit 310 are not in a data *or* a strobe path. Appx40. And Hiraishi’s strobe generating circuit 376 receives a *clock signal* as the input, which the Board found “is not on the ‘data path’ as mapped by Petitioner[.]” Appx42. Nor does the strobe generating circuit delay a signal through a data or strobe path; instead, it merely *outputs* a strobe signal (hence the name “strobe generating circuit”). *See id.*

Samsung’s Ground 2 obviousness theory based on Tokuhiko fails under Samsung’s construction for similar reasons. That theory mapped the claimed delay circuit to Tokuhiko’s “delay elements DR1 and DR2,” which Samsung argued would be placed in Hiraishi’s strobe generating circuit 376:



Appx229 (re-annotated); Appx68-70. But, as just explained, the strobe generating circuit 376 does not delay a signal through a data *or* strobe path; rather, it receives a clock signal from outside the data path and then outputs a strobe signal. See Appx69 (citing Appx7296-7297(¶144)); Appx40.

Samsung does not dispute any of these findings on appeal. But they are dispositive. Because certain components comprising Samsung’s alleged “delay circuit” do not lie in the data path *even as Samsung construed it*—and because those components do not delay signals through that path—the “*entire ‘delay circuit’*” is not “included in the data path,” as Samsung concedes is required by the claims. BBr.39 (emphasis added). Thus, the Board’s factual findings compel affirmance even under Samsung’s construction. See *HD Silicon Sols. LLC v. Microchip Tech. Inc.*, 127 F.4th 919, 923-24 (Fed. Cir. 2025) (affirming Board’s

findings as “equally supported” based on the record evidence even though “the Board erred in construing” a key claim term). The Court can end its analysis of the petition’s theory there.

B. In any event, the Board’s claim construction is correct.

Samsung’s claim-construction arguments also fail on the merits. The Board properly construed “data path corresponding to ... each data signal line” as requiring the claimed path to accommodate only data signals. That construction comports with the claim language, which makes clear that the data path “correspond[s] to” the *data* signal line, not some other signal line. And the specification supports that plain reading.

1. The Board correctly construed “data path corresponding to ... each data signal line” as requiring the path to accommodate only data signals.

a. The full claim language goes a long way toward resolving this dispute. Claim 1 recites in relevant part:

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and *a plurality of sets of data/strobe signal lines*, the memory module comprising:

....

a plurality of buffer circuits ... ,

[e] the each respective buffer circuit including *a data path corresponding to each data signal line in the respective set of data/strobe signal lines, ... ,*

[f] wherein *the data path corresponding to the each data signal line includes ... a delay circuit configured to delay a signal through the data path* by an amount determined by the command processing circuit in response to at least one of the module control signals.

Appx117(19:43-55) (emphases added). As shown, the claimed “buffer circuit includ[es] a data path corresponding to each data signal line in the respective set of data/strobe signal lines.” All agree that a “data signal line” refers to a signal line outside the buffer that accommodates *only* data signals, in contrast to a “strobe signal line,” which is separately claimed and accommodates *only* strobe signals. BBr.50 (“[T]he data and strobe signals will travel on different lines.”); Appx7053(52:8-17); Appx7055(54:3-7) (Samsung’s expert agreeing that strobe signals do not “travel over DQ [i.e., data] signal lines”); Appx7248-7249(¶70) (Netlist’s expert testifying that “a data signal line is different from a strobe signal line”); *see* Appx17 (Board noting that claim 1 “differentiates between data signal lines and strobe signal lines”); Appx18 (Board noting that data signal lines “carry data signals only”).

And, importantly, claim 1 singles out *only* data signal lines from among the “set of data/strobe signal lines” as “corresponding to” the claimed data paths within the buffer. The phrase “corresponding to,” in turn, indicates that there is a

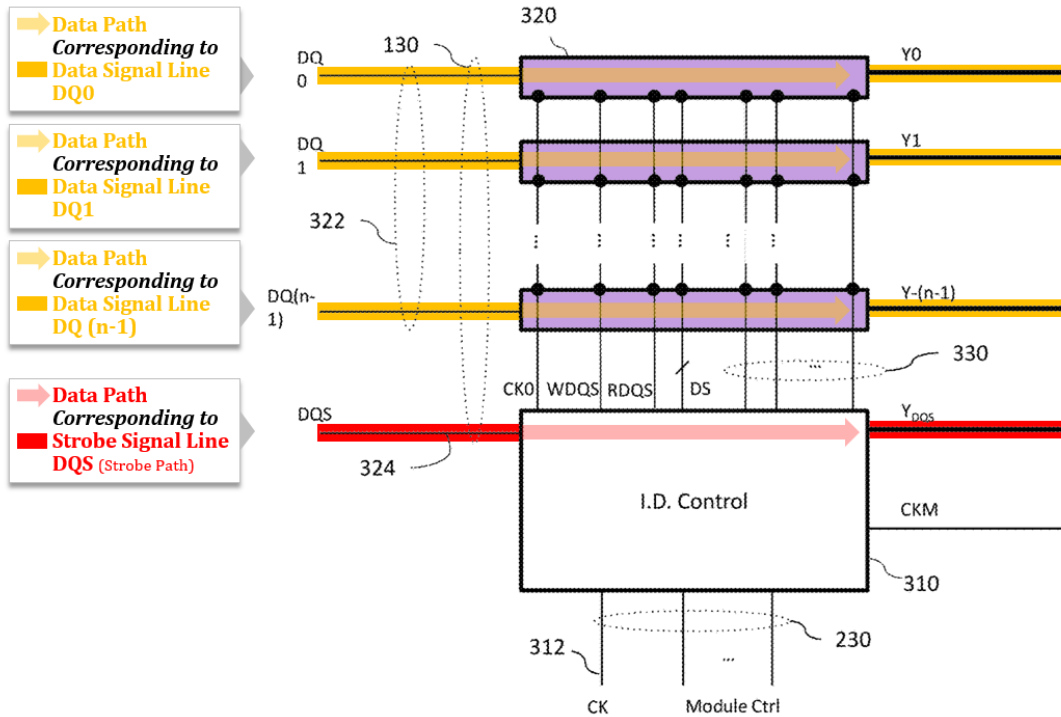
correspondence between the data path and signal line—i.e., the data path is the route that data signals travel from a data signal line on one side of the buffer to a data signal line on the other side of the buffer. It follows that the claimed data path accommodates *only* data signals, not strobe (or some other) signals. Appx24. The data path, moreover, must “include” the claimed delay circuit. And, because only data signals traverse the data path, the delay circuit must be configured to delay data signals—not strobe signals—through the path. Appx6941-6942; Appx16-19; Appx40.²

In short, the claim language plainly specifies that the “data paths” of interest are those on which the corresponding *data* signals travel.

b. The specification likewise supports the Board’s construction.

Figure 3, for example, shows separate paths for data signals (orange) and strobe signals (red) through a buffer circuit 118:

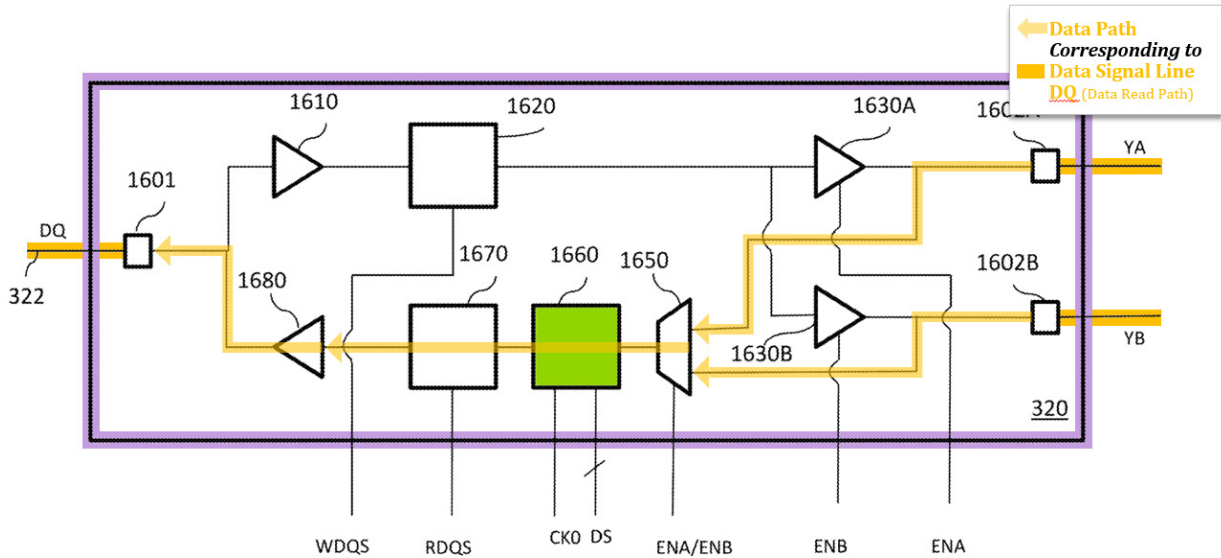
² Consider, by analogy, a highway and a train track that run side-by-side and go through a mountain via tunnels. The tunnel includes a path corresponding to the road, which would accommodate only cars, and a path corresponding to the train tracks, which would accommodate only trains. If one specified that the path through the tunnel “corresponding to the road” includes a speed bump, it would be clear that the speed bump delays only the cars, not the trains. Just so with the claims: the delay circuit is in the path through the buffer circuit that corresponds to the data signal line, so it delays data signals, not some other type of signal.



Appx87(Fig. 3) (annotated); Appx109(3:27-29, 4:30); see Appx88-89(Figs. 4A-4B); Appx91(Fig. 6); Appx6935-6936; Appx9797-9798; Appx7248-7250(¶¶70-72). In particular, the buffer circuit connects to various “sets” of signal lines 130. Appx112(10:31-35). There are multiple “data (DQ) signal lines 322” that carry “data signals,” and at least one “strobe (DQS) signal line 324” that carries “strobe signal DQS.” *Id.* The paths traversed by data signals are *different* from the path traversed by the associated strobe signals. Thus, as the Board noted, Figure 3 “confirms” what claim 1’s plain language makes clear—the “data path” within the buffer circuit corresponding to the data signal line does not accommodate strobe signals. Appx17-18.

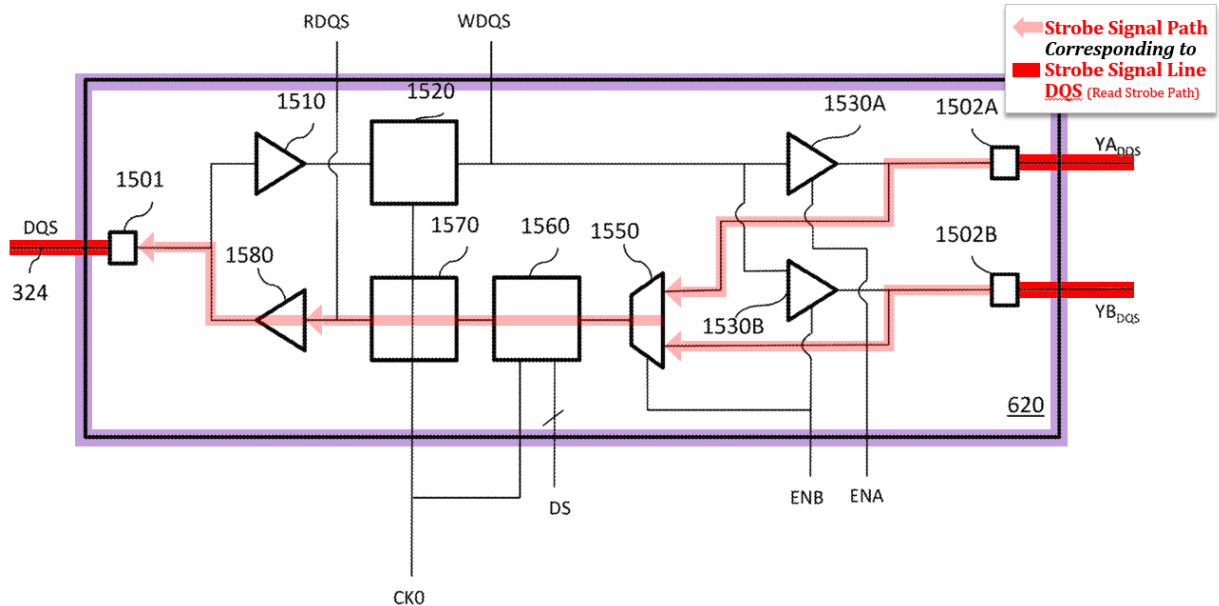
Other figures likewise distinguish between data paths and strobe paths.

Figure 16, for example, depicts data paths within a data routing circuit 320 (purple, which is a component of the buffer circuit shown in Figure 3):



Appx104(Fig. 16) (annotated). The figure depicts a data signal line (DQ) 322 (orange) carrying data signals to the routing circuit. Appx116(17:56-60). The patent describes the data signal line as corresponding to a “read data path” (orange arrows) that connects one end of the routing circuit to the other and that runs through claimed delay circuit 1660 (green). Appx116(17:48-54); *see also* Appx116(17:23-33) (referring to a first and second “write data path” in the same circuit). In other words, the data path that includes the delay circuit is the path through the buffer on which data signals travel. Appx6937-6938; Appx6941-6942; Appx7252-7253(¶¶75-76); Appx7257-7258(¶82).

Strobe signals, by contrast, travel along their *own, separate paths*. Figure 15 shows a routing circuit that accommodates strobe signals:



Appx103(Fig. 15) (annotated). The figure depicts a strobe signal line (DQS) 324 (red), which the patent refers to as corresponding to a “read strobe path” (red arrows). Appx116(17:8-15); *see also* Appx115(16:47-57) (referring to a first and second “write strobe path” in the same circuit); Appx7250-7251(¶¶73-74). As the Board concluded, these figures “support that there are separate data paths for data signals and for strobe signals.” Appx19; Appx7253(¶77).

In short, if there were any ambiguity in the claim language (there is not), the specification resolves it in Netlist’s favor.

2. Samsung’s claim-construction arguments fail.

Rejecting a plain reading of claim 1, Samsung argues that the claim permits

the data path to include both data signal lines and strobe signal lines. That construction is wrong for multiple reasons. Indeed, it reads the disputed limitation out of the claim altogether.

a. Samsung improperly conflates the claimed “data path corresponding to each data signal line” with any “data path.”

A major premise of Samsung’s argument is that the term “data path,” in general, “is broad enough to have different types of signals traversing through it, including data signals and strobe signals.” BBr.38, 45. This misses the point. A path can, in the abstract, accommodate different types of signals and lines (as claim 10 shows, *see infra* Section I.B.2.c). But the path recited in claim 1 is narrower in scope: it must “*correspond[] to a data signal line*” from among a “set of data/strobe signal lines.” Appx117(19:43-45). That added specificity matters—while not “all data paths [must] exclude strobe signals,” BBr.51, the specific “data path” recited in claim 1 does.

Samsung’s construction effectively reads out the phrase “corresponding to each data signal line in the respective set of data/strobe signal lines.” But it is legally impermissible to “rewrite claims” that way. *Taurus IP, LLC v. DaimlerChrysler Corp.*, 726 F.3d 1306, 1321 (Fed. Cir. 2013); *see Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”

(citation omitted)).

Samsung also argues that the claim recites a single data path corresponding to “*each* data signal line,” meaning the path can include multiple lines (i.e., data signal lines and strobe signal lines). BBr.38-39 (emphasis added). But this again misreads the claim, which recites a “data path corresponding to the each data signal line.” Appx117(19:49-50). That is, each data signal line has a corresponding data path. And, again, regardless of whether a data path, in the abstract, can include multiple signal lines, the data path of claim 1 “corresponds to” only a *data* signal line. Thus, when the claim states that “a signal” is delayed through the data path, it is referring to the specific type of signal traversing the data path “corresponding to” the data signal line—a data signal. *Contra* BBr.38.

In sum, the premise on which Samsung’s entire claim-construction argument is built is flawed. Without that premise, Samsung’s argument crumbles.

b. Samsung misinterprets the phrase “corresponding to” in isolation to give it no effect in the claim.

Samsung’s remaining arguments also fail. Fixating on a couple sentences of the Board’s analysis in isolation, for example, Samsung contends that the Board improperly “equat[ed]” the phrase “corresponding to” with “is in.” BBr.35-36 (citing Appx17-18). In Samsung’s telling, “corresponding to” is broader in scope and “encompasses two things that are ‘functionally related to one another,’” such

as a data signal and its associated strobe signal. BBr.35-36. Samsung is wrong.

As an initial matter, Samsung twists the Board's words to make it seem as though the Board concluded that the claimed data path must literally be "in" (i.e., "confined to") a physical data signal line. Appx17-18. But in context, it is clear that the Board used the word "in" to convey that the claimed data path accommodates data signals that travel through the buffer from one data signal line to another. Stated differently, the claimed data path "is the path that data is transmitted on." Appx17. Regardless of whether one uses the word "in" or "on," the Board's conclusion is the same: the claimed data path is the path on which the data signals from data signal lines travel through the buffer.³

Nor did the Board equate "data path" with "data signal line." See Appx17-18; *contra* BBr.37-38. Rather, the Board determined that the data path must "correspond[] to" the data signal line, exactly as the plain language of claim 1 requires and as Samsung's own case makes clear. See *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013) ("Indeed the claim does not use language of equation but of correspondence[.]"). Specifically, the "data path" is the path on which data travels through the buffer, and it "corresponds to" the physical

³ With that understanding in mind, the mere fact that the claimed delay circuit is "in" the data path does not in any way undermine the Board's statement that the data path is in the data signal line. *Contra* BBr.39.

data signal lines that carry the data to and from the buffer. Appx17-18; *see* Appx116(17:48-50). Samsung may think that this distinction is not “meaningful,” BBr.50, but the claim must be interpreted based on how it is written, not on what Samsung thinks it should mean. *Rembrandt Data Techs., LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011).

Further, Samsung’s construction of “corresponding to” as meaning merely “functionally related to” makes no sense in the context of the ’608 patent claims. *IGT v. Bally Gaming Int’l, Inc.*, 659 F.3d 1109, 1117 (Fed. Cir. 2011) (“Extracting a single word from a claim divorced from the surrounding limitations can lead construction astray.”). Samsung cites (at 36) *Respironics, Inc. v. Invacare Corp.*, 303 F. App’x 865 (Fed. Cir. 2008), but the claims there were very different. They recited “outputting a signal corresponding to” the flow rate or volume of breathing gas in a CPAP machine. *Id.* at 880-81. In that context, the Court determined that “corresponding to” means “functionally related” since “the magnitude of the outputted signal varies *as a function of* the magnitude of the sensed flow rate or volume.” *Id.* at 881. That meaning does not fit in claim 1 of the ’608 patent, which describes the conceptual relationship between a data path and data signal line, not a mathematical relationship between two measurable quantities. In short, the Board

correctly read claim 1 exactly as it is written.⁴

c. Samsung misreads dependent claim 10.

Samsung next turns to claim 10 (disclaimed during the IPR, Appx6126), which indirectly depended from claim 1. The claim recites “a first data path for transmitting a strobe signal” and “a second data path for transmitting a ... data signal.” Appx117(20:49-51). According to Samsung, the claim’s reference to a data path “for transmitting a strobe signal” proves that the data path in claim 1 can also transmit a strobe signal. BBr.43.

Not so. Claim 10 refers to “*a* first data path”—that is, an additional data path, not “*the* data path” recited in claim 1. It is *that* additional path that accommodates strobe signals, as the Board found. Appx18. That claim 10 adds a data path for accommodating strobe signals has no bearing on whether the data path *in claim 1* also accommodates strobe signals. As explained above, it does not. Appx9799; Appx7253-7254(¶78).

For this reason, Samsung’s cited cases are inapposite. They involved a dependent claim narrowing the scope of a limitation recited in the independent claim, where the lower tribunal’s construction ignoring that difference effectively

⁴ Samsung’s interpretation of claim 1 raises more questions than it answers. What would it mean for a path and signal line to be “functionally related”? How related must they be to satisfy the claim? Samsung does not say.

gave the dependent claim “no scope” or artificially narrowed the scope of the independent claim. *Littelfuse, Inc. v. Mersen USA EP Corp.*, 29 F.4th 1376, 1380 (Fed. Cir. 2022); *see also Samsung Elecs. Co. v. Power2B, Inc.*, 2025 WL 471124, at *4 (Fed. Cir. 2025). The Board’s construction here gives the claims sufficient scope: claim 10 covers two data paths beyond the data path recited in claim 1, one for transmitting data signals and one for transmitting strobe signals.

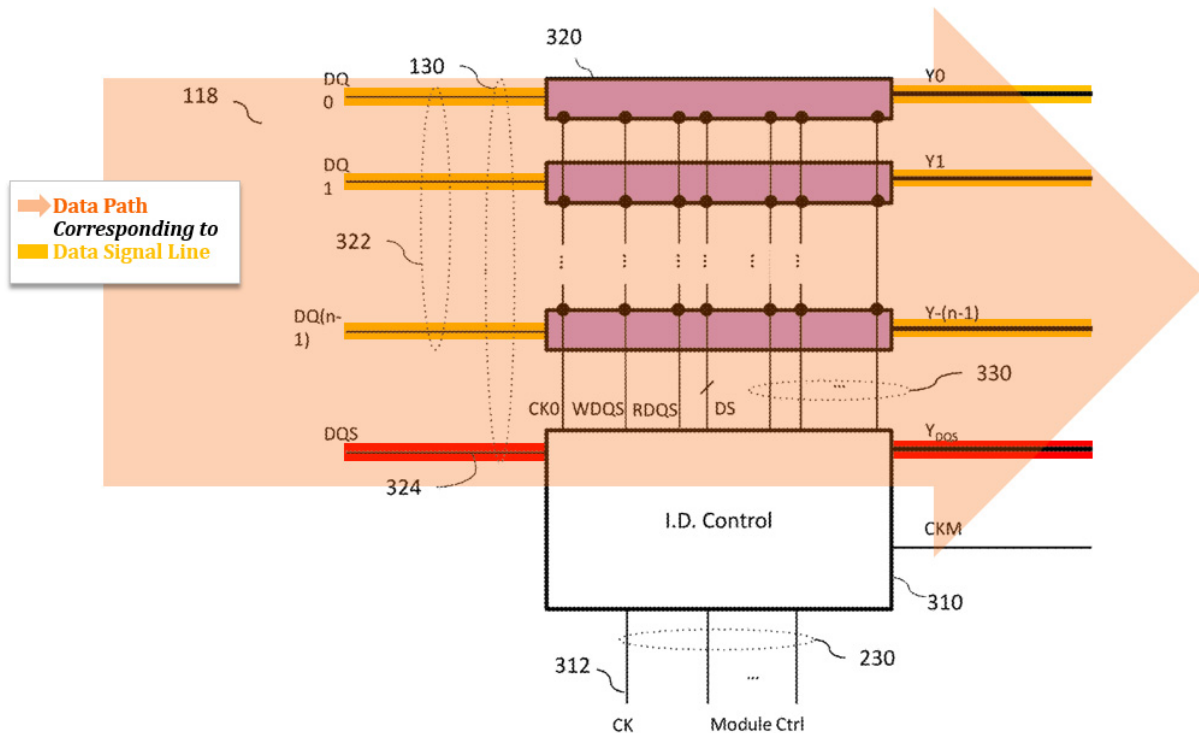
Samsung offers a tortured reading of the claims to salvage its argument. According to Samsung, the “first” and “second” data paths in claim 10 do not refer to *additional* paths but rather to a *subset* of the data path of claim 1. BBr.45-46. Under this reading of the claims, the data path in claim 1 could accommodate both data and strobe signals, which traverse the first and second data paths in claim 10, respectively.

That is an implausible interpretation. If that were the inventors’ intent, they could have drafted claim 10 to specify that “*the data path includes a first and second data path*, wherein the first data path transmits a strobe signal ... and the second data path transmits a first data signal.” Samsung impermissibly “read[s] language into the claim that is simply not there.” *Uniloc 2017 LLC. v. Netflix, Inc.*, 2022 WL 17688150, at *3 (Fed. Cir. 2022).

d. Samsung misinterprets the specification by assuming the very construction it purports to prove.

Samsung tries in vain to find support for its construction in the specification.

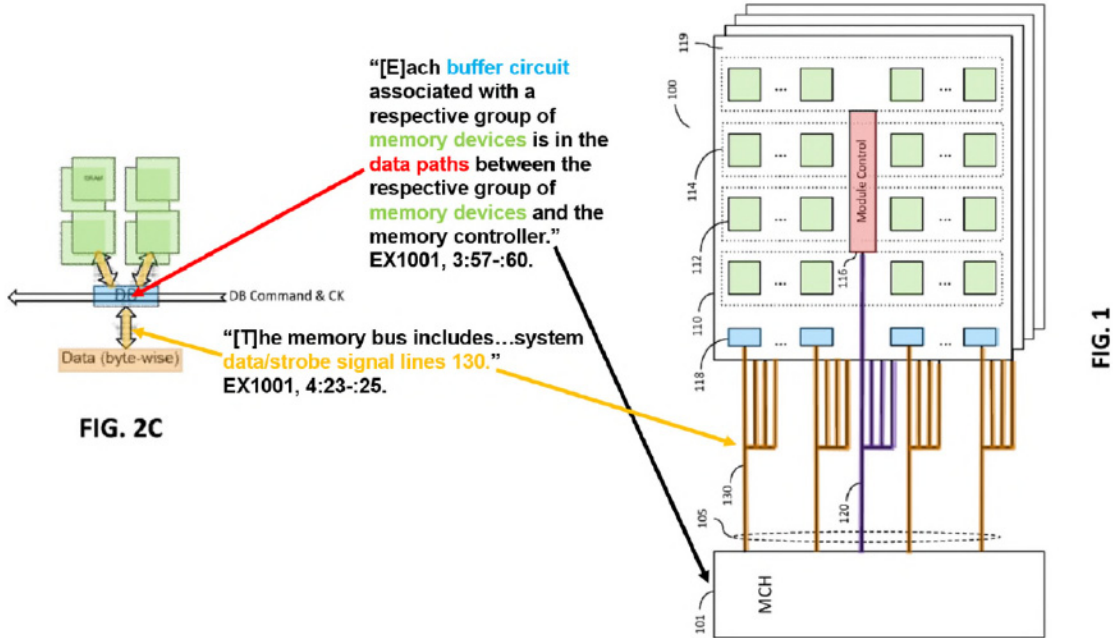
Pointing to Figure 3, Samsung argues that, because the buffer circuit 118 is coupled to both data and strobe signal lines, the data path through the buffer circuit must correspond to both types of signals:



BBr.47-48 (citing Appx87) (annotated). But that argument flips Figure 3 on its head. The figure does not show a single path traversed by *both* data signals and strobe signals. It shows multiple paths—one corresponding to each data signal line—traversed *only* by data signals and a separate path traversed *only* by strobe signals. See *supra* pp.33-34.

Samsung next faults the Board for its reliance on Figures 15 and 16. BBr.51. Samsung argues that the figures' use of the phrases "data path" (in Figure 15) and "strobe path" (in Figure 16) "does not require all data paths to exclude strobe signals." *Id.* Once again, while not all data paths exclude strobe signals, the data path "corresponding to the data signal line" recited in claim 1 does. Indeed, Figure 15 shows such a "data path," and Figure 16 shows that strobe signals do not traverse that path. *See supra* p.35-36. The Board did not "limit" claim 1 to this embodiment, as Samsung contends (at 51), but instead interpreted the claim consistent with the embodiments described in the patent.

Samsung's reliance on Figures 1 and 2C, BBr.46-48, is likewise misplaced. Samsung argues that the buffer circuit (blue) is "*in* the data path" but that the figures show the "data/strobe signal lines 130" (orange) *outside* the buffer circuit, meaning the data path cannot be "*in*" the data signal line:



BBr.46; Appx82(Fig. 1); Appx85(Fig. 2C); Appx109(3:57-60). As an initial matter, this argument is based on the faulty premise that the Board found that the data path must be literally “in” the signal line. *See supra* pp.38-39. More fundamentally, that the data and strobe signal lines are outside the buffer says nothing about the question here: which path inside the buffer “correspond[s] to each data signal line in the respective set of data/strobe signal lines”? It is, of course, the path through which the data signals *from the data signal line* travel—not the path through which strobe signals travel. That is exactly what the Board found. Appx24.

e. Samsung’s extrinsic evidence does not support Samsung’s construction and, in any event, cannot supplant the intrinsic record.

Finally, Samsung argues that the Board ignored extrinsic evidence indicating that data signals and strobe signals must “travel together within a very tight tolerance.” BBr.40-43; *see also id.* at 1, 5, 7, 37, 39, 49-50, 67. Samsung’s resort to extrinsic evidence is misplaced given the clarity of the intrinsic record. *See Immunex Corp. v. Sanofi-Aventis U.S. LLC*, 977 F.3d 1212, 1221 (Fed. Cir. 2020). In any event, this “tight tolerance” requirement does not support Samsung’s construction.

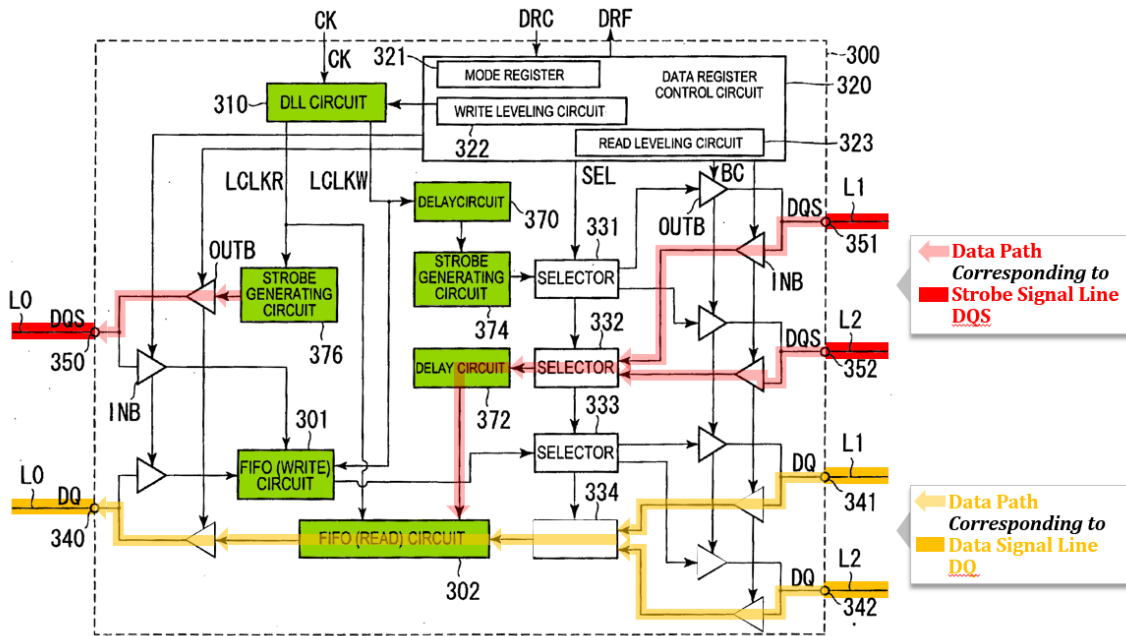
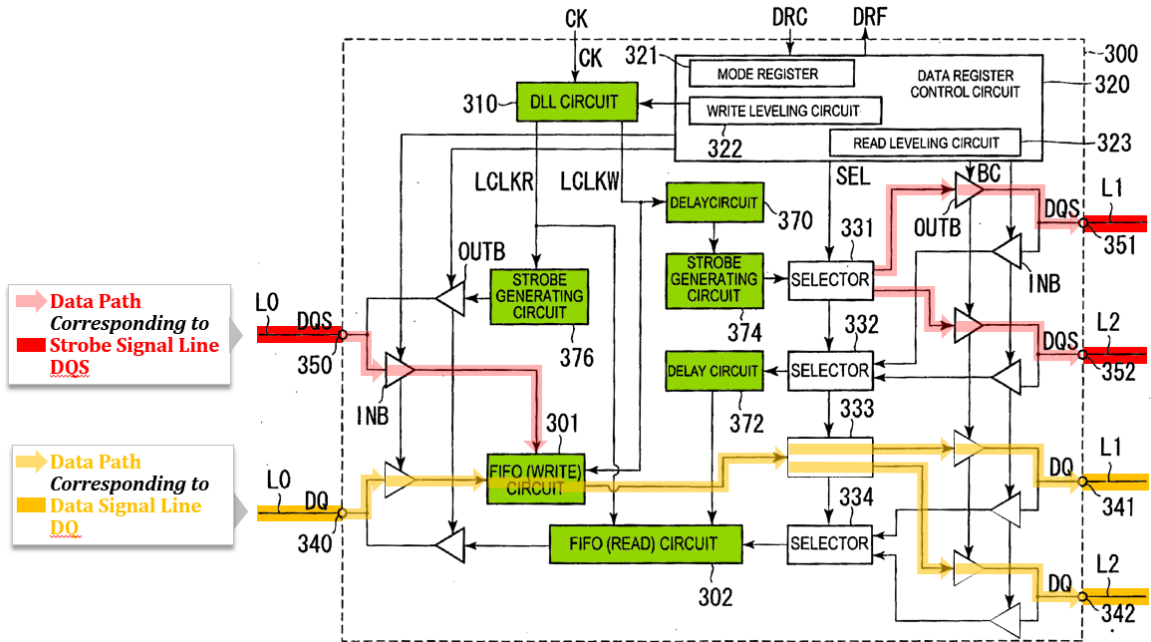
The Board itself made this point when it observed that, regardless of the correlation between data and strobe signals, the fact remains that they “travel on different transmission lines.” Appx19; Appx7055(54:3-12); *contra* BBr.42 (incorrectly stating that the Board “ignored this evidence”). A strobe signal is a synchronization signal that tells a receiving circuit to sample the data being transmitted. By temporally synchronizing the signals, the system ensures “accurate timing for sampling/capturing DQ data.” Appx10479 (quoting Appx6921). But that tight *temporal* tolerance requirement has nothing to do with the *path* the signals traverse. Appx19; Appx7055(54:3-12). (Consider by analogy a group of fighter jets in a tight formation—each one still travels along its own path.) Indeed, before DDR modules, data signals were aligned with clock signals. Appx7056(55:2-16).

But clock signals need not traverse the same path as data signals. The Board’s findings on this score are supported by more than substantial evidence. *See Restem*, 130 F.4th at 944.

Further, Samsung’s argument is in tension with itself. If, as Samsung argues, the only way to achieve “tight tolerance” is for the data and strobe signals to travel on the same path, then claim 1 would *exclude* embodiments in which the signals travel along *different* paths. But Samsung does not argue that such embodiments should be excluded from the claim scope. Rather, Samsung simply argues that claim 1 “is not limited” to such embodiments. BBr.36-37. That Samsung’s argument about the extrinsic evidence conflicts with its own construction demonstrates that the evidence does not actually aid Samsung’s cause.

C. Samsung does not dispute that its petition’s theories fail under the Board’s claim construction.

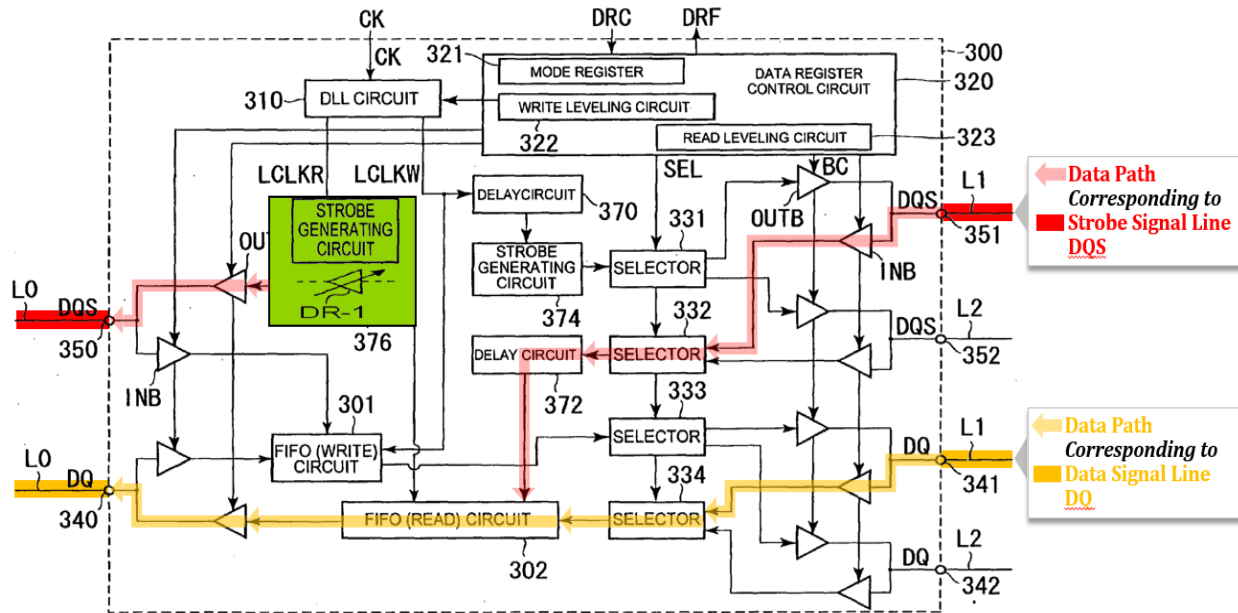
Samsung does not dispute that its petition’s obviousness theories fail under the Board’s construction of “data path corresponding to ... each data signal line.” *See* BBr.52-53. Nor could it. As the Board found, *see* Appx31-45, most of the components in Hiraishi that Samsung’s petition mapped onto the claimed “delay circuit” (green) in Ground 1, *see* Appx179, are not in the claimed data path (orange arrows).



Appx174 (re-annotated).

Samsung’s Ground 2 theory of obviousness based on Tokuhiko also fails under the Board’s construction. There, the claimed delay circuit is mapped onto Tokuhiko’s “delay elements DR1 and DR2,” which Samsung argued would be

placed in Hiraishi’s strobe generating circuit 376. But the strobe generating circuit is also not in the claimed data path under the Board’s construction:



Appx229 (re-annotated); Appx68-70.

D. Samsung’s “alternative” Ground 2 theory based on Tokuhiko likewise fails.

Trying to salvage its petition arguments, Samsung contends (at 74-76) that the Board purportedly “ignore[d]” an “alternative combination” embedded within Ground 2. In Samsung’s telling, it contended below that a skilled artisan would use “delay elements similar to Tokuhiko’s DR elements ... instead of Hiraishi’s FIFO circuit” and that these delay elements would constitute the *entire delay circuit*.

BBr.75. This “alternative” obviousness theory, Samsung asserts, would satisfy the

Board’s construction of “data path” because “Tokuhiko’s delay circuit would be physically on [Hiraishi’s] DQ data line.” *Id.*

Samsung’s appellate argument is flawed on multiple levels. Samsung forfeited its alternative Ground 2 theory by failing to develop it sufficiently below. And, in any event, the Board did not abuse its discretion in interpreting this alternative argument to fail for all the same reasons that the other arguments failed.

1. Samsung forfeited reliance on its alternative theory by failing to develop it below.

Samsung has not preserved its “alternative” Ground 2 theory for appeal. Samsung’s explanation of this “alternative” comprised one sentence of a 114-page petition. That sentence is reproduced below in italics, along with the paragraph in which it appears and the accompanying figure:

In [Ground 2], Tokuhiko’s read delay functionality (DR-1, purple) is added to Hiraishi’s data buffer to remove large fly-by delays. Based on Tokuhiko’s teachings, the read delay circuit DR-1 (purple) is added to the Strobe Generating Circuit 376 to delay both the strobe signal DQS 350 and the signal clocking out data from FIFO (Read) Circuit 302 so that the delayed data DQ 340 from the Read FIFO is in sync with the delayed strobe 350. *Alternatively, delay elements similar to Tokuhiko’s DR elements can be used instead of (or in addition to) Hiraishi’s FIFO circuit for delaying the read data.*

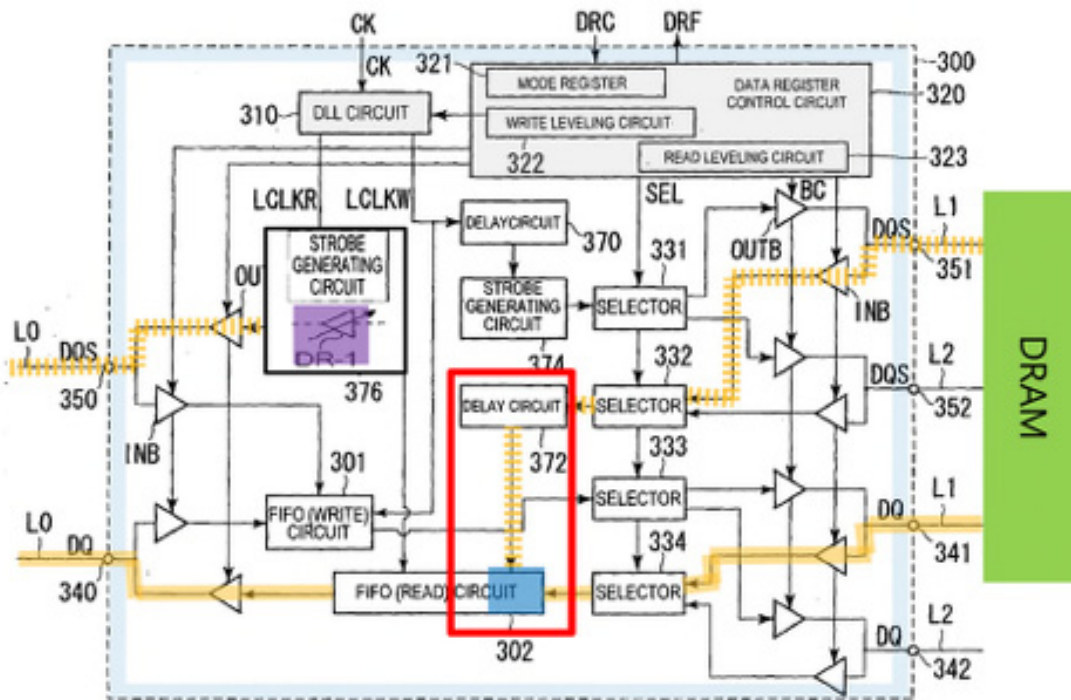


FIG.5

Appx229-230 (citations omitted). In support of the italicized sentence, Samsung cited a paragraph of its expert's declaration that parrots the sentence nearly verbatim (without additional explanation). *See* Appx784-785(¶262) (“A Skilled Artisan would have also understood that, in alternative implementations, delay elements similar to Tokuhiro’s DR elements can be used instead of or in addition to Hiraishi’s FIFO circuit for delaying the read data.”).

Samsung did not elaborate on this “alternative” argument in reply. It accused Netlist of “ignor[ing] the alternative combination for Ground 2” but did not further describe the combination or explain why it would disclose the claimed “delay circuit” under *either* party’s construction of “data path.” Appx10502.

That “skeletal [and] underdeveloped argument”—supported only by equally conclusory expert testimony—is insufficient to preserve the issue for appeal. *Fresenius USA, Inc. v. Baxter Int’l, Inc.*, 582 F.3d 1288, 1296 (Fed. Cir. 2009); *see TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (“conclusory expert testimony is inadequate to support an obviousness determination on substantial evidence review”). Based on the single sentence Samsung provided, it is anyone’s guess what, precisely, would constitute the alleged “delay circuit” in this “alternative”—meaning it is impossible to know whether that delay circuit is in the claimed “data path.” The sentence certainly does not suggest—as Samsung now says it was intended to, *see, e.g.*, BBr.28, 75—that the *entire* delay circuit in this alternative theory would lie within the footprint of Hiraishi’s FIFO (read) circuit. *Cf. Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“A petitioner may not rely on a vague, generic, and/or meandering petition and later fault the Board for failing to understand what the petition really meant.”).

Samsung’s appellate argument is thus forfeited. *See Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1074 (Fed. Cir. 2017) (finding forfeiture where appellant “did not present to the Board the full argument that it present[ed] on appeal”); *Broadcom Corp. v. Int’l Trade Comm’n*, 542 F.3d 894, 901 (Fed. Cir. 2008) (similar).

2. The Board did not abuse its discretion in interpreting Samsung’s “alternative” theory as failing for the same reasons that Samsung’s other theories failed.

In any event, the Board’s treatment of Samsung’s alternative theory, *see* Appx68-70, was more than adequate.

To the extent the petition’s description of the alternative theory can be deciphered, it suggests that, even in this “alternative” arrangement, the strobe generating circuit would be part of the alleged “delay circuit,” and the signals being delayed would be *strobe signals and signals clocking out data*, not data signals themselves. The petition’s statement that delay elements can be used “in addition to[] Hiraishi’s FIFO circuit,” Appx230 reinforces this interpretation of the alternative combination.⁵ That is how Netlist and the Board interpreted the theory below. *See* Appx69-70; Appx9815-9816. And the Board was well within its discretion to interpret the theory this way. *See Netflix*, 84 F.4th at 1377 (“The Board is entitled to discretion in how it interprets petitions.”); *Microsoft Corp. v. Enfish, LLC*, 662 F. App’x 981, 989 (Fed. Cir. 2016) (holding that “[t]he Board reasonably interpreted” the petition as arguing that two features of a prior-art reference collectively disclosed the limitations in question, “even if that [was] not the only possible reading” of the petition, and noting that if the petitioner meant to

⁵ Samsung’s brief omits the “in addition to” language via ellipsis. BBr.75.

argue that a single feature disclosed the limitations, “it should have done so with greater clarity”). Reading the passage this way makes sense, moreover, because Samsung argued its petition *exclusively* under its incorrect construction. Samsung had no reason in its petition to argue that the entirety of its alleged delay circuit would lie in the path of the data signal line, because at that time it (mistakenly) believed the claims imposed no such requirement.

But mapping the claimed delay circuit to include Hiraishi’s strobe generating circuit does not work under *either* Samsung’s construction (*see supra* Section I.A) *or* the Board’s construction (*see supra* Section I.C). The Board’s finding that Samsung’s Ground 2 theory fails to disclose a delay circuit in the data path, as required by the claims, *see* Appx68-70, is therefore well-supported.

To the extent Samsung wishes the Board had done more, it has only itself to blame. This Court does not “find fault in the Board’s arguably limited treatment of ... arguments” if the Board’s treatment is “commensurate with [a party’s presentation of those issues to the Board.” *Novartis AG v. Torrent Pharms. Ltd.*, 853 F.3d 1316, 1327-28 (Fed. Cir. 2017); *accord Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 905 (Fed. Cir. 2018). “[I]t is the petitioner’s burden to make clear when alternative arguments are being presented and to sufficiently expound on each one.” *Netflix*, 84 F.4th at 1380. Having chosen to devote one conclusory

sentence to its “alternative” Ground 2 theory, Samsung can hardly complain about the Board’s limited treatment of it.

* * *

In sum, both of the obviousness grounds in Samsung’s petition—including the under-developed “alternative” theory embedded within Ground 2—fail under any plausible interpretation of the claims. So the only thing left of Samsung’s appeal is the obviousness theory made for the first time in reply. But that theory fails too, as discussed below.

II. The Court should affirm the Board’s finding that Samsung’s new reply theories likewise failed to show that the prior art discloses a delay circuit in the claimed data path.

The obviousness theories that Samsung proffered for the first time in its petitioner’s reply also fail. The reply—in stark contrast to Samsung’s petition—argued that Hiraishi’s FIFOs *alone* constitute the claimed delay circuit. The Board rejected this theory on the facts, concluding that Samsung’s new interpretation of Hiraishi was not supported by the evidence and finding Netlist’s expert’s contrary testimony regarding the operation of Hiraishi credible. Indeed, the new theory was contradicted by Samsung’s own expert, who conceded that *multiple* Hiraishi components were required to comprise the claimed delay circuit. Appx49.

Perhaps recognizing that it cannot surmount the demanding substantial-evidence standard, Samsung casts most of its challenges to the Board’s findings as

collateral-estoppel arguments based on the 236 IPR. To follow the structure of Samsung’s brief, we first explain *infra* Section II.A why Samsung’s generic collateral-estoppel arguments (BBr.53-62) fail, and additionally point out that the collateral-estoppel arguments on specific factual points sprinkled throughout BBr.62-74 were not preserved for appeal. We then explain *infra* Section II.B why the Board’s findings on the points raised at BBr.62-74 are supported by substantial evidence and (even setting aside Samsung’s forfeiture) consistent with the 236 IPR findings.

A. Collateral estoppel does not apply.

The Board did not err in declining to apply collateral estoppel based on the 236 IPR. Samsung’s contrary arguments (at 53-61) ignore the material differences between the issues in the two proceedings.

1. The 236 IPR involved materially different claims and materially different issues of invalidity.

The Board did not “refus[e] to apply collateral estoppel” based only on “differences in claim language and obviousness grounds.” *Contra* BBr.56. Collateral estoppel does not apply here because there are material differences in *both* the claims *and* the factual issues relevant to invalidity in the two proceedings.

“[C]ollateral estoppel requires that the issues of patentability be identical.” *Google*, 54 F.4th at 1381. If the differences between the claims materially alter the question of invalidity, collateral estoppel does not apply. *See id.* (citing *Ohio*

Willow Wood, 735 F.3d at 1342). Here, the Board relied on Netlist’s expert’s un rebutted testimony that there are “important differences” between the two patents. Appx21-23. Those differences led to different issues being argued and adjudicated in this IPR and the 236 IPR.

Specifically, claim 1 of the ’035 patent recites “each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation.” Appx20. Unlike the ’035 patent claims—which explicitly recite that the data paths have data *and strobe signals* transmitted on them—claim 1 of the ’608 patent recites that its *data path corresponds to each data signal line* in the respective set of data/strobe signal lines. Appx20-21. So the Board’s findings that the prior art disclosed the “data path” element of the ’035 patent cannot, as a matter of logic, compel any finding that the prior art discloses the narrower “data path” element of the ’608 patent. Appx20-21.

The Board also explained that “the ’035 patent “uses ‘timing information’ to ‘control timing of respective data and strobe signals,’ while the ’608 patent delays a signal through a data path corresponding to a data signal line with a delay circuit that is included in the data path”; and that “the ’608 patent recites both a tristate buffer and delay circuit in the data path, which the ’035 patent does not.” Appx21-22. And the Board agreed with Netlist that the ’608 patent claims include additional significant limitations not recited in the ’035 patent. Appx22.

Further, the Board correctly determined that the unpatentability theories in the two IPRs—and hence the underlying factual issues about how the prior art maps to the claims—are different. Appx23. For example, in the 236 IPR, the Board relied on Hiraishi’s “input buffers (INB)” to teach “controlling the timing of the data and strobe signals on the data paths on which those signals travel.” Appx6737. In contrast, Samsung’s expert below testified that Hiraishi’s input buffers are not part of the alleged delay circuit, Appx7032 (31:23-25)—meaning the Board’s findings about the INB logically could not support Samsung’s arguments about the delay circuit below. Appx23. And Samsung’s arguments in the 236 IPR did not involve moving Tokuhiko’s delay element into the data buffer. Appx23; Appx9802.

In short, the issues of patentability are far from identical across the two proceedings.

2. The Board correctly addressed—and rejected—all Samsung’s estoppel arguments concerning factual issues.

The Board did not “fail[] to address whether the underlying factual findings” identified by Samsung were identical and otherwise met the requirements for collateral estoppel. *Contra* BBr.29, 54. The Board addressed and correctly rejected every collateral-estoppel argument Samsung made.

Samsung argued before the Board that collateral estoppel applied to three issues relevant here: (i) the claim construction of “data path,” Appx10470-10472; (ii) the finding that Osanai/Hiraishi teaches controlling timing of data and strobe signals on the data paths, Appx10481-10482; and (iii) the finding that the DRC signal in Osanai/Hiraishi causes the data buffer to perform read and write leveling, Appx10485-10486.

As to issue (i), Samsung does not contest the Board’s determination that its construction of “data path” was not precluded by the 236 IPR, *see* Appx20-22. For good reason: the Board correctly observed that, “unlike claim 1 of the ’608 patent ... claim 1 of the ’035 patent does not recite that the ‘data path’ is ‘corresponding to *each data signal line* in the respective set of data /strobe signal lines.” Appx20-21. Thus, the issues of claim construction were materially different across the IPRs.

As to issue (ii), Samsung argues that the 236 IPR decision identified Hiraishi’s data buffer as controlling timing of data and strobe signals. BBr.56. But the Board correctly found that this finding is not relevant here because, in the 236 IPR, the Board relied upon Osanai’s input buffers to teach “controlling the timing of the data and strobe signals on the data paths,” while, in the present IPR, Samsung’s expert admitted that “*the input buffers were not part of the delay*

circuit.” Appx23; *see* Appx51 (determining collateral estoppel does not apply because Samsung did not argue below that the buffers delay a signal).

The Board also squarely addressed and correctly rejected argument (iii). Appx50-51. The Board’s finding in the 236 IPR that Osanai’s read and write leveling processes performed in response to a DRC signal *generally adjust timing of data and strobe signals on the data path*, Appx6735-6736, does not preclude a finding that Hiraishi’s read and write leveling processes do not cause the alleged delay circuit to *delay a signal on a data path corresponding to a data signal line* (as required by the ’608 patent’s claims). Appx50-51. That is particularly so given that the Osanai components identified as adjusting timing in the 236 IPR— selectors 334 and the input/output buffers INB/OUTB—were not included as part of the alleged “delay circuit” in Hiraishi in Samsung’s arguments below. Appx51.

Samsung’s argument (at 3-4, 54, 58) that the Board improperly focused *only* on differences in the claims of the patents ignores most of these findings. Samsung also mischaracterizes the portions of the Board’s decision with which it does engage. For example, Samsung repeatedly quotes the Board’s statement that “[t]he claims of the ’035 patent and the instant ’608 patent are different.” BBr.54, 58. But that statement was addressing Samsung’s (now abandoned) argument that Netlist’s *claim construction of “data path”* was foreclosed by the 236 IPR. Appx19-20. Naturally, the Board focused on the differences in claim language in addressing

that argument. Elsewhere—as explained above—the Board addressed Samsung’s other, more fact-specific collateral estoppel arguments.

Underlying Samsung’s arguments is a misguided attempt to divorce the Board’s factual findings from the claims at issue in the 236 IPR. That makes no sense: materially different claims, by definition, give rise to materially different legal and factual issues of invalidity. That is why this Court begins collateral-estoppel analyses by assessing whether the claims at issue are materially different. *See, e.g., Papst Licensing GMBH & Co. KG v. Samsung Elecs. Am., Inc.*, 924 F.3d 1243, 1252-53 (Fed. Cir. 2019). Here, the stark differences between the claims are exactly what gave rise to the factual differences in the IPR proceedings and foreclosed estoppel. Indeed, Samsung itself recognized this point when it argued below that a prior IPR cited by Netlist was inapposite because it involved *different claim language*. *See* Appx10500.⁶

3. Samsung forfeited most of its appellate collateral-estoppel arguments by failing to assert them below.

Raising new theories of issue preclusion that were not before the Board, Samsung argues that additional factual findings made in this IPR are precluded by

⁶ Because collateral estoppel does not apply, Samsung’s contentions that the Board’s findings are arbitrary because they conflict with the 236 IPR, BBr.60-62, are meritless. The material differences between the claims appropriately led to different findings on the obviousness inquiries.

the 236 IPR. BBr.62-74. Samsung forfeited these arguments.

“It is well-established that a party generally may not challenge an agency decision on a basis that was not presented to the agency.” *In re DBC*, 545 F.3d 1373, 1378 (Fed. Cir. 2008). Here, Samsung failed to present before the Board its preclusion arguments related to the Board’s findings that: (i) Hiraishi’s MRS command is not used for read/write leveling, BBr.62; (ii) Hiraishi’s write leveling is not done to determine delays in DQ data signal lines to account for different flight time delays for L1/L2, BBr.64-65; and (iii) Hiraishi’s FIFOs do not delay data signals during write and read leveling, BBr.69, 72.

Samsung does not offer any excuse for its forfeiture or make any attempt to establish this is an exceptional case—nor could it. *See In re Google Tech. Holdings LLC*, 980 F.3d 858, 863 (Fed. Cir. 2020). So the Court should not consider these new estoppel arguments.

In any event, the Board’s findings on these points are entirely consistent with the 236 decision. We address these issues in the following section in connection with Samsung’s substantial-evidence arguments.

B. Substantial evidence supports the Board’s factual findings about Hiraishi.

With its collateral-estoppel argument dismantled, Samsung is left with a run-of-the-mill substantial-evidence challenge to the Board’s rejection of Samsung’s

reply arguments. But the Board correctly concluded that Hiraishi's FIFO does not teach the claimed "delay circuit." Appx46-68. Samsung's quibbles with the factual findings underlying that conclusion lack merit.

One point bears emphasis at the outset: in making the disputed findings, the Board expressly credited Netlist's expert's testimony about how Hiraishi functions. *See, e.g.*, Appx57; Appx62. Credibility determinations of this sort "can virtually never be clear error." *Anderson v. City of Bessemer City, N.C.*, 470 U.S. 564, 575 (1985). Indeed, it is even worse for Samsung than that: despite presenting a new theory during trial, Samsung submitted *no expert testimony whatsoever* to support it—and the expert testimony Samsung submitted with its *petition* is actually *inconsistent* with the reply theory. Appx49; Appx62.

1. Hiraishi's mode register setting operation is performed in Step S3, which is separate from Step S4 read/write leveling.

The Board correctly found that Hiraishi's mode register setting (MRS) operation is performed in Step S3 of Figure 13, which is a separate step from Step S4 read/write leveling. This finding is supported by substantial evidence, including Hiraishi's express teachings and Samsung's own expert's testimony. Appx65-67. Samsung's arguments otherwise (BBR.62-64) lack merit.

As an initial matter, even if Samsung could show error on this point (it cannot), the error would be harmless. Hiraishi's FIFOs do not qualify as the

claimed “delay circuit” regardless of whether Hiraishi’s S4 read/write leveling are triggered by an MRS command. *See infra* Section II.B.3. Indeed, Samsung does not even try to explain how the Board’s findings regarding MRS commands are relevant to the Board’s ultimate determination that the claims are not unpatentable. *See* BBr.62-64.

In any event, the Board’s finding was correct. As shown in Figure 13 below, Hiraishi teaches that, upon power-on (Step S1), the system performs an “initialization operation” that “includes a mode register setting operation” in “Step S3.” Appx870(¶139).

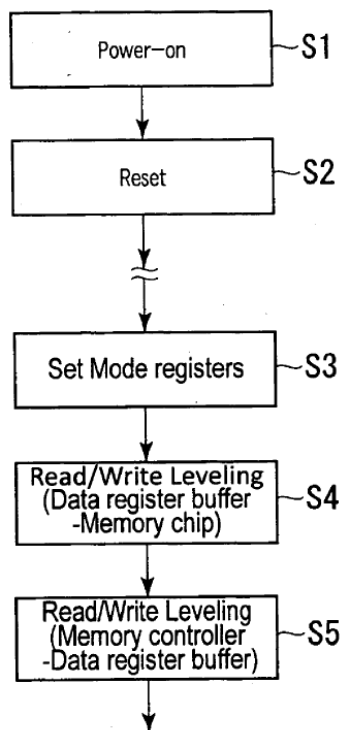


FIG.13

Appx845. Next, “a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4).” Appx870(¶140). So Hiraishi’s mode register setting and read/write leveling operations are performed at different steps. And that is what the Board found: “mode register setting occurs, not as part of the S4 read/write leveling, but rather as a separate step (S3)” that is “not ... relevant to S4 read/write leveling.” Appx66 (citing Appx870(¶¶139-140); Appx845(Fig. 13)).

The Board also evaluated Dr. Wedig’s testimony that a command “*similar to* the mode switching commands and mode register set commands” would be used to trigger S4 read/write leveling. Appx66-67 (emphasis added; citing Appx713-714(¶176)). The Board correctly noted that Dr. Wedig did “not testify that an MRS command is used in Hiraishi; he only testifie[d] that some other unidentified ‘similar’ command would be used in S4 read and write leveling.” Appx66-67. So Samsung failed to show that an MRS command is used in Hiraishi’s S4 read/write leveling.

Samsung contends that the Board “ignored” a skilled artisan’s “familiarity with the JEDEC standard,” which (according to Samsung) “teaches that read/write leveling is performed in response to the MRS command.” BBr.63 (citing Appx3142). But the pages of the JEDEC standard Samsung cites say nothing of the sort. *See* Appx3142; Appx3128; Appx3135; Appx3151-3152. Moreover, even if the JEDEC standard required use of an MRS command in Hiraishi’s Step S3, the

Board found that an MRS command is not used in Step *S4*. Appx65-67. The Board’s finding is consistent with Dr. Wedig’s testimony that Hiraishi’s *S4* leveling would be triggered by a command that is merely “similar to” an MRS command—testimony that Samsung does not even address.

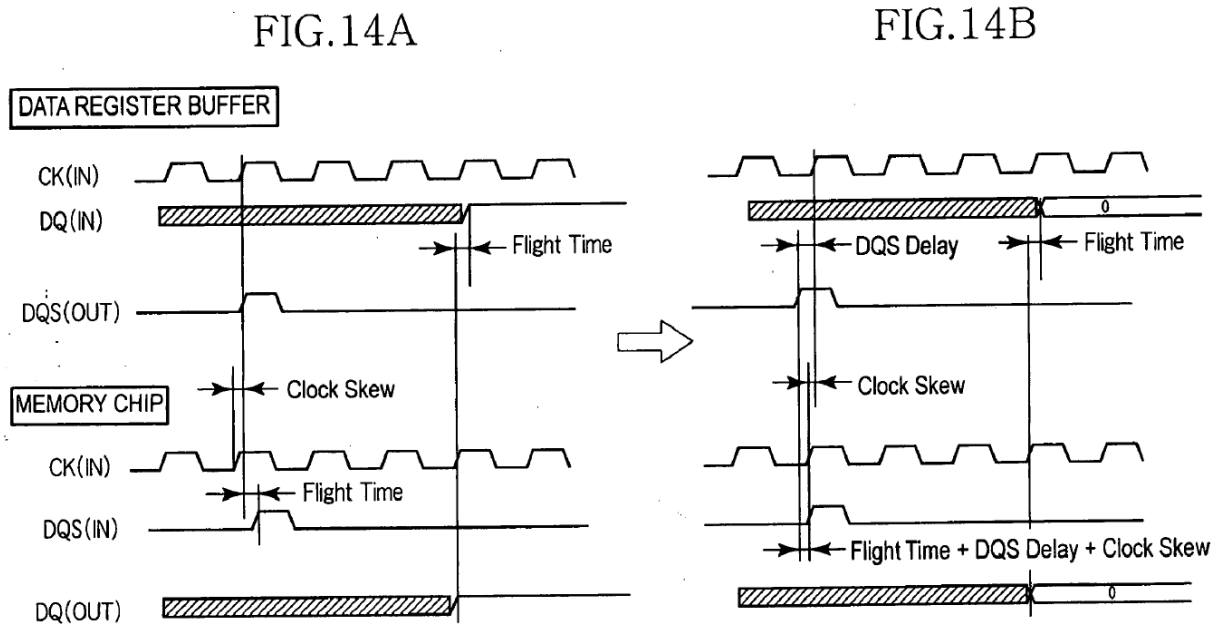
Nor is the Board’s finding inconsistent with the 236 decision. That decision mentions Micron’s argument that Hiraishi would perform “write leveling” “in response to a memory command such as the Mode Register Set command,” Appx6731-6732, but it nowhere squarely finds that Hiraishi performs *S4 read/write leveling in response to an MRS command* (which is what Samsung argued below, *see* Appx65-66). And Samsung has not even tried to show that the finding it relies on from the 236 decision was essential to that judgment. *But see Google*, 54 F.4th at 1381 (party asserting collateral estoppel must show both that the issue is “identical to one decided in the first action” and “essential to a final judgment in the first action”).

2. Hiraishi’s *S4* write leveling does not account for different flight-time delays between data lines L1 and L2.

Substantial evidence likewise supports the Board’s findings that Hiraishi does not teach applying the delays for *strobe* signals measured during *S4* write leveling to *data* signals in subsequent write operations, Appx57-62, and that

Hiraishi’s S4 write leveling does not account for flight-time delays between data lines L1 and L2, Appx62-63.

a. All agree that Hiraishi’s S4 write leveling addresses mismatches between the clock signal CK and the data strobe signal DQS at the memory chip. Appx56-57; BBr.64-65. Hiraishi illustrates S4 write leveling in Figures 14A and 14B, below. Appx870(¶142). Hiraishi explains that, “[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timing of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” Appx870(¶143). This timing mismatch between the clock signal CK and the data strobe signal DQS at the memory chip is shown in Figure 14A.



Appx846.

S4 write leveling synchronizes the clock signal CK and the data strobe signal DQS received by the memory chip by changing “an output timing of the data strobe signal DQS.” Appx870(¶¶143-145); *see* Appx870(¶146) (“Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.”). This synchronization is shown in Figure 14B, above.

This much is undisputed. Indeed, the Board noted the experts’ agreement that “Hiraishi’s S4 write leveling is used to address mismatches between the clock signal CK and the data strobe signal DQS.” Appx57 (citing Appx7274(¶¶109-110); Appx7061(60:7-12).

b. Samsung contends, however, that Hiraishi’s S4 write leveling *also* accounts for different flight-time delays between data lines L1 and L2. BBr.64-65. Hiraishi does so, according to Samsung, by applying “the delay measured during the write leveling ... to both the DQ data signals and the DQS strobe signals during subsequent write operations.” BBr.65-67. Samsung argues that the “Re-Timing” of Hiraishi’s Figure 12 illustrates applying the strobe delay from S4 write leveling to data signals during subsequent write operations. *Id.*

The Board relied on substantial evidence in finding otherwise. The Board found that Hiraishi does not teach a “two-step method where delays in write

leveling during initialization is applied to the retiming write operation during normal operation.” Appx57-62. Instead, “write leveling is a separate step than re-timing used in the write operation.” Appx58. “[S]everal disclosures in Hiraishi,” the Board found, support this interpretation. Appx58. Namely, Hiraishi teaches that S4 write leveling is performed during the initialization operation shown in Figure 13, whereas normal write operations (such as that shown in Figure 12) occur *after* initialization. Appx58-62 (citing Appx870(¶¶138, 146); Appx844-845(Figs. 12-13); Appx7277-7278(¶113); *see* Appx62 (noting Samsung’s expert’s admission “that the leveling processes occurs during the initialization period”) (citing Appx7058(57:3-10); Appx63 (“[W]rite leveling is used to address mismatches between the time of receipt of the clock signal and the data strobe signal DQS ... not to account for delays in data signal lines.”)).

The Board expressly credited Dr. Mangione-Smith’s testimony on this issue. *See* Appx59-63 (citing Appx7276-7279(¶¶112, 114-115)). With respect to Hiraishi’s “Re-Timing” in Figure 12, Dr. Mangione-Smith testified that “the DQ data re-timing from a write latency of 4 clock cycles (WL=4) to a write latency of 5 clock cycles (WL=5) is indicted as a distinct occurrence” from the results of S4 write leveling. Appx7278-7279(¶114). His annotated Figure 12 below (reproduced in the Board’s decision) shows re-timing (green) and S4 write leveling (red) as distinct adjustments:

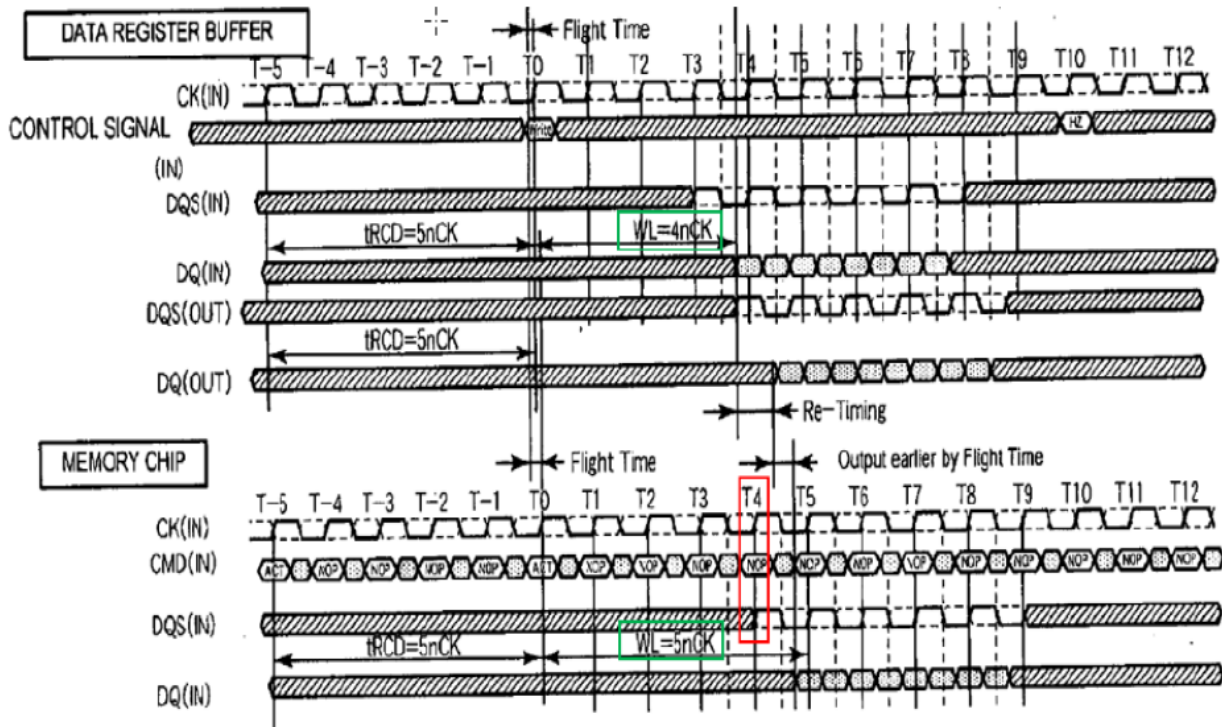


FIG. 12

Appx60; Appx7278-7279(¶¶114-115). Dr. Mangione-Smith explained that a skilled artisan would understand “that the result of Hiraishi’s write leveling which is stored is not used to delay data and data strobe signals during subsequent write operations, but instead is used to delay or advance DQS signal to match the module-level clock signal CK with DQ(IN) and DQ(OUT).” Appx7276-7277(¶112). Hiraishi’s Re-Timing in Figure 12, in contrast, addresses flight delays during write operations by merely increasing latency by one clock cycle.

Appx7279-7288(¶¶116-131); Appx57.

The Board credited this testimony because it was both consistent with Hiraishi’s teachings and unrebutted. Appx62. Samsung’s lawyers may disagree

with Dr. Mangione-Smith’s account of the reference—but their attorney argument does not and cannot show that the Board’s decision to credit that account lacks substantial evidence. *See In re Riggs*, 131 F.4th 1377, 1386 (Fed. Cir. 2025) (“[A] party’s position that is based on attorney argument rather than record evidence does not undermine substantial evidence that supports the Board’s findings.”).

Moreover, even if Hiraishi could be interpreted as Samsung argues, that does not mean the Board lacked substantial evidence for its interpretation of Hiraishi. *See Incept LLC v. Palette Life Scis., Inc.*, 77 F.4th 1366, 1373 (Fed. Cir. 2023); *Roku*, 63 F.4th at 1326. After careful review of Hiraishi and the expert testimony, the Board found that the weight of the evidence favored of Netlist. Such findings should not be disturbed on substantial-evidence review.

c. The Board’s findings are consistent with the 236 decision. *Compare* Appx56-57, *with* Appx6714. Like the decision below, the 236 decision found that Hiraishi’s S4 write leveling is needed “[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.” Appx6714 (quoting Hiraishi). “To compensate for that, ‘write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS.’” Appx6714 (quoting Appx870-871(¶151)).

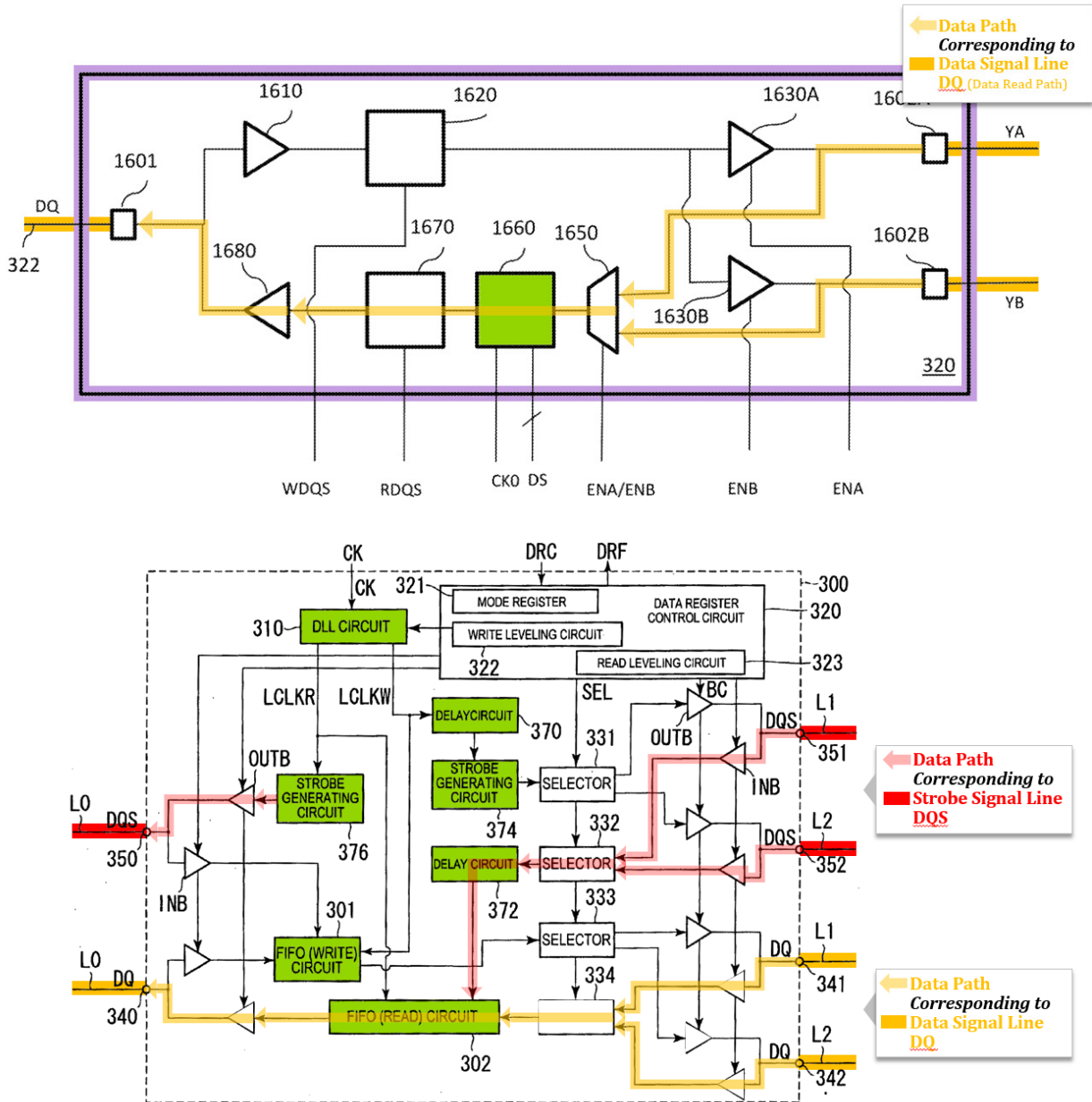
The panel in the 236 IPR was not presented with, and thus did not decide, the issue of whether the delays that are determined during S4 write leveling are somehow later used to delay data signals during subsequent write operations. Rather, the panel evaluated whether Hiraishi and Tokuhiko taught an element of the '035 patent requires merely “control[ing] timing” of data and strobe signals—not specifically delaying a data signal, as required by the '608 patent claims. Appx6727; Appx6736. Unsurprisingly, neither of the portions of the 236 decision that Samsung quotes (BBr.65) speaks to the question of whether S4 write leveling somehow maps onto that element of the '608 patent. *See* Appx6736; Appx6727. And, in any event, Samsung again does not even attempt to show that any of these points were essential to the judgment. They plainly are not; on the contrary, the Board was simply summarizing Micron’s arguments. Samsung has again failed to show that collateral estoppel applies.

3. Neither of Hiraishi’s FIFOs 301 and 302 is a “delay circuit.”

Finally, substantial evidence supports the Board’s findings that neither of Hiraishi’s FIFOs 301 (write direction) or 302 (read direction) satisfies the claimed “delay circuit.” Appx49-50; *contra* BBr.69-74.

The Board rejected Samsung’s argument—re-urged on appeal, BBr.71—that similarities between Hiraishi’s Figure 5 and the '608 patent Figure 16 demonstrate obviousness. Appx50. Indeed, juxtaposing these figures highlights the key

difference: “Figure 16 has a delay circuit 1660.” Appx50. As shown below, the ’608 patent’s data path (top figure) includes a delay circuit (in green), which is absent in Hiraishi (bottom figure):



Compare Appx104(Fig. 16) (annotated), with Appx837(Fig. 5) (annotated).

Hiraishi describes FIFOs 301/302 as mere data buffers, not as delay circuits.

Appx866(¶84). This is telling—Hiraishi’s buffer 300 includes “delay” circuits 370/372, demonstrating that, when Hiraishi intended a circuit to be a delay circuit, it said so.

The Board also correctly stated that, despite presenting a new theory that Hiraishi’s FIFOs alone qualify as the claimed “delay circuit,” Samsung did not provide any support from its expert. Appx49-50. Samsung notes Dr. Wedig’s testimony that Hiraishi’s alleged delay circuit “includes” the FIFOs 301/302. BBr.70. But Dr. Wedig admitted that a *group* of elements, including the FIFOs, *collectively* teach the claimed “delay circuit”—not that the FIFO alone was sufficient. Appx693-695(¶161); Appx701-703(¶166); Appx7018-7019(17:23-18:5). Samsung’s argument on appeal that the FIFO alone qualifies as a delay circuit is thus contrary to the testimony of its own expert. And Samsung cannot show that the Board’s rejection of its arguments lacks substantial evidence simply by quoting the reference and making attorney argument about what the disclosures mean. *See* BBr.73-74; *Riggs*, 131 F.4th at 1386.

Samsung also argues that the Board’s finding excludes the patent’s preferred embodiment because delay circuit 1660 (green above) receives a delay signal (DS) from outside the data path. BBr.71. Not true. The claims require the “delay circuit,” not a delay signal (DS) input to the delay circuit, to be in the data path.

Finally, the Board’s findings below are again consistent with the panel’s findings in the 236 IPR. Samsung does not point to any finding in that decision that Hiraishi’s FIFO qualifies as a delay circuit, *see* BBr.69, 72—because there is not one. The 236 panel relied on “input buffers (INB),” which are timed by Hiraishi’s S4 read leveling, to teach “controlling the timing of the data and strobe signals on the data paths on which those signals travel.” Appx6737; *see* Appx23. In contrast, Samsung’s expert conceded below that the INB is not part of the alleged delay circuit. Appx7032 (31:23-25). And it is certainly not part of Hirashi’s FIFOs. The Board’s findings about the INB have no logical relevance to Samsung’s arguments about the delay circuit below.

Samsung mischaracterizes the 236 decision when it states that “the Board *rejected*” the argument that Hiraishi’s “read leveling process delays the internal signals that turn on [the] input buffers.” BBr.73. The Board expressly found that Hiraishi—by using read leveling to adjust the timing of the input buffers, which “act a gate allowing data and strobe signals to either pass through or not pass through”—“teach[es] controlling the timing of the data and strobe signals.” Appx6737. That finding, again, has nothing to do with whether Hiraishi’s FIFOs delay a data signal as required by the ’608 patent claims.

* * *

Samsung's new reply argument—which the Board did not even have to consider—fails along with its petition arguments. There is no collateral estoppel; Samsung lost on the facts; and it cannot surmount the substantial-evidence standard of review, particularly given that its new reply theory is contradicted by the testimony of its own expert.

CONCLUSION

The Court should affirm.

July 28, 2025

Respectfully submitted,

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**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

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Case Number: 2025-1378

Short Case Caption: Samsung Electronics Co., Ltd. v. Netlist, Inc.

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