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Paper No. 8
Entered: July 21, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00730
Patent 9,128,632 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE *Administrative Patent Judges.*

CLEMENTS, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–5, 12–14, 19, and 20 ("the challenged claims") of U.S. Patent No. 9,128,632 B2 (Ex. 1001, "the '632 patent"). Paper 1 ("Pet."). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner does not establish a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '632 patent. Accordingly, pursuant to 35 U.S.C. § 314, we deny institution of an *inter partes* review of claims 1–5, 12–14, 19, and 20 of the '632 patent.

A. Related Proceedings

Petitioner represents that the '632 patent is not involved in any other legal proceedings to its knowledge. Pet. 1. Patent Owner identifies U.S. Patent Application No. 14/846,993 as the only related matter. Paper 5, 1.

B. The '632 patent

The '632 patent, titled "Memory Module with Distributed Data Buffers and Method of Operation," issued September 8, 2015, from U.S.

Patent Application No. 13/952,599. Ex. 1001 at [54], [45], [21]. The '632 patent generally relates to a memory module that includes memory devices, a module control device, and data buffers (also called "buffer circuits" or "isolation devices"). *Id.* at 3:8–10. "The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices." *Id.* at 3:33–36. "Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock." *Id.* at 3:36–39. "Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller." *Id.* at 3:39–42. "Thus, the memory controller does not have direct control of the memory devices." *Id.* at 3:42–43.

Figure 1 of the '632 patent is reproduced below.

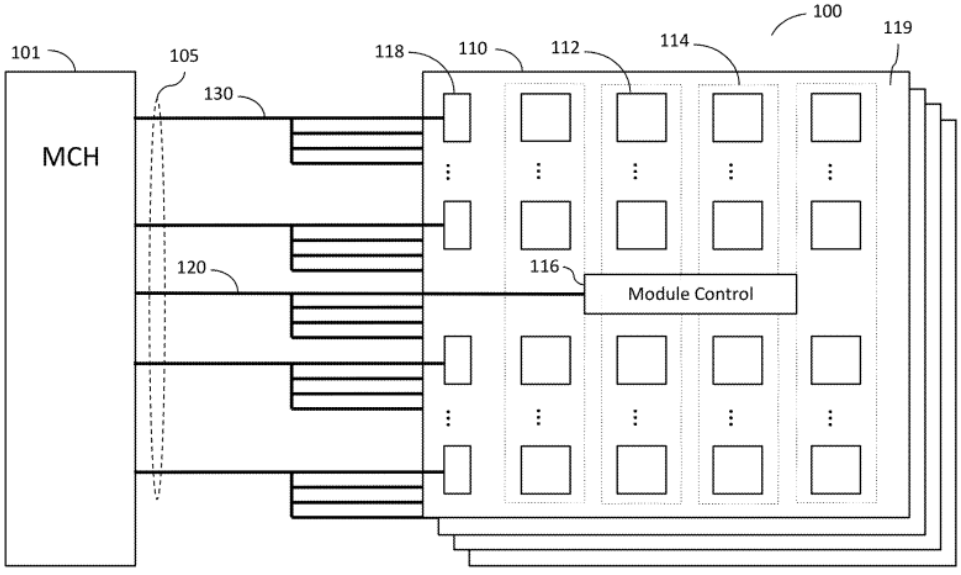

FIG. 1

As shown in Figure 1, memory controller (MCH) 101 and one or more memory modules 110 are coupled by memory bus 5, which includes command/address (C/A) signal lines 120 and groups of system data/strobe signal lines 130. *Id.* at 4:1–5. "[E]ach memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114." *Id.* at 4:6–7. Each memory module 110 also includes module control circuit 116 coupled to MCH 101 via C/A signal lines 120, and a plurality of buffer circuits or isolation devices 118 coupled to MCH 101 via respective groups of system data/strobe signal lines 130. *Id.* at 4:7–13. "[S]ystem 100 depends on the isolation devices 118 to properly time the transmission of the read data and strobe signals to the MCH 101." *Id.* at 7:47–49.

Figure 12A, reproduced below, is a timing diagram for a write operation according to one embodiment. *Id.* at 14:60–61.

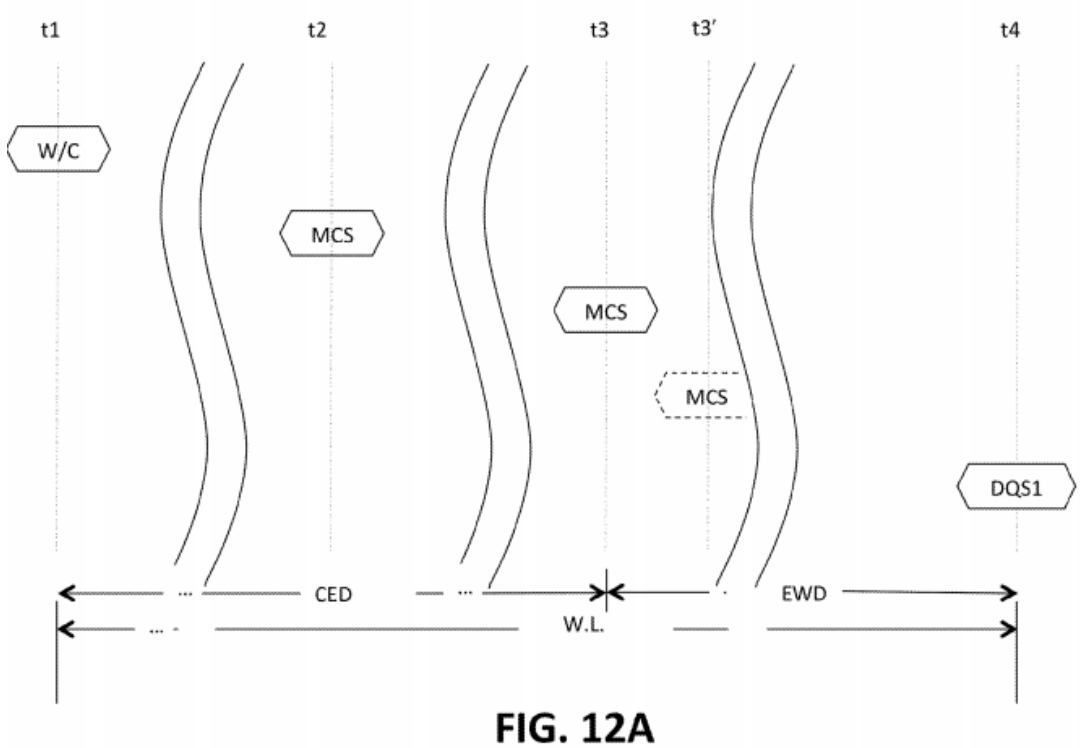

FIG. 12A

As shown in Figure 12A, in response to a write command issued at t1, module control circuit 116 issues one or more enable signals at time t2. *Id.* at 14:61–65. Those signals are received by isolation device 118 at t3, which then receives one or more strobe signals DQS at t4. *Id.* at 14:65–15:1. The one or more enable signals are received by a different isolation device 118 at t3′. *Id.* at 14:65–15:4. The time between t1 and t4 is the write latency "W.L." and is known to the isolation device 118. *Id.* at 15:4–7. The time interval between t4 and t3 (the "enable-to-write data delay" or "EWD") can be determined by isolation device 118. *Id.* at 15:7–10. Isolation device 118 can then determine the time interval between t1 and t3 (the "command-to-enable delay" or "CED"), "which can be used by the isolation device 118 to properly time transmission of read data to the MCH." *Id.* at 15:10–15.

C. Illustrative Claim

Of the challenged claims, claims 1 and 12 are independent, claims 2–5 depend from claim 1, and claims 13, 14, 19, and 20 depend from claim 12. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to the memory command signals;

> memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and
>
> a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and
>
> wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and
>
> wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

Ex. 1001, 18:38–19:12.

D. Evidence Relied Upon

Petitioner relies upon the following prior art references:

Saito	US 2010/0309706 A1	Dec. 9, 2010	Ex. 1005
Swain	US 7,808,849 B2	Oct. 5, 2010	Ex. 1006
Kim	US 6,184,701 B1	Feb. 6, 2001	Ex. 1007

Pet. 2. Petitioner also relies upon the Declaration of Trevor Mudge ("Mudge Decl.") (Ex. 1003).

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 2):

Reference(s)	Basis	Claim(s) challenged
Saito and Swain	§ 103	1–5, 12–14, 19, and 20
Saito, Swain, and Kim	§ 103	3, 13, and 14

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner proposes constructions for "memory module," "memory system," "memory controller," "memory bus," "memory command signals," "module command signals," "module control signals," and "metastability." Pet. 6–10. Patent Owner argues only that, "[f]or the purposes of this Response, the Patent Owner submits that all claims terms should be accorded their ordinary and customary meaning as understood by one of ordinary skill in the art." Prelim. Resp. 22. On this record, we determine that it is not necessary to expressly construe any of these terms in order to resolve the parties' disputes.

B. Claims 1–5, 12–14, 19, and 20: Obviousness over Saito and Swain

Petitioner argues that the claims 1–5, 12–14, 19, and 20 are unpatentable under 35 U.S.C. § 103(a) as obvious over Saito and Swain. Pet. 15–49. In light of the arguments and evidence of record, we are not persuaded that Petitioner has established a reasonable likelihood that the claims are unpatentable as obvious over Saito and Swain.

1. Saito (Ex. 1005)

Saito is directed to a memory module that includes a plurality of memory chips, a plurality of data register buffers, and a command/address/control register buffer. Ex. 1005, Abstract. Figure 7 of Saito is reproduced below.

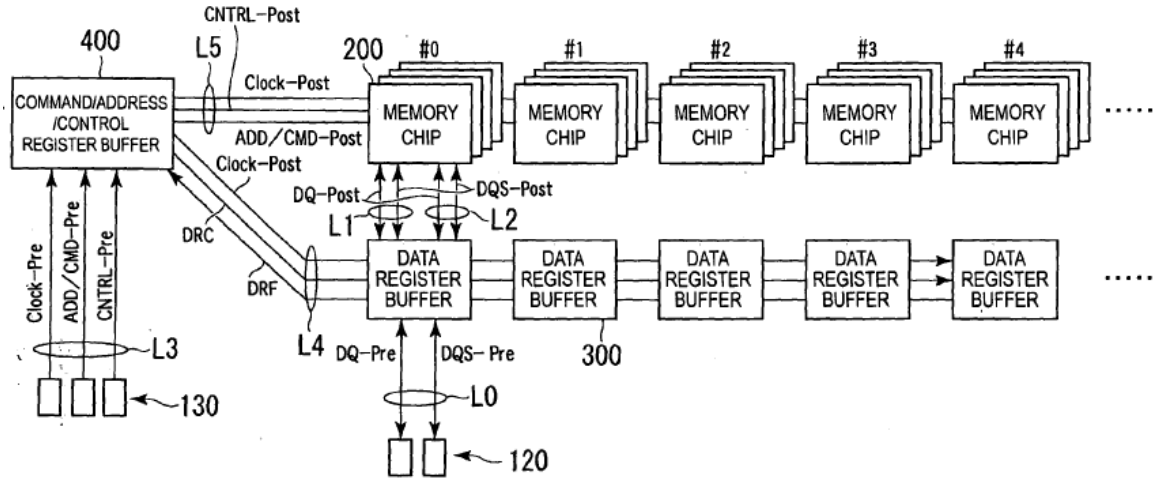

FIG.7

As shown in Figure 7, "the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200." Ex. 1005 ¶ 100. "[B]ecause the data DQ is buffered by data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post." *Id.* ¶ 101. As a result, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner." *Id.*

2. *Swain (Ex. 1006)*

Swain is directed to "[r]ead leveling of memory units designed to receive access requests in a sequential chained topology writing a data pattern to the memory array." Ex. 1006, Abstract. Swain teaches that its memory controller performs write leveling of a DRAM. *Id.* at 5:44–45. "Write leveling entails determining the various delays that may be required to reliably write (store) data into DRAM 120A" and "can be performed

using one of several known approaches." *Id.* at 5:45–48. Swain teaches that the memory controller sets a test value for a read operation, and that "any available information (e.g., parameters determined while write leveling of above) can be used in choosing the test value for different iterations." *Id.* at 5:49–65. The memory controller then reads a data portion from DRAM based on the test value set for the compensation delay. *Id.* at 5:66–6:1.

3. Analysis

Claim 1 recites

> wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

Ex. 1001, 19:4–12 (the "Timing Limitation").

For determining a respective time interval, Petitioner relies upon Saito's write leveling operation performed by write leveling circuit 322 of data register buffer 300. Pet. 28–29. This operation, depicted in Figures 14A and 14B of Saito, determines an amount of time by which to shift the output of DQS from data register buffer 300 so that it arrives at memory chip 200 substantially matched with clock signal CK. Ex. 1005 ¶¶ 140–144. Petitioner also relies upon Saito's read leveling operation performed by read leveling circuit 323 of data register buffer 300. Pet. 29. This operation, depicted in Figure 15 of Saito, determines "a time A . . . for each of the memory chips 200 . . . [that is] used in an adjustment of an activation timing of the input buffer circuit INB and the like." Ex. 1005 ¶ 149.

For timing transmission of read data signals, Petitioner relies upon Saito's teaching of a "re-timing" during read operations:

> Saito also discloses that its memory module has a known read latency, referred to as CAS latency, that "is set to five clock cycles (CL=5)" in the initialization examples in the specification. Saito discloses that its memory module's known CAS latency ("*read latency*") is used during read operations during normal operation as well. Ex. 1005 at [0126]. And the timing adjustment ("*respective time interval*") that is the result of the read leveling operation during initialization is used with that CAS latency ("*read latency*") to time transmission during read operations. *Id*. at [0128]; Ex. 1003 at ¶127.

Pet. 29. Saito's read operation is depicted in Figure 11, reproduced below.

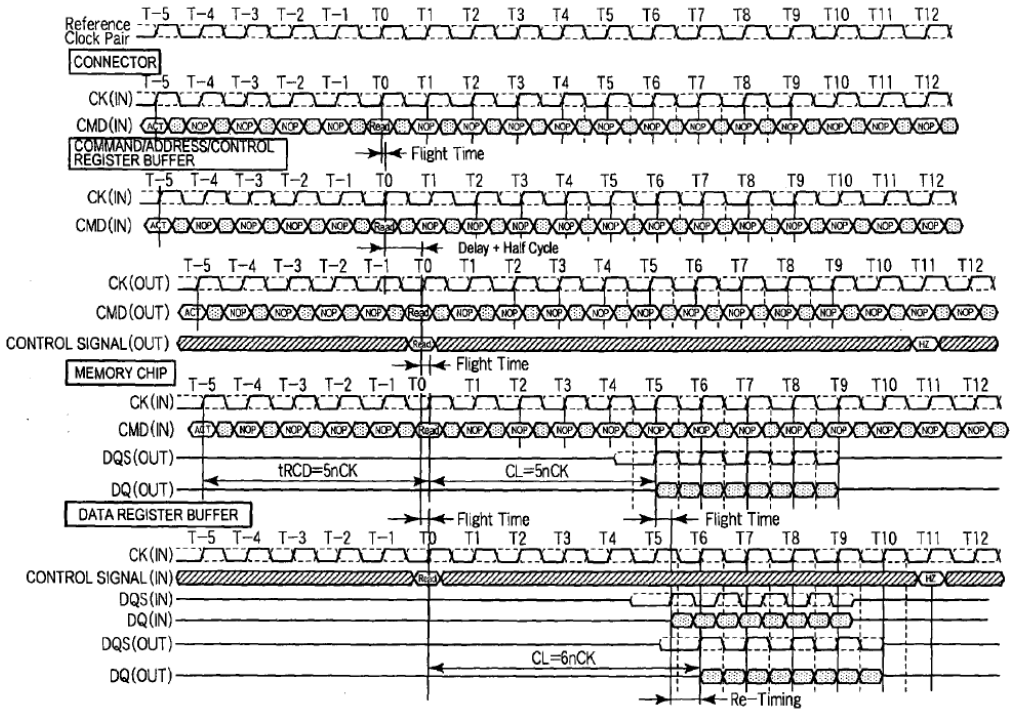

FIG.11

Ex. 1005, Fig. 11 (depicting, at the bottom of the figure, a "Re-Timing" to CL=6nCK). About this re-timing, Saito discloses only that "data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR . . . to convert CL into CL=6, and outputs the read data DQ and the

data strobe signal DQS," as a result of which, "it becomes possible for the memory controller to receive the read data DQ in a correct manner." *Id.* ¶ 128.

Thus, according to Petitioner, Saito teaches data register buffers configured to time transmission of read data signals, but those buffers use a time interval determined during a *read* leveling operation instead of using a time interval determined during a *write* operation, as required by the claim. Pet. 30. As a result, Petitioner relies upon Swain for "using the timing intervals determined during write leveling operations in the read leveling operations as well." *Id.* Petitioner contends that it would have been obvious to a person of ordinary skill to apply this teaching from Swain to the system of Saito. *Id.* at 31–33.

Patent Owner argues, *inter alia,* that Saito's re-timing to CL=6 is not "time[d] . . . in accordance with" any time interval determined during read/write leveling, as Petitioner contends. Prelim. Resp. 24–32.

We agree with Patent Owner. Saito describes data register buffers re-timing to CL=6 during a read operation (Ex. 1005 ¶ 128) and, therefore, arguably teaches "tim[ing] transmission of a respective set of read data signals received from the respective group of memory devices . . . during a memory read operation." Saito does not, however, teach that its re-timing is "in accordance with [a] time interval" that is "determine[d] . . . based on signals received by the each respective buffer circuit during a memory" read or write "operation." Paragraph 128 of Saito says that "data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR . . . to convert CL into CL=6," but does not explain how CL=6 was chosen. Petitioner argues that it is related to the time interval determined during the

read leveling operation by read leveling circuit 323, but that operation determines a "time A" that is used to adjust timing of "the *input buffer circuit INB* and the like." Ex. 1005 ¶ 149. Saito does not teach time A being used to adjust timing of data *output* by data buffer circuit 300 to the system controller (i.e., to "time transmission of a respective set of read data signals,") as recited in the claim.

Moreover, Saito describes a scenario in which re-timing to CL=6 appears to be inadequate to account for the "time A" determined during read leveling. Specifically, Saito describes a "long" example of a read-leveling operation, depicted in Figure 15 of Saito, in which data arrives from memory chip 200-19 right before T6. Ex. 1005 ¶ 149. In that example, it is not clear that re-timing to CL=6 would account adequately for the "time A" in this example, which undermines Petitioner's contention that the re-timing is in accordance with this time interval.

Moreover, Saito describes memory controller 12 performing its own read-leveling to compensate for the unpredictably-timed transmission of DQ(OUT) from data buffer 300. Ex. 1005, Fig. 17, ¶¶ 155–159. As a result of this process, "memory controller 12 can find a time B . . . for each of the data register buffers 300" that is "used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like." *Id.* ¶ 159. As with the re-timing operation above, Saito describes using the determined time interval only to adjust the timing of an *input* buffer of memory controller 12, not to adjust the timing of *output* by data register buffer 300. The '632 patent explicitly distinguishes its system and method from such memory-controller-based leveling:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Ex. 1001, 2:14–21. *See also id.* at 14:54–55 ("Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing.").

As a result of the foregoing, we agree with Patent Owner that Petitioner has not established persuasively that Saito's re-timing to CL=6 is "time[d] . . . in accordance with" any time interval determined during read/write leveling, as Petitioner contends, and therefore does not, even in combination with Swain, teach the Timing Limitation.

4. Conclusion

On this record, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–5, 12–14, 19, and 20 are unpatentable as obvious over the combination of Saito and Swain.

C. Claim 3, 13, and 14: Obviousness over Saito, Swain, and Kim

Petitioner argues that claims 3, 13, and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Saito, Swain, and Kim. Pet. 49–53. Claim 3 depends from independent claim 1, and claims 13 and 14 depend from independent claim 12. As discussed above, we are not persuaded claims 1 and 12 would have been obvious over the combination of Saito and

Swain because we are not persuaded that they teach the Timing Limitation. In this ground, Petitioner relies upon Kim only for teaching the metastability detection circuit and signal adjustment circuit recited in claims 3, 13, and 14. Pet. 50–53. As a result, Kim does not cure the deficiency noted above with respect to Saito and Swain's teaching of the Timing Limitation. On this record, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 3, 13, and 14 are unpatentable as obvious over the combination of Saito, Swain, and Kim.

III. CONCLUSION

For the foregoing reasons, we are not persuaded that Petitioner has demonstrated a reasonable likelihood that it would prevail in establishing the unpatentability of claims 1–5, 12–14, 19, and 20 of the '632 patent.

IV. ORDER

Accordingly, it is ORDERED that the Petition is *denied*, and no trial is instituted.

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