The Air Spacer Technology for Improving the Cell Distribution in 1 Giga Bit NAND Flash Memory

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1. Introduction

Recently the cell integration density of NAND flash memory increases rapidly due to its simple structure suitable for high resolution lithography. However as the cell integration density increases, NAND flash memory cell shows the problem of increased parasitic capacitance between the cells. The problems are generated by the floating-gate interference during cell operation. In order to reduce the floating gate interference, it is necessary to adopt low-k dielectric material.

In this work, we would like to propose the air spacer which has the lowest dielectric constant. We applied the air spacer technology on poly-Si/Wsix stack gate of 90 nm design-rule NAND flash device for the first time, which improved the cell operation characteristics.

2. Experiment

The process flow to form an air spacer is shown in Fig. 1. After patterning 90 nm design-rule cell, buffer oxide, nitride and thick oxide were deposited. After that, the thick oxide below the gate poly was removed by dry etch as shown in Fig. 1(b). Then to form the mini spacer inside gate to gate space, the SiN was deposited and etched as in Fig. 1(c). After the oxide inside the mini spacer was removed by wet etch, air gap was formed inside the gate to gate space as shown in Fig. 1(d). Devices with nitride spacer and oxide spacer were also fabricated for comparison[1]. In Fig. 2 the air gap can be clearly observed from the scanning electron microscope(SEM) picture of the fabricated device. The on cell current in best/worst case situation and the program speed were measured at TEG(Test of Elements Group) pattern[2]. It is 32-cell NAND string, in which each cell is sequentially named from the common ground to the bit-line direction as WL0 cell to WL31 cell[1]. In the main cell of 1giga bit memory, the cell V_{th} distribution was measured by single pulse program. In addition, the reliability evaluation was conducted to verify the program V_{th} distribution of cell after performing the P/E cycling 100 K.

3. Results and Discussion

In the conventional concept, the floating gate voltage was determined by the control gate voltage with a coupling ratio of $\gamma = C_{ono}/C_{ono}+C_{tun}$[3], where C_{ono} is the control gate to floating gate capacitance and C_{tun} is the tunnel oxide capacitance. As the design rule of NAND flash memory is scaled down, it is hard to ignore its parasitic effects on the cell operation. In addition to C_{ono} and C_{tun}, there are many other parasitic capacitors surrounding the floating gate[1]. The coupling voltage and the floating-gate interference coupling ratio can not be expressed simply by using V_{ono}, V_{tun} because they are affected by surrounding potential via the parasitic capacitors. In consideration of the parasitic capacitances, they should be expressed by C_{fgx}, C_{fgy} and C_{fgcg}. Among them, C_{fgx} and C_{fgy} indicate the floating gate capacitance of bit-line and word-line directions respectively. C_{fgcg} is the capacitance between the floating gate and the adjacent control gate[1]. As C_{fgy} which indicates the dielectric constant of gate spacer becomes lower, the floating-gate interference coupling ratio is reduced but the coupling voltage on the floating gate is increased[1].

Fig. 3 and Fig. 4 shows the on cell current at the best and worst situation at read voltage of 5.0 V with SiN, oxide and air spacer. In the reading operation, the reading voltage is applied to the control gate of the cell. The on cell current of the air spacer is the largest due to the coupling voltage increased by lower parasitic capacitance. Also the programming speed is faster for air spacer as shown in Fig. 5. Fig. 6 shows the cell V_{th} distribution of WL30 and WL31 in 90 nm cells having SiN, oxide and air spacer. The cell V_{th} on WL30 are shifted by programming the adjacent cells in the same word line and WL31 cell in the same bit line. In case of air spacer, the shift in the cell V_{th} was the smallest. The reduced shift with air spacer is due to its lower parasitic capacitance[1], [2]. Fig. 7 compares the cell V_{th} distribution of 1G bit cell by single pulse program. The cell V_{th} distribution was dramatically improved with air spacer due to the improved floating gate voltage shift. The endurance characteristics of the air spacer in comparison to SiN and oxide spacer are shown in Fig. 8. After P/E cycling, negligible difference in the threshold voltage distribution between the air spacer and others was observed.

4. Conclusion

The 1G bit NAND flash cell using the air spacer was successfully fabricated. We could improve the on cell current, program speed compare to the SiN and oxide spacer. Also, the cell V_{th} was dramatically improved.

5. References

[1] J.D. Lee et al., EDL pp. 264-266, 2002.
[2] J.H. Park et al., IEDM pp. 873-876 2004.
[3] Y.S. Hisamune et al., IEDM pp. 19-22, 1993.

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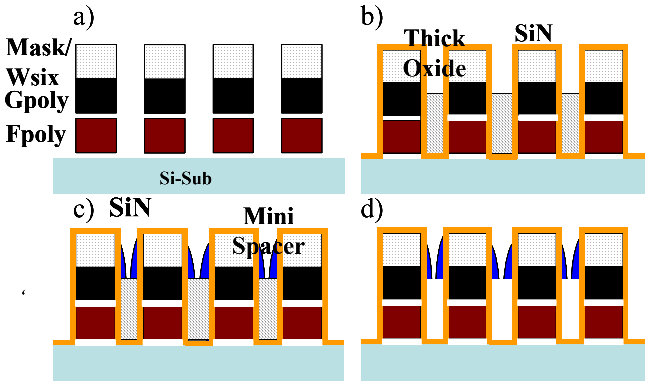

Fig.1 The process flow of the air spacer a) the gate patterning b) the barrier SiN, thick oxide deposition and thick oxide is removed by dry etch c) The spacer is formed d) The thick oxide inside gate to gate space is removed by wet etch.

① **Gate Pattern**
② **Barrier Deposition**
• **SiN**
③ **Deposition & Etch**
• **Oxide**
④ **Deposition & Etch**
• **SiN**
⑤ **Oxide Wet Etch**

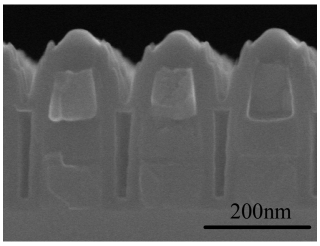

Fig.2 The process flow of the air spacer and the SEM picture of the fabricated device.

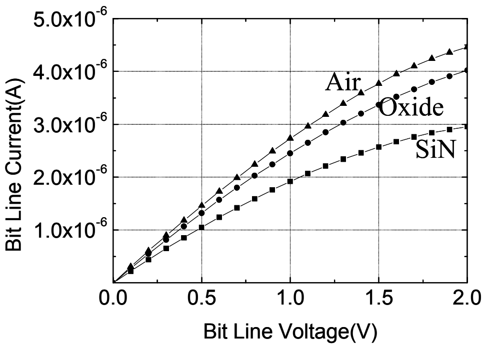

Fig.3 "On" cell current characteristics at 80℃ for the best case situations(other cells are all erased) .

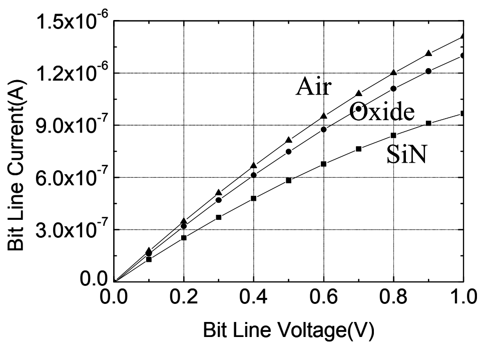

Fig.4 "On" cell current characteristics at 80℃ for the worst case situations(other cells are all programmed) .

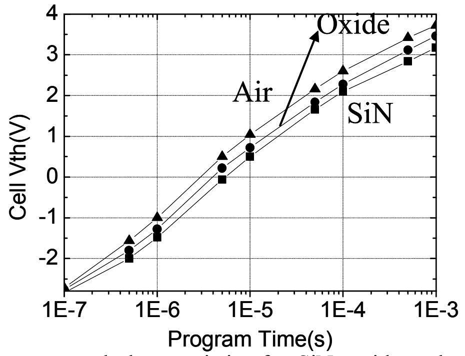

Fig.5 Program speed characteristics for SiN, oxide and air spacer. The program voltage is estimated to be about 20V.

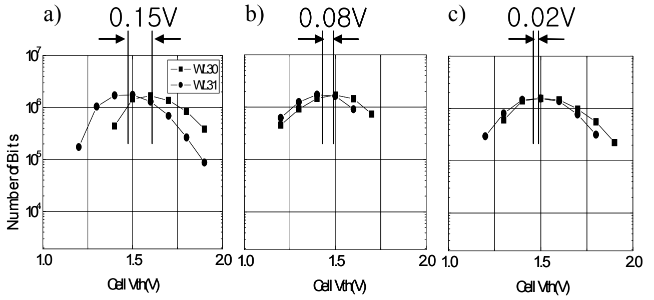

Fig.6 Threshold voltage shift by floating gate interference was measured on WL30 a) SiN spacer b) Oxide spacer c) Air Spacer

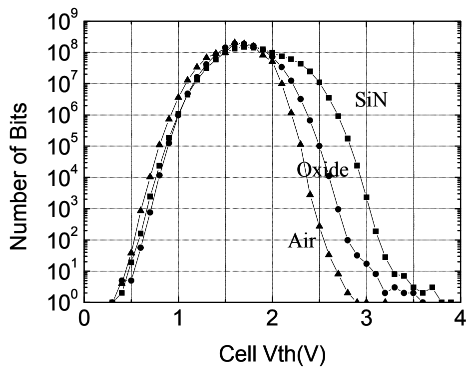

Fig.7 The cell V_{th} distribution shifted by floating gate interference

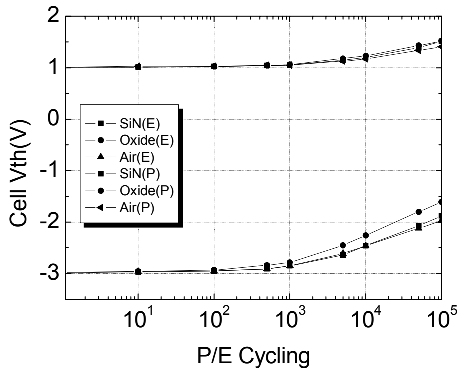

Fig.8 The endurance characteristics after 100K P/E cycling