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(54) **METHOD FOR MANUFACTURING DUAL-SPACER STRUCTURE**

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(52) **U.S. Cl.** **438/694**; 438/696
(58) **Field of Search** 438/230, 231, 438/232, 303, 305, 306, 689, 694, 696, 697

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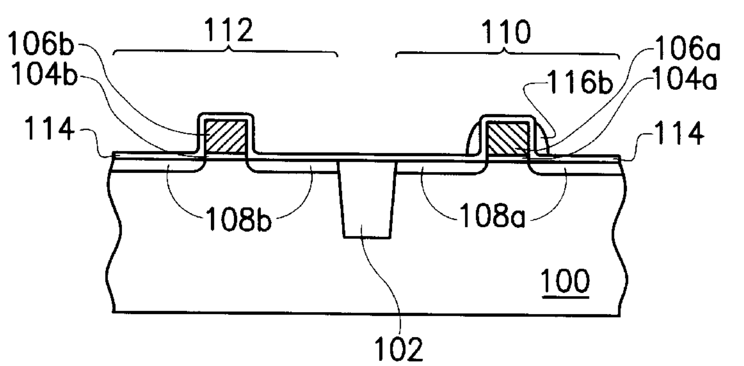
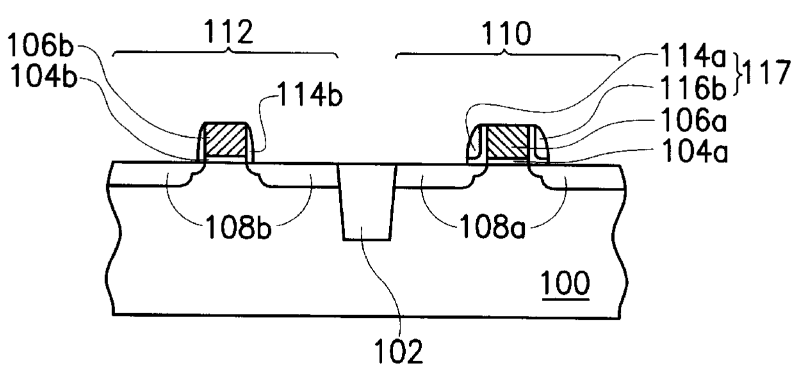
(57) **ABSTRACT**

A method of manufacturing a field effect transistor with a dual-spacer structure. A substrate having a first device region and a second device region is provided. The first device region comprises a first gate formed over the substrate and the second device region comprises a second gate formed over the substrate. A first dielectric layer is formed over the substrate. A second dielectric layer is formed on the first dielectric layer. A portion of the second dielectric layer is removed to expose a portion of the first dielectric layer in the second device region. A portion of the remaining second dielectric layer is removed to form a first spacer on the second dielectric layer on the sidewall of the first gate. A portion of the first dielectric layer is removed to form a second spacer on the sidewall of the second gate. The first spacer and the remaining second dielectric layer between the first spacer and the first gate together form a third spacer.

16 Claims, 2 Drawing Sheets





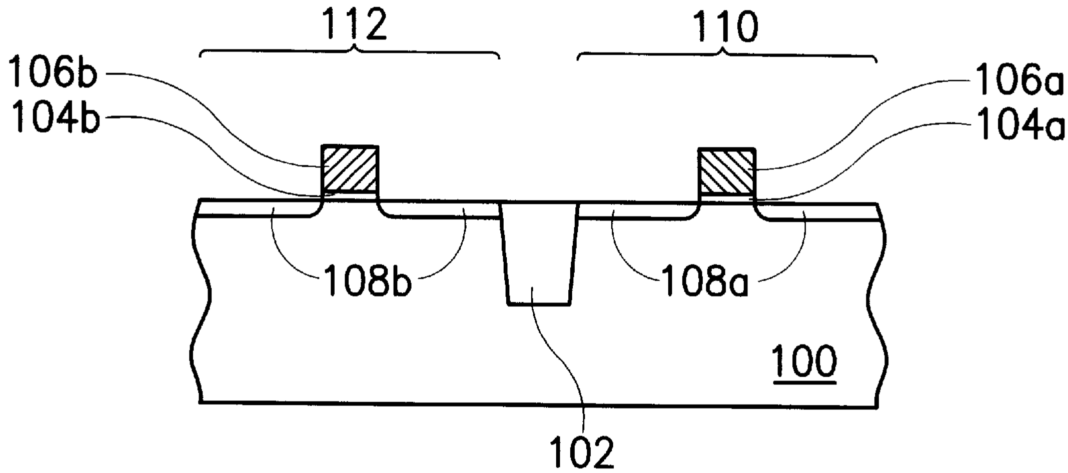


FIG. 1

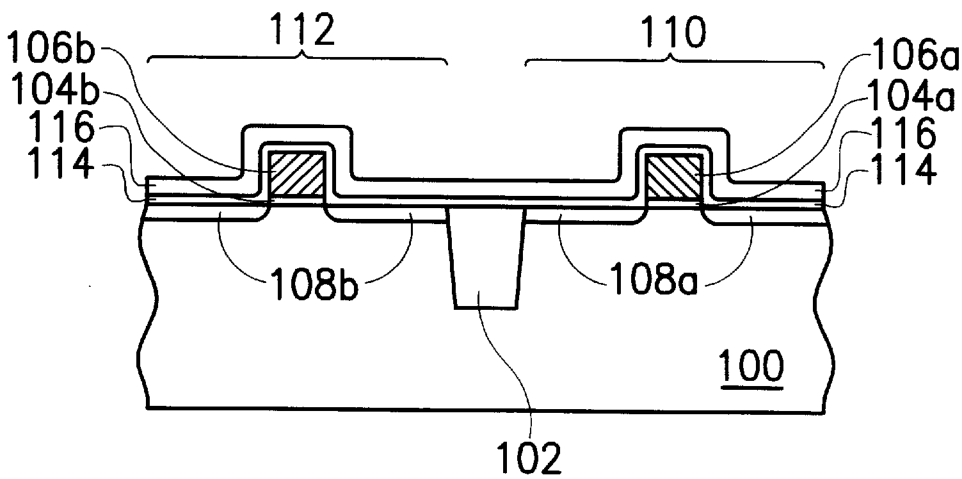


FIG. 2

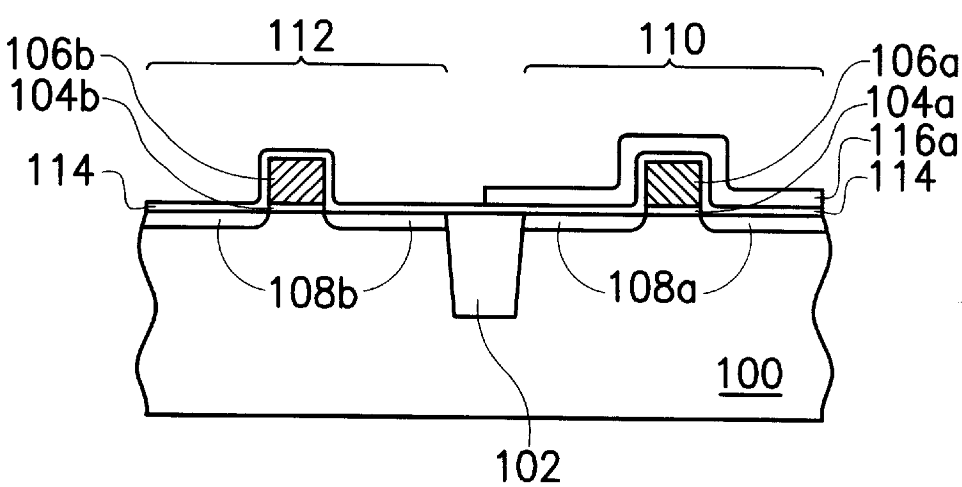
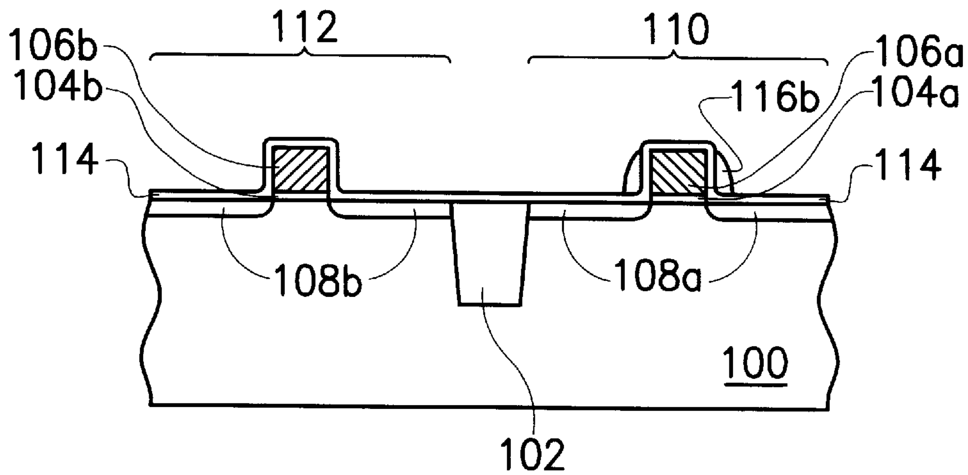
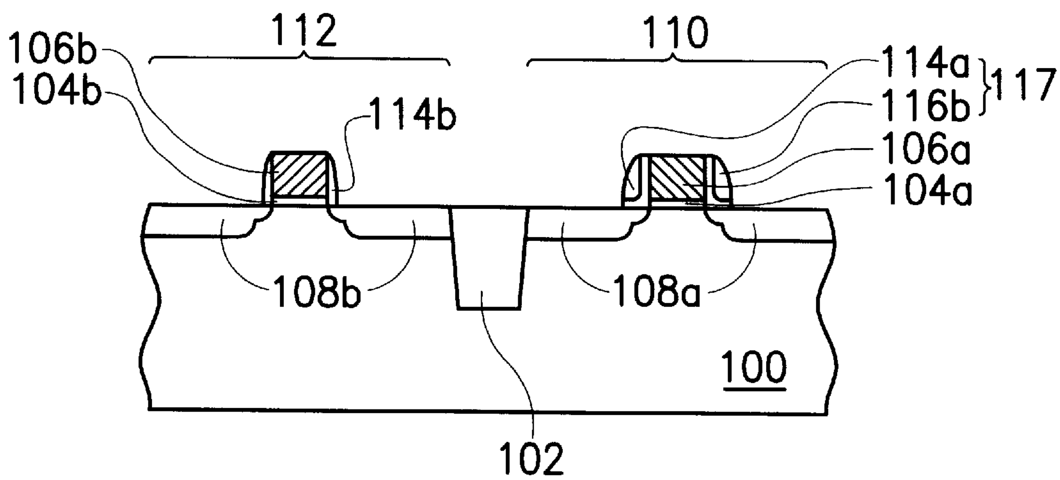


FIG. 3



112
110
106b
104b
114
106a
116b
104a
114
108b
108a
100
102

FIG. 4



112
110
106b
104b
114b
114a
116b
117
106a
104a
108b
108a
100
102

FIG. 5

METHOD FOR MANUFACTURING DUAL-SPACER STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to a method for manufacturing a field effect transistor (FET). More particularly, the present invention relates to a method for manufacturing a FET with a dual-spacer structure.

2. Description of Related Art

When the integration of the device is increased, the energy consumption of the NMOS becomes a main problem in producing and designing integrated circuit by using NMOS as a basic element. Therefore, the COMS with a low-energy-consumption advantage is used to replace NMOS and to be a main element in manufacturing the devices.

However, because different type dopants with different diffusion rate, such as the diffusion rate of the P-type dopants is faster than that of the N-type dopants, the dopant diffusion in each source/drain region is uneven at the annual step in the formation of the source/drain region in the coexist P-type FET and N-type FET. Since the dopant diffusion of each source/drain region result is unequal, the short channel effect happens in the P-type FET when the source/drain region in N-type FET is not yet formed.

In order to improve the unequal diffusion rate mentioned above, different types of dopants with different dosage are used in the implantation process to adjust the diffusion rate of different types of dopants. Nevertheless, it is difficult to accurately control this diffusion-rate adjustment so that the shape of the source/drain region cannot be well controlled.

SUMMARY OF THE INVENTION

The invention provides a method of manufacturing a field effect transistor with a dual-spacer structure. A substrate having a first device region and a second device region is provided. The first device region comprises a first gate formed over the substrate and the second device region comprises a second gate formed over the substrate. A first dielectric layer is formed over the substrate. A second dielectric layer is formed on the first dielectric layer. A portion of the second dielectric layer is removed to expose a portion of the first dielectric layer in the second device region. A portion of the remaining second dielectric layer is removed to form a first spacer on the second dielectric layer on the sidewall of the first gate. A portion of the first dielectric layer is removed to form a second spacer on the sidewall of the second gate. The first spacer and the remaining second dielectric layer between the first spacer and the first gate together form a third spacer.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

FIGS. **1** through **5** are schematic, cross-sectional views of the process for manufacturing a FET with a dual-spacer structure in a preferred embodiment according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. **1** through **5** are schematic, cross-sectional views of the process for manufacturing a FET with a dual-spacer structure in a preferred embodiment according to the invention.

As shown in FIG. **1**, a substrate **100** with a first device region **110** and a second device region **112** is provided. The first device region **110** is isolated from the second device region **112** by an isolation structure **102**. The substrate **100** is made of silicon, for example. In the first device region **110**, a first gate dielectric layer **104***a* is formed on the substrate **100** and a first gate **106***a* is formed on the first gate dielectric layer **104***a*. Similarly, in the second device region **112**, a second gate dielectric layer **104***b* is formed on the substrate **100** and a second gate **106***b* is formed on the second gate dielectric layer **104***b*. The first gate dielectric layer **104***a* and the second gate dielectric layer **104***b* are formed from silicon oxide by thermal oxidation, for example. The first gate **106***a* and the second gate **106***b* are formed from doped polysilicon, metal silicide or doped polysilicon/silicide by chemical vapor deposition (CVD), for example.

Moreover, the first device region can be a P-type FET region or a high voltage device such as I/O region, for example. The second device region can be an N-type FET region or a low voltage device such as core region, for example.

A first lightly doped drain (LDD) region **108***a* and a second LDD region **108***b* are respectively formed at the first device region **110** and the second device region **112** in the substrate **100** by using the first gate **106***a* and the second gate **106***b* as mask layers. The first and the second LDD regions **108***a* and **108***b* are formed by implanting arsenic ions or phosphorus ions into the substrate **100** with a dosage of about 5E12–5E14 ions/cm^2 and under an energy of about 40–80 KeV, for example.

As shown in FIG. **2**, a dielectric layer **114** is formed over the substrate **100**. The dielectric layer **114** is formed from silicon oxide by CVD, for example. A dielectric layer **116** is formed on the dielectric layer **114**. The dielectric layer **116** is made of silicon nitride, for example.

As shown in FIG. **3**, a portion of the dielectric layer **116** in the second device region **112** is removed to expose a portion of the dielectric layer **114**. The remaining dielectric layer **116** in the first device region **110** is denoted as dielectric layer **116***a*. The method for removing the portion of the dielectric layer **116** can be photolithography, for example. Preferably, the method for removing the portion of the dielectric layer **116** comprises dry etching or the wet etching, for example.

As shown in FIG. **4**, a portion of the dielectric layer **116***a* in the first device region **110** to form a first spacer **116***b* on dielectric layer **114** located at the sidewall of the gate **106***a* and gate dielectric layer **104***a*. The method for removing the portion of the dielectric layer **116***a* is anisotropic etching, for example. The zenith of the first spacer **116***b* is at the same level as the top surface of the gate **106***a*.

As shown in FIG. **5**, a portion of the dielectric layer **114** is removed to form a second spacer **114***b* on the sidewall of the gate **106***b* and the gate dielectric layer **104***b* and to expose a portion of the substrate **100**. A remaining dielectric layer **114***a* is left between the first spacer **116***b* and the first gate **106***a*. The remaining layer **114***a* and the first spacer **116***b* together form a third spacer **117**. The method for removing the portion of the dielectric layer **114** is anisotropic etching, for example. Preferably, the anisotropic etching is performed with CF_4 plasma, for example.

An implantation process is performed to form a first source/drain region **118***a* and a second source/drain region **118***b* in the substrate exposed by the first gate **106***a*, the third spacer **117**, the second gate **106***b* and the second spacer **114***b*.

Since the thickness of the third spacer **117** and the second spacer **114***b* can be adjusted by the diffusion rate of the implanted ions, the shape of the doped region after the anneal process can be well controlled. When the diffusion rate of the implanted ions is relatively fast, the spacer used as a mask in the implantation process is relatively thick so that the distance between the source/drain can be enlarged. Therefore, the shape of the source/drain with implanted ions possess relative fast diffusion rate can be well controlled and the short channel effect can be avoided. On the other hand, when the diffusion rate of the implanted ions is relatively slow, the spacer used as a mask in the implantation process is relatively thin so that the distance between the source/drain is relatively short. Hence, the source/drain with implanted ions possess relative slow diffusion rate can be well shaped.

According to the present invention, the problem caused by different diffusion rate of the different-type implanted ions can be solved by adjusting the thickness of the spacer. Therefore, the dopants with different diffusion rate can evenly diffuse in the substrate and the shape of the source/drain region can be well controlled.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A method of manufacturing a field effect transistor with a dual-spacer structure, comprising the steps of:

providing a substrate having a first device region and a second device region, wherein the first device region comprises a first gate formed over the substrate and the second device region comprises a second gate formed over the substrate;

forming a first dielectric layer over the substrate;

forming a second dielectric layer on the first dielectric layer;

removing a portion of the second dielectric layer to expose a portion of the first dielectric layer in the second device region;

removing a portion of the remaining second dielectric layer to form a first spacer on the second dielectric layer on the sidewall of the first gate; and

removing a portion of the first dielectric layer to form a second spacer on the sidewall of the second gate, wherein the first spacer and the remaining second dielectric layer between the first spacer and the first gate together form a third spacer.

2. The method of claim **1**, wherein the first dielectric layer is made of silicon oxide.

3. The method of claim **1**, wherein the second dielectric layer is made of silicon nitride.

4. The method of claim **1**, wherein the first device region is a P-type field effect transistor region.

5. The method of claim **1**, wherein a first voltage used in the first device region is higher than a second voltage used in the second region.

6. The method of claim **1**, wherein the second device region is an N-type field effect transistor region.

7. The method of claim **1**, wherein the step of removing the remaining portion of the second dielectric layer comprises an anisotropic etching process.

8. The method of claim **1**, wherein the step of removing the first dielectric layer comprises an anisotropic etching process.

9. A method of manufacturing a field effect transistor with a dual-spacer structure, comprising the steps of:

providing a substrate having a plurality of gate formed thereon;

forming a first dielectric layer over the substrate;

forming a second dielectric layer on the first dielectric layer;

removing a portion of the second dielectric layer to expose a specific region of the first dielectric layer;

removing a portion of the remaining second dielectric layer to form a first spacer on the second dielectric layer on the sidewall of a portion of the gates in the specific region; and

removing a portion of the first dielectric layer to form a second spacer on the sidewall of the gates excluding the gates with the first spacer, wherein the first spacer and the remaining second dielectric layer between the first spacer and the first gate together form a third spacer.

10. The method of claim **9**, wherein the first dielectric layer is made of silicon oxide.

11. The method of claim **9**, wherein the second dielectric layer is made of silicon nitride.

12. The method of claim **9**, wherein the specific region is an N-type field effect transistor region.

13. The method of claim **9**, wherein a first voltage used in the specific region is lower than a second voltage used in a region excluding the specific region.

14. The method of claim **9**, wherein a region excluding the specific region is a P-type field effect transistor region.

15. The method of claim **9**, wherein the step of forming the first spacer comprises an anisotropic etching process.

16. The method of claim **9**, wherein the step of forming the second spacer comprises an anisotropic etching process.

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