US 20110032763A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2011/0032763 A1

(43) Pub. Date: Feb. 10, 2011

Kwak et al.

(54) SEMICONDUCTOR DEVICES INCLUDING FIRST AND SECOND BIT LINES

(75) Inventors: **Dong-Hwa Kwak**, Gyeonggi-do (KR); **Jae-Kwan Park**, Gyeonggi-do (KR); **Jae-Hwang Sim**, Seoul (KR); **Jin-Ho Kim**, Gyeonggi-do (KR); **Ki-Nam Kim**, Seoul (KR)

Correspondence Address:
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627 (US)

(73) Assignee: **Samsung Electronics Co., Ltd.**

(21) Appl. No.: **12/909,223**

(22) Filed: **Oct. 21, 2010**

Related U.S. Application Data

(62) Division of application No. 11/623,269, filed on Jan. 15, 2007, now Pat. No. 7,842,571.

(30) **Foreign Application Priority Data**

Oct. 19, 2006 (KR) 2006-0101957

Publication Classification

(51) **Int. Cl.**
G11C 16/04 (2006.01)

(52) **U.S. Cl.** **365/185.05**

(57) **ABSTRACT**

In some embodiments, a semiconductor device includes first bit lines connected to respective first contacts. Spacers are disposed on sidewalls of the first bit lines. A second bit line is self-alignedly disposed between adjacent spacers, and a second contact is self-aligned with and connected to the second bit line.

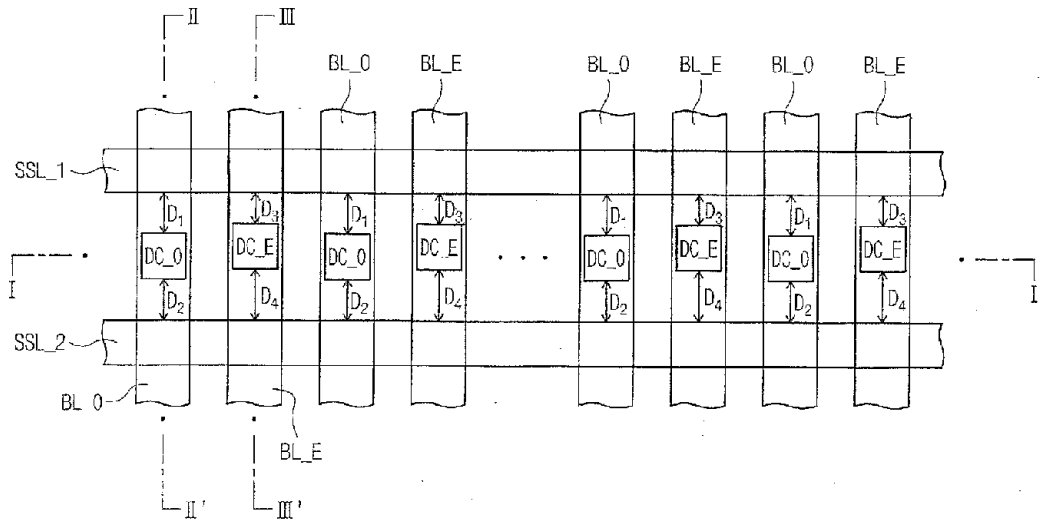


Fig. 1

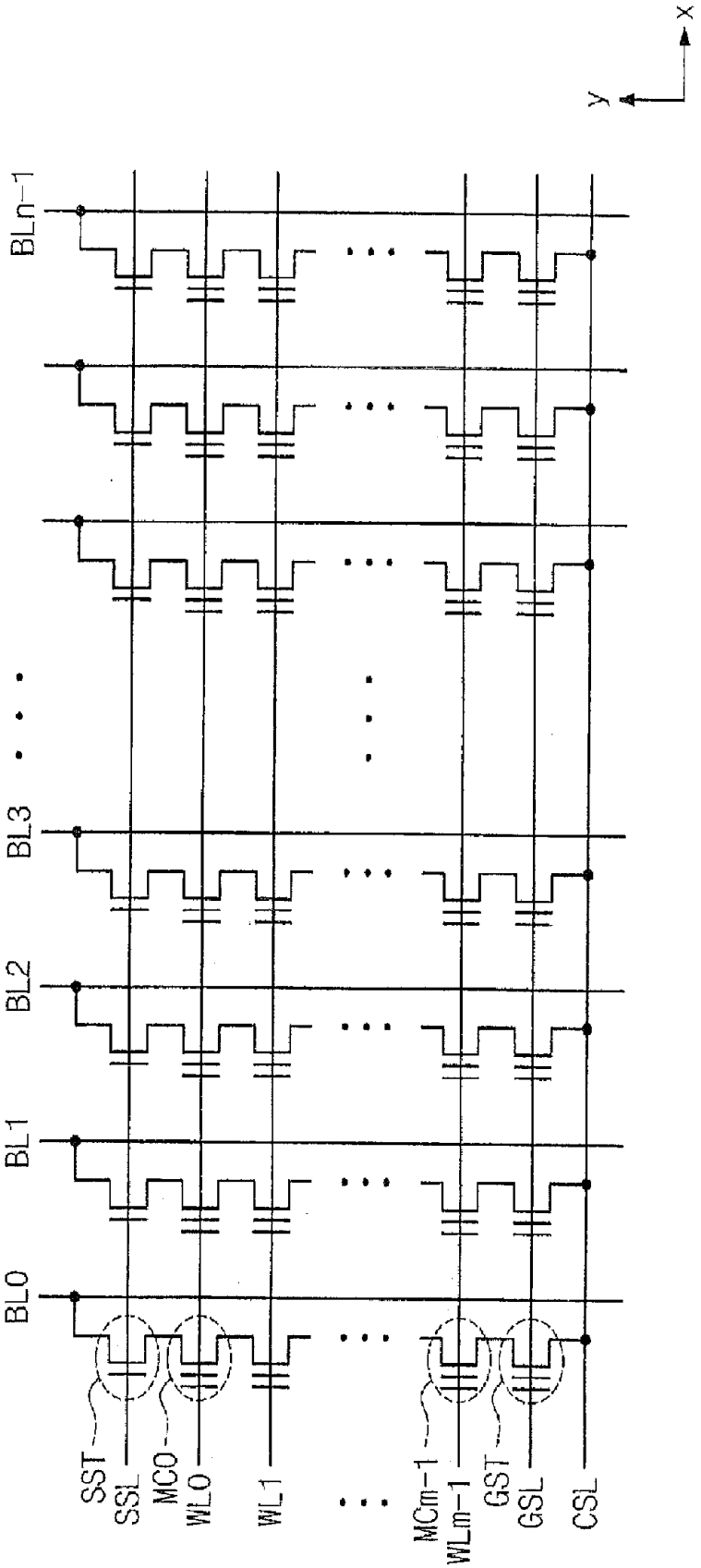

x
y
BLn-1
BL3
BL2
BL1
BL0
SST
SSL
MC0
WL0
WL1
MCm-1
WLm-1
GST
GSL
CSL

Fig. 2

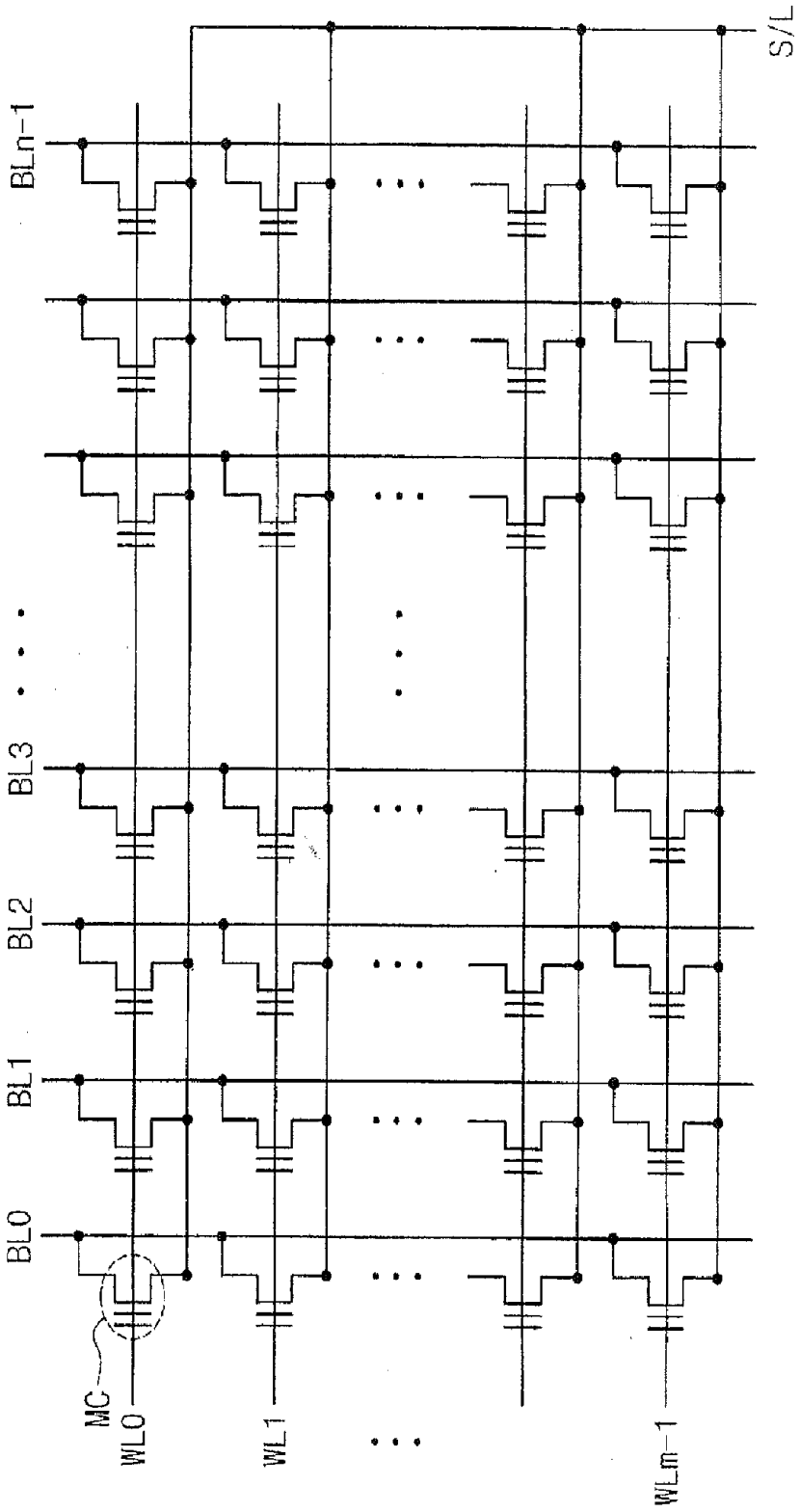


Fig. 3

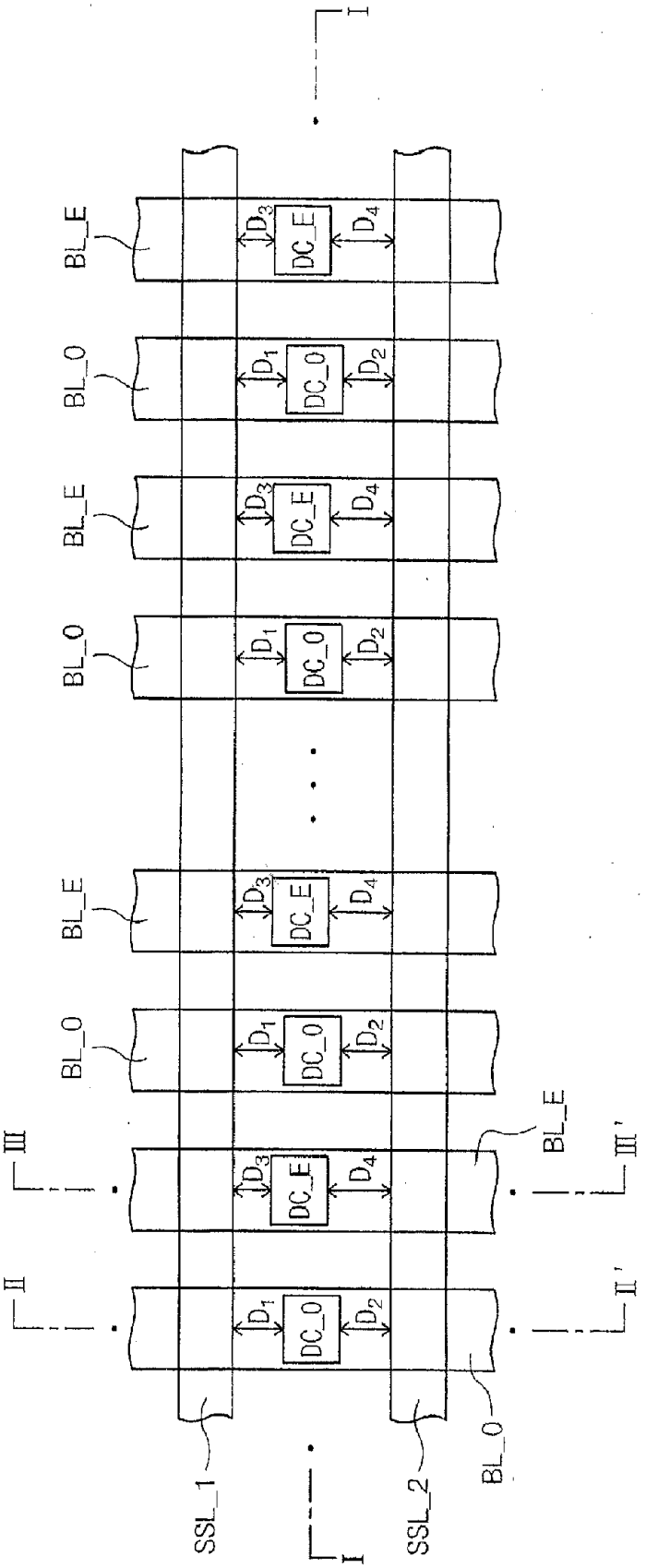


Fig. 4

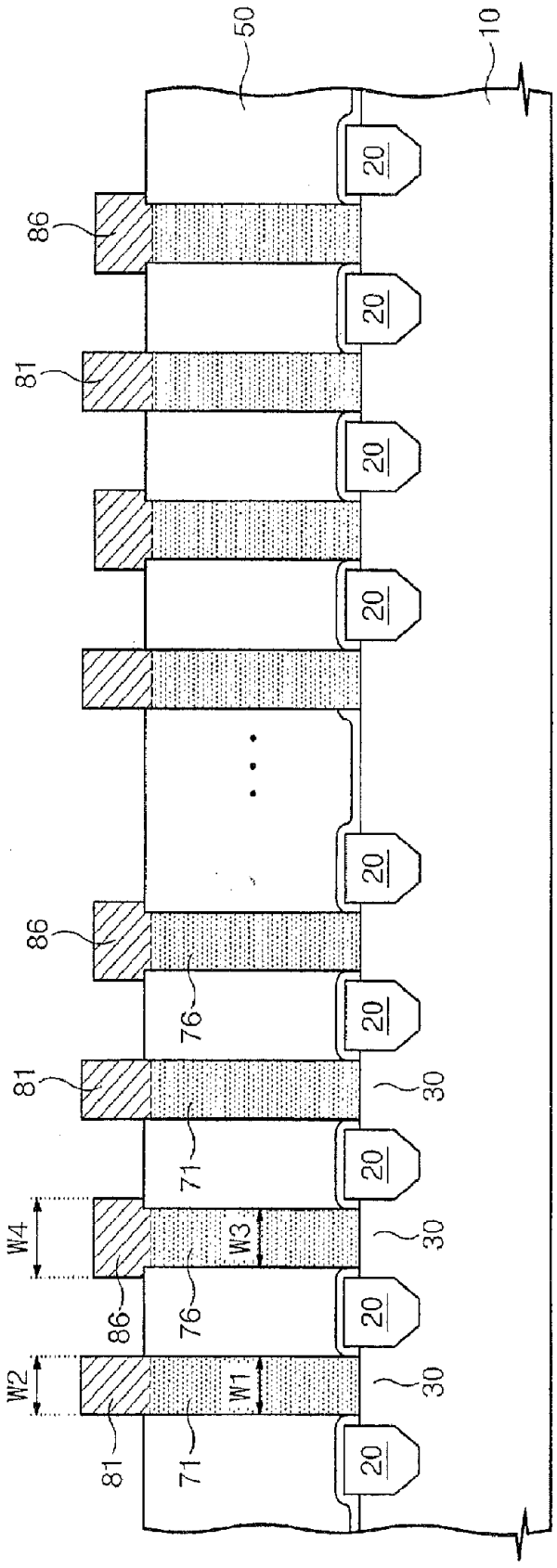


Fig. 5

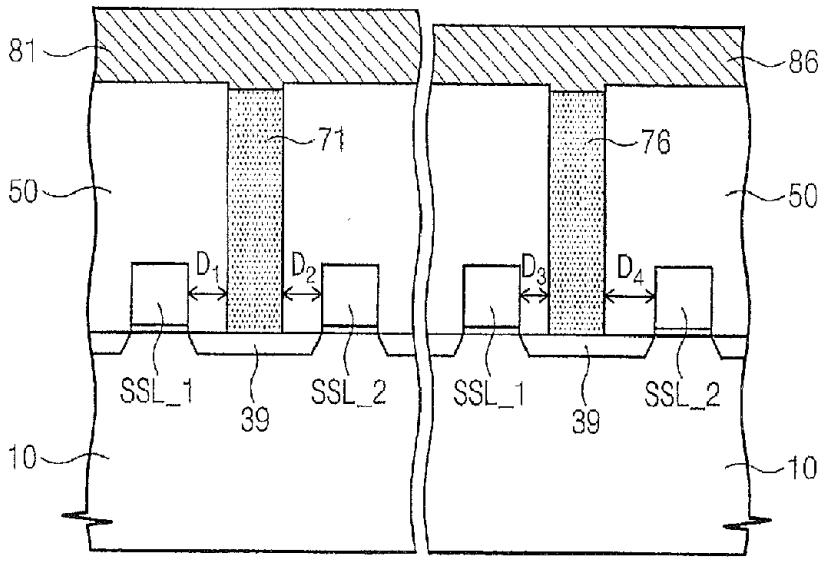

81
86
71
76
50
50
D_1
D_2
D_3
D_4
SSL_1
39
SSL_2
SSL_1
39
SSL_2
10
10

Fig. 6

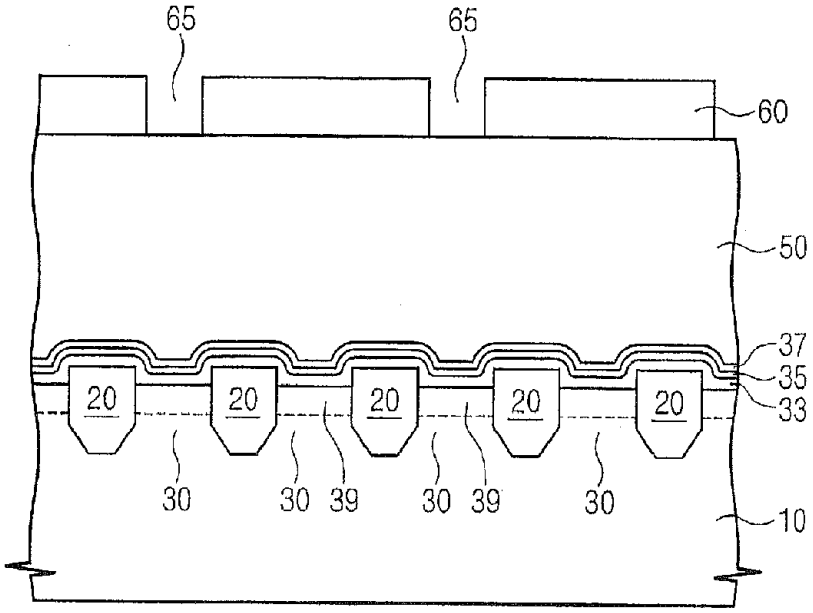

65
65
60
50
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 7

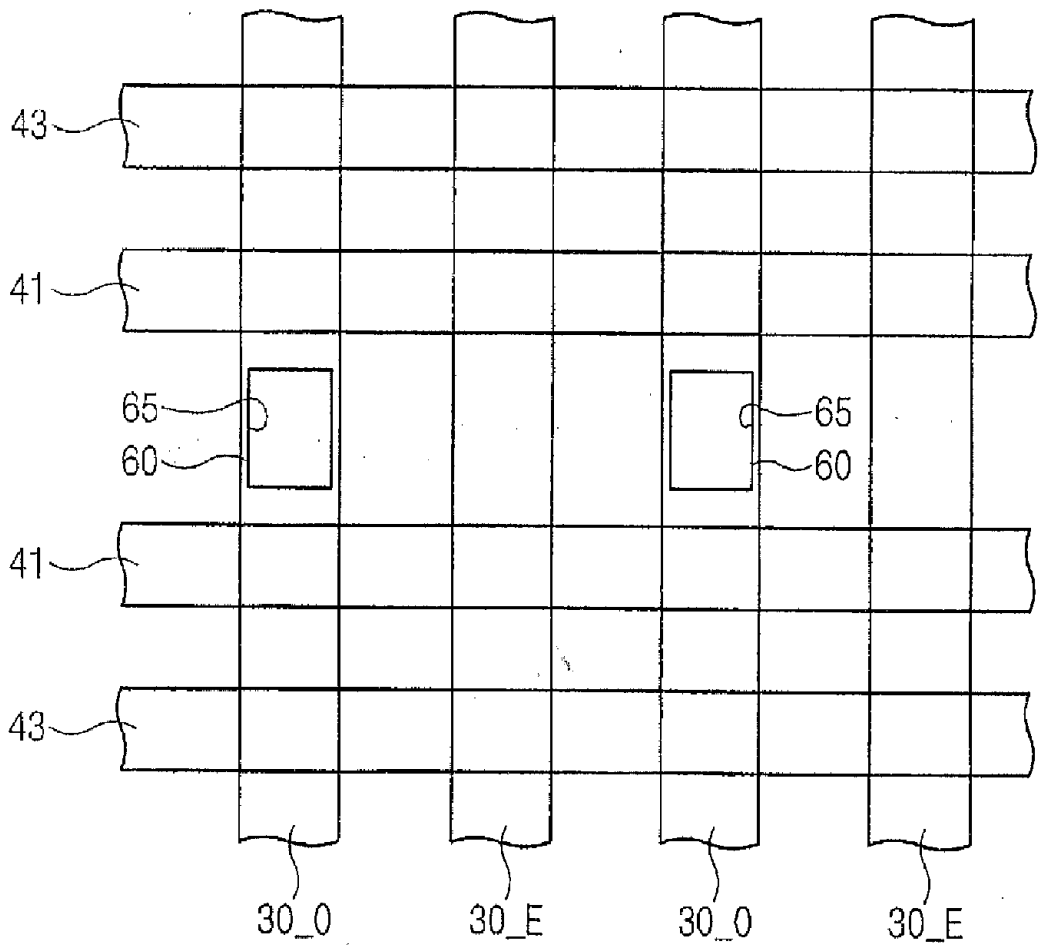


Fig. 8

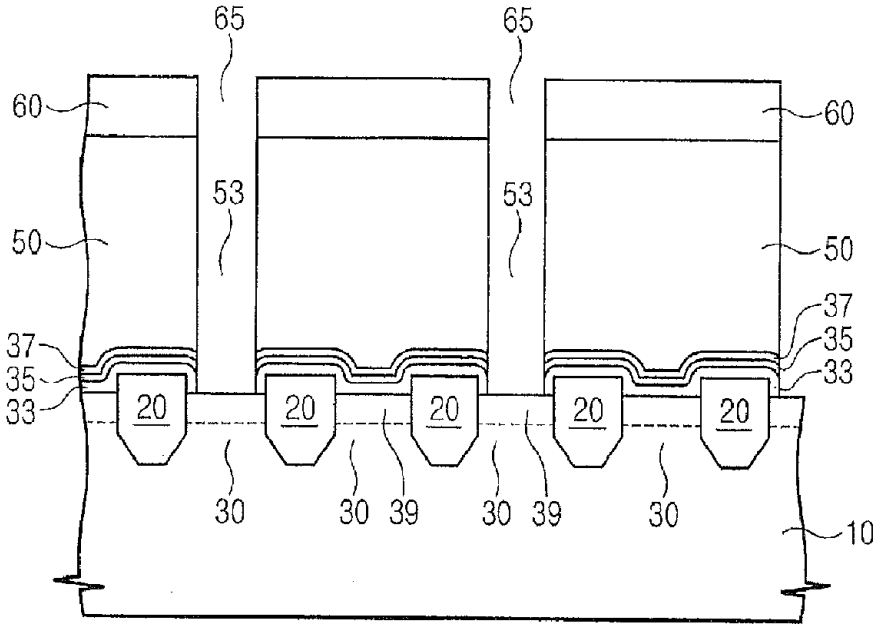

65
65
60
60
53
53
50
50
37
35
33
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 9

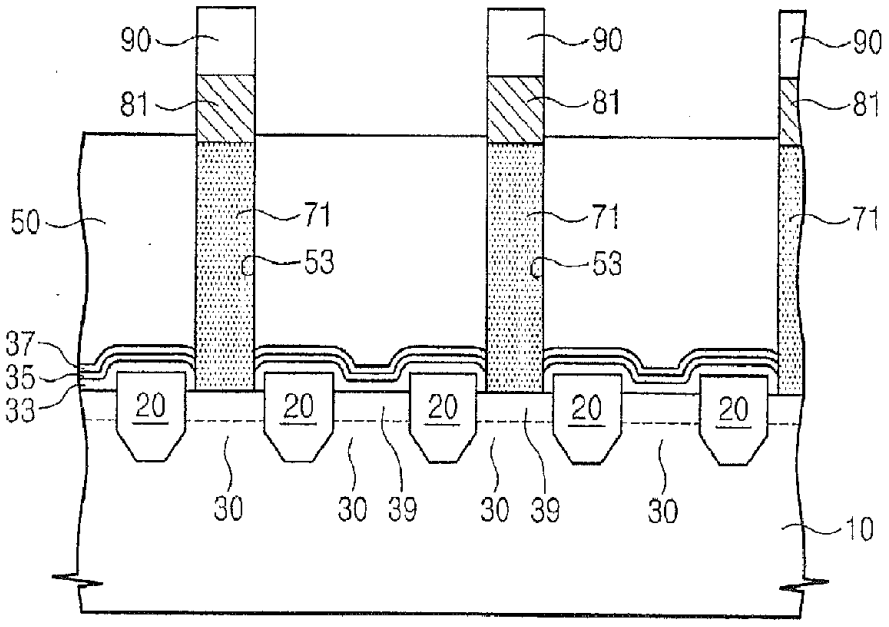

90
90
90
81
81
81
50
71
71
71
53
53
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 10

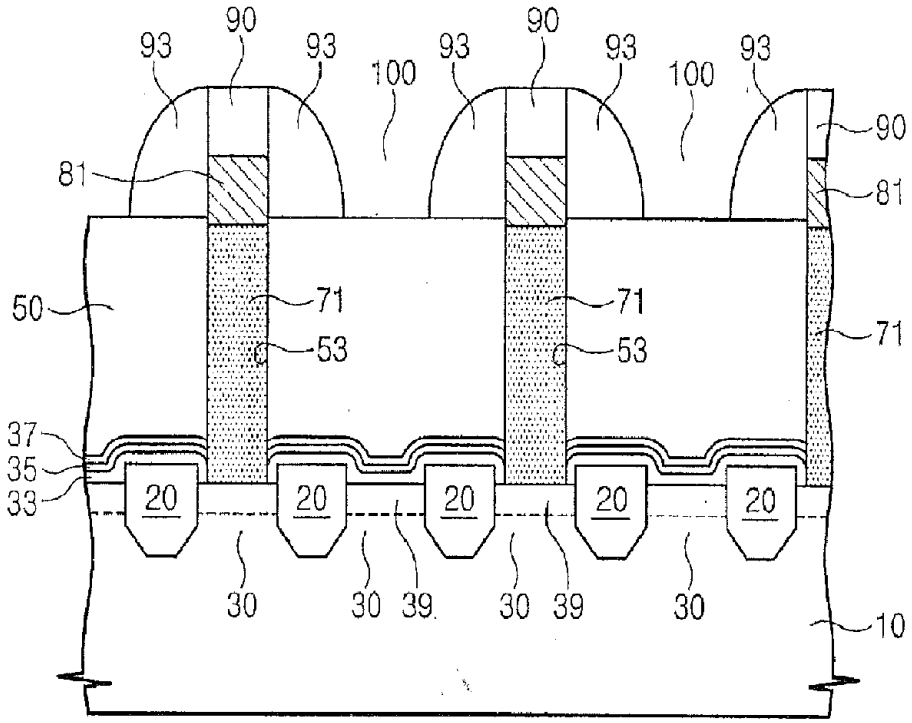

93
90
93
100
93
90
93
100
93
90
81
81
50
71
53
71
53
71
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 11

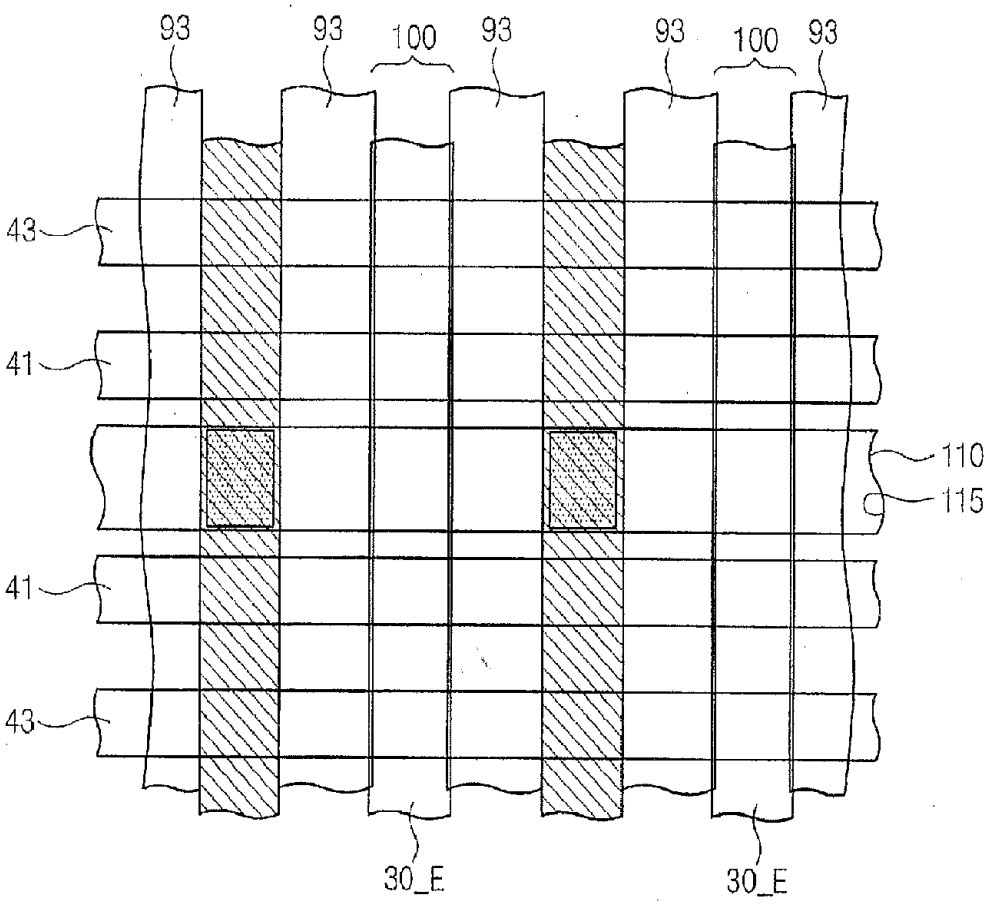


Fig. 12

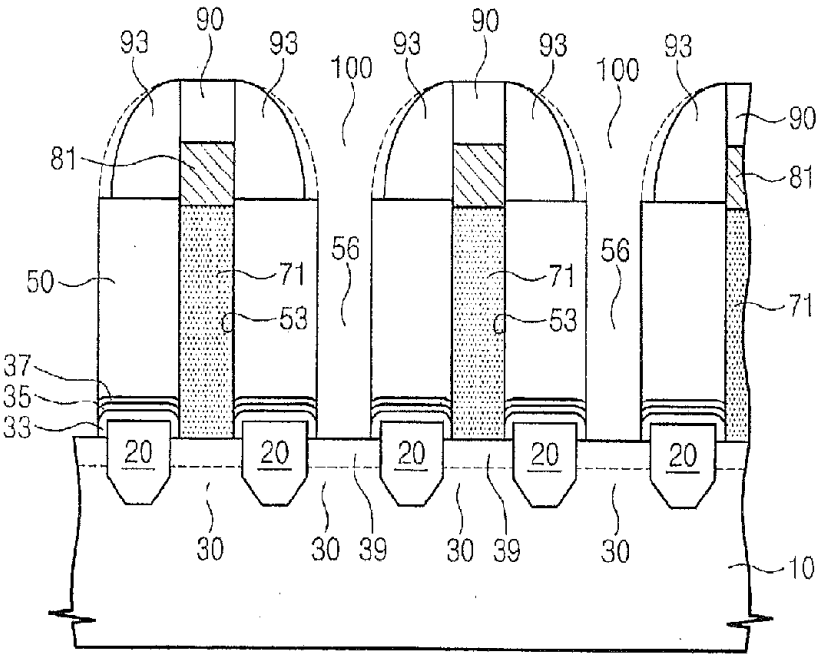

93
90
93
100
93
90
93
100
93
90
81
81
50
71
53
56
71
53
56
71
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 13

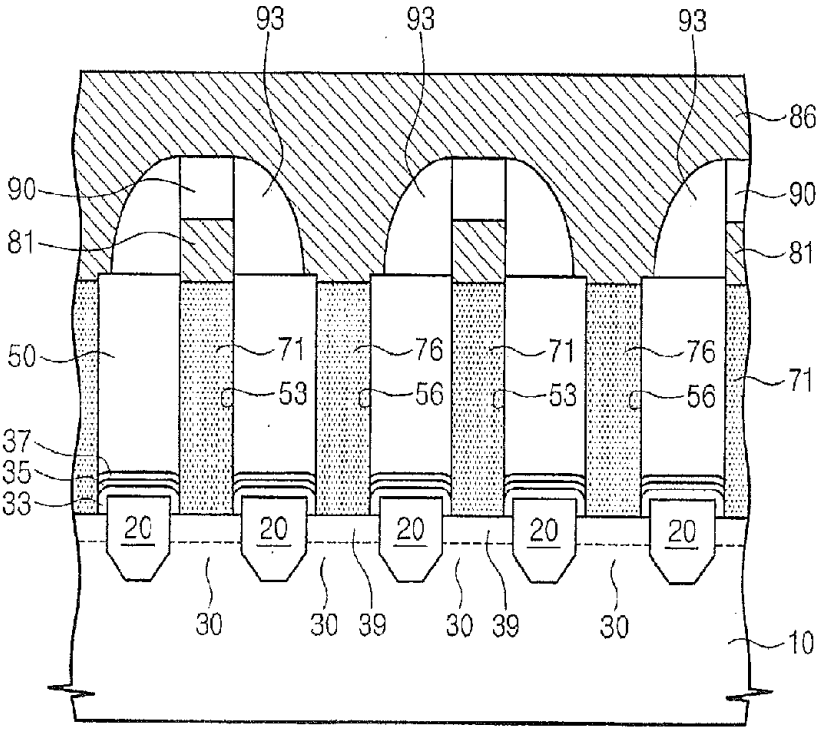

93
93
93
86
90
90
81
81
50
71
53
76
56
71
53
76
56
71
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 14

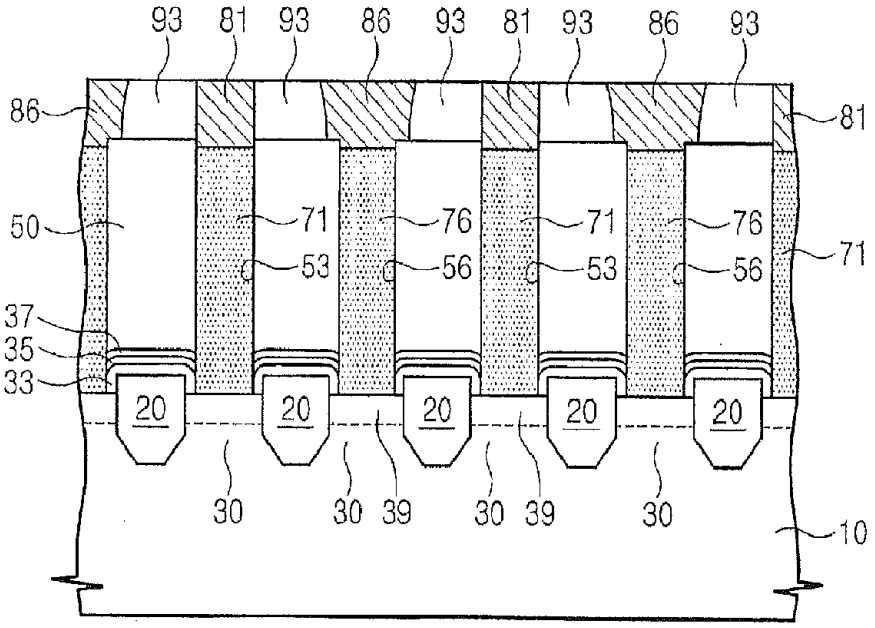

93
81
93
86
93
81
93
86
93
86
81
50
71
76
71
76
53
56
53
56
71
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 15

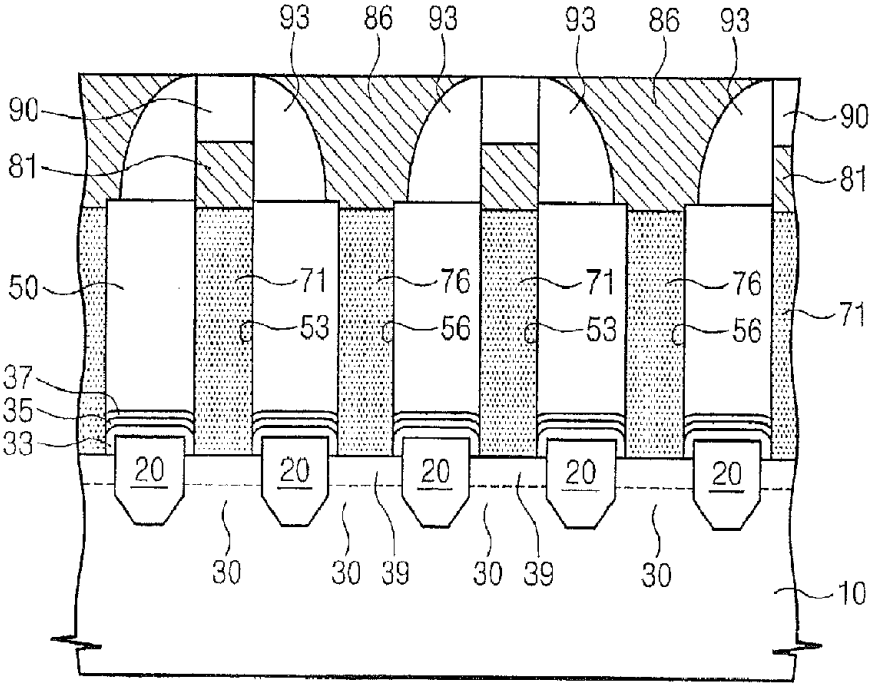

93
86
93
93
86
93
90
81
90
81
50
71
76
71
76
53
56
53
56
71
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 16

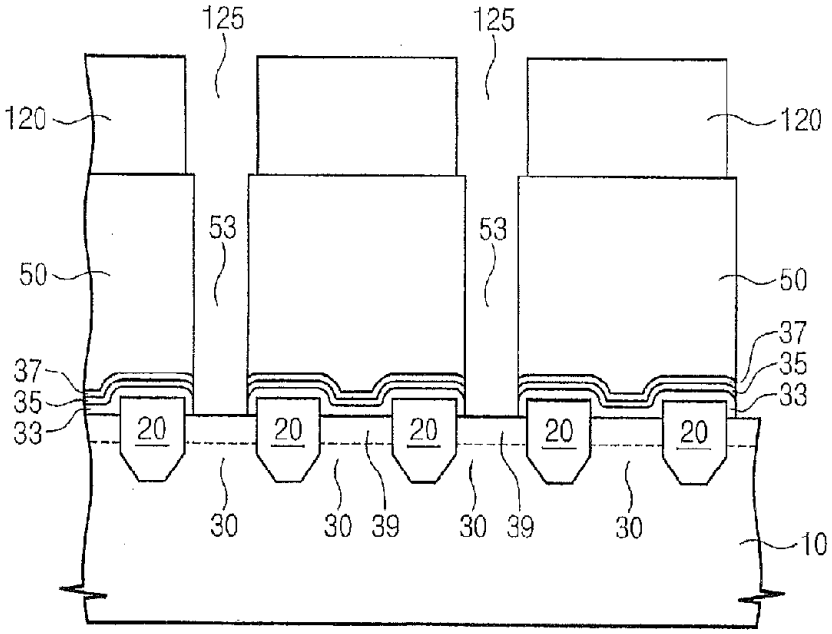

125
125
120
120
53
53
50
50
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 17

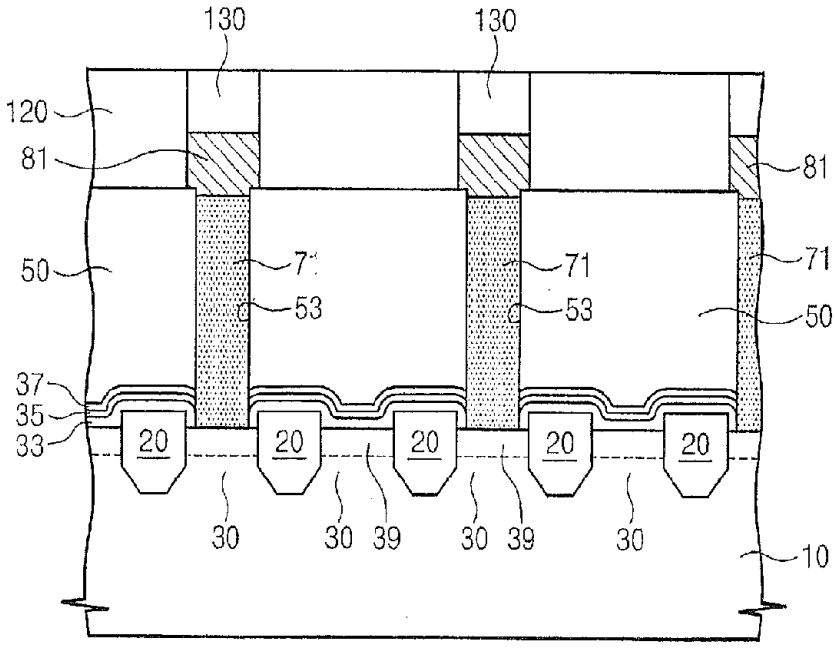

130
130
120
81
81
50
71
71
53
53
71
50
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 18

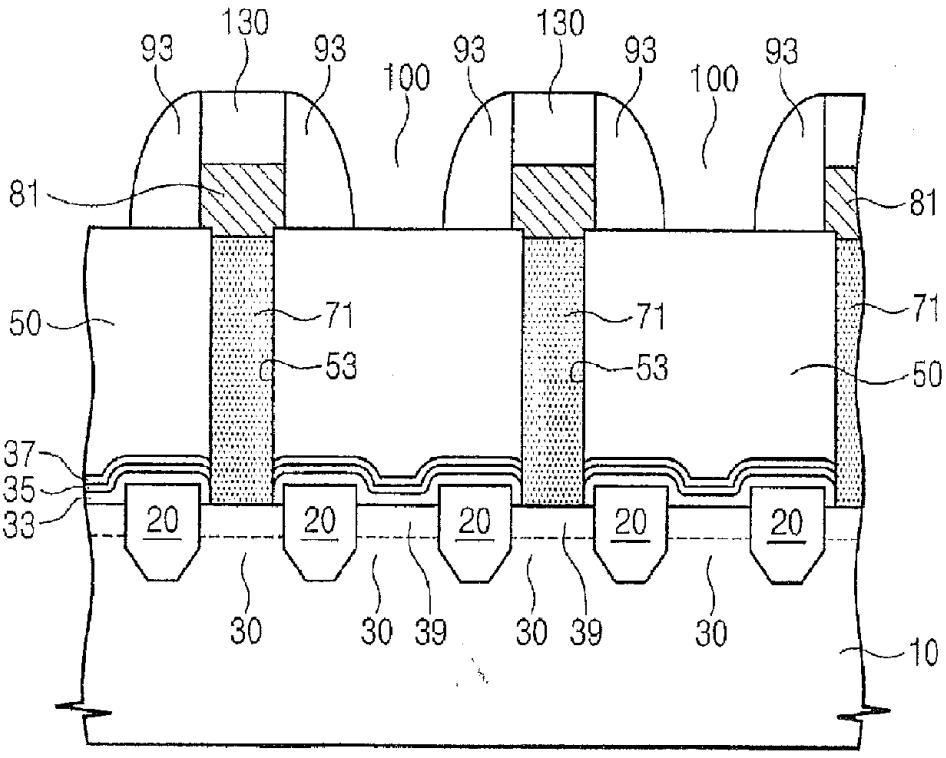

93
130
93
100
93
130
93
100
93
81
81
50
71
53
71
53
71
50
37
35
33
20
20
20
20
20
30
30
39
30
39
30
10

Fig. 19

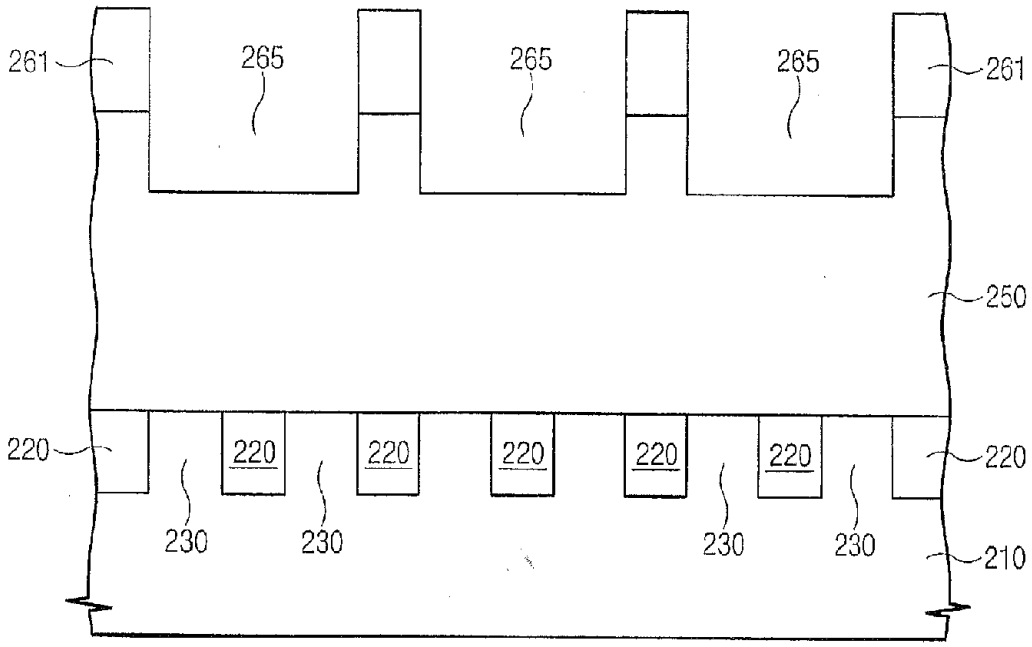

261
265
265
265
261
250
220
220
220
220
220
220
220
230
230
230
230
210

Fig. 20

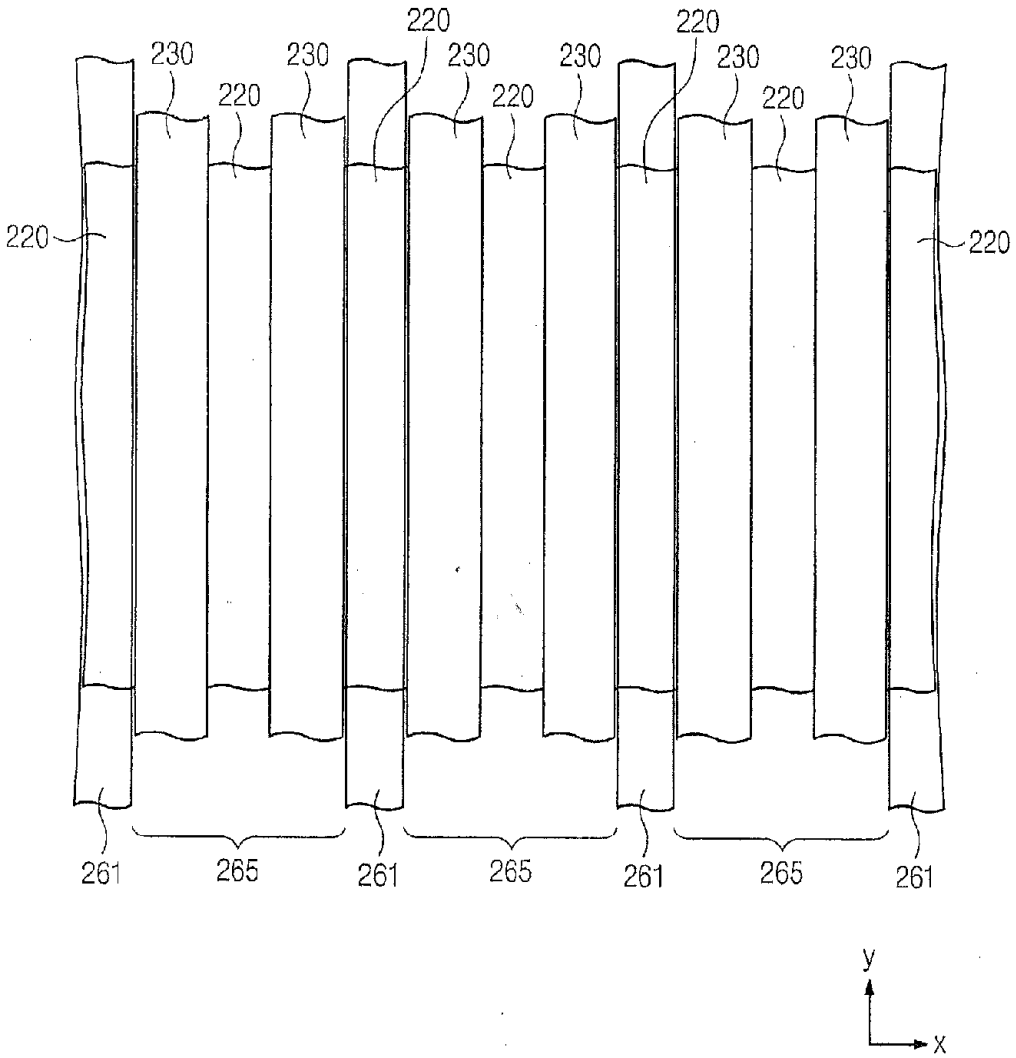

220
230
220
230
220
230
220
230
220
230
220
230
220
220
261
265
261
265
261
265
261
y
x

Fig. 21

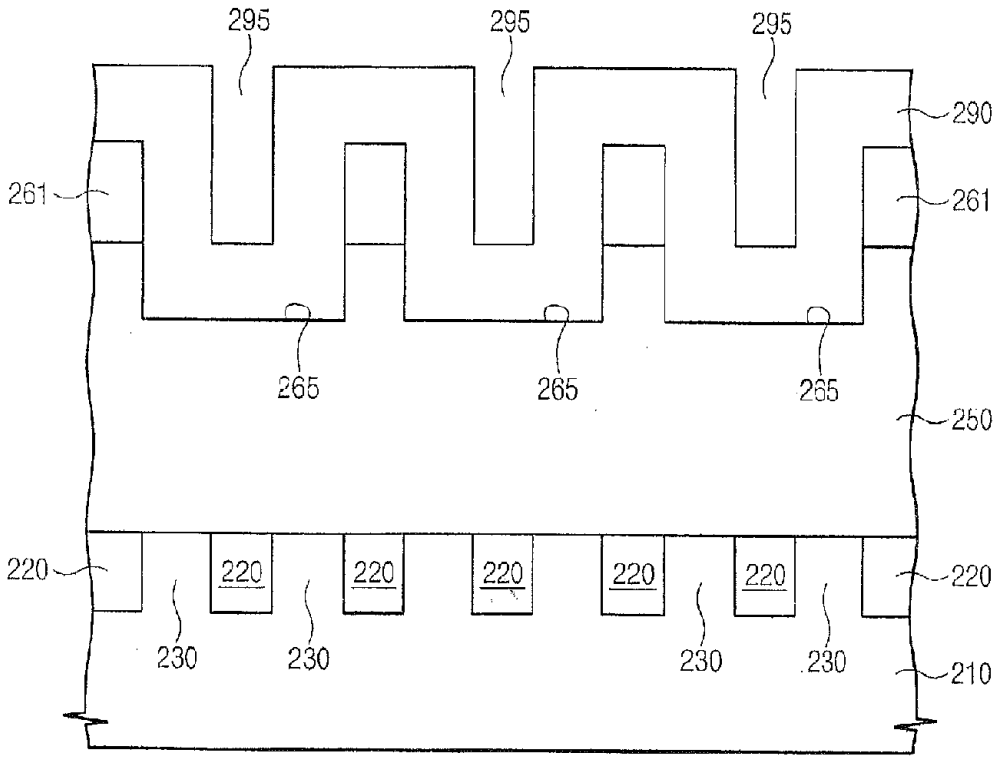

295
295
295
290
261
261
265
265
265
250
220
220
220
220
220
220
220
230
230
230
230
210

Fig. 22

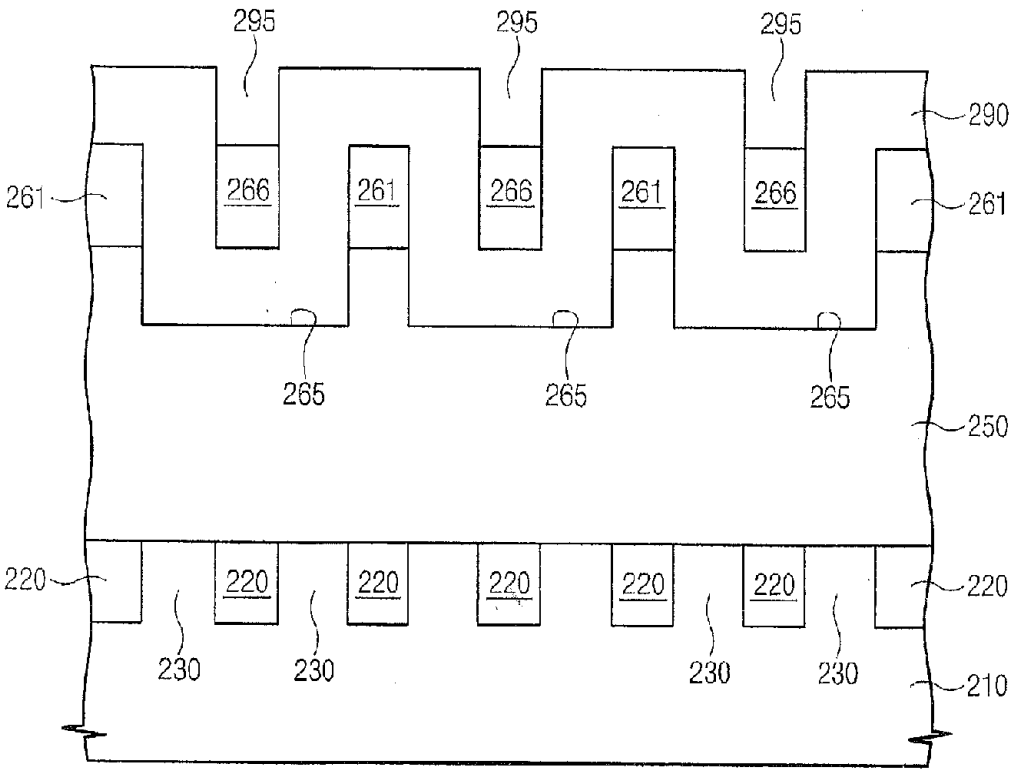

295
295
295
290
261
266
261
266
261
266
261
265
265
265
250
220
220
220
220
220
220
220
230
230
230
230
210

Fig. 23

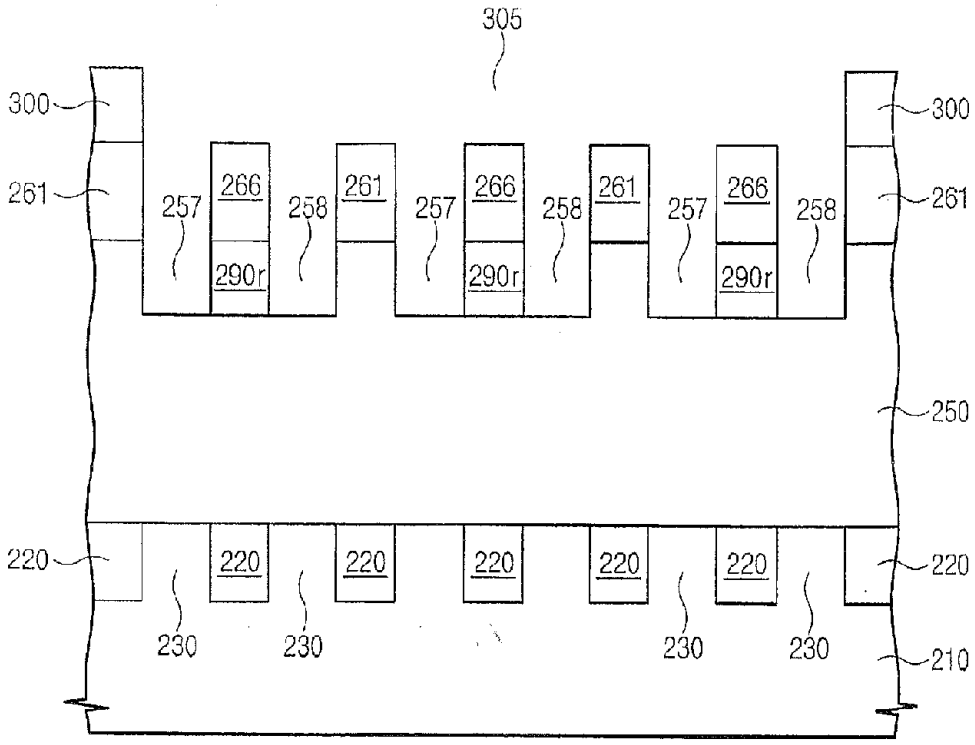

305
300
261
257
266
290r
258
261
257
266
290r
258
261
257
266
290r
258
300
261
250
220
220
220
220
220
220
220
230
230
230
230
210

Fig. 24

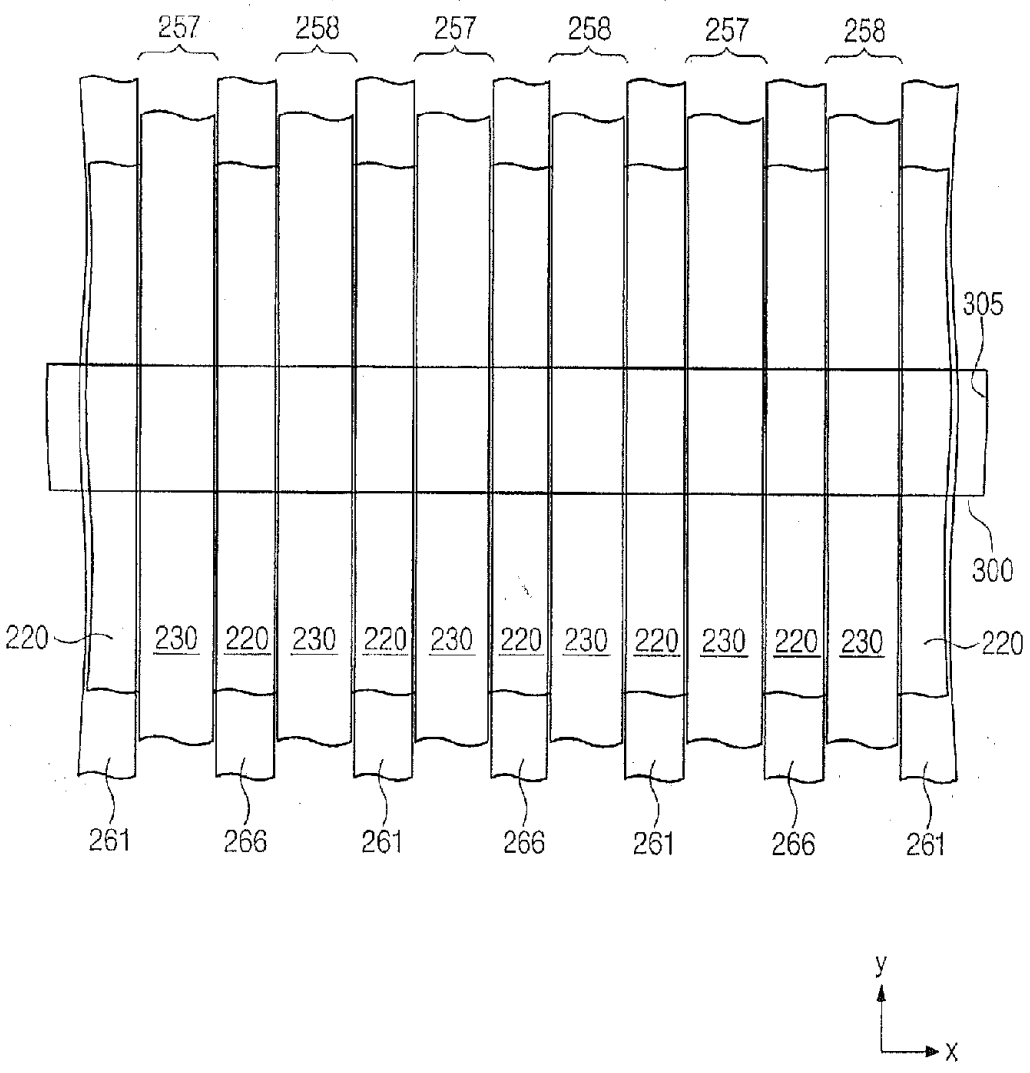


Fig. 25

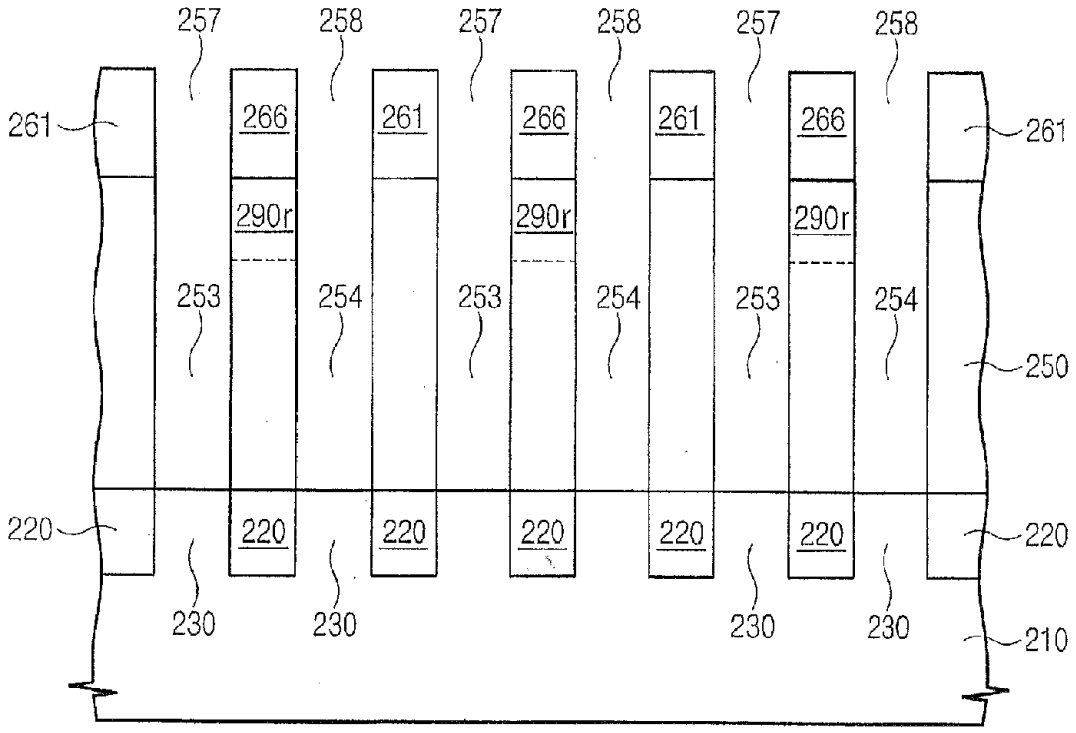

257
258
257
258
257
258
261
266
261
266
261
266
261
290r
290r
290r
253
254
253
254
253
254
250
220
220
220
220
220
220
220
230
230
230
230
210

Fig. 26

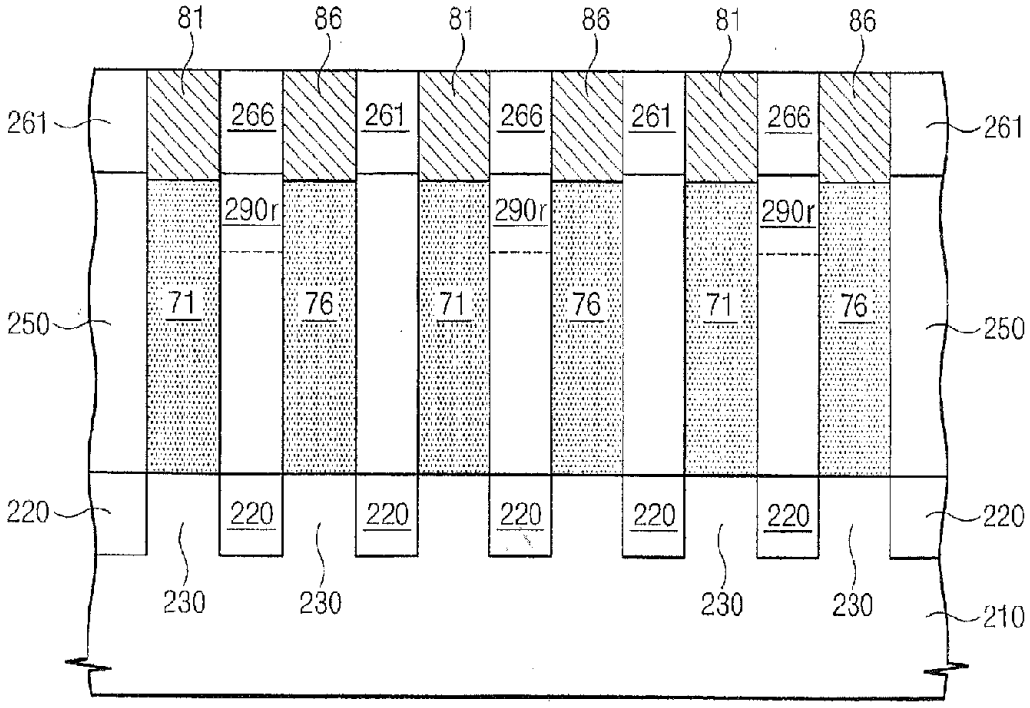

81
86
81
86
81
86
261
266
261
266
261
266
261
290r
290r
290r
250
71
76
71
76
71
76
250
220
220
220
220
220
220
230
230
230
230
210

Fig. 27

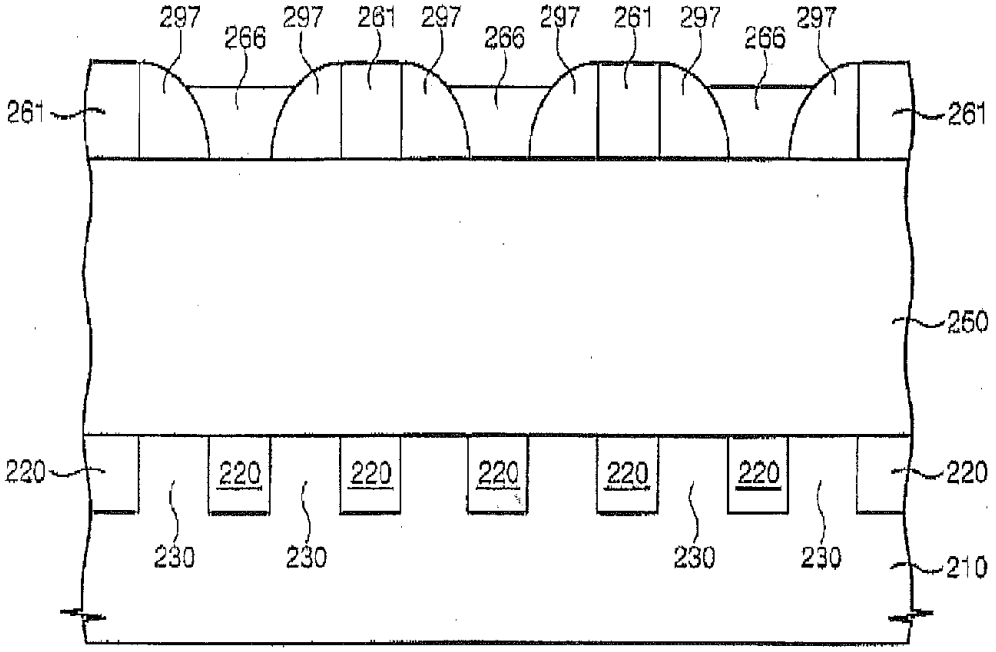

297
266
297
261
297
266
297
261
297
266
297
261
261
250
220
220
220
220
220
220
230
230
230
230
210

Fig. 28

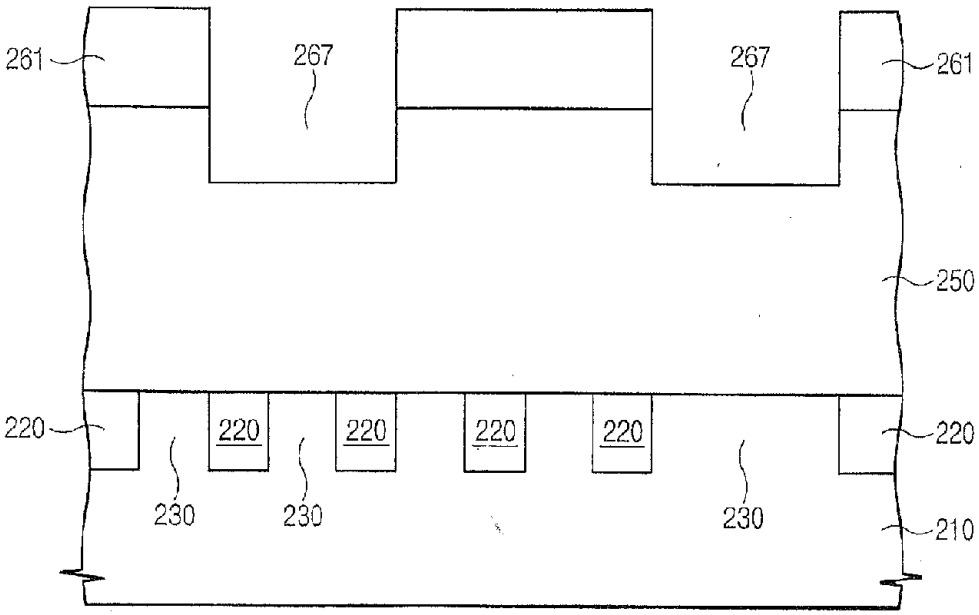


Fig. 29

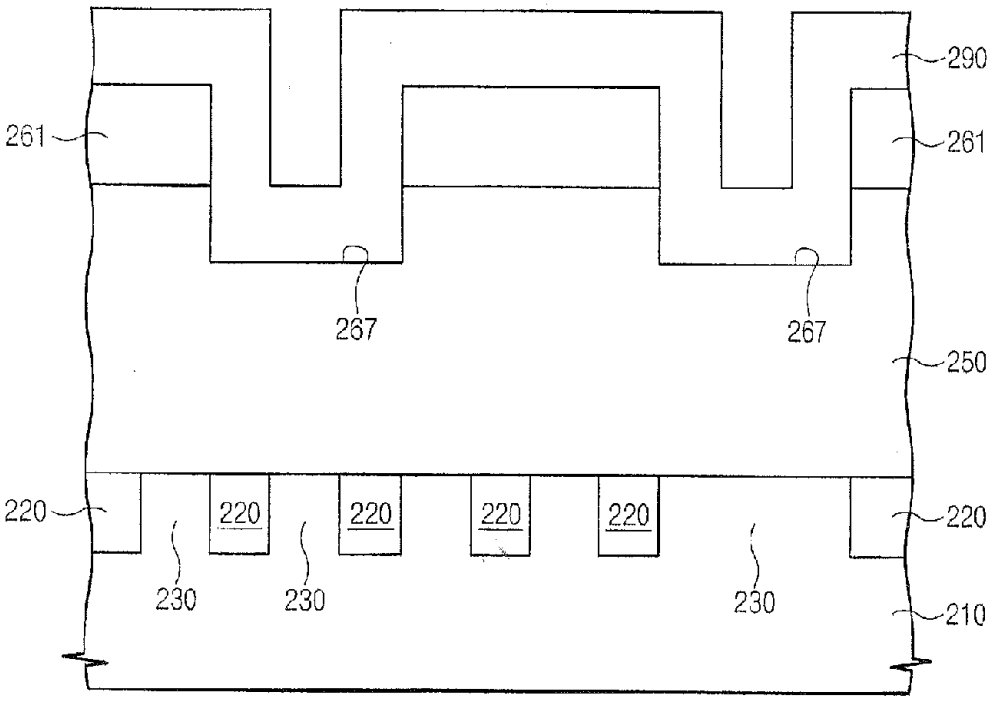


Fig. 30

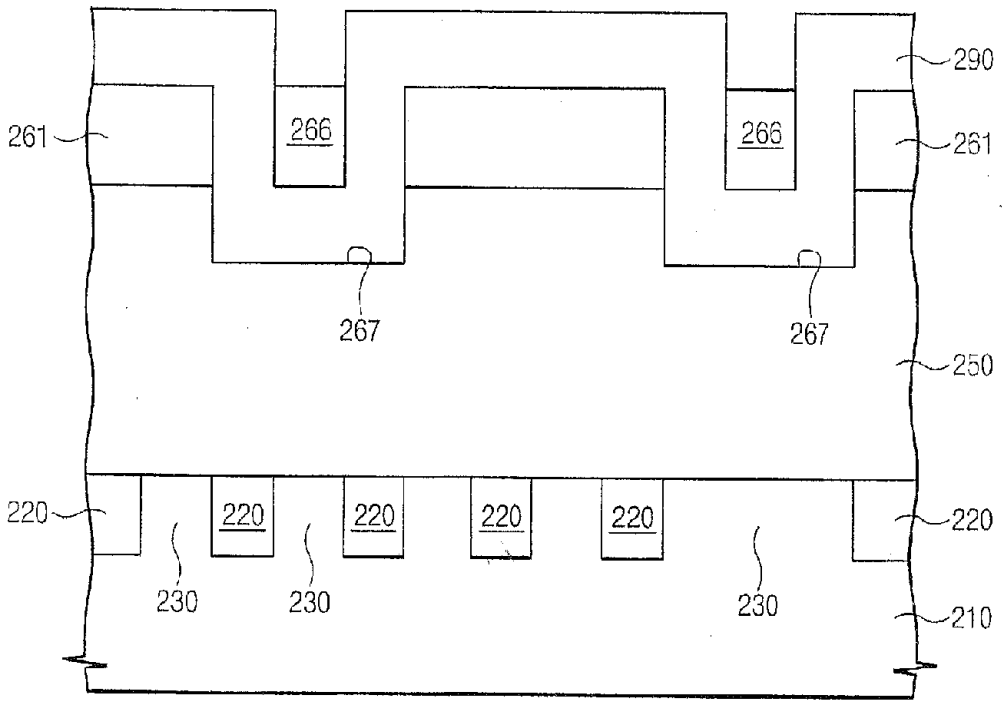

290
261
266
266
261
267
267
250
220
220
220
220
220
220
230
230
230
210

Fig. 31

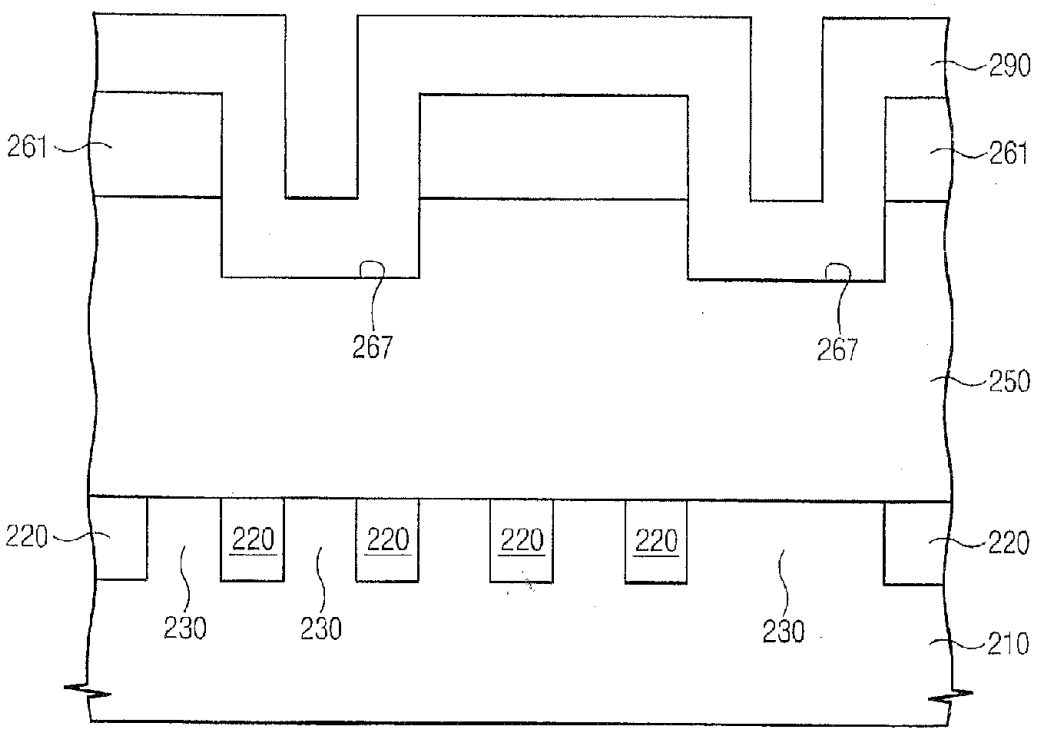


Fig. 32

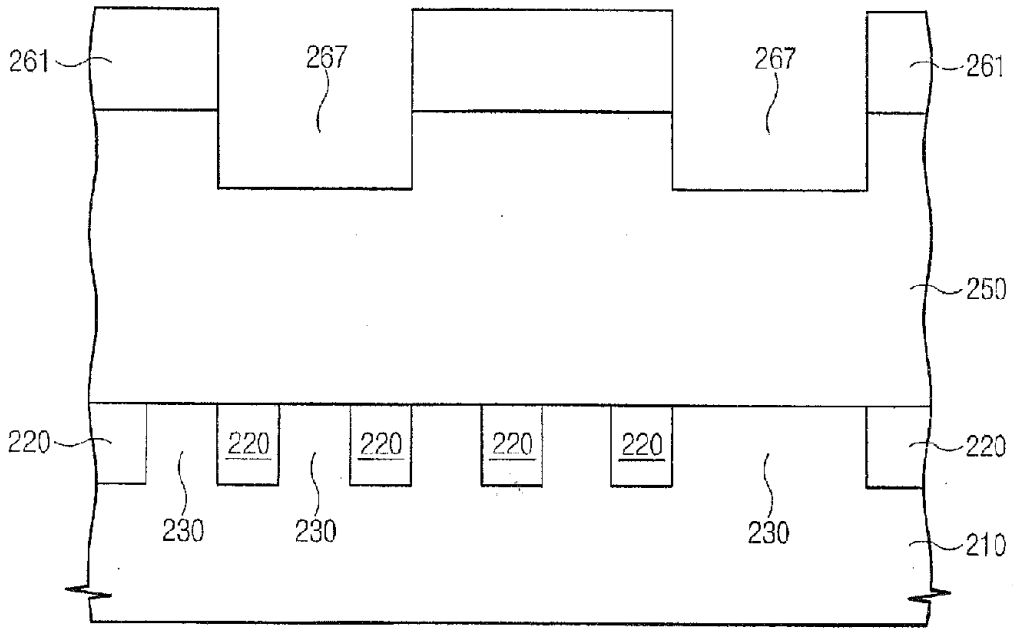


Fig. 33

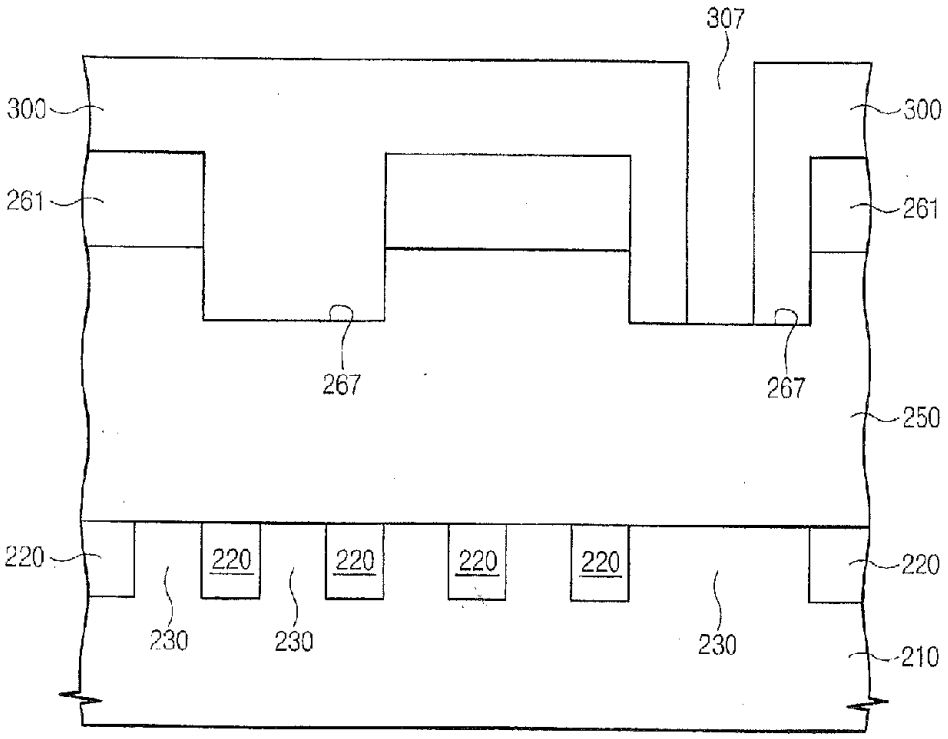

307
300
300
261
261
267
267
250
220
220
220
220
220
220
230
230
230
210

Fig. 34

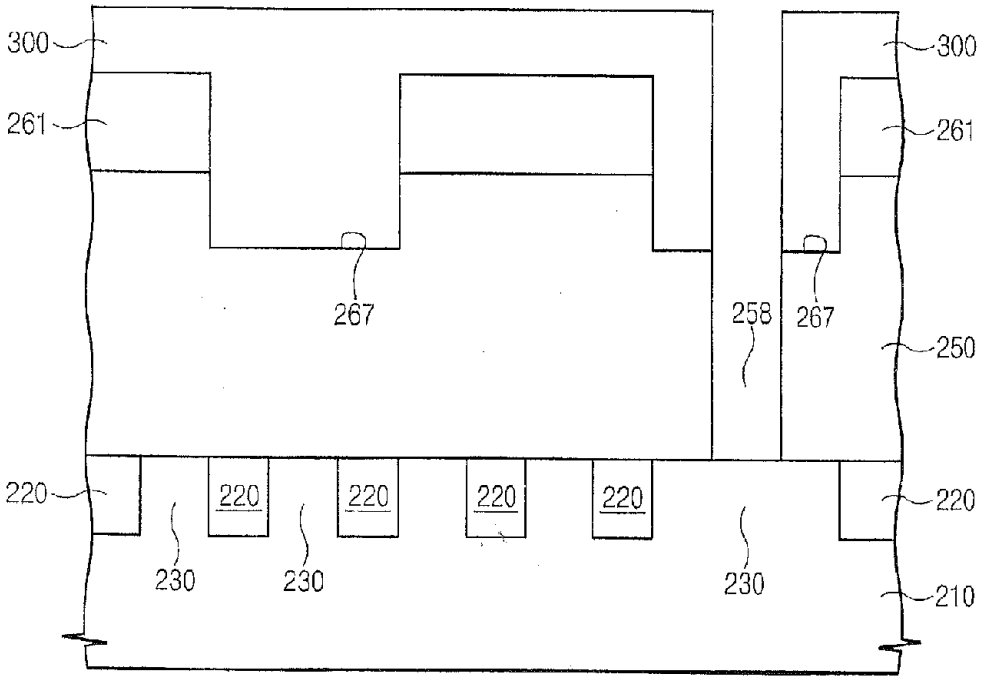

300
261
267
258
267
300
261
250
220
220
220
220
220
220
230
230
230
210

Fig. 35

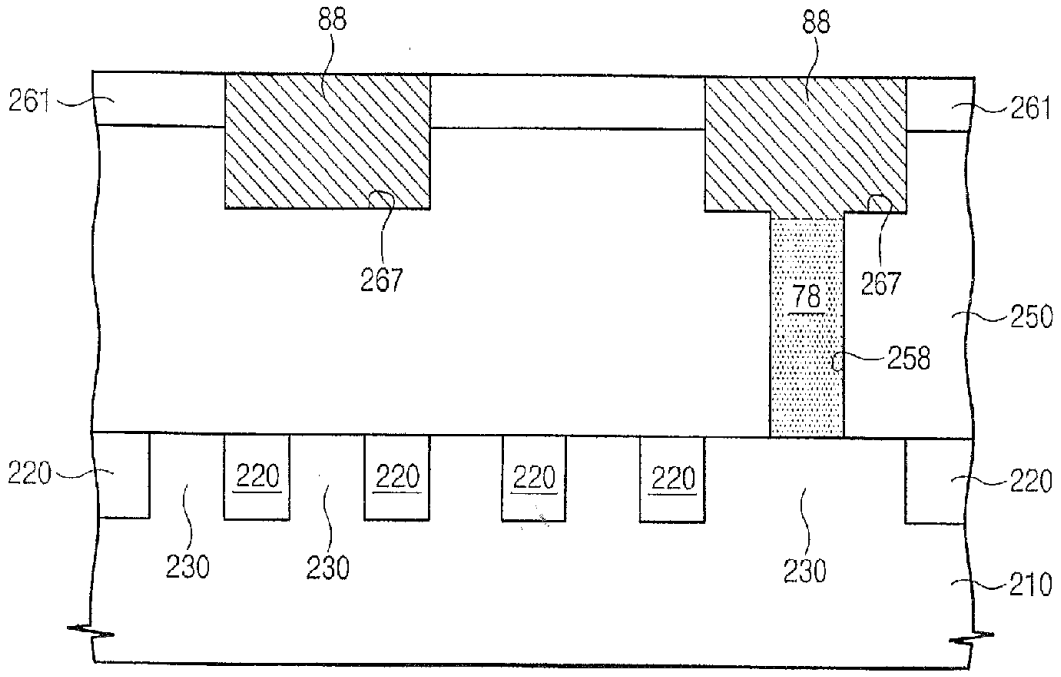

88
88
261
261
267
267
78
250
258
220
220
220
220
220
220
230
230
230
210

Fig. 36

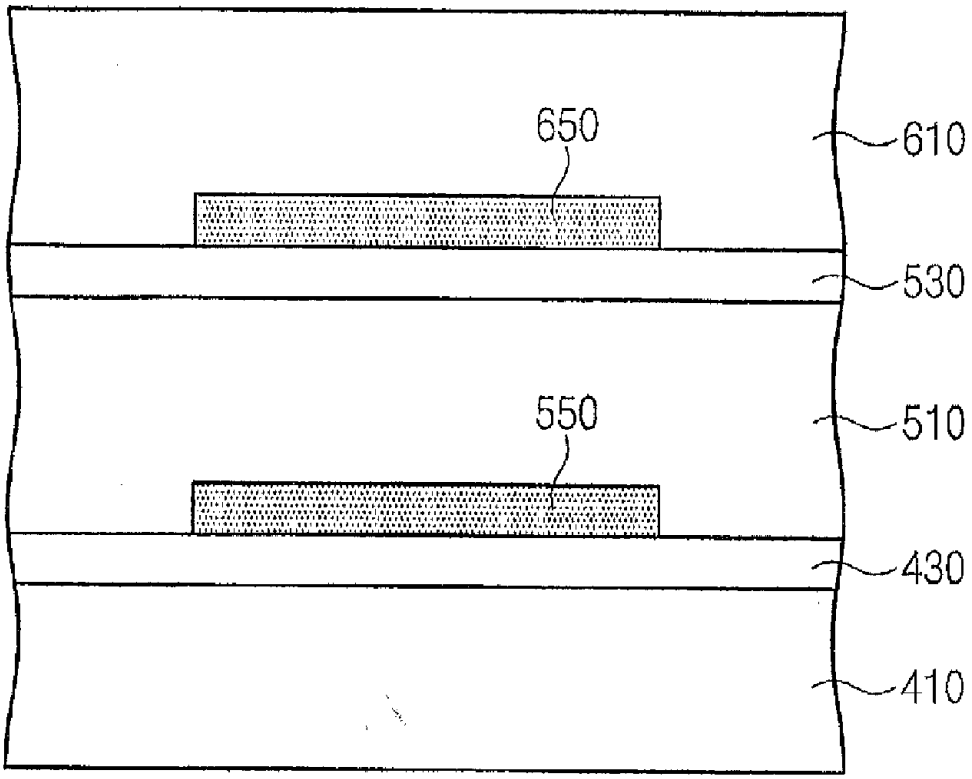


Fig. 37

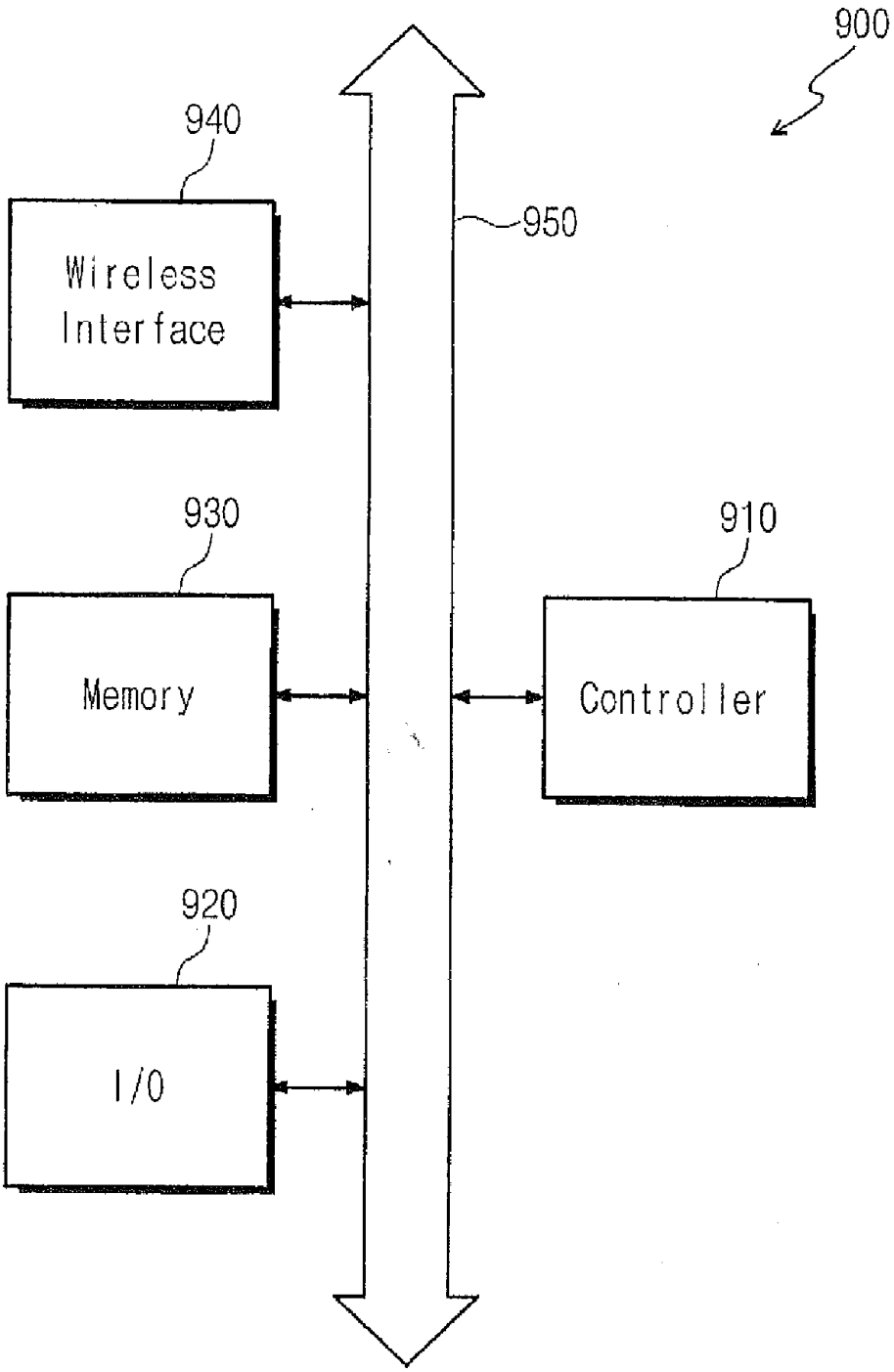
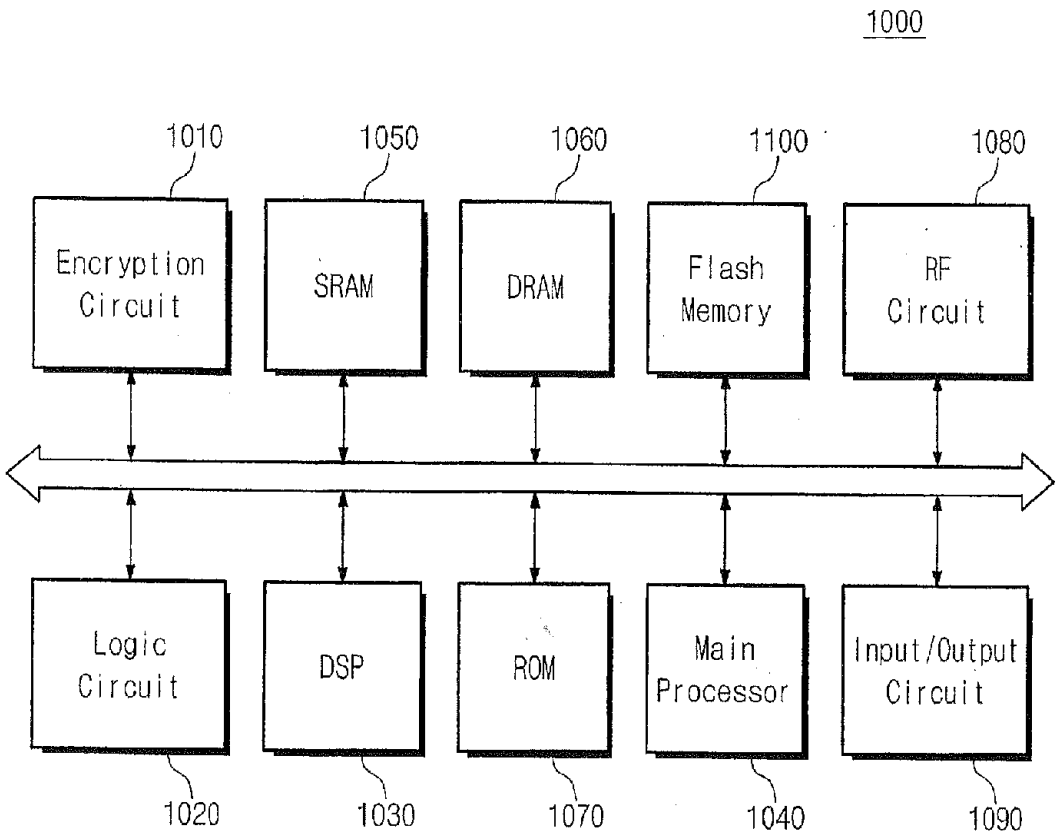

900
940
950
Wireless Interface
930
910
Memory
Controller
920
I/O

Fig. 38


1000
1010
1050
1060
1100
1080
Encryption Circuit
SRAM
DRAM
Flash Memory
RF Circuit
Logic Circuit
DSP
ROM
Main Processor
Input/Output Circuit
1020
1030
1070
1040
1090

SEMICONDUCTOR DEVICES INCLUDING FIRST AND SECOND BIT LINES

CLAIM OF PRIORITY

[0001] The present application is a divisional of and claims priority from U.S. patent application Ser. No. 11/623,269, filed Jan. 15, 2007, which claims the benefit of Korean Patent Application No. 10-2006-0101957, filed on Oct. 19, 2006, the disclosures of which are hereby incorporated by reference herein in their entireties.

BACKGROUND

[0002] Exemplary embodiments disclosed herein generally relate to formation of lines and, more particularly, to formation of bit lines in a semiconductor device. Exemplary embodiments disclosed herein also relate to bit lines in a semiconductor device such as a non-volatile memory device and a method for forming the same.

[0003] As semiconductor devices become increasingly integrated, the widths of patterns and the intervals between adjacent patterns decrease. Conventionally, fine patterns are formed by performing various photolithography processes. However, as the degree to which semiconductor devices are integrated increases, a misalignment margin in such photolithography processes decreases. Accordingly, fine patterns (e.g., contacts) are often misaligned with respect to underlying conductive regions during photolithography processes. For example, when even a slight degree of a misalignment occurs during a photolithography process for forming a bit line, misalignment between bit lines and bit line contacts occurs, thereby bridging one bit line to an adjacent bit line. Moreover, due to the reduction of a photolithography process margin, adjacent bit lines can become electrically connected to each other.

SUMMARY

[0004] Exemplary embodiments described herein provide a conductive line structure and a method for forming the same. Exemplary embodiments described herein also provide a non-volatile memory device including a bit line and a method for forming the same. Exemplary embodiments described herein also provide a memory card including the non-volatile memory device. Exemplary embodiments described herein also provide a stacked memory device including a non-volatile memory device.

[0005] One embodiment exemplarily described herein can be characterized as a method for forming a conductive line that includes forming an insulation layer on a substrate, the substrate including a plurality of first regions and a plurality of second regions, each of the second region being disposed between adjacent first regions; forming a plurality of first conductive lines on the insulation layer, the first conductive lines being electrically connected to respective first regions through respective first contacts through the insulation layer; forming a plurality of spacers on sidewalls of the first lines; forming a plurality of contact holes between the adjacent first contacts by removing the insulation layer between the adjacent ones of the plurality of spacers, the contact holes exposing respective second regions; and forming a plurality of second contacts filling respective contact holes and forming a plurality of second conducive lines electrically connected to respective second contacts.

[0006] Another embodiment exemplarily described herein can be characterized as a method of forming a non-volatile memory device that includes forming a string select line, a ground select line, and a plurality of word lines between the string select line and the ground select line on a substrate having a plurality of active regions, the string and ground select lines and the plurality of word lines crossing over the active regions; forming an insulation layer covering the ground select line, the string select line, and the plurality of word lines; patterning the insulation layer to form a plurality of first contact holes; forming a plurality of first contacts within respective first contact holes and forming a plurality of first bit lines electrically connected to respective first contacts; forming a plurality of spacers on sidewalls of the first bit lines; forming a second contact hole between adjacent ones of the plurality of first contact holes by removing the insulation layer between the adjacent ones of the plurality of spacers; and forming a second contact within the second contact holes and a second bit line electrically connected to the second contact.

[0007] Still another embodiment exemplarily described herein can be characterized as a stacked memory device that includes a plurality of substrates having at least two stacked substrates; and a memory device disposed on at least one of the substrates. In such an embodiment, the memory device can be formed according to the method disclosed in the immediately preceding paragraph.

[0008] Still another embodiment exemplarily described herein can be characterized as a memory card that includes a microprocessor; and a memory device coupled to the microprocessor. In such an embodiment, the memory device can be formed according to the method disclosed in the immediately preceding paragraph.

[0009] Yet another embodiment exemplarily described herein can be characterized as a semiconductor device that includes a plurality of first bit lines and a plurality of first contacts connected to respective first bit lines; a spacer formed on a sidewall of each of the first bit lines; and a second bit line self-alignedly disposed between the adjacent spacers and a second contact self-aligned with and connected to the second bit line.

[0010] A further embodiment exemplarily described herein can be characterized as a non-volatile memory device that includes a substrate including a plurality of active regions defined by a device isolation region; a string select line, a ground select line, and a plurality of word lines disposed between the string select line and the ground select line, the string and ground select lines and the plurality of word lines crossing over the active regions; an insulation layer covering the string select line, the ground select line, the plurality of word lines, and the active regions; first contacts through the insulation layer and electrically connected to odd active regions; first bit lines electrically connected to respective first contacts; a spacer formed on a sidewall of the first bit lines; and a second bit line self-alignedly disposed between the adjacent spacers and a second contact self-aligned with and connected to the second bit line.

[0011] Yet another embodiment exemplarily described herein can be characterized as a method of forming a semiconductor device that includes forming a first insulation layer on a substrate; forming a first mask on the first insulation layer, the first mask defining an opening; forming a first groove within the first insulation layer using the first mask; forming a second insulation layer on the first mask and on a

side of the first groove to define a second groove, the second groove having a smaller width than the first groove; forming a second mask filling the second groove; forming a plurality of third grooves for bit lines by removing the second insulation layer, each third groove being between the first and second masks; forming a third mask having an opening exposing the third grooves; forming a plurality of contact holes disposed between the adjacent first and second masks and self-aligned with respect to the third grooves by patterning the first insulating layer using the third, second and first masks as an etching mask; forming a conductive material on the first and second masks to fill the third grooves and respective contact holes; and forming a plurality of conductive lines and a plurality of contacts by performing an etching process on the conductive material, the contacts being self-aligned with respective conductive lines.

[0012] Still another embodiment exemplarily described herein can be characterized as a method of forming a line that includes forming a first insulation layer on a substrate; forming a first mask on the first insulation layer, the first mask defining a first groove therein; forming a second mask dividing the first groove, the second mask disposed within the first groove and defining a plurality of third grooves between the first and second masks; forming a third mask, the third mask having an opening crossing over at least one of the plurality of third grooves; forming a plurality of contact holes self-aligned with third grooves by patterning the first insulation layer using the third mask, the second mask, and the first mask as an etching mask; and forming a plurality of conductive lines and a plurality of contacts self-aligned with respect to corresponding conductive lines by filling the contact holes and the third grooves with a conductive material and etching the conductive material.

[0013] Another embodiment exemplarily described herein can be characterized as a method for forming a semiconductor device that includes forming a first insulation layer on a substrate; forming a plurality of first contacts through the first insulation layer; forming a second contact through the first insulation layer between adjacent ones of the plurality of first contacts; forming an insulation structure on the first insulation layer, the insulation structure defining a groove, wherein at least a portion of the first insulation layer defines a lower surface of the groove; forming a plurality of first conductive lines on the first insulation layer, the plurality of first conductive lines electrically connected to corresponding ones of the plurality of first contacts; and forming a second conductive line within the groove, the second conductive line electrically connected to the second contact, wherein the insulation structure is formed on sidewalls of adjacent ones of the plurality of first conductive lines.

[0014] Yet another embodiment exemplarily described herein can be characterized as a semiconductor device that includes a first insulation layer on a substrate; a plurality of first contacts through the first insulation layer; a second contact through the first insulation layer and between adjacent ones of the plurality of contacts; an insulation structure on the first insulation layer, the insulation structure defining a groove, wherein at least a portion of the first insulation layer defines a lower surface of the groove; a plurality of first conductive lines on the first insulation layer, the plurality of first conductive lines electrically connected to corresponding ones of the plurality of first contacts; and a second conductive line within the groove, the second conductive line electrically connected to the second contact, wherein the insulation structure is formed on sidewalls of adjacent ones of the plurality of first conductive lines.

[0015] Lastly, another embodiment exemplarily described herein can be characterized as a method of forming a semiconductor device that includes forming a first insulation layer on a substrate; forming a plurality of first bit lines on the first insulation layer; forming an insulation structure on the first insulation layer; and forming a second bit line on the first insulation layer between the plurality of first bit lines, wherein the second bit line is self-aligned with respect to the insulation structure.

BRIEF DESCRIPTION OF THE FIGURES

[0016] The accompanying figures are included to provide a further understanding of the exemplary embodiments, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the present invention and, together with the description, serve to exemplarily explain principles of the present invention. In the figures:

[0017] FIG. **1** is an equivalent circuit diagram of one embodiment of a non-volatile memory device;

[0018] FIG. **2** is an equivalent circuit diagram of another embodiment of a non-volatile memory device;

[0019] FIG. **3** is a plan view exemplarily illustrating connections between bit lines and corresponding bit line contacts in a non-volatile memory device according to one embodiment;

[0020] FIG. **4** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along line I-I' thereof;

[0021] FIG. **5** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along lines II-II' and III-III' thereof;

[0022] FIGS. **6-14** are cross-sectional views illustrating an exemplary embodiment of a method for forming a non-volatile memory device;

[0023] FIG. **15** is a cross-sectional view of another embodiment of a non-volatile memory device;

[0024] FIGS. **16-18** are cross-sectional views illustrating another exemplary embodiment of a method for forming a non-volatile memory device;

[0025] FIGS. **19-26** are cross-sectional views illustrating yet another exemplary embodiment of a method for forming a non-volatile memory device;

[0026] FIG. **27** is a cross-sectional view illustrating still another exemplary embodiment of a method for forming a non-volatile memory device;

[0027] FIGS. **28-35** are cross-sectional views illustrating yet another exemplary embodiment of a method for forming a non-volatile memory device;

[0028] FIG. **36** is a cross-sectional view of an exemplary embodiment of a stacked memory device including a non-volatile memory device;

[0029] FIG. **37** is a block diagram of an exemplary embodiment of a system including a non-volatile memory device; and

[0030] FIG. **38** is a block diagram of an exemplary embodiment of a memory card incorporating a non-volatile memory device.

DETAILED DESCRIPTION

[0031] Exemplary embodiments will be described below in more detail with reference to the accompanying drawings.

These embodiments may, however, be realized in different forms and should not be constructed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art.

[0032] In the figures, the dimensions of layers and regions are exaggerated for clarity of illustration. It will also be understood that when a layer (or film) is referred to as being 'on' another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being 'under' another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being 'between' two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

[0033] A 'semiconductor substrate' or a 'substrate' mentioned in the exemplary embodiments may refer to a structure based on an arbitrary semiconductor. The structure based on the semiconductor may include a silicon-on-insulator (SOI) having silicon on an insulation layer, silicon-on-sapphire (SOS) having silicon on sapphire, silicon-germanium, doped or undoped silicon, an epitaxial layer formed by an epitaxial growth technology, and another semiconductor structure. Additionally, a 'semiconductor substrate' or a 'substrate' may be a semiconductor substrate or a substrate where an arbitrary semiconductor device, e.g., a memory device, is already formed.

[0034] The terms 'odd bit line' and 'even bit line', as used herein below, are relative. When one bit line is called an 'odd bit line', a bit line adjacent to the one bit line is called an 'even bit line'. Conversely, when one bit line is called an 'even bit line', a bit line adjacent to the one bit line is called an 'odd bit line'. For example, when considering adjacent two bit lines, when one bit line is an 'odd bit line', the other one is an 'even bit line', and vice versa.

[0035] Exemplary embodiments described herein relate to a method of forming lines and the line structure resulting therefrom. The exemplary embodiments also relate to formation of bit lines in a semiconductor device such as a memory device. The exemplary embodiments may also relate to bit lines of a non-volatile memory device and to a method for forming the same. Hereinafter, various types of lines will be exemplary described. Moreover, a bit line of a non-volatile memory device will be described as an example.

[0036] FIG. 1 is an equivalent circuit diagram of one embodiment of a non-volatile memory device such as a NAND flash memory device.

[0037] Referring to FIG. **1**, a string select line SSL and a ground select line GSL are disposed in a row direction (e.g., an x-axis direction), and word lines WL**0** to WLm-**1** are disposed between the string select line SSL and the ground select line GSL. Bit lines BL**0** to BLn-**1** are disposed in a column direction (e.g., a y-axis direction) to cross over the word lines WL**0** to WLm-**1**.

[0038] A plurality of memory cells are coupled to each of the word lines WL**0** to WLm-**1** such that a plurality of memory cells MC**0** to MCm-**1** arranged in the column direction are connected in series to form a unit NAND string. A string select transistor SST and a ground select transistor GST are disposed on both sides of each unit NAND string. Gates of the string select transistors SST arranged in a row direction are connected to each other to form the string select line SSL, and gates of the ground select transistors GST arranged in a row direction are connected to each other to form a ground select line GSL. A bit line is connected to respective string select transistor SST (e.g., via a drain region) of each NAND string. Source regions of the ground select transistors GST are connected to a common source line CSL.

[0039] FIG. **2** is an equivalent circuit diagram of one embodiment of a non-volatile memory device such as a NOR flash memory device.

[0040] Referring to FIG. **2**, and unlike the NAND flash memory device of FIG. **1**, a bit line BL and a source line S/L are connected to each memory cell. That is, the memory cells arranged in a column direction are separated from each other.

[0041] The types and forms of memory cells that may be combined in a word line may be numerous. For example, memory cells can include a tunneling insulation layer, a memory layer (or a charge storage layer), and a control insulation layer (or an inter-gate dielectric layer) which are sequentially stacked on a semiconductor substrate. The memory layer may include a material capable of storing electric charges that are injected from the substrate through the tunneling insulation layer. For example, a memory layer can include an insulator material capable of trapping electric charges with a high trap density. Such an insulator material can include, for example, nitride, aluminum oxide (Al_2O_3), hafnium oxide (HfO), hafnium aluminum oxide (HfAlO), hafnium silicon oxide (HfSiO) or combinations thereof. Additionally, polysilicon nano-particles, metal nano-particles, fullerenes, or the like, can be used as, or incorporated within, a memory layer. A floating gate such as polysilicon also can be used as a memory layer.

[0042] In the NAND flash memory device of FIG. **1**, drain regions of the string select transistors SST arranged in a column direction are connected to the respective lines BL**0** to BLn-**1**. In the NOR flash memory device of FIG. **2**, the bit lines BL**0** to BLn-**1** are connected to each memory cell. Accordingly, to form a reliable highly-integrated flash memory device, the bit line is connected to the corresponding string select transistor SST in the NAND flash memory device, and is connected to the respective memory cell MC in the NOR flash memory device.

[0043] According to the embodiments described herein, the bit line of the NAND flash memory device is connected to a drain region of a string select transistor SST through a bit line contact and the bit line of a NOR flash memory device is connected to a source/drain region of the memory cell. In one embodiment, bit lines may be provided as either a first bit line or a second bit line, wherein second bit lines can be disposed between adjacent first bit lines. Accordingly, odd bit lines may be referred to as first bit lines and even bit lines may be referred to as second bit lines. Each bit line is electrically connected to a respective bit line contact. In one embodiment, the first bit line and the second bit line can have different structures and, therefore, can be formed according to different methods. The bit lines will be described with reference to FIGS. **3** through **5**.

[0044] FIG. **3** is a plan view showing connections to odd bit lines BL_O and even bit lines BL_E and respective odd bit line contacts DC_O and even bit line contacts DC_E in a NAND flash memory device, according to one embodiment.

[0045] Referring to FIG. **3**, the odd bit lines BL_O are connected to the respective odd bit line contacts DC_O, and the even bit lines BL_E are connected to the respective even

bit line contacts DC_E. In one embodiment, the even bit lines BL_E and the odd bit lines BL_O may have the same structure or may have different structures. The even bit lines BL_E and the odd bit lines BL_O may be structurally different when, for example, the even bit lines BL_E and odd bit lines BL_O are formed according to different methods. For example, the odd bit lines BL_O can be formed using a photolithography process while the even bit lines BL_E can be formed between the odd hit lines BL_O in a self-aligned manner. Moreover, the even bit line contact DC_E can be formed on the respective even bit lines BL_E in a self-aligned manner.

[0046] Because the even bit line contacts DC_E and corresponding even bit lines BL_E can be formed in a self-aligned manner, an overlapping area between the odd bit lines BL_O and the respective odd bit line contacts DC_O can, in one embodiment, be less than or substantially equal to an overlapping area between the even bit line BL_E and the respective odd bit line contact DC_E. In one embodiment, a distance between the odd bit line contact DC_O and a string select line SSL (or a string select gate) may be different from or substantially equal to a distance between the even bit line contact DC_E and the string select line (or a string select gate).

[0047] Referring to FIG. **3**, a distance D1 between an odd bit line contact DC_O and a first string select line SSL_**1** (or a first string select gate) may be greater than a distance D**3** between the even bit line contact DC_E and the first string select line SSL_**1** (or the first string select gate). A distance D**2** between the odd bit line contact DC_O and a second string select line SSL_**2** (or a second string select gate) may be shorter than a distance D**4** between the even bit line contact DC_E and the second string select line SSL_**2** (or the second string select gate). As described above, the structural difference may be result from that the odd bit line and the even bit line are formed by different methods.

[0048] FIG. **4** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along line I-I'.

[0049] Referring to FIG. **4**, an active region **30** may be defined in a substrate **10** by a device isolation region **20**. Adjacent active regions **30** may be electrically insulated from each other by a device isolation region **20**. A bit line is electrically connected to the respective active region **20** through a bit line contact. For example, bit line contacts **71** and **76** are formed through an insulation layer **50** to electrically contact the active regions. In one embodiment, an odd bit line and an even bit line can have the same or different structures (e.g., different widths, different heights, or different widths and heights). For example, the height of the even bit line **86** may be less than the height of the odd bit line **81**. Moreover, the width w_1 of the odd bit line contact **71** and the width w_2 of the odd bit line **81** can be substantially the same. Further, the width w_3 of the even bit line contact **76** may be less than the width w_4 of the even bit line **86** and the width w_2 of the odd bit line contact **81** may be less than the width w_4 of the even bit line **86**. The even bit line contact **76** is self-aligned with respect to a respective even bit line **86**. However, when the odd bit line **81** is formed by a photolithography process, the odd bit line **81** may be misaligned with respect to a respective odd bit line contact **71** within an acceptable range.

[0050] FIG. **5** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along lines II-II' and Specifically, a left-illustrated portion of FIG. **5** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along line II-II' and shows a cross-sectional view of odd bit lines while a left-illustrated portion of FIG. **5** is a cross-sectional view of the non-volatile memory device shown in FIG. **3**, taken along line III-III' and shows a cross-sectional view of even bit lines.

[0051] Referring generally to FIG. **5**, each bit line **81** and **86** is electrically connected to an active region outside a string select line (or a string select gate), i.e., a drain region **39**. Specifically, the bit lines **81** and **86** are electrically connected to the drain region **39** between the first string select line SSL_**1** and the second string select line SSL_**2** via bit line contacts **71** and **76**, respectively.

[0052] FIGS. **6-14** are views illustrating an exemplary embodiment of a method for forming a non-volatile memory device. Specifically, FIGS. **6**, **8-10** and **12-14** are cross-sectional views taken along line I-I' of FIG. **3**; and FIGS. **7** and **11** are plan views corresponding to FIGS. **6** and **10**, respectively.

[0053] Referring to FIGS. **6** and **7**, a device isolation region **20** is formed on a substrate **10** to define a plurality of active regions **30**. A string select line **41**, a ground select line (not shown) and a plurality of word lines **43** between the string and ground select lines are also formed according to well known methods; therefore, a detailed discussion of their formation will be omitted for conciseness. Briefly however, after forming a tunneling insulation layer **33**, a memory layer **35**, a control insulation layer **37** and a conductive layer (not shown), for word lines and select lines, the conductive layer is patterned to form a string select line **41**, word lines **43** and the ground select line (not shown), all of which cross over the active regions **30** and the device isolation regions **20**. The conductive layer, the tunneling insulation layer **33**, the memory layer **35** and the control insulation layer **37** can be patterned concurrently during a patterning process for the conductive layer. By performing an ion implantation process, the drain region **39** is formed on the active region outside the string select line **41**, a source region (not shown) is formed on the active region outside the ground select line, and a source/drain region (not shown) is formed on the active region between the word lines **43**.

[0054] An insulation layer **50** is formed on the substrate **10** to cover the string select line **41**, the ground select line (not shown), and the word lines **43**. In one embodiment, the insulation layer **50** may include a material such as an oxide. In another embodiment, the insulation layer **50** may include a multilayer structure of an oxide and a nitride. A first mask **60** having a plurality of first openings **65** defining odd bit line contacts is formed on the insulation layer **50**. The first openings **65** of the first mask **60** are disposed over the drain regions formed on odd active regions **30**_O outside the string select lines **41**. That is, drain regions formed on odd active regions **30**_O outside the string select lines **41** are disposed within the first openings **65** of the first mask **60**. As exemplarily illustrated, the first openings **65** may overlap with odd active regions **30**_O (i.e., odd drain regions).

[0055] Referring to FIG. **8**, the first mask **60** may be used as an etching mask to etch the insulation layer **50**, the control insulation layer **37**, the memory layer **35** and the tunneling insulation layer **33**, thereby forming odd contact holes **53** that expose the drain regions **39** in the odd active regions **30**_O.

[0056] Referring to FIG. **9**, the first mask **60** is removed, odd contacts **71** are formed within the odd contact holes **53** and odd bit lines **81** are electrically connected to respective odd contacts **71**. The odd contacts **71** and odd bit lines **81** can be formed according to any of various exemplary methods.

[0057] In one exemplary method, odd bit lines **81** can be formed after forming the odd contacts **71**. That is, after a

material having a good step coverage (e.g., silicon) is formed on the insulation layer **50** to fill the odd contact holes **53**, a planarization process (e.g., chemical mechanical polishing (CMP), etch-back or the like) is performed to form the odd contacts **71** in the odd contact holes **53**. Next, after forming a conductive material for a bit line on the odd contacts **71** and the insulation layer **50**, a patterning process is performed on the conductive material to form odd bit lines **81** that are electrically connected to respective ones of the odd contacts **71**. Here, a capping layer **90** including a material such as a nitride can be formed on the odd bit lines **81**. The conductive material from which the bit lines **81** are formed may include a material such as a metal, a metal alloy, a silicide, a conductive metal nitride, a conductive metal oxide, silicon, or the like or combinations thereof.

[0058] In another exemplary method, the odd contacts **71** and corresponding odd bit lines **81** can be formed concurrently. That is, a conductive material may be formed on the insulation layer **50** to fill the odd contact holes **53**, and then a patterning process may be performed to form the odd contacts **71** and the odd bit lines **81**. The conductive material may include a material such as a metal, a metal alloy, a silicide, a conductive metal nitride, a conductive metal oxide, silicon, or the like or combinations thereof. In one exemplary embodiment, if a bit line is to formed as a multilayer structure, a first conductive material (e.g., silicon) may be formed on the insulation layer **50** to fill the odd contact holes **53** and a second conductive material (e.g., a metal having a low electrical resistance) may be formed on the first conductive material. Then, a patterning process can be performed to pattern the second conductive material or the second and first conductive materials.

[0059] Referring to FIGS. **10** and **11**, spacers **93** are formed on sidewalls of the odd bit lines **81**. The spacers **93** may include a material having a suitable etching selectivity with respect to the insulation layer **50**. When the insulation layer **50** is formed in a multilayer, the spacers **93** may include a material having an etching selectivity with respect to the uppermost insulation layer of the multilayer insulation layer **50**. For example, the spacers **93** may include a nitride (e.g., silicon nitride), an oxide (e.g., aluminum oxide) or a nitride oxide (e.g., silicon oxynitride). Since the spacers **93** are formed on sidewalls of adjacent the odd bit lines **81**, adjacent spacers **93** form line-type grooves **100**. In one embodiment, these line-type grooves **100** can be used to define where even bit lines are to be subsequently formed. In another embodiment, adjacent ones of the even and odd bit lines can be insulated from each other by a spacer **93** provided therebetween.

[0060] Next, and as illustrated in FIG. **11**, a second mask **110** is formed to define odd bit line contacts. The second mask **110** includes a second opening **115** that exposes regions where the even bit line contacts are to be subsequently formed. For example, the second opening **115** overlaps at least one drain region **39** formed on the even active region **30**_E. In one embodiment, the second opening **115** of the second mask **110** may be disposed between adjacent string select lines **41**, and extend in a direction of the string select line **41** to overlap at least two even active regions **30**_E and the odd active regions **30**_O therebetween. Accordingly, the second opening **115** may be bar- or line-shaped such that the second opening **115** exposes at least two adjacent line-type grooves **100** and exposes the odd bit lines **81** therebetween. The second mask **110** and the spacers **93** formed can be collectively used as an etch mask to form even bit line contacts **76** between string select lines **41**. Accordingly, the even bit line contacts **76** can be confined between the spacers **93** and be self-aligned with respect to line-type grooves **100** where even bit lines **86** are to be subsequently formed.

[0061] Referring to FIG. **12** by using the second mask **110** and the spacers **93** as an etching mask, the exposed insulation layer **50**, the control insulation layer **37**, the memory layer **35** and the tunneling insulation layer **33** are etched to form even contact holes **56** between adjacent odd contacts **71**. Because the spacer **93** has an etching selectivity with respect to the insulation layer **50**, it serves as an etching mask. During the etching process, a portion of the spacers **93** may be etched. In this embodiment, even contact holes **56** may be completely self-aligned with respect to corresponding line-type grooves **100** where even bit lines **86** are to be subsequently formed. Moreover, misalignment between the line-type grooves **100** and even contact holes **56** does not occur. During the etching process, when a portion of a spacer **93** is etched, the width of a subsequently formed even bit line **86** may be greater than the width of the odd bit line **81**. On the other hand, the width of the line-type groove **100** can be adjusted by varying the width of the spacers **93**. Thus, the width of subsequently formed even bit lines **86** can be appropriately adjusted, as well as the ratio between the widths of the even and odd bit lines **71** and **76**, by controlling the width of the spacers **93**.

[0062] The even contacts **76** and even bit lines **86** can be formed according to any of various exemplary methods. For example, and with reference to FIG. **13**, even bit line contacts **76** may be formed by filling the even contact holes **56** and the line-type groove **100** between spacers **93** with a conductive material and subsequently performing an etch-back process. Before performing the etch-back process, a CMP process can be performed. A conductive material for bit lines **86** may then be formed on the even bit line contacts **76** to fill the line-type groove **100** between the spacers **93**.

[0063] Referring to FIG. **14**, even bit lines **86** are formed in a self-aligned manner between spacers **93** and are electrically connected to respective ones of even bit line contacts **76** by etching the conductive material for the bit lines **86**. For example, a CMP process may be performed until the top surface of the odd bit lines **81** is exposed, thereby forming the even bit lines **86**. The conductive material from which the bit lines **86** are formed may include a material such as a metal, a metal alloy, a silicide, a conductive metal nitride, a conductive metal oxide, silicon, or the like or combinations thereof.

[0064] In another exemplary method, the even bit lines and even bit line contacts can be formed concurrently. That is, a conductive material may be formed to fill the even contact holes **56** and the line-type grooves **100** between spacers **93** and a planarization process may then be performed to form the even bit lines **86** and respective even bit line contacts **76**.

[0065] According to the illustrated embodiment, misalignment between the even bit lines and respective bit line contacts does not occur. Additionally, because even bit lines are formed between the odd bit lines in a self-aligned manner after the odd bit lines are formed, a distance between the adjacent bit lines can be decreased beyond the resolution of a photolithography process (i.e., beyond a design rule). Moreover, an electrical connection between adjacent bit lines can be prevented.

[0066] The conductive material may be subjected to various etches to form the bit lines **86**. For example, when an etching amount is adjusted, the even bit lines can be formed in

various structures. For example, if a planarization process is performed until the capping layer **90** on the odd bit line is exposed after forming the conductive material for a bit line **86** (e.g., as shown in FIG. **13**), then, as exemplarily illustrated in FIG. **15**, the top of the even bit lines **86** may be higher than the top of the odd bit lines **81**. By further performing an etching process on the conductive material for bit lines **86**, the top of the even bit lines **86** may be made lower than the top surface of capping layer **90**, or may be lower than or substantially equal to the top of the odd bit lines **81**. Moreover, the capping layer **90** can be formed on the even bit line **86**.

[0067] Although the odd bit lines are formed by performing a patterning process in the above embodiment, they can be formed according to a damascene process. In this case, misalignment between the even bit lines and the even bit line contacts does not occur and misalignment between the odd bit lines and respective odd bit line contacts does not occur. Such a damascene process will be described in greater detail with reference to FIGS. **16-18**.

[0068] Referring to FIG. **16**, a device isolation region **20**, an active region **30**, a string select line SSL, a word line, and ground select line GSL may be formed on the substrate **10** in the same or similar manner as described above with respect to FIG. **6** and then an insulation layer **50** may be formed. The insulation layer **50** may include a single layer of a material such as oxide or may include multilayer structure of materials such as oxide and nitride. A mold layer **120** may then be formed on the insulation layer **50**. The mold layer **120** may include a material having an etching selectivity with respect to the insulation layer **50**. For example, when the insulation layer **50** includes an oxide layer, the mold layer **120** may include a material such as a nitride. As shown in FIG. **16**, a patterning process is performed on the mold layer **120** to form odd line-type openings **125** and odd contact holes **53**. Each odd line-type opening **125** defines an odd bit line while each odd contact hole **53** is self-aligned with the odd line-type opening **125** and defines an odd bit line contact. In the illustrated embodiment, the width of the odd line-type opening **125** may be wider than or substantially equal to the width of the odd contact hole **53**.

[0069] Referring to FIG. **17**, odd bit line contacts **71** and odd bit lines **81** are formed by filling each odd contact hole **53** and each odd line-type opening **125** with conductive material. For example, after a conductive material is formed on the mold layer **120** to fill the odd contact holes **53** and the odd line-type openings **125**, a planarization process is performed until the mold layer **120** is exposed, thereby forming odd bit lines **81** and odd bit line contacts **71**. In one embodiment, the odd bit lines **81** may partially fill the odd line-type openings **125** and an insulation layer including a material such as nitride may be used to fill the remaining portion of the line-type openings **125**, thereby forming a capping layer **130**. In one embodiment, the top surface of the capping layer **130** may be made lower than the top surface of the mold layer **120** by performing an additional etch-back process on the odd bit line **81**. In one embodiment, the capping layer **130** may include an oxide (e.g., aluminum oxide, silicon oxide, etc.).

[0070] Referring to FIG. **18**, after removing the mold layer **120**, spacers **93** are formed on sidewalls of the odd bit lines **81** in a similar manner as discussed with respect to FIG. **10**. In a similar manner as described with respect to FIG. **11**, a second mask having a second opening may be formed to define an even contact hole. Since subsequent processes are identical to those of the previous embodiments, description will be omitted for conciseness.

[0071] As described above with respect to FIGS. **16-18**, a misalignment between the even bit line and the even bit line contact and between the odd bit line and the odd bit line contact does not occur.

[0072] Referring to FIGS. **19-26**, a method for forming a bit line according to another embodiment will be described. FIGS. **19**, **21-23**, **25** and **26** are cross-sectional views taken along a line perpendicular to a bit line direction. FIGS. **20** and **24** are plan views corresponding to FIGS. **19** and **23**, respectively.

[0073] Referring to FIGS. **19** and **20**, a first insulation layer **250** is formed on a substrate **210**. The first insulating layer **250** may include a material such as an oxide. The substrate **210** includes a plurality of active regions **230** that are defined by a device isolation region **220**. Adjacent active regions **230** are electrically isolated by the device isolation region **220**. That is, the active region **230** is defined between the adjacent device isolation regions **220** such that the device isolation region and the active region are alternately disposed on the substrate **210**. A first mask pattern **261** is formed to cover odd device isolation regions. The first mask pattern **261** extends in a column direction (e.g., a y-axis direction) to cover the odd device isolation regions. Because the first mask pattern **261** is formed on the first insulation layer **250** to cover the odd device isolation regions, a plurality of first grooves **265** are defined within portions of the first insulation layer **250** exposed by the first mask pattern **261**. The first mask pattern **261** may be formed such that each of the first grooves **265** overlaps (or exposes) the even device isolation regions **220** and the active regions **230** on the both sides of the exposed even device isolation regions **220**. The first groove **265** extends in the column direction. The first mask pattern **261** includes a material (e.g., a nitride) having an etching selectivity with respect to the first insulation layer **250**. For example, after forming a silicon nitride layer on the first insulation layer **250**, the first mask pattern **261** may be formed by performing a photolithography process to pattern the silicon nitride layer. At this point, a portion of the first insulation layer **250** between the first mask patterns **261** may be etched.

[0074] Referring to FIG. **21**, a second insulation layer **290** having an etching selectivity with respect to the first mask pattern **261** is formed. For example, the second insulation layer **290** may include an oxide (e.g., silicon oxide). In one embodiment, the second insulation layer **290** may have a substantially uniform thickness and be formed on the side and top surfaces of the first mask pattern **261** and within the plurality of first grooves **265** defined within the first insulation layer **250**. Accordingly, the second insulation layer **290** defines a plurality of second grooves **295** overlapping (or exposing) even device isolation regions **220**. The second grooves **295** extend in the column direction to overlap (or expose) the even device isolation regions **220**.

[0075] Referring to FIG. **22**, a second mask pattern **266** is formed by filling the second groove **295** with a material (e.g., silicon nitride) having an etching selectivity with respect to the first insulation layer **250** and the second insulation layer **290**. For example, after forming a silicon nitride layer on the second insulation layer **290** to fill the second groove **295**, the second mask pattern **266** is formed by removing portions of the silicon nitride layer outside the second grooves **295** via an

etch-back process. As a result of the etch-back process, the second mask pattern **266** covers the even device isolation regions **220**.

[0076] Referring to FIG. **23**, an etching process is performed on the second insulation layer **290** to remove portions of the second insulation layer **290** on the first mask pattern **261** and portions of the second insulation layer **290** between the first mask pattern **261** and the second mask pattern **266**, thereby concurrently forming third grooves **257** and **258**. In the illustrated embodiment, the third grooves **257** can be used to define where a subsequently formed odd bit line will be formed and the third grooves **258** can be used to define where a subsequently formed even bit line will be formed.

[0077] In the illustrated embodiment, the second mask pattern **266** is formed between adjacent sidewalls of the first mask pattern **261** through a self-aligned method using the second insulation layer **290**. Thus, the third grooves **257** and **258** are defined between the first mask pattern **261** and the neighboring second mask pattern **266** in a self-aligned method.

[0078] Referring now to FIGS. **23** and **24**, a third mask **300** is formed to have an opening **305** defining a bit line contact hole. The opening **305** of the third mask **300** may be bar- or line-shaped and extend in a row direction (e.g., in an x-axis direction) to define a plurality of bit line contact holes concurrently. For example, the opening **305** of the third mask **300** concurrently exposes the third grooves **257** and the third grooves **258** to define where even bit line contact holes and odd bit line contact holes will be concurrently formed.

[0079] Referring to FIG. **25**, using the third mask **300**, the second mask pattern **266** and the first mask pattern **261** as an etching mask, the first insulation layer **250** is patterned to form odd bit line contact holes **253**, self-aligned with respect to the third grooves **257**, and even bit line contact holes **254**, self-aligned with respect to the third grooves **258**. The third mask **300** is then removed.

[0080] Referring to FIG. **26**, a conductive material for a bit line contact and a bit line is then provided to fill the contact holes **253** and **254** and the third grooves **257** and **258**. A planarization process is performed on the conductive material until the first mask pattern **261** and the second mask pattern **266** are exposed, thereby forming bit lines **81** and **86** and bit line contacts **71** and **81**. In the illustrated embodiment, even bit lines and odd bit lines are formed concurrently. Moreover, misalignment between the even bit lines and corresponding even bit line contacts does not occur and misalignment between the odd bit lines and corresponding odd bit line contacts does not occur. According to this embodiment, the even bit lines and the odd bit lines may have the substantially the same structure. For example, the heights and widths of the even and odd bit lines may be substantially the same and the top surfaces of the even and odd bit lines may be substantially coplanar.

[0081] Referring to FIGS. **19-26**, a remaining portion **290***r* of the second insulation layer may remain below the second mask pattern **266**. That is, although the first insulation layer **250** is disposed between an even device isolation region and the first mask pattern **261**, the remaining portion **290***r* may remain between the odd device isolation region and the second mask pattern **266**.

[0082] The bit line contacts **71** and **81** and the bit lines **81** and **86**, formed according to the process exemplarily described above with respect to FIGS. **19-26**, can be formed in a manner similar to the processes exemplarily described above with respect to FIGS. **6-15**.

[0083] Referring to FIG. **27**, the second insulation layer **290** can, in another embodiment, be formed on the sidewall of the first mask pattern **261** (e.g., within grooves of the first mask pattern **261**) as a spacer **297** instead of being formed by filling the first groove **265** as shown in FIG. **21**. In such an embodiment, the aforementioned first grooves **265** are not defined within the first insulation layer **250** and, after forming the second insulation layer **290**, an etch-back process is performed to form spacers **297** on sidewalls of the first mask pattern **261**. Due to the formation of spacers **297**, the second mask pattern **266** directly contacts the first insulation layer **250**. The process for forming the bit line contacts and bit lines may then proceed as described with respect to FIG. **23**.

[0084] In the embodiment of FIGS. **19** through **26**, after the third mask **300** is formed, portions of the second insulation layer **290** between the first mask pattern and the second mask pattern can be removed to define the third grooves **257** and **258**. That is, after forming the odd and even bit line contact holes, the second insulation layer **290** between the adjacent first mask and second mask is removed to form the third grooves **257** and **258** for an odd and even bit line.

[0085] FIGS. **19-26** illustrate processes to form a conductive line on a cell region. According to another embodiment exemplarily illustrated in FIGS. **28-35**, a conductive line can also be formed on a peripheral circuit region of the substrate, concurrently with the formation of the bit lines over the cell region.

[0086] Referring to FIG. **28**, the aforementioned first mask pattern **261** may be formed over a cell region and over a peripheral circuit region concurrently with the process described with respect to FIGS. **19** and **20**. In the illustrated embodiment, the first mask pattern may further include fourth grooves **267** where conductive lines are to be formed.

[0087] Referring to FIGS. **29** and **30**, the aforementioned second insulation layer **290** and second mask **266** may be formed over the cell region and the peripheral circuit region concurrently with the process described with respect to FIGS. **21** and **22**.

[0088] Referring to FIGS. **31-32**, after forming the second mask pattern **266** and before forming the aforementioned third mask **300**, an etch process is performed to remove the portion of second mask pattern **266** and second insulation layer **290** within the fourth groove **267** over the peripheral circuit region while retaining the fourth groove **267** defined by the first mask pattern **261** in the peripheral circuit region. For example, after forming the second mask pattern **266** and the second insulation layer **290** on the cell and peripheral circuit regions, a protective mask (not shown) may be formed to cover the cell region. Then, the second mask pattern **266** is removed in a peripheral circuit region where is not covered by the protective mask.

[0089] Referring again to FIG. **32**, when removing the second insulation layer **290** on and between the first mask pattern **261** and the second mask pattern **266** over the cell region, the portion of the second insulation layer **290** within the fourth groove **267** over the peripheral region is also removed also (e.g., in the manner as described with respect to the embodiment shown in FIG. **23**), to expose the fourth groove **267**.

[0090] In another embodiment, the second mask pattern and the second insulation layer can be selectively formed only on the cell region instead of forming second mask pattern and second insulation layer on the cell and peripheral regions and

then selectively removing portions of the second mask pattern and the second insulation layer over the peripheral circuit region. In such an embodiment, a process for removing the second insulation layer and the second mask layer over the peripheral circuit region will be omitted.

[0091] Referring to FIG. **33**, when forming the aforementioned third mask **300** having the third opening **305** as described with respect to FIGS. **23** and **24**, the third mask **300** may also be formed on the first mask **261** and the first insulation layer **250** in the cell and peripheral circuit regions and further include an opening **307** exposing the fourth groove **267** over the peripheral circuit region.

[0092] Referring to FIG. **34**, when forming the aforementioned contact holes as described above with respect to FIG. **25**, the first insulation layer **250** may be patterned to form a contact hole **258**. As shown, the contact hole **258** is self-aligned with respect to the fourth groove **267**.

[0093] Referring to FIG. **35**, when the aforementioned conductive material is planarized by, for example, etching to form bit lines and bit line contacts as shown in FIG. **26**, a conductive line **88** and a contact **78** for a conductive line may be similarly formed in the peripheral circuit region.

[0094] The method for forming bit lines in the above embodiments can be applied to various fields. For example, the methods can be applied to form a conductive line that is electrically connected to corresponding conductive region below the conductive line through a contact plug. Additionally, the methods can be applied to form a cross-point memory device having a memory layer defined at a cross-point of top and bottom electrodes (i.e., at a region where the top and bottom electrodes cross each other). Thus, when the top electrode and the bottom electrode are connected through a contact plug in the cross-point memory device, the methods exemplarily described in the above embodiments can be applied.

[0095] A method for forming a semiconductor device and/or a method for forming a non-volatile memory device according to the embodiments of the present invention can be applied to a stacked memory device or a three dimensional memory device. In one embodiment, the stacked memory device may include stacked substrates. At least one substrate of the plurality of stacked substrates may include a memory device or a memory chip, and at least one memory device may include a non-volatile memory device fabricated according to the embodiments exemplarily described above.

[0096] FIG. **36** is a cross-sectional view of one embodiment of a stacked memory device including a non-volatile memory device.

[0097] Referring to FIG. **36**, the stacked memory device may, for example, include a first level substrate **410**, a second level substrate **510**, and a third level substrate **610**. The second level substrate **510** and the third level substrate **510** include memory devices **550** and **650**. Substrates can be insulated from each other via insulation layers **430** and **530**. However, the memory devices **550** and **650** on each substrate may be or may not be electrically connected to each other.

[0098] The memory device in the substrates may be configured the same or differently. For example, the memory device **550** in the second level substrate **510** may be a flash memory device and the memory device **650** in the third level substrate **610** may be a volatile memory device, or vice versa. Additionally, the memory device in a specific level substrate may include different types of memory devices. For example, the memory device **550** of the second level substrate **510** may include a volatile memory device, a ferroelectrics memory, a resistance memory, a phase-change memory, a magnetic memory or combinations thereof in addition to a non-volatile memory device. The memory device may be a memory capable of storing one bit or more than two bits of a multi bit.

[0099] FIG. **37** is a block diagram of a system **900** including a non-volatile memory device according to an embodiment of the present invention. The system **900** can be used in a wireless communication device such as a PDA, a laptop computer, a portable computer, a web tablet, a wireless phone, a mobile phone, a digital music player, or all devices transmitting and/or receiving information via a wireless environment.

[0100] The system **900** may include a controller **910**, an input/output device **920** such as a keypad, a keyboard and a display, a memory **930**, and a wireless interface **940** combined each other through a bus **950**. The controller **910** may include more than one microprocessor, a digital signal processor, a microcontroller, or any devices similar to those. The memory **930** can be used to store commands executed by the controller **910**. The memory **930** includes a flash memory according to the embodiments of the present invention. The memory **930** includes another type of a memory, a volatile memory where arbitrary access is possible, or various types of memory.

[0101] The system **900** may use a wireless interface **940** transmitting data into a wireless communication network or receiving data from the network. For example, the wireless interface **940** includes an antenna and a wireless transceiver.

[0102] The system **900** can be used in a communication interface protocol of a third generation communication system such as CDMA, GSM, NADC, E-TDMA, WCDAM, and CDMA2000.

[0103] The semiconductor device and/or the non-volatile memory exemplarily device described herein can be applied to a memory card. FIG. **38** is a block diagram of a memory card **1000** applied with a non-volatile memory device **1100** according to an exemplary embodiment.

[0104] Referring to FIG. **38**, the memory card **1000** may include an encryption circuit for encoding, a logic circuit **1020**, a digital signal processor (DSP), and a main processor **1040**. Additionally, the memory card system **1000** includes a flash memory device **1100** and other various kinds of memories such as SRAM **1050**, DRAM **1060**, and ROM **1070**. The memory card system **1000** includes RF (high frequency/microwave) circuit **1080** and an input/output circuit **1090**. Function blocks **1010** in the memory card **1000** are connected to each other through a system bus.

[0105] The memory card **1000** operates according to a control of the external host (not shown), and the non-volatile memory device **1100** stores data or output the stored data according to a control of the host.

[0106] According to the embodiments exemplarily described above, misalignment between the bit line and the bit line contact can be prevented.

[0107] According to the embodiments exemplarily described above, a more highly integrated memory device can be obtained.

[0108] Accordingly, one embodiment can be exemplarily characterized as a method for forming a conductive line that includes forming an insulation layer on a substrate, the substrate including a plurality of first regions and a plurality of second regions, each of the second regions being disposed between adjacent first regions. A plurality of first lines are formed on the insulation layer, the first lines being electrically

connected to respective first regions through respective first contacts penetrating the insulation layer. Spacers are formed on a side of the first lines. A plurality of contact holes are formed between the adjacent first contacts by removing the insulation layer between the adjacent spacers, the contact holes exposing respective second regions. A plurality of second contacts are formed to fill the corresponding contact holes and a plurality of second lines are formed to be electrically connected to respective second contacts.

[0109] Other embodiments can be exemplarily characterized as a method of forming a non-volatile memory device may include forming a string select line, a ground select line, and a plurality of word lines between the string select line and the ground select line on a substrate having a plurality of active regions, the string and ground select lines and the plurality of word lines crossing over the active regions. An insulation layer is formed to cover the ground select line, the string select line, and the plurality of word lines. The insulation layer is patterned to form a plurality of first contact holes. A plurality of first contacts are formed to fill respective first contact holes and a plurality of first bit lines are formed to be electrically connected to respective first contacts. A spacer is formed on a side of each of the first bit lines. A second contact hole is formed between the adjacent first contact holes by removing the insulation layer between the adjacent spacers. A second contact is formed to fill the second contact holes and a second bit line is formed to be electrically connected to the second contact.

[0110] Still other embodiments can be exemplarily characterized as a semiconductor device including a plurality of first bit lines and a plurality of first contacts connected to respective first bit lines. A spacer is provided on a side of each of the first bit lines. A second bit line is self-alignedly disposed between the adjacent spacers. A second contact is self-aligned and connected to the second bit line.

[0111] Still, other embodiments can be exemplarily characterized as a non-volatile memory device including a substrate including a plurality of active regions defined by a device isolation region. A string select line, a ground select line, and a plurality of word lines between the string select line and the ground select line are provided to cross over the active regions. An insulation layer covers the string select line, the ground select line, the plurality of word liens, and the active regions. A first contact penetrates the insulation layer to electrically connect to odd active regions, and a bit line is electrically connected to respective first contacts. A spacer is provided on a side of each of the first bit lines. A second bit line is provided self-alignedly between the adjacent spacers. A second contact is self-aligned and connected to the second bit line.

[0112] Yet other embodiment can be exemplarily characterized as a method of forming a semiconductor device that includes forming a first insulation layer on a substrate. A plurality of spaced apart first masks are formed on the first insulation layer. A plurality of first grooves are defined between adjacent first masks. A second insulation layer is formed on a side of each of the first masks to define a plurality of second grooves, the second groove having a smaller width than the first grooves. A plurality of second masks are formed to fill respective second grooves. A plurality of second masks are formed to fill respective second grooves. A plurality of third grooves for a bit line are formed by removing the second insulation layer, each of the third grooves being disposed between adjacent first and second masks. A third mask is formed, the third mask having an opening exposing the third groove. A plurality of contact holes are formed between the adjacent first and second masks and self-aligned with respective third grooves by patterning the first insulation layer using the third mask, the second mask, and the first mask as an etching mask. A conductive material is formed on the first masks and the second mask to fill the third groove and respective contact hole. A plurality of conductive lines and a plurality of contacts are formed by performing an etching process on the conductive material, the contacts being self-aligned with respective lines.

[0113] A further embodiment can be exemplarily characterized as a method of forming a conductive line that includes forming a first insulation layer on a substrate. A plurality of spaced first masks are formed on the first insulation layer. A plurality of second masks are formed to divide a first groove defined between the adjacent first masks, each of the second masks being disposed between the adjacent first masks. A third mask is formed, the third mask having opening crossing over at least one of a plurality of third grooves, the third groove being defined by the adjacent first mask and the second mask. A contact hole self-aligned with respective third groove is formed by patterning the first insulation layer using the third mask, the second mask, and the first mask as an etching mask. A plurality of conductive lines and a plurality of contacts self-aligned with respective conductive lines are formed by filling the contact holes and the third grooves with a conductive material and etching the filled conductive material.

[0114] Some embodiments can be exemplarily characterized as a stacked memory device including a plurality of substrates. A memory device is disposed on the at least one substrate. The memory device may include the non-volatile memory device formed by exemplary embodiments.

[0115] Other embodiments can be exemplarily characterized as a memory card including a microprocessor and a memory device coupled to the microprocessor. The memory device may include the non-volatile memory device formed by exemplary embodiments.

[0116] The above-disclosed subject matter is to be considered as illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, which fall within the true spirit and scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

That which is claimed is:

1. A semiconductor device comprising:

a plurality of first bit lines and a plurality of first contacts connected to respective ones of the first bit lines;

a plurality of spacers on sidewalls of the first bit lines; and

a second bit line self-alignedly disposed between adjacent ones of the spacers, and a second contact self-aligned with and connected to the second bit line.

2. The semiconductor device of claim **1**, wherein an overlapping area between one of the first bit lines and the one of the first contacts connected thereto is larger than an overlapping area between the second bit line and the second contact.

3. The semiconductor device of claim **1**, wherein a height of one of the first bit lines is different from a height of the second bit line.

4. The semiconductor device of claim 1, wherein a width of one of the first bit lines is different from a width of the second bit line.

5. The semiconductor device of claim 1, further comprising a string select line, a ground select line, and a plurality of word lines between the string select line and the ground select line, the first contacts and the second contact being electrically connected to respective drain regions outside the string select line.

6. The semiconductor device of claim 5, wherein a distance between the string select line and one of the first contacts is different from a distance between the string select line and the second contact.

7. A non-volatile memory device comprising:

a substrate including a plurality of active regions defined by a device isolation region;

a string select line, a ground select line, and a plurality of word lines disposed between the string select line and the ground select line, the string and ground select lines and the plurality of word lines crossing over the active regions;

an insulation layer covering the string select line, the ground select line, the plurality of word lines, and the active regions;

first contacts through the insulation layer and electrically connected to odd-numbered ones of the active regions;

first bit lines electrically connected to respective first contacts;

a plurality of spacers on sidewalls of the first bit lines; and

a second bit line self-alignedly disposed between adjacent ones of the spacers, and a second contact self-aligned with and connected to the second bit line.

8. The non-volatile memory device of claim 7, wherein an overlapping area between one of the first contacts and the one of the first bit lines connected thereto is larger than an overlapping area between the second contact and the second bit line.

9. The non-volatile memory device of claim 7, wherein a distance between the string select line and one of the first contacts is different from a distance between the string select line and the second contact.

10. The non-volatile memory device of claim 7, wherein a height of one of the first bit lines is different from a height of the second bit line.

11. The non-volatile memory device of claim 7, wherein a width of one of the first bit lines is different from a width of the second bit line.

* * * * *