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Dielectric Barrier, Etch Stop, and Metal Capping Materials for State of the Art and beyond Metal Interconnects

Sean W. King[*,z]

Logic Technology Development, Intel Corporation, Hillsboro, Oregon 97124, USA

Over the past decade, the primary focus for improving the performance of nano-electronic metal interconnect structures has been to reduce the impact of resistance-capacitance (RC) delays via utilizing insulating dielectrics with ever lower values of dielectric permittivity. The integration and implementation of such low dielectric constant (i.e. low-*k*) materials has been fraught with numerous challenges. For intermetal and interlayer (ILD) low-*k* dielectrics, these challenges have been largely associated to integration with metal interconnect fabrication processes and well documented and reviewed in the literature. Although equally important, less attention has been given to other low-*k* dielectrics utilized in metal interconnect structures that are commonly referred to as low-*k* dielectric barriers (DB), etch stops (ES), and/or Cu capping layers (CCL). These materials present numerous challenges as well for integration into metal interconnect fabrication processes. However, they also have more stringent integrated functionality requirements relative to low-*k* ILD materials that serve only a basic purpose of electrically isolating adjacent metal lines. In this article, we review the integration challenges and associated integrated functionality requirements for low-*k* DB/ES/CCL materials with a focus on the current status and future direction needed for these materials to facilitate both Moore's law (i.e. More Moore) and More than Moore scaling.
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Unlike complementary metal oxide semiconductor (CMOS) transistors where traditional Dennard[1] dimensional scaling has resulted in tremendous gains,[2] dimensional scaling of the associated metal interconnect leads to increases in resistance (R), capacitance (C), and combined RC delays that degrade the overall interconnect performance.[3–6] This reverse effect of dimensional scaling became particularly apparent in the late 90's as the industry left the realm of the micron (i.e. micro-electronics) and entered into the realm of the nanometer (i.e. nano-electronics).[7,8] To mitigate this ominous effect of interconnect dimensional scaling (and avoid influencing overall device performance), nano-electronic interconnects have experienced over the past two decades intense research and development and undergone significant changes involving both new materials and fabrication processes.[9,10] The implementation of new materials has been nearly continuous and began with the introduction of new insulating dielectrics with reduced values of dielectric permittivity (k) for use as the intermetal (IMD) or interlayer (ILD) dielectric.[11,12] These so called "low-k" dielectrics were primarily introduced to help reduce the increase in interconnect capacitance resulting from reduced metal line separation brought about by continuous transistor dimensional scaling.[13–15]

The first such low-k IMD/ILD implemented was silicon oxyflouride (SiOF, $k \cong 3.6$–3.8),[16,17] and was quickly followed by the replacement of aluminum (Al) with copper (Cu) as the interconnect metal/conductor to reduce the resistance of the interconnect.[18,19] The latter also led to the inversion of the interconnect fabrication process from subtractive metal to subtractive dielectric or "damascene" processing.[20,21] At a similar time, new inorganic-organic "carbon doped" oxide (a-SiOC:H) materials with reduced values of dielectric permittivity ($k \cong 3.1$–3.3) were also introduced to replace SiOF.[22,23] Since then, there has been a slow but steady progression to low-k ILD materials with ever lower values of dielectric permittivity.[24,25] The slow progression has been mostly related to the difficulties in integrating these new materials with already established patterning and metallization schemes and is well documented in the literature.[26–33]

The conversion to Cu and damascene interconnect fabrication methods, however, required the addition of other insulating dielectric materials to serve various new and sometimes simultaneous roles.[34,35] Depending on the details of the interconnect fabrication scheme, additional dielectrics were needed to serve as either a diffusion barrier (DB),[36] Cu capping layer (CCL),[37] etch stop (ES),[38] hard mask (HM),[35,38] and/or polish stop (PS).[39] In most cases, plasma enhanced chemically vapor deposited (PECVD) amorphous hydrogentated silicon nitride (a-SiN:H)[40] was initially utilized for these various applications. Unfortunately, the DB, CCL, and ES layers typically remain in the interconnect stack and contribute to the effective capacitance of the interconnect. Therefore, low-k forms of these materials were also needed to reduce the impact of the relatively high-k of PECVD a-SiN:H ($k = 6.5$–7.0).[41–43] The low-k DB/CCL/ES materials implemented to date have been primarily carbon doped silicon nitrides (a-SiNC:H) with k values of 4.5–5.8,[44–51] dense oxygen doped silicon carbides (a-SiCO:H) with k values of 4.0–4.8,[52–58] and pure silicon carbides (a-SiC:H) with k values of 4.0–7.0.[59–66] Similar to low-k ILDs, these materials have proven equally difficult and challenging to integrate with Cu interconnect fabrication processes.[67,68] However unlike low-k ILDs, the challenges associated with low-k DB/CCL/ES materials have been related to both integration with downstream fabrication processes and meeting numerous additional integrated functionality requirements.

While various aspects of the challenges associated with low-k DB/CCL/ES materials in metal interconnects have been covered in the literature, the authors are unaware of a comprehensive examination of their requirements, status, and future direction. To address this shortcoming, we review in this article the technical literature related to all aspects of low-k DB, CCL, and ES materials. We begin by examining the various material properties and integrated functionalities required for these layers, and then review the current status of the materials employed as DB, CCL, and ES layers. We conclude by examining potential new and upcoming materials and the future direction for DB, CCL, and ES materials needed to both sustain Moore's Law[69] (i.e. "More Moore") and "More than Moore"[70,71] dimensional scaling.

Low-k DB/CCL/ES Integration Requirements

While low-k ILD materials are perhaps more challenging to integrate into Cu interconnect fabrication processes,[26–33] low-k

*Electrochemical Society Active Member.
zE-mail: sean.king@intel.com

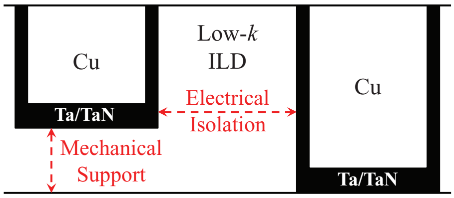

Figure 1. Schematic diagram illustrating the different functionalities of a low-k ILD in a low-k/Cu interconnect.

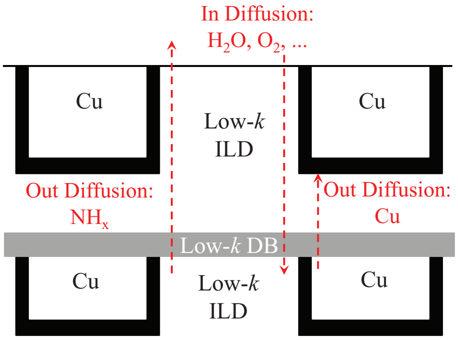

Figure 2. Schematic diagram illustrating the different functionalities of a low-k DB in a low-k/Cu interconnect.

DB/CCL/ES materials have the most integrated functionality requirements of the two. As shown in Figure 1, low-k ILD materials serve a basic purpose of establishing a medium in which to inlay and electrically isolate metal lines. The low-k ILD also provides some mechanical support to metal lines during downstream processing of multiple metal layers and packaging. The low-k DB/CCL/ES, however, serves these and many other additional integrated functionalities such as: preventing Cu out-diffusion into overlying metal layers,[36,37,72–76] preventing in-diffusion of moisture[77–79] and other aqueous cleaning chemicals[80–83] that can corrode lower metal and ILD layers (see Figure 2), passivating the top surface of the Cu line to reduce/prevent electromigration,[84–88] halting/stopping the trench or via ILD etch to prevent over etching into the underlying metal layer and to facilitate unlanded vias (see Figure 3),[89,90] and prohibiting resist poisoning during next layer metal patterning (see Figure 2).[91,92] As these functionality requirements all relate to the material properties of the DB/CCL/ES, we briefly outline and review the basic electrical, mechanical, thermal and optical material property requirements for these layers in a general nano-electronic metal interconnect. We then examine the additional needed material properties set by the integrated functionality requirements for these layers in a typical single or dual damascene (DD) low-k/Cu interconnect structure. Since a single film/layer typically can serve as both a DB, CCL, and ES, we will generically refer to these layers as DBs going forward unless discussing a different specific application.

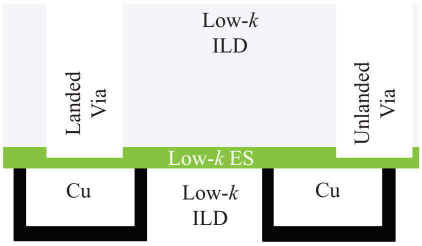

Figure 3. Schematic diagram illustrating functionality of a low-k ES in a low-k/Cu interconnect for stopping the via etch over landed and unlanded contacts.

Electrical requirements.— All dielectrics in a metal interconnect structure must be electrical insulators that exhibit both extremely low leakage currents and high dielectric breakdown strength. In this regard, a-SiO_2 is an ideal metal interconnect dielectric with leakage currents typically $<10^{-8}$ A/cm^2 (up to 6-8 MV/cm)[93–95] and dielectric breakdown strengths of $\geq$ 10 MV/cm.[96–98] Another dielectric that also exhibits excellent electrical insulating properties is a-Si_3N_4 with leakage currents of $<10^{-8}$ A/cm^2 (up to 4-6 MV/cm)[41,99,100] and dielectric breakdown strengths of 6–8 MV/cm.[100–102] Due to differences in dry etch selectivity and other considerations to be discussed later, a-SiO_2, a-Si_3N_4, and related a-SiN:H complement one another and make an excellent choice as the ILD and DB in Cu interconnect structures.[103–106]

However as mentioned above, insulators are needed with dielectric permittivity values substantially less than that of PECVD SiO_2 (k = 4.0–4.4) and PECVD a-SiN:H (k = 6.5-7.0) to reduce RC delays in advanced interconnect structures. To meet this need, low-k a-SiOC:H ILDs and a-SiCN:H DBs with dielectric permittivity values of 3.0–3.2 and 5.5–5.8, respectively, were introduced and implemented by the semiconductor industry in the early-mid 2000's.[22,23,25] According to the 2013 edition of the International Technology Roadmap for Semiconductors (ITRS),[107] the dielectric permittivity of low-k ILD and DB materials utilized in high volume manufacturing are currently 2.5–3.0 and 4–5, respectively. In another decade, these values are anticipated / expected to be reduced to <2.0 and <4.0, respectively.

A final electrical requirement for both low-k ILD and DB materials is immunity or extreme resistance to time-dependent-dielectric-breakdown (TDDB).[108] This phenomenon is the sudden breakdown of the insulating properties of a material (conversion from high resistance to low resistance state) after extended stressing at electrical fields substantially below the ultimate breakdown strength measured in a typical current-voltage (IV) measurement. The phenomenon is generally attributed to various molecular bonding breakdown mechanisms creating a conducting percolating path of defect or traps states through the dielectric.[108] However, models for predicting TDDB are typically more empirical than physics based (i.e. E vs. 1/E vs. $\sqrt{E}$ models).[108–114] Unfortunately, low-k ILD materials exhibit significantly reduced TDDB lifetimes relative to SiO_2, and this is a significant, well documented concern for low-k/Cu interconnect reliability.[115–118] As will discussed later, low-k DB materials have also been observed to exhibit reduced TDDB lifetimes relative to a-Si_3N_4 and a-SiN:H.[119–122]

Mechanical requirements.— Another basic requirement of interconnect dielectric materials is to provide reinforcing mechanical support to the various metal layers and help distribute thermal and shear stresses produced during downstream processing and packaging.[123–128] The low-k ILD and DB material properties most focused on from this viewpoint are Young's modulus and hardness as determined by nanoindentation.[129,130] Due to limitations in spatial resolution and substrate effects that have become increasingly significant as target film thicknesses decrease below 100 nm,[9,131] a number of alternative techniques have recently attracted attention such as contact resonance-atomic force microcopy (CR-AFM)[132–134] and bulge testing[135,136] as well as non-contact optical techniques such as picosecond laser ultrasonics (PLU),[137–140] Brillouin light scattering (BLS),[141–146] and surface acoustic wave spectroscopy (SAWS)[146,147]. However despite the extreme emphasis on measuring Young's modulus for low-k materials, the author is unaware of any established critical thresholds for these properties in either low-k ILD or DBs.

The lack of a clearly defined minimum threshold for Young's modulus or hardness is probably a result of the inability to predict mechanical failure based on these properties alone. For brittle dielectric materials, mechanical failure is predicted by the Griffith equation.[129,148] The Griffith equation relates the applied stress to a critical flaw or crack size according to the following relation:

$$\sigma_c = Y\sqrt{(E\Gamma/\pi a)} \quad [1]$$

where σ_c is the critical stress, a is the critical flaw size (or film thickness), E is Young's modulus, Γ is the fracture strength of the material, and Y is a stress intensity factor that is shape and geometry dependent. E and Γ are sometimes combined as fracture toughness: $K = \sqrt{(E\Gamma)}$. Accordingly, resistance to fracture / mechanical failure does scale with E, but not E alone. The emphasis on E is likely a result of the ease of performing this measurement using nanoindentation measurements. Fracture toughness / energy measurements require either detailed nanoindentation measurements[129] or more time intensive four point bend (4pb)[149] or double cantilever beam (DCB) measurements.[150]

The original ILD material (SiO_2) utilized in damascene Cu interconnect structures exhibited reasonably robust Young's modulus and fracture toughness values of 60-80 GPa[141] and 0.6-0.8 MPa$\sqrt{m}$,[129] respectively. However relative to SiO_2, low-*k* a-SiOC:H ILD materials exhibit substantially reduced values for Young's modulus (3-20 GPa)[136–147] and fracture toughness / energy ($\leq$0.2 MPa$\sqrt{m}$).[151–154] Unfortunately, the reduction in mechanical properties scales with reductions in dielectric permittivity,[14,66,155–57] and is one of the contributing factors for why low-*k* ILD materials with increasingly lower values of *k* have been so challenging to integrate.[158] UV curing technologies have enabled some reduction in dielectric permittivity (through introduction of interconnected porosity) without a significant reduction in Young's modulus.[159–164] A survey of the literature suggests that low-*k* ILDs with Young's moduli of 5-10 GPa have been successfully integrated into high volume manufacturing interconnect fabrication processes.[24,25,148]

Similar to low-*k* ILDs, low-*k* DB materials also exhibit reduce mechanical properties relative to the PECVD a-SiN:H films originally employed. However, the reduction in mechanical properties has not been as severe with reported Young's moduli and fracture toughness values of 40–120 GPa[74,139,142] and 0.5–4 MPa$\sqrt{m}$,[164–169] respectively. Compared to the Young's moduli of 100-200 GPa[135,140,142] and fracture toughness of 1-10 MPa$\sqrt{m}$[170–172] reported for PECVD a-SiN:H, the low-*k* DB mechanical property reduction is fairly modest. Also as the reduced values for low-*k* DB materials are substantially higher than those for low-*k* ILD materials, there has been generally less concern for these properties when considering new low-*k* DBs.

Another important mechanical material property to consider for both low-*k* ILD and DB materials is the post deposition film stress.[173] Due to differences in coefficients of thermal expansion (CTE) between the film and substrate, tensile or compressive stresses can develop in a thin film on cooling from the deposition temperature.[174,175] In addition for plasma deposition processes, ion bombardment of the surface during deposition can lead to development of additional stresses and in many cases is used to intentionally manipulate the final post deposition stress.[176] For low-*k* ILD plasma deposited materials, ion bombardment is typically minimized[177,178] and CTE mismatch between the film and substrate leads to the development of tensile stresses.[154–156] These tensile stresses are generally undesired as they can lead to spontaneous channel crack formation (see Figure 4).[154,179–185] As shown by Beuth,[179] channel crack formation for a thin film on a thick substrate can be described according to a relation analogous to the Griffith equation, i.e.:

$$\sigma_c = Z\sqrt{(\Gamma E/h_c)} \qquad [2]$$

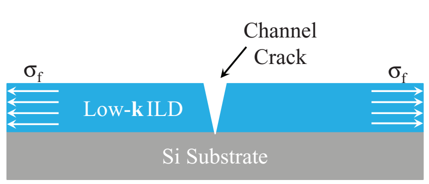

Figure 4. Schematic diagram illustrating the formation of a channel crack in a low-*k* ILD thin film deposited on a Si substrate and with an intrinsic tensile stress (σ_f).

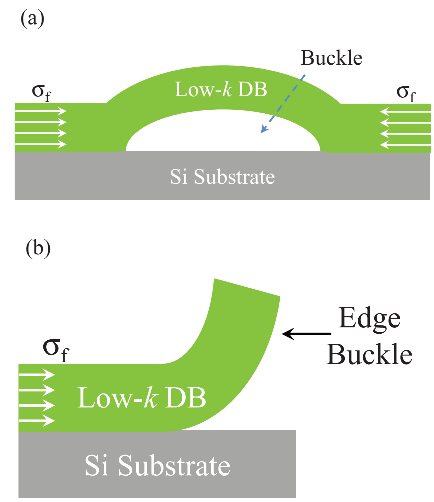

Figure 5. Schematic diagrams illustrating (a) a buckle delamination and (b) an edge delamination of a compressive low-*k* DB thin film deposited on a Si substrate.

where σ_c is the critical stress for channel crack formation, Z is a scaling factor dependent on the elastic properties of the film and substrate, h_c is the critical thickness at which channel crack formation may occur and Γ and E are as previously. This expression is based on the fact that as the thickness of a tensile film increases so does the stored elastic energy (or energy release rate). Once the film reaches a critical thickness (h_c), the amount of stored elastic energy equals the fracture energy (Γ) of the material and formation of a channel crack is energetically favorable. For this reason, the use of relatively thick and tensile low-*k* ILD films is generally undesirable. As Γ and E decrease with *k*, the critical thickness for a low-*k* ILD will also decrease with *k*. As an example, h_c for a typical non-porous, $k = 3.1$ a-SiOC:H ILD (with $E = 10$ GPa, $\Gamma = 5$ J/m^2, $\sigma_f = 50$ MPa) is $\sim$ 14 microns, whereas for a porous, $k = 2.5$ a-SiOC:H ILD (with $E = 5$ GPa, $\Gamma = 2$ J/m^2, $\sigma_f = 40$ MPa) h_c is $\sim$ 4 microns.

For low-*k* DB plasma deposited materials, ion bombardment is intentionally more significant resulting in films with more desirable compressive stresses.[50,77] The compressive stresses are useful for counteracting the tensile stresses present in the low-*k* ILD from both a mechanical reliability perspective and from a more mundane wafer curvature perspective where overly bowed wafers can create wafer pick-up, chucking, and registration issues on manufacturing tools.[186] However, there are limitations to the amount of desirable compressive stress in a low-*k* DB material. At sufficiently high stresses, mechanical failure can also occur for a compressive film via out of plane buckling of the DB.[187–193] In this situation, the likelihood for buckling is dependent on not just the stress and properties of the DB but also the adhesion strength of the DB to the underlying film or substrate. For a typical half moon buckle clamped on both ends (see Figure 5a), the critical stress for buckling of a free standing film is given from beam theory as:[189]

$$\sigma_b = \pi^2 E/12(1 - \upsilon^2) \times (h/b)^2 \qquad [3]$$

where σ_b is the critical compressive stress for buckling, b is the width of the buckle, ν is Poisson's ratio, and E and h are as before. Accounting for adhesion of the film to the substrate leads to more detailed analytical expressions relating the interfacial facture energy (Γ_i) to the critical buckle stress (σ_b) and residual film stress of the buckled film (σ_r). Specifically,

$$\Gamma_i(\Psi) = (1 - \upsilon^2)h(\sigma_r - \sigma_b)(\sigma_r + 3\sigma_b)/2E, \qquad [4]$$

$$\sigma_r = \sigma_b[0.75(\delta/h)^2 + 1], \qquad [5]$$

where δ is the out plane height of the buckle and Ψ is the phase angle of the loading that is defined as the ratio of shear to normal forces at the crack tip of the buckle.

The role between film stress, interface energy, film thickness and likelihood for buckling is difficult to interpret in a straight forward manner from the above equations. However, more insight can be gained from considering a simple edge buckle delamination (see Figure 5b). In this case, the critical stress takes a similar form to equations 1 and 2, i.e.:[187]

$$\sigma_c = Z_b\sqrt{(\Gamma_i E/h_c)} \quad [6]$$

where Z_b is a scaling factor for a buckle edge delamination and Γ_i is again the film/substrate interface work of adhesion. As for channel cracking, the critical stress for buckle delamination decreases with decreasing interface energy and increasing film thickness. As an example, the critical edge buckle thickess for a DB material with a typical compressive stress of 250 MPa, E = 100 GPa, and adhesion energy of 10 J/m^2 would be close to 16 microns, well beyond a typical DB thickness target in a metal interconnect. However, for a highly compressive DB with poor adhesion energy (σ_f = 1 GPa, E = 200 GPa, Γ_i = 0.5 J/m^2), the critical thickness for an edge buckle greatly reduces to ∼100 nm which is on the order of typical DB thickness targets for upper metal layers.

The possibility for buckling failure leads us to another important mechanical property of low-*k* DB and ILD films which is general delamination or adhesion failure due to other external forces.[194] As with Young's modulus / hardness, larger values are generally believed to always be better. As for critical thresholds, two rule of thumbs have been established in the industry and literature. The first is a basic "Scotch tape" test where a general purpose adhesive tape is attached to the film surface and utilized to attempt to peal the film off the substrate.[195] Any observed delamination is generally viewed as a hard failure. However, tape testing is a qualitative measurement and a passing result is typically viewed as insufficient evidence for eventual success in a fully integrated interconnect.[196,197] More stringent and quantitative adhesive / interfacial toughness measurement techniques have been developed such as nanoindentation,[197,198] superlayer/buckle,[189–192] and scratch testing.[199,200] However, the predominate test utilized in the low-*k*/Cu interconnect community has been four point bend (4 pb) testing.[201–205] For this metrology, an adhesive energy of 5 J/m^2 has been previously established as a general rule of thumb for acceptable adhesion in a low-*k*/Cu interconnect structure.[202]

Thermal requirements.— For thermal properties, it has been previously mentioned that differences in CTE between a thin film and substrate can lead to the evolution of stresses in the film on cooling from the deposition temperature. Similarly, differences in CTE between the low-*k* ILD, DB, Cu and other interconnect and packaging materials can lead to the development of significant stresses during interconnect fabrication and packaging thermal cycling events.[123,206,207] For this reason, materials with large CTE values significantly different from those of other materials in the interconnect structure are highly undesirable. The CTE for Si, SiO_2, Si_3N_4 and most low-*k* DB materials are all generally low and in the 3-5 ppm/°C range.[208–213] However, the reported CTEs for low-*k* a-SiOC:H ILDs and Cu are substantially larger at 10-20 ppm/°C[213,214] and ∼17 ppm/°C,[215] respectively. Polymeric low-*k* ILDs have been reported to have even higher CTE values of 30-60 ppm/°C,[216,217] and this has been one of the reasons cited for their general lack of main-stream adoption for low-*k*/Cu interconnect fabrication.[218,219]

Another thermal property of significant importance for low-*k* DB and ILD materials is thermal conductivity. Dissipation of thermal energy produced directly in the metal interconnect is becoming a significant concern as continued dimensional and density scaling is leading to increased Joule heating resulting from the associated increases in metal line resistance and current density.[220] If not sufficiently dissipated away, this added thermal energy can lead to increases in local interconnect temperatures that can reduce the reliability of the interconnect structure and accelerate failure mechanisms such as TDDB and electromigration.[221] While metals have a high thermal conductivity and can self dissipate a lot of thermal energy from the interconnect structure, the effeciency of this is anticipated to diminish as the effective thermal conductivity of the metal decreases due to grain boundary and interfacial phonon scattering mechanisms becoming significant at <20 nm dimensions.[222] For this reason, insulating dielectrics with a high thermal conductivity are highly desirable, particularly for preventing hot spot generation where metal line density is either sparse or asymmetric.

Bulk Cu has a high reported thermal conductivity of ∼400 W/mK.[223] In comparison, the thermal conductivity of Si_3N_4 and SiO_2 are typically reported to be lower at 0.5–1.0 W/mK[223,224] and 1.0–1.5 W/mK,[225–229] respectively. Typical low-*k* ILD a-SiOC:H dielectrics have even lower thermal conductivities of 0.01–0.4 W/mK that similarly scale with decreases in *k* as with mechanical properties.[225–235] The thermal conductivity for low-*k* DB materials exhibit similar decreases and scaling with *k*, but due to a higher density, typically exhibit values of 0.6–0.8 W/mK.[66,236,237]

Optical requirements.— For basic Cu metal interconnect structures, the optical requirements for low-*k* ILD and DB materials are comparatively loose relative to the electrical, thermal, and mechanical properties. Generally, optical transparency is desired to facilitate optical lithography and more importantly optical registration / overlay to underlying metal layers.[238] However, reflectivity issues arising from local variations in the optical properties of the low-*k* ILD, DB, and other substrate materials are typically of more concern due to the potential to cause variations and defects in the overlying photoresist pattern. These problems are typically managed via a variety of means involving hard masks (metal or dielectric) and anti-reflection coatings incorporated in the photoresist patterning stack.[20,21,24]

With the implementation of new UV curing technologies for strengthening porous low-*k* ILD materials, there has been a renewed interest in understanding the optical absorption spectrum of low-*k* dielectric materials in the UV-VUV range.[239–242] For low-*k* DB materials, there has been some concern regarding what UV curing will do the material properties of the DB given the smaller band-gap and larger absorption coefficient in the UV-VUV spectrum for these materials.[50,243] While exhaustive studies have not been reported, several studies of PECVD a-SiN:H have shown that UV curing leads to hydrogen loss, densification and a decrease in compressive stress (or increase in tensile stress).[244–246] Additional studies have shown that UV curing can also result in an increase in paramagnetic defect densities and leakage currents.[247]

Integrated requirements.—Cu/metal diffusion resistance.—An obvious integrated requirement for any dielectric diffusion barrier / metal capping layer is to prevent diffusion of the metal wire into the surrounding ILD. The presence of metal contamination in the ILD has been attributed to a number of reliability issues[248] such as increased leakage currents,[249–251] decreased TDDB lifetime[252–258] and shifts in CMOS device performance.[259–264] A number of Cu barrier performance tests have been reported in the literature. Most are based on forming an interface between Cu and the barrier material and using techniques such as secondary ion mass spectroscopy (SIMS) or Rutherford backscattering to monitor for Cu in-diffusion into the barrier and ILD material,[265,266] or X-ray diffraction to detect Cu diffusion into the underlying Si substrate and formation of $CuSi_x$.[267,268] Various electrical[269–273] and electrochemical[274,275] tests have also been reported in the literature for evaluating the Cu diffusion resistance of barrier materials. Based on these various methods, PECVD a-SiN:H has been shown to be an excellent Cu diffusion barrier.[36,37,73,75] Similar tests have also shown that a-SiC:H[59,60,64] and a-SiCN:H[44,45] can perform equivalently to a-SiN:H as Cu diffusion barriers with reduced values of dielectric permittivity as low as 4.2–4.9.[276,277] Recent studies have also indicated that dense a-SiCO:H dielectrics can also serve as Cu diffusion barriers with *k* values as low as 3.5.[51–53,55] Given that rapid Cu diffusion through SiO_2 and low-*k* a-SiOC:H with *k* values as high ∼ 2.9 have been previously reported,[273,278,279] the break point for Cu diffusion through materials in the SiO_xC_y:H system must be somewhere between $k = 3.0 - 3.5$.

H_2O/O_2 & wet chemical diffusion resistance.—In addition to serving as a barrier to Cu out-diffusion, the interconnect DB must also serve as a barrier to in-diffusion of ambient H_2O and O_2 into underlying metal layers during interconnect fabrication. In many cases, the DB may also be expected to serve as a hermetic seal for the final integrated device during operation. The need for the DB to block H_2O/O_2 in-diffusion is due to the demonstrated ability of low-k a-SiOC:H ILD materials to readily uptake moisture[280–284] and the many deleterious resulting effects that have been reported. Specifically, moisture and O_2 permeation into a metal interconnect structure has been shown to result in a number of effects ranging from increased ILD viscoplasticity,[285] dielectric constants,[286–288] and leakage currents[289–291] to reduced ILD fracture strength,[292–296] ILD/DB adhesion,[297–299] DB/metal adhesion,[300] TDDB lifetimes,[301,302] and electromigration lifetimes.[303,304]

Some of the above reliability issues, such as ILD/DB and DB/metal adhesion and electromigration, have been directly linked to H_2O/O_2 diffusion through the DB and oxidation of the underlying metal and via/trench barrier.[304] Oxidation of the latter can lead to dewetting of the metal from the via/trench barrier furthering aggravating other reliability issues such as electromigration. However, many other reliability issues are believed to be due to the susceptibility of SiO_2 and a-SiOC:H materials to the phenomenon of stress-corrosion-cracking (SCC).[305,306] SCC is essentially water assisted fracture of SiO_2 at mechanical stress levels below those predicted by the Griffith equation.[307,308] SCC is sometimes referred to as "slow fracture," and, in some regard, SCC is the mechanical analog of TDDB. The basic model for SCC involves three steps: (1) H_2O diffusion and adsorption at a strained crack tip, (2) reaction of H_2O with a strained Si-O-Si bond to form two hydrogen bonded silanol groups (i.e. Si-OH(OH)-Si), and (3) cleavage of the hydrogen bond to form SiOH + SiOH and a new fracture surface.[307,308]

Based on the above SCC model, an additional desired requirement for a DB material would be immunity to SCC. Although a few studies have shown that a-SiC:H and related DB materials can react with ambient H_2O,[309–311] the DCB studies of Matsuda have shown that the fracture energy of a-SiC:H and a-SiCN:H DB materials are insensitive to moisture in humidity levels ranging from 20 to 70%.[168,169] However, the fracture energy for a-SiCO:H DB materials were shown to be sensitive to moisture with the level of sensitivity being dependent on the concentration of Si-O-Si network bonding present in the material.[168,312]

Beyond ambient H_2O and O_2, low-k/Cu interconnect structures are exposed to additional oxidizing and corrosive chemicals during Cu chemical mechanical planarization (CMP), and wet chemical and dry plasma photoresist removal and cleans.[313–315] A low-k DB material accordingly needs to be a robust diffusion barrier to the oxidizing and corrosive reagents in these processing steps to prevent oxidation, corrosion, and etching of the underlying metal and ILD that can create many of the previously mentioned low-k/Cu interconnect reliability issues.[316] In some regards, this requirement is more demanding than the H_2O/O_2 requirement in that the concentration and/or energy of the corrosive species involved in these processes is substantially larger than ambient H_2O/O_2.[317,318]

Electromigration.—Electromigration is the movement of atoms in a conducting line under the influence of an electron flow (i.e. current), and can be viewed as the self-diffusion of metallic ions in response to an electric field.[84,85] The flux of metal atoms created by the electron wind force is balanced by a back stress that pushes the metal atoms in the opposite direction of the current. An imbalance in these two opposing forces can result in the formation of voids or extrusions that at critical sites in the metal line can result in failure of the metal interconnect.[87] At sites where there is a net depletion of atoms, local stresses become increasingly tensile, which can eventually lead to voiding in the interconnect once a critical tensile stress value is reached. At sites where there is a net accumulation of atoms, the local stresses become increasingly compressive, which can lead to the formation of metallic extrusions, short circuits, and/or mechanical failure.

For Al, the fastest self diffusion path was through grain boundaries.[319,320] However for Cu, the top surface has been identified as the fastest self diffusion path,[321] and numerous studies have identified the DB/Cu interface as the dominate electromigration path in low-k/Cu interconnects.[84–88,322] For this reason, the DB in a low-k/Cu interconnect also serves as a Cu surface capping layer to passivate the top Cu surface and reduce Cu surface diffusion contributing to electromigration.[322] This implies a need for strong bonding between the DB and Cu to both minimize Cu surface diffusion and to withstand the back stresses produced by electromigration.[324–327]

Obtaining strong bonding between the DB and Cu is particularly challenging. Prior to DB deposition, the top Cu surface will have been exposed to a variety of Cu CMP and cleaning chemicals.[328] To prevent oxidation and corrosion of the exposed Cu surface in air, it is common for the Cu CMP clean to incorporate a Cu corrosion inhibitor such as benzotriazole (BTA).[329–331] In order for the strong bonding to be achieved between the DB and Cu, these corrosion inhibitors as well as Cu surface oxides and other organic contamination must be reduced and removed. Thus, a plasma surface clean is typically performed in-situ prior to DB deposition to remove Cu surface contaminants and allow strong bonding between the DB and Cu to be achieved. A variety of NH_3/N_2 and H_2 plasma cleans have been reported in the literature[332–335] and demonstrated to facilitate both increased adhesion strengths for the DB/Cu interface and improved electromigration lifetimes.[335–338]

These pre-DB deposition plasma surface-treatments have also been shown to have additional benefits of improving the DB/ILD adhesion strength[339,340] and increasing low-k/Cu interconnect TDDB lifetimes.[341,342] Unfortunately, these same plasma surface treatments also have the ability to create plasma damage in the underlying low-k ILD leading to increased effective capacitance and degraded mechanical and electrical properties.[340] Specifically, several studies have shown that H_2 and NH_3/N_2 plasma treatments tend to abstract methyl (CH_3) groups from the low-k a-SiOC:H ILD surface that can weaken the electrical and mechanical properties of the ILD and be replaced by OH groups that increase dielectric permittivity.[343,344] The abstraction of surface methyl groups and ion bombardment from the plasma also results in a densified surface (or "crust") layer that can contribute to an increase in dielectric permittivity.[343–345] To mitigate this effect, Urbanowicz has shown that performing a He plasma treatment prior to a NH_3/N_2 plasma clean can help reduce the overall depth of plasma damage induced by the NH_3/N_2 plasma.[346–348]

Etch resistance / Selectivity.—In order for a material to be used as an etch stop for trench or via patterning of an SiO_2 or low-k a-SiOC:H ILD, the material must exhibit some resistance to common fluorinated plasma etches utilized to transfer optical lithographically defined photoresist patterns into the ILD.[349–351] As mentioned previously, Si_3N_4 and a-SiN:H typically show an etch selectivity of 2-4 relative to SiO_2 and a-SiOC:H in typical low-k ILD plasma etches.[349] This selectivity has generally been attributed to differences in the thickness of a fluorinated carbon (CF_x) layer that forms during dry plasma etching of SiO_2 and Si_3N_4/a-SiN:H with SiO_2 surfaces exhibiting <1.5 nm thick films and Si_3N_4 exhibiting film thicknesses ranging from 1.5–4 nm.[352] The differences in CF_x film formation during fluorinated plasma etching have been attributed to differences in the ability of SiO_2 vs. Si_3N_4 surfaces to consume deposited surface carbon during the etching reactions. More specifically, it is believed that deposited carbon is quickly returned to the gas phase via formation of volatile species such as CO, CO_2, COF_2 on SiO_2 vs. CNF on Si_3N_4 due to differences in bond strengths and the volatility of the etch by products.[352]

Low-k a-SiC:H and a-SiCN:H ES/DB materials have also been reported to exhibit high etch selectivities (2–10) relative to SiO_2 and low-k a-SiOC:H ILD materials.[38,353,354] The high etch selectivity has been similarly attributed to differences in the thickness of a deposited CF_x layer that forms on the various surfaces during plasma etching.[104,351–354] Additional studies by Posseme[355] and Standaert[106] have shown that the composition of the CF_x layer is also an important consideration with lower etch rates being observed for CF_x layers with reduced fluorine composition. These same studies have also shown that the exact composition of the CF_x layer is dependent on the plasma etch chemistry and plasma conditions. However in the case of a-SiC:H and a-SiCN:H low-*k* DB materials, the formation of a CF_x surface layer is likely aided by the presence of carbon already in the film and that helps contribute in some cases to an increased etch selectivity.

Regarding specific ILD/ES etch selectivity requirements, these will be highly dependent on the type of interconnect fabrication scheme employed. For a via first dual damascene approach, an ILD/ES etch selectivity as high 50:1 may be required to facilitate the following trench etch without unintentionally breaking through the ES early and etching into the underlying Cu and ILD.[316] This etch selectivity requirement can be reduced by using other sacrificial via fill materials,[316] or other trench first, partial via/trench patterning schemes.[20,21]

Resist poisoning.—"Resist poisoning" is a phenomenon where photoresist patterns generated in an optical lithography process are not precisely formed as intended.[91] One mechanism largely believed to lead to resist poisoning in low-*k*/Cu interconnect patterning is a reaction between the photoresist and residual amines (NH_3) in the low-*k* ILD that prevents the photoresist from developing properly.[91,92] Based on this mechanism, an additional integrated requirement for low-*k* DB materials is to prevent amines present in underlying metal layers from outgassing into the top metal layer being patterned. This requirement also implies that the low-*k* DB may not be a source of amines. This can be a challenging and conflicting requirement for a-SiN:H and a-SiCN:H DB materials that are typically deposited using NH_3 and/or silazane precursors and can contain significant amounts of residual amines after deposition.[41–51] The no amines requirement can also be a challenge for a-SiC:H and a-SiCO:H DB materials that do not incorporate nitrogen in the deposition process, but that may utilize an NH_3 plasma pre-treatment to improve adhesion of the DB to the underlying Cu and low-*k* ILD surfaces.[331–334]

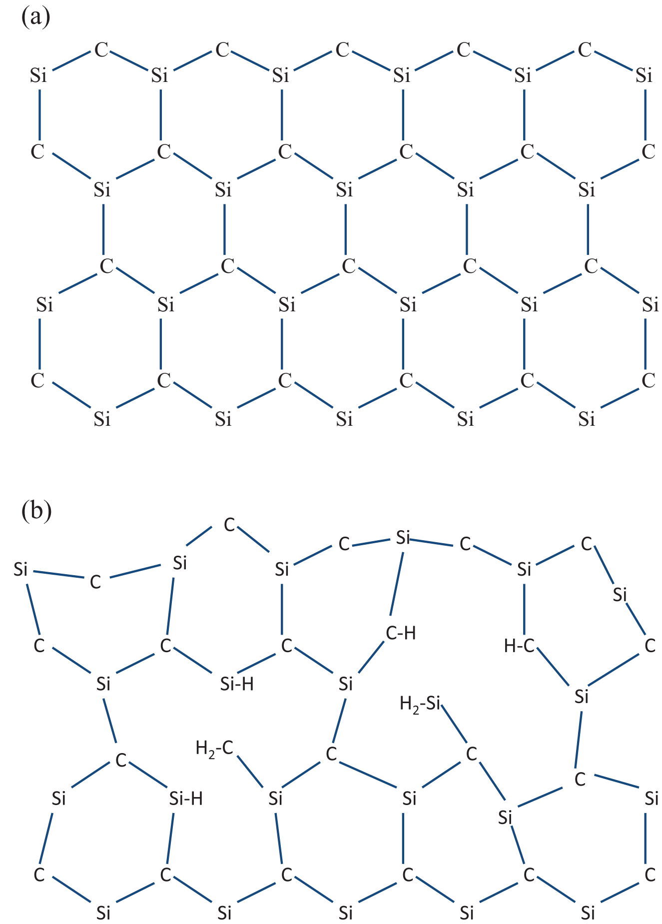

Figure 6. Schematic diagrams illustrating (a) the dense crystalline SiC structure and (b) the dense structure for a low-*k* a-SiC:H DB.

Current Status of Low-*k* DB/CCL/ES Materials and R & D

Deposition methods and atomic structure.— As mentioned previously, thin films of a-SiC, a-SiCN:H, and a-SiCO:H low-*k* DB materials are primarily deposited by PECVD methods using a variety of silane, silazane, organosilane, and alkoxysilane precursors[357,358] in combination with reactive and diluent gases such as NH_3, N_2, CO_2, O_2, H_2, and He. Reductions in dielectric constant are primarily achieved via intentionally introducing controlled levels of nanoporosity through the incorporation of terminal hydrogen or organic groups during film deposition.[310,311] These terminal groups disrupt the SiC, Si_3N_4 or SiO_2 network structure resulting in a material with increased free volume (and/or porosity).[66] The effective *k* of the material is then the volume average of the *k* for the free volume ($k = 1$) and that for the matrix.[16,359]

Similar precursors and methods are also utilized to deposit low-*k* ILD materials. As shown schematically in Figures 6 and 7, the primary difference between low-*k* ILD and DB materials is the starting network structure, the type and concentration of network disrupting terminal groups, and the resulting amount of nano-porosity created. For low-*k* DB materials, SiC and Si_3N_4 matrices are preferred due to a dense network structure (see Figure 6a). Incorporation of terminal hydrogen groups disrupts this dense network structure and helps create nano-porosity leading to a decreased effective dielectric constant (see Figure 6b). In plasma deposition processes, this is typically achieved by utilizing primarily hydride precursors and/or plasma process conditions that expose the growing film surface to significant amounts of ion bombardment that facilitates elimination of terminal hydrogen bonding and densification of the film.[176] The remaining nano-porosity in low-*k* DB materials is undetectable by techniques commonly utilized to investigate porosity in low-*k* ILD materials such as ellipsometric porosimetry,[360] and requires more sensitive techniques such as positronium annihilation lifetime spectroscopy (PALS)[361] to be detected. Detailed PALS investigation have shown that the diameter of nano-pores in robust DB materials are typically <0.4–0.5 nm.[52,56,77]

For low-*k* ILD materials, SiO_2 network materials are preferred due to the more open network structure of SiO_2 and the corresponding lower starting *k* exhibited relative to SiC and Si_3N_4 (see Figure 7a).[77] To make a low-*k* material from SiO_2, terminal organic groups (most commonly methyl (CH_3)) are incorporated in the film during deposition.[15,25] These larger terminal organic groups help to create larger nano-pores and greater reductions in *k* (see Figure 7b). Incorporation of terminal organic groups in plasma deposited low-*k* ILD films is typically achieved using either organosilane or alkoxysilane precursors in combination with plasma conditions that minimize film surface ion bombardment.[156,177,178] The resulting pores in typical low-*k* ILD materials are also larger at ≥0.8 nm.[77] Thus, despite using similar precursors and deposition methods, the significantly different material properties exhibited between low-*k* DB and ILD materials are due to differences in the network structure, terminal bonding ligands, and size of nanopores.

Material structure-property trends.— In addition to reducing *k*, the introduction of nano-porosity also reduces the value of many other important material properties for low-*k* DB and ILD materials. Thus, a common goal for both low-*k* DB and ILD materials is to achieve the maximum desired material properties (electrical, mechanical, thermal, . . .) for the lowest possible desired value of dielectric permittivity. For low-*k* ILD materials, this has resulted in numerous *k* vs. material property trends reported in the literature. Due to the extremely reduced thermal and mechanical properties exhibited by

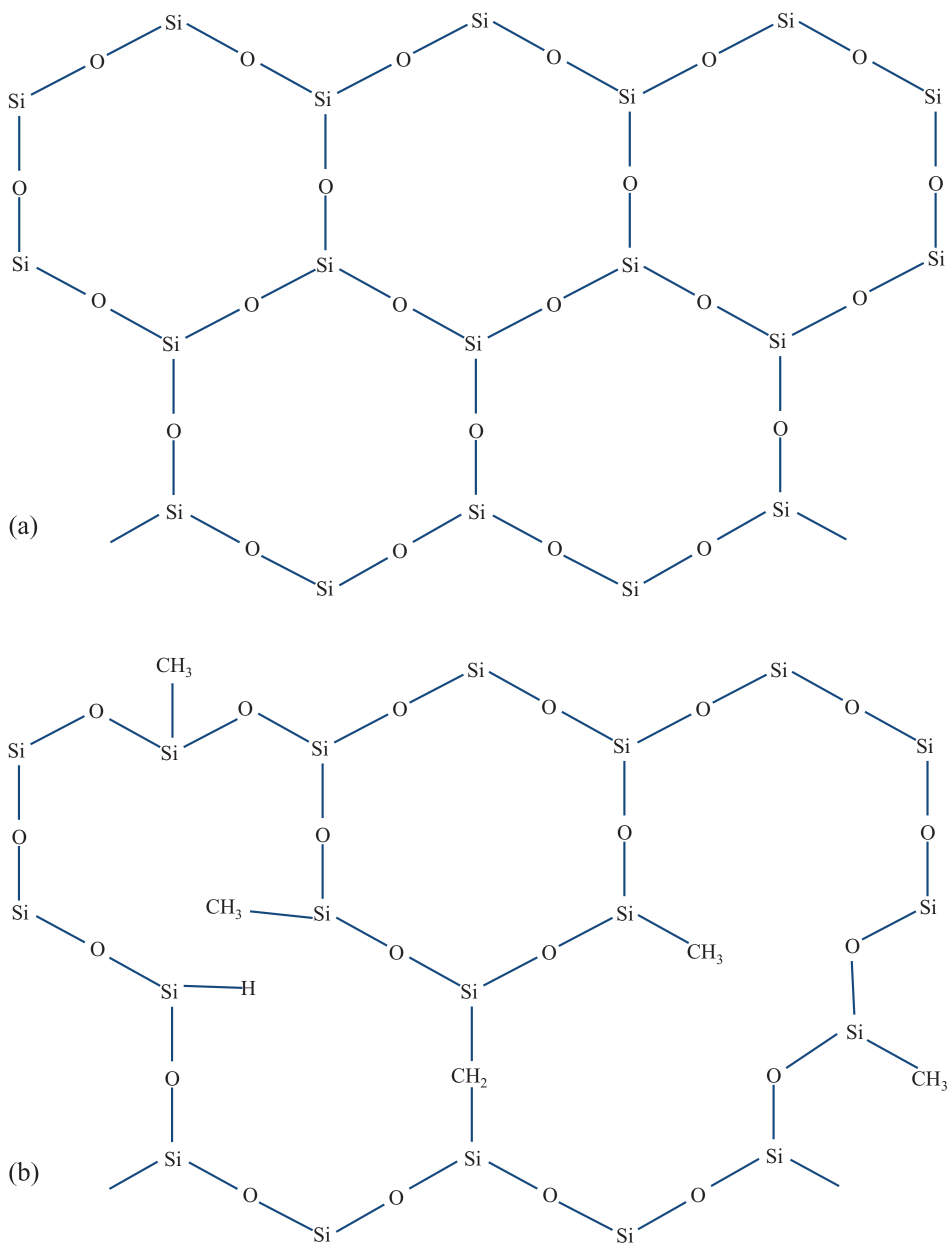

Figure 7. Schematic diagrams illustrating (a) the crystalline SiO_2 structure and (b) the structure for a low-*k* a-SiOC:H ILD.

low-*k* ILD materials relative to SiO_2, *k* vs. Young's modulus[136–147] and thermal conductivity[223–235] trends have been perhaps the most frequently reported in the literature. Correlations between porosity and low-*k* ILD thermal and mechanical properties have also been frequently reported in the literature owing to the interdependence of *k* and porosity and the exponential increase in difficulty associated with integrating low-*k* ILD materials with increasing levels of interconnected porosity.[157,230,362] All of these studies have shown a general deterioration in thermal and mechanical properties with decreasing *k* and increasing porosity.

For low-*k* DB materials, the relation between *k* and various material properties have been similarly investigated.[44–68] As shown in Figure 8, a-SiC:H DB materials exhibit exactly the same trend of decreasing Young's modulus with decreasing *k* as that observed for low-*k* ILD materials.[66] Similar correlations between *k* and hardness, fracture energy, and thermal conductivity for low-*k* DB materials have also been reported in the literature.[138,168–170]

For a-SiC:H DB materials, the relation between *k* and other material properties has been shown to be more fundamentally tied to the average bond coordination of the material through bond constraint and rigidity percolation theory.[77,362,364] The average bond coordination of a material ($\langle r \rangle$) is simply the average number of bonds formed by all the atoms in the system. Bond constraint and rigidity theory predict that for amorphous systems essentially all material properties should be a direct function of $\langle r \rangle$.[365,366] However, constraint theory also predicts the existence of a critical coordination number ($\langle r \rangle_c$) that below which the material properties of the system will be invariant with further reductions in $\langle r \rangle$. For four fold coordination network materials such as SiO_2, Si_3N_4 and SiC, $\langle r \rangle_c = 2.4$.[367,368] As shown in Figure 9, the nanoindentation Young's modulus for a-SiC:H exhibits an $\langle r \rangle^{3/2}$ dependence for $\langle r \rangle > 2.4$ but is invariant at $\langle r \rangle < 2.4$, consistent with rigidity and constraint theory predictions.[77]

One interesting aspect of constraint theory is the prediction of increased resistance with decreasing $\langle r \rangle$ (or *k*).[369] Such an inverse correlation between *k* and electrical resistivity has been recently observed for a-SiC:H (see Figure 10).[77] In this case, the increase in resistivity also correlated with a decrease in paramagnetic defect density as measured by electron paramagnetic resonance (EPR) measurements.[370] This suggests that the variation in resistivity may also be tied to the presence of point defects in a-SiC:H along with the average coordina-

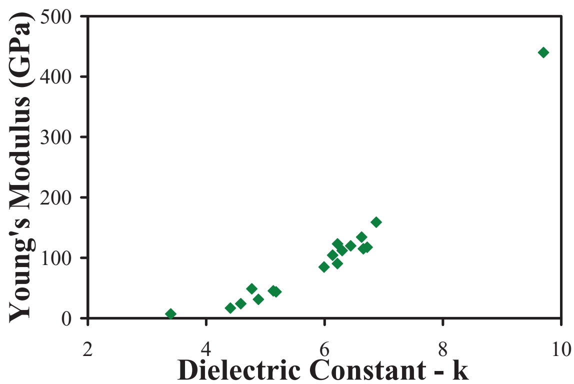

Figure 8. Young's modulus vs. dielectric constant – *k*, for a-SiC:H DB materials.

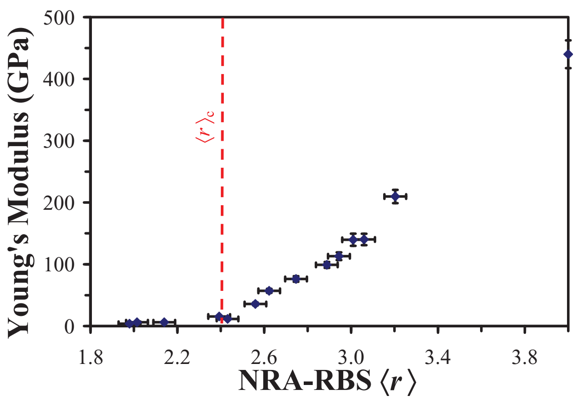

Figure 9. Nanoindentation Young's Modulus vs. average bond coordination (⟨*r*⟩) for a-SiC:H DB materials.

tion. The increase in EPR paramagnetic defects with increasing *k* is believed to be due to the plasma deposition conditions that involved increasing levels of ion bombardment to densify the film and increase *k*.[370] EPR measurements on low-*k* ILD a-SiOC:H dielectrics have shown similar trends where clear differences in resistivity and EPR defect density were observed between a-SiOC:H films deposited by plasma vs. spin-on deposition where the latter involves condensation reactions as opposed to bond scission reactions in plasma deposition processes.[371] This is perhaps one of the few cases where a desired improvement has been observed while decreasing *k* for a material.

For low-*k* DB materials, integrated properties such as diffusion and etch resistance are typically of more interest. In this regard, the diffusion barrier performance and etch selectivity of a material should intuitively be more directly related to porosity and/or atomic/mass density than *k*. As DB materials are generally determined to be non-porous based on typical techniques such as ellipsometric porosimetry,[360] and thin film mass density is easily measured using X-ray reflectivity (XRR)[372–374] and other readily available techniques, a comparison of low-*k* DB material properties and diffusion resistance against mass density can provide more insight. Figure 11 shows the *k* vs. XRR mass density trend for a-SiC_xN_y:H films of varying composition. Each trace represents a statistical design of experiment (DOE) where gas pressure and RF power were adjusted around a specific $(CH_3)_xSiH_{4-x}$/ammonia gas ratio to generate films with a range of dielectric constants and density with similar compositions. As can be seen, each $(CH_3)_xSiH_{4-x}$/ammonia gas ratio exhibits a unique linear relation between mass density and dielectric constant with *k* increasing with mass density. For a given mass density, the lowest *k* is given by pure a-SiN:H films. This is due to fully dense / crystalline SiC having a higher *k* than fully dense / crystalline Si_3N_4.[77]

For the a-SiC_xO_y:H system, a completely opposite trend for *k* vs. density has been observed. As shown in Figure 12 for another series of design of experiments involving various $CO_2/(CH_3)_xSiH_{4-x}$ ratios, the *k* for a-SiCO:H has actually been observed to decrease with increasing mass density.[77] This counter intuitive trend is a result of the SiCO:H composition changing along with mass density. Specifically, the higher density films were found to have <5-10% carbon via X-ray photoelectron spectroscopy (XPS) measurements[77] and exhibited transmission Fourier-transform infra-red (FTIR) spectra similar to SiO_2. XPS of the lower density films showed 20-40% carbon and transmission FTIR showed prominent Si-C bonding stretching modes at 800 cm^{-1} in addition to the asymmetric Si-O-Si stretch absorption band at 1010 cm^{-1}. This indicates that while mass density is increasing, the SiCO:H films are becoming more oxide like and adopting a more open network structure with larger diameter nano-pores.

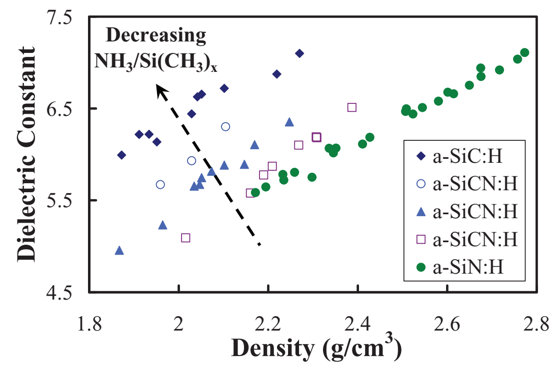

Figure 11. Dielectric constant (*k*) vs. XRR mass density for a series of low-*k* a-SiC_xN_y:H DB materials.

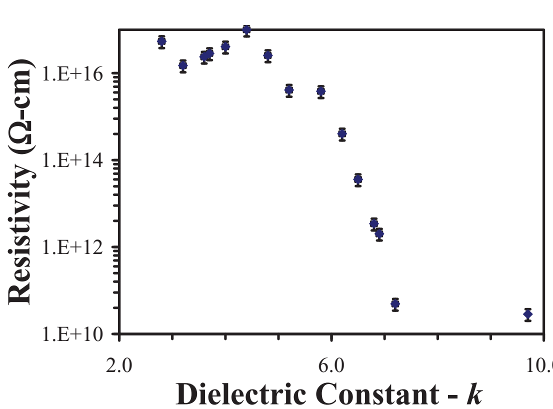

Figure 10. Electrical resistivity vs. ⟨*r*⟩ for a-SiC:H DB materials.

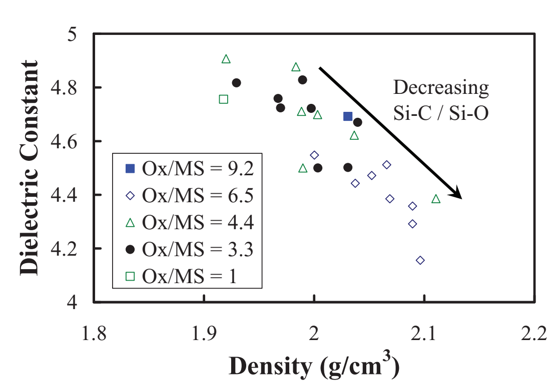

Figure 12. Dielectric constant (*k*) vs. XRR mass density for a series of low-*k* a-SiC_xO_y:H DB materials.

The above k vs. density trends have serious implications regarding k scaling for diffusion barrier applications. As we will discuss next, critical thresholds in mass density and nano-porosity exist for preventing Cu and H_2O diffusion. These thresholds in turn place limitations on the lowest possible k that can be achieved for a given composition to prohibit diffusion of a particular specie.

Integrated structure-property trends.—Cu and H_2O diffusion resistance.—As mentioned in previous sections, reducing the k of a DB material involves the controlled introduction of increasing levels of nano-porosity that in turn increases the likelihood for in-diffusion of ambient moisture/oxygen, wet chemicals, and plasma activated species and out-diffusion of the metal conductor and other metallic/ionic species. Accordingly, it can be anticipated that a critical threshold for nano-porosity and/or mass density will exist where a material may no longer adequately perform as a DB. In fact, such critical thresholds have been previously reported in the literature.[52,77]

Perhaps the first study to investigate critical nano-porosity thresholds in low-k DB materials was that by Ishimaru where the authors investigated the barrier performance of SiCO:H materials to diffusion of Cu, H_2O, O ions and O radicals using a variety of tests.[52] To investigate Cu barrier performance, they deposited 100 nm of a-SiOC:H on a 150 nm Cu/30 nm Ta/50 nm TaN/Si substrate and used secondary ion mass spectroscopy (SIMS) to detect Cu diffusion into the film after annealing at 450°C. In these experiments, they observed that the PALS pore diameter needed to be <0.51 nm and the XRR density> 2.06 g/cm^3 in order to prevent Cu diffusion. Ishimaru correlated this critical pore diameter to the diameter of atomic Cu and Cu^+ which are 0.26 and 0.19 nm, respectively, and roughly half the diameter of the average pore size. Based on this, they rationalized that the diffusing Cu specie may possibly be CuO which has a slightly higher diameter of 0.38 nm.[52]

To investigate H_2O diffusion, Ishimaru utilized a 500 nm phosphosilicate glass (PSG) film with 5 wt% phosphorous deposited by PECVD as a moisture detector and coated this film with the a-SiOC:H barrier films of interest.[52] The authors utilized transmission FTIR to monitor a decrease in the intensity of the P = O bond in this material that is well know to react with moisture and convert to P-O.[52,56] By monitoring the decrease in intensity of the P = O absorption band and the appearance of any related SiO-H absorption, moisture diffusion through the a-SiOC:H film and into the underlying PSG film could be monitored. After a 24 hour bake in a 2 atmosphere pressure cooker, Ishimaru noted moisture diffusion through all the a-SiCO:H films investigated.

More detailed studies of the moisture diffusion resistance for a variety of low-k a-SiC:H, a-SiN:H, a-SiCN:H, and a-SiCO:H DB materials have been recently reported by King et al.[77] In this study, the authors utilized a 2 micron thick SiO_2 layer whose stress became increasingly more compressive on exposure to and absorption of H_2O. By coating the SiO_2 H_2O detector film with DB materials of varying mass density and nano-porosity and observing stress changes in the composite stack over time, the authors were able to observe moisture diffusion through the barrier film as a function of time. As shown in Figure 13, no change in wafer bow was observed for 50 nm thick DB films with mass density > ∼ 2.25 g/cm^3 which was determined to be the critical mass density for prohibiting moisture diffusion at room temperature.

By combining the above results with additional PALS measurements of the same DB materials, King et al. where also able to correlate H_2O diffusion to pore diameter. In their case, they found no detectable penetration of H_2O was observed within the scale of the experiments (1 month) for films with pore diameters ≤ ∼ 0.45 nm. These results are consistent with the previously mentioned Ishimaru study where all the a-SiCO:H films investigated had a PALS pore size > 0.44 nm.[52] However similar to the Ishimaru study, the observed critical pore diameter is close to twice the reported molecular diameter of H_2O (0.27 nm).[375] These combined observations indicate that pore size is perhaps not the rate limiter, but instead the interstices between the pores. These results suggest that the ratio of pore size to pore interstitial in low-k DB materials is ∼ 2:1.

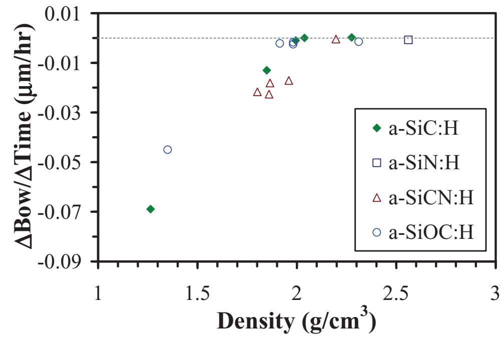

Figure 13. 50 nm DB/2 micron SiO_2 wafer bow drift/time for a series of low-k DB materials of varying density and composition.

The results of Ishimaru and King have serious implications for k scaling of DB materials. These two studies combined indicate that for a material to be a robust DB, the mass density must be >2.2 g/cm^3 and the median pore diameter must be <0.4 nm. Referring to Figure 14 where we plot k vs. massy density for a-SiC:H, it can be seen that the lowest possible k achievable at ≥2.2 g/cm^3 is 6.7 for a-SiC:H. However as shown in Figure 11, the addition of nitrogen to a-SiC:H can enable the k to be decreased significantly while still maintaining a mass density >2.2 g/cm^3. For a pure a-SiN:H film, Figure 11 indicates that a k as low as 5.5 may be achieved at 2.2 g/cm^3.

The above predictions are consistent with many other low-k DB studies reported in the literature.[100–103] Specifically, Cui has reported significant Cu penetration and diffusion in a-SiCN:H and a-SiC:H films with k values of 4.9-5.1 and 4.4-4.6 respectively.[120,121] Based on Figure 11, the mass density (and pore sizes) for these films are likely less (greater) than the 2.2 g/cm^3 (0.5 nm) thresholds previously discussed. Similarly, Chen et al have reported that higher nitrogen content a-SiCN:H films exhibit improved barrier properties against Cu penetration.[121] As we have shown, for a specific dielectric constant, higher nitrogen content films have a higher density / lower pore diameter that should lead to improved barrier performance. Cheng et al have also investigated the diffusion barrier performance of a wide range of a-SiN, a-SiC:H, a-SiOC:H, a-SiCN:H and a-SiOCN:H films with roughly similar dielectric constants.[68] They observed that the Cu diffusion performance increased in the following order a-SiC:H <a-SiOC:H <a-SiCN:H <a-SiOCN:H <a-SiN:H. These observations are consistent with our general observation that a-SiC:H and a-SiN:H are denser materials with smaller pore sizes and that a-SiN:H offers the lowest k for a given density / pore size.

It is important to note that while the minimum k for a robust a-SiCN:H Cu/H_2O diffusion has been shown to be ≈ 5.5, utilization of a-SiCN:H and a-SiOC:H DB layers with k values significantly less than this are commonly reported in the literature.[47,341] The reason for

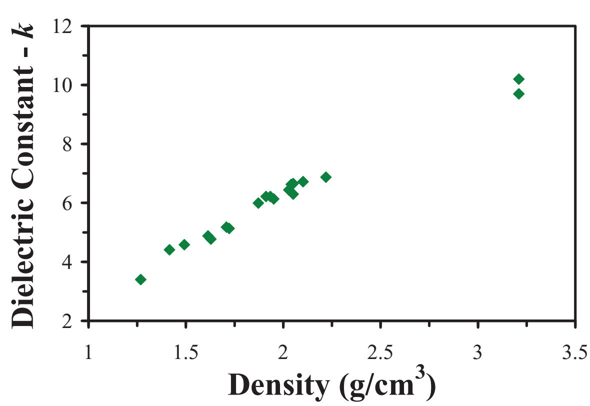

Figure 14. Dielectric constant – k vs. XRR mass density for a-SiC:H.

utilizing such DB layers is likely due to the previously mentioned need to reduce the impact of the DB k on the interconnect RC performance. This illustrates the delicate balancing act and trade offs that semiconductor manufacturers must face between interconnect performance and reliability. It is likely that the successful utilization of such $k < 5.5$ DB layers is addressed by minimizing processing times between various processing steps in the low-k/Cu interconnect fabrication and/or minimizing exposure to various acqueous chemistries during processing steps such as wet chemical photoresist removal and CMP.

Electromigration.—A number of methods have been identified and reported for improving the electromigration resistance of the DB/Cu interface beyond performing *in-situ* pre-DB deposition surface cleaning. Many of the reported methods involve either doping the Cu lines with a few percent of select alloying elements,[376–382] or selectively forming an additional surface passivation layer material between the DB and Cu.[383–393] In most cases, these methods involve additional processing steps separate from the DB deposition process. However, one method that has been integrated with the DB deposition involves selectively forming a CuSiN interfacial layer between the DB and Cu.[383–391] This is achieved *in-situ* prior to DB deposition by pre-exposing the post Cu CMP interconnect surface to SiH_4 which selectively and catalytically decomposes on the Cu line to form a $CuSi_x$ surface layer. This surface layer is then converted into CuSiN by performing a nitridizing plasma treatment that is then followed by the DB deposition. To prevent the entire Cu line from converting to $CuSi_x$, the SiH_4 pre-treatment is typically performed at temperatures of 200-275°C that are substantially below the typical DB deposition temperatures of 350-400°C. In principle, the lower SiH_4 treatment temperature lowers the diffusion coefficient of Si and limits the $CuSi_x$ formation to just 1-2 nm of the Cu surface before the nitridization occurs that essentially locks the Si to Cu/DB interface. This method has been reported to provide up to a 2-4X improvement in electromigration lifetime relative to pure Cu.[386,387,390] The primary drawbacks to this approach are the non-isothermal processing which can require multiple process chambers / stations and variations in line resistivity that can occur due to differences in the amount of Si incorporated into wide vs. narrow metal lines.

Other methods for doping Cu lines typically involve incorporating the dopant directly into the Cu target utilized for physical vapor deposition of the initial Cu seed layer.[376–383] Numerous different types of dopants elements beyond Si have been reported for Cu with Sn, Al, Mg, and Mn being perhaps the most popular. In this method, the improvements in electromigration are believed to be due to the dopant atom segregating from the bulk Cu and diffusing to the Cu/DB interface and helping passivate the Cu surface and/or improving the adhesion strength between Cu and the DB. This method of improving EM has been reported to increase Cu electromigration lifetimes by 10–1000×[380,382] depending on the type and concentration of the alloying element. The primary drawback to this method is the resulting increase in Cu line resistivity from adding the alloying agent.

One final method for improving the electromigration resistance of the DB/Cu interface is to selectively deposit a passivating metal on the Cu surface typically using electroless plating methods.[392,393] CoWP and CoSnP are two passivating metals that have been commonly reported in the literature that can be electrolessly plated on Cu and that have been utilized to increase the electromigration resistance of DB/Cu interfaces by >100X. The primary drawbacks to this approach are the difficulty of achieving perfect selectivity in the presence of inevitable surface defects, compatibility of the selective metal caps with next metal layer patterning and cleaning steps, and the added cost associated with the additional processing step.

Etch selectivity.—While significant effort has been focused on understanding the influence of plasma etch chemistry,[349–356] low-k ILD porosity,[394] and ILD composition[395] on the low-k ILD plasma etch mechanisms and profiles, most ILD/ES etch selectivity studies have focused on a singular a-SiN:H or a-SiC:H ES material. Relatively little work has been reported investigating in detail how the properties and composition of the low-k ES can influence etch selectivity. As we will show next, the composition and properties of both the ES/DB and ILD are important considerations for etch selectivity in addition to the plasma etch chemistry and other photoresist pattern transfer details.

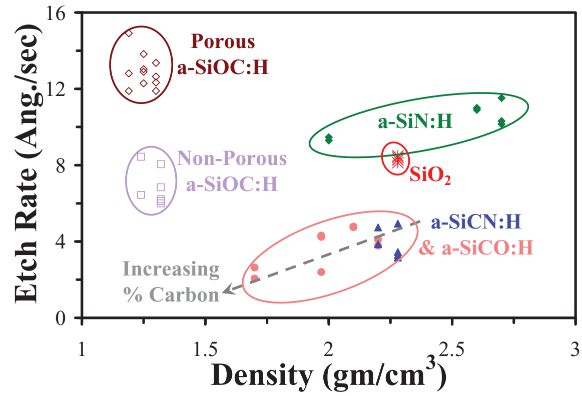

Figure 15. CHF_3 dry plasma etch rate for a series of ILD (SiO_2 and a-SiOC:H) and ES/DB (a-SiN:H, a-SiCN:H, a-SiC:H, a-SiCO:H) films as a function of XRR mass density.

To investigate the influence of low-k ES and ILD composition on etch selectivity, a series of ILD (SiO_2 and low-k a-SiOC:H) and ES/DB (a-SiN:H, a-SiCN:H, a-SiC:H, a-SiCO:H) thin film 1×1" coupons were fixed time blanket etched together in a 300 mm diameter stand alone Oxford plasma etcher utilizing two different plasma etches typically used for selective SiO_2 and Si_3N_4 etching. To measure the blanket etch rate for each film, a portion of the sample was physically masked using a smaller 1×1 cm^2 Si wafer coupon placed on top of the film. A surface profilometer was used to determine the etch thickness by measuring the step height created between the etched and un-etched portions of the sample.

The first plasma etch investigated was a common CHF_3 based etch commonly used for selectively etching SiO_2 with a Si_3N_4 etch stop. Figure 15 shows the measured etch rates for the various low-k ILD and DB films investigated as a function of their mass density as measured by XRR. Numerous different trends can be observed. First, one can see that there is a relatively small difference in etch rate for SiO_2 vs. a-SiN:H with the a-SiN:H ES films etching slightly faster. In contrast, the a-SiCN:H and a-SiCO:H ES materials etch 2-4X slower than SiO_2. A similar though smaller reduction in etch rate is also observed for the non-porous a-SiOC:H films relative to SiO_2. As mentioned previously, this can be possibly attributed to the presence of carbon in these films and the buildup of a thicker CF_x surface layer during etching. More data to support this hypothesis will be shown later.

For the a-SiN:H, a-SiCN:H, and a-SiCO:H films, a small but noticeable decrease in etch rate is observed with decreasing mass density. These trends seem somewhat counterintuitive as one might expect that as mass density decreases, the number of chemical bonds needing to be broken would decrease and etch rate should go up with decreasing mass density if everything else remains the same. However, this is not the case. For the a-SiN:H films, the Si/N ratio slowly decreases below 1:1 for films with mass density of 2.5 g/cm^3 to 0.8-0.9:1 for films with mass density of 2.0 g/cm^3. Similarly for the a-SiCN:H and a-SiCO:H films, the carbon content increases with decreasing mass density. Thus, the decreases in etch rate with decreasing mass density are attributed to the formation of thicker CF_x surface layers due to the presence of carbon in the film. This is further supported by Figure 16, where we show additional etch rates for all the previous films as a function of percent carbon as determined by XPS.

In both Figures 15 and 16, one can observed that the etch rate for the porous a-SiOC:H low-k ILD films is higher relative to both SiO_2 and the non-porous a-SiCO:H films. In this case, we attribute the increased etch rates to the ability of the reactive ions and radicals generated in the plasma to diffuse further below the surface of the film and accelerate etching from the inside out.

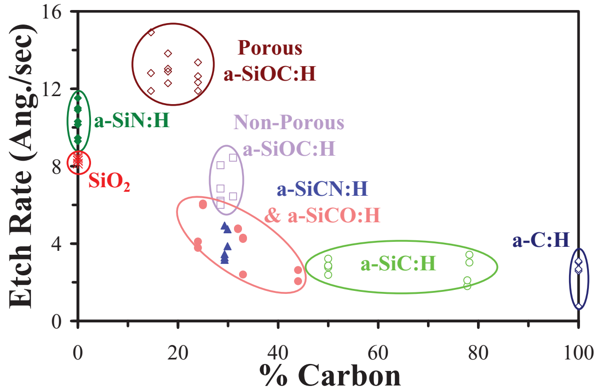

Figure 16. CHF_3 dry plasma etch rate for a series of ILD (SiO_2 and a-SiOC:H) and ES/DB (a-SiN:H, a-SiCN:H, a-SiC:H, a-SiCO:H) films as a function of XPS carbon content.

The second plasma etch investigated was a common CF_4/O_2 based etch commonly used for selectively etching Si_3N_4 relative to SiO_2. In this case (see Figure 17), we see that the a-SiN:H and a-SiCN:H films have 4-30X higher etch rates relative to SiO_2 and both the non-porous and porous low-k a-SiOC:H films. We also observe the intuitive trend of increasing etch rate with decreasing density for the a-SiN:H and a-SiCN:H ES films. Interestingly, while a-SiCN:H and a-SiCO:H exhibited similar etch rates using the CHF_3 etch, the two have very different etch rates using CF_4/O_2. The fast etch for the a-SiCN:H could possibly be attributed to the presence of oxygen in the plasma helping to clear the etch surface of CF_x polymer residue via formation of CO, CO_2 and COF, while the for a-SiCO:H the presence of oxygen in the film somehow prohibits this mechanism.

As plasma etch chemistry and photoresist composition are also important details, it is possible that the above results and trends are specific to the plasma etches and hard mask utilized, and that different results/trends may be observed using other plasma etch chemistries and photoresist. However, the above results highlight the roles that the composition of both the ES/DB and ILD can play in determining dry etch selectivity for a metal interconnect fabrication process. Although numerous other previously mentioned integration requirements may place constraints on the composition of the ES/DB, careful attention to the composition of the ES/DB and ILD may allow for enhanced etch selectivities and process latitude to be achieved in a metal interconnect fabrication process.

Permittivity scaling limitations.—Diffusion resistance vs. thickness vs. topography.—As DB materials typically have a higher k relative to the ILD in metal interconnect structures, there is always a desire to minimize the thickness of the DB in order to minimize the impact to the overall capacitance and RC delay of the interconnect. This raises the question of what is the minimum required thickness for a material to serve as an adequate diffusion barrier to both Cu and amine out-diffusion and H_2O/O_2 in-diffusion. This is a particularly germane question as the 2013 ITRS projects the thickness of the DB in a low-k/Cu interconnect will need to be only 1–2 nm thick in the next decade.[107] Unfortunately, early studies of the Cu diffusion barrier performance of a-SiN:H DB materials utilized relatively thick (>=100 nm) films,[37,73,75] and more recent studies of low-k DB materials have focused on evaluating Cu and H_2O barrier performance at thicknesses of 30–100 nm.[44–68] Only a few studies have attempted to investigate the ultimate limits in terms of DB thickness scaling.[36,66,396] Of these, Vogt has shown that 10 nm of plasma deposited a-SiN:H can serve as a Cu barrier in bias temperature stress (BTS) testing of metal-insulator-semiconductor (MIS) devices.[36] More recently, Usami has demonstrated that an ultra thin 3 nm a-SiN:H layer in conjunction with a 42 nm, $k = 3.6$ a-SiCN:H etch stop layer that can serve as both a moisture and Cu blocking diffusion layer.[396] King has also investigated in more detail the influence of thickness scaling from 50 to <10 nm on H_2O diffusion barrier performance for low-k a-SiC:N:H, a-SiCO:H, and a-SiC:H DB films.[66] In this case, a-SiCN:H and a-SiC:H films which were good barriers at 50 nm were observed to maintain their barrier performance down to 10 nm. However, a-SiCO:H films that were good H_2O barriers at 50 nm were not observed to remain so at 10 nm. This was attributed to these a-SiCO:H films having slightly larger pore diameters relative to the a-SiC:H and a-SiCN:H films investigated.[66]

However, it should be noted that all of the previously mentioned Cu and H_2O diffusion barrier tests should be viewed as a rather optimistic assessment of the ultimate barrier performance of the dielectric films (and deposition process). It is well established in the literature that the presence of incoming surface defects / topography on a substrate can create seams and "pinholes" in the barrier film during deposition and limit the diffusion barrier performance of the material.[397–401] King has previously shown that a 25 nm PECVD a-SiN:H film can serve as an excellent H_2O diffusion barrier when deposited on a flat Si wafer with essentially zero topography.[66] However, when deposited over an oxide with 100 nm deep plasma etched trenches, the same PECVD a-SiN:H film no longer behaves as a moisture diffusion barrier.[42] This is due to both the less than unity step coverage and non-uniform sidewall growth exhibited by most plasma deposition processes. The latter is particularly important as King was able to show that by switching to a plasma enhanced atomic layer deposition (PEALD) process, the non uniform a-SiN:H sidewall growth could be eliminated and an H_2O diffusion barrier film could be formed over the same oxide topographic structures.[42]

The implications of the above discussion are that traditional Cu and H_2O diffusion barrier tests may over estimate the performance of various dielectric films in actual low-k interconnect structures due to the inevitable presence of both surface defects/particulates and topography. Due to this, more stringent test methods that account for or simulate the presence of surface defects and topography such as those demonstrated by King need to be adopted to understand the true barrier performance of future DB materials in interconnect structures. Similarly, traditional PECVD methods for depositing low-k materials may be challenged to meet the future goals of 1-2 nm DB films forecasted by the ITRS. Accordingly, new super conformal ALD and PEALD methods may need to be developed and adopted to meet the need for future low-k DBs.

Etch selectivity vs. thickness.—Similar to DB materials, there is always a desire to minimize the thickness of an ES in order to minimize the impact to the overall capacitance and RC delay of the interconnect. In this case, the minimum possible thickness is bounded by both material property constraints (i.e. ES/ILD etch selectivity), etch process constraints, and overall patterning scheme. Due to the multi-variate nature and complexity of this problem, very few investigations of

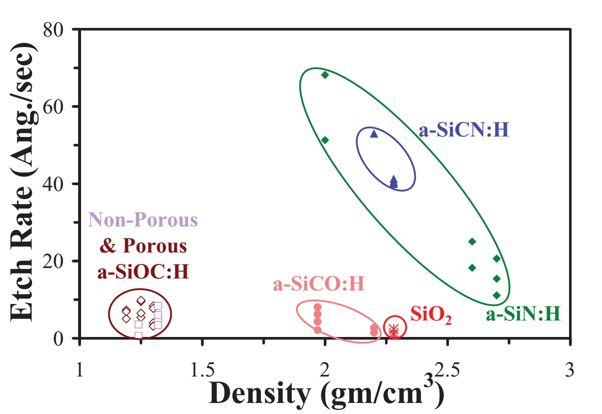

Figure 17. CF_4/O_2 dry plasma etch rate for a series of ILD (SiO_2 and a-SiOC:H) and ES/DB (a-SiN:H, a-SiCN:H, a-SiC:H, a-SiCO:H) films as a function of XRR mass density.

the minimum required ES thickness in a DD patterning process have been reported in the literature.[316] This may be due to the minimum DB thickness exceeding the minimum required ES thickness in most patterning schemes. However, this could change as the DB thickness decreases to 1–2 nm as forecasted by the ITRS.[107]

Future Trends and Research Needed for Low-*k* DB and ES Materials

Beyond thickness scaling, the ITRS also forecasts continued *k* scaling for both low-*k* ILD and DB/ES materials.[107] For low-*k* DB and ES layers, it is anticipated that diffusion barrier materials with $k < 3.0$ will be needed in manufacturing by the 2020 time frame. Based on the prior discussion, the *k* of current state of the art a-SiC:H, a-SiCN:H, and a-SiCO:H materials range from 3.5–5.8. Therefore, new methods for achieving lower *k* DB films will be needed. In this and the following sections, we review some of the research directions currently being explored to meet both the *k* and thickness scaling challenges set by the ITRS for low-*k* DB and ES materials. We cover both scaling of traditional low-*k* materials in the Si-C-O-N-H phase diagram as well as new materials outside this composition space. The latter will also lead to discussion of previously mentioned alternative DB/ES deposition methods such as ALD and PEALD.

Continued k scaling in Si-O-C-N system.— One interesting method that has been recently described by Shimizu attempts to utilize the incorporation of long Si-$(CH_2)_x$-Si networks to achieve both a reduction in *k* and improvement in diffusion barrier performance for a-SiC:H thin films.[402–405] Shimizu's results using precursors such as 1,1-divinyl silacyclopentane (DVScP) and 5-silaspiro-[4,4]-nonane (SSN) have shown that a-SiC:H films with a significant improvement in mass density can be achieved for a given dielectric constant relative to a-SiC:H films deposited using traditional tetramethylsilane (4MS) precursors.[403] Using similar precursors, 100 nm a-SiC:H films with *k* values as low as 3.1 that show Cu diffusion barrier performance equivalent to higher $k = 5.0$ a-SiCN:H have also been demonstrated.[402,404] Matsuda has also shown that similar a-SiC:H films can exhibit increased fracture strength due to increased crack tip plasticity arising from the more ductile -$(CH_2)_x$- bonding.[406] The combination of such ductile films with traditional low-*k* a-SiOC:H ILDs was also found to significantly improve the interfacial toughness of the underlying ILD/DB interface.[407]

Despite these compelling results, it is important to note that for both the above mentioned Si-$(CH_2)_x$-Si network a-SiC:H and a-SiCN:H films the mass densities fall well below the critical mass density of 2.25 g/cm^3 previously determined for robustly prohibiting H_2O diffusion. This indicates that while these materials may impede Cu diffusion, they will likely not completely stop Cu and H_2O diffusion and may be unsuitable for certain applications, particularly when scaled from 100 nm (as tested) to thicknesses of <2 nm as forecasted by the ITRS.[107]

*Alternate low-*k *DB materials.*— Although further investigation of Si-$(CH_2)_x$-Si network a-SiC:H and other related films is merited, it is likely that further advancements will be needed to achieve robust dielectric barrier films with either reduced dielectric constant and/or that exhibit robust diffusion barrier performance at <2 nm thickness. The progress of research in low-*k* DB to date suggests that new materials outside the Si-C-N-O phase diagram will need to be identified and examined. In the following sections, we examine the factors that determine the *k* of a material and consider several different materials outside the Si-C-N-O composition space that offer the potential for continued DB *k* and thickness scaling.

Factors contributing to k and review of periodic table.—In order to rationally describe a search for new alternative low-*k* DB materials, it will be useful to first examine the factors that contribute to the dielectric constant of a material. The low frequency (0.1-1 MHz) dielectric constant of a material is determined by three different contributions arising from electronic, ionic, and configurational polarizabilities.[16,359] The electronic contribution arises from polarization created by the distortion of electron clouds surrounding the nuclei of the atoms that comprise the solid, while the ionic contribution arises from the polarization created by the motions of the atomic nuclei relative to one another. The configurational contribution appears when entities with permanent dipole moments align with the applied electric field. From the perspective of engineering new low-*k* dielectric materials, this means that one wants to use light elements with very few electrons and protons and that prefer to form covalent as opposed to ionic bonds. This effectively limits low-*k* dielectric materials to the top two rows of the periodic table (in contrast to those working on high-*k* dielectrics[408] where essentially the entire periodic table is available to select and choose from).

Starting at the top of the periodic table, one quickly realizes the limited composition space for obtaining new low-*k* materials. Specifically, the first two elements (hydrogen and helium) are both gases and not useful network formers (although hydrogen does play an important role as a network modifier in current low-*k* materials). Starting with the next row, one has lithium (Li) which is a poor network former and more commonly acts as a network modifier[409] similar to how hydrogen and terminal methyl groups are utilized in traditional low-*k* a-SiOC:H and a-SiCN:H dielectrics. In this regard, Li may be useful as an alloying agent to reduce the dielectric constant of high-*k* materials such as Al_2O_3.[410] However, the use of Li in this manner could be problematic due to the high diffusivity it exhibits in many dielectric materials which has made it attractive for solid state battery applications.[411,412] Next are beryllium (Be) and boron (B) based materials which will be discussed more in the following sections. Beyond B and Be, one quickly starts to return to the Si-C-O-N composition space.

Be network materials.—Beryllium is the fourth element in the periodic table and forms stable oxide, nitride, and carbide compounds.[413–415] ALD BeO has most recently garnered significant interest as a gate dielectric for Si[416] and III-V[417,418] transistor devices due to excellent passivation[419] and other electrical properties.[413] From a DB perspective, ALD BeO has also been recently demonstrated as an effective oxygen diffusion barrier for high-*k* gate dielectric formation on Si.[420] This is most likely due to the absence of p-orbitals for Be and similar electronegativity to O that results in the formation of short Be-O bonds and a dense covalent atomic structure.[421] Unfortunately, this dense atomic structure also results in BeO exhibiting a relatively high *k* with values of ∼6.8 being reported for ALD BeO thin films.[413] However, the dense atomic structure remains attractive for DB applications with thickness targets <2 nm. Additionally, BeO may be amenable to reductions in *k* via similar methods of H/CH_3 network modification as in current a-SiOC:H and a-SiCN:H low-*k* materials.

Relative to BeO, comparatively little is known regarding beryllium nitride (Be_3N_2) and carbide (Be_2C) with only a few reported theoretical and experimental investigations.[414,422] Early interest in beryllium nitride and carbide compounds was primarily for nuclear applications,[421,423] with a few recent investigations focused on Be_3N_2 and Be_2C compounds as super hard semiconducting materials.[422,424] For Be_3N_2, theoretical investigations of the electronic structure for Be_3N_2 do indicate a relatively dense atomic structure.[425] Experimental investigations of laser ablated and sputter deposited a-BeN thin films have reported relatively high optical dielectric constants ranging from ∼ 4 to 5.7 and wide band gaps of 3.8 – 4.2 eV.[414,426,427] For Be_2C, only a few basic theoretical and experimental investigations of the band structure have been reported.[422,428] This may be primarily due to the reported difficulty in synthesizing Be_2C,[429] and the propensity for Be_2C to hydrolyze in ambient conditions to $Be(OH)_2$.[422] The latter would clearly limit the utility of Be_2C as a moisture DB.

Another possible limitation for Be based DB materials is the high toxicity exhibited by Be.[430] In fabrication of Be ALD precursors, it has been clearly noted that beryllium compounds are highly toxic and should be carefully handled in fume hoods at all times.[431] Utilization of a Be compound as a DB, ES, or HM may require similar pre-cautions in downstream etch and metallization steps such as those utilized for handling III-V semiconductor compounds.[432]

B network materials.—B follows Be on the periodic table and also forms stable oxide, nitride, and carbide compounds.[433–435] Boron oxide (B_2O_3) may be a potential low-*k* dielectric, but it is difficult to obtain accurate *k* values for this material due to an extremely hygroscopic behavior.[434,436] For this reason, B_2O_3 is likely unsuitable for low-*k* interconnect applications. Boron nitride (BN) does not exhibit the same extreme hygroscopic behavior as B_2O_3 and has been investigated for numerous electronic applications as a gate dielectric,[437] ILD,[434] ES,[438] DB,[439] HM,[440] polish stop,[441] and UV photo-detector / light emitting diode.[442,443] PECVD a-BN:H films have been reported to have reasonably low *k* values of 4.0–5.7 and high mass densities of 1.7–1.9 g/cm^3 that make it of interest for potential low-*k* DB interconnect applications.[434,439] Related CVD a-BCN:H films have been reported to have slightly lower *k* values of 3.7–4.6 with similar mass densities.[444,445] These films have exhibited good adhesion strengths to Cu and low-*k* a-SiOC:H ILDs[445] and similar TDDB lifetimes to a-SiCN:H in Cu gated metal-insulator-semiconductor (MIS) capacitor devices.[446] From a DB perspective, CVD a-BCN:H films as thin as 4 nm have been demonstrated as porous ILD pore sealants,[447] and as a Ge passivation and surface oxidation diffusion barrier.[448] Even lower *k* values of 1.9–2.2 have been reported for some PECVD a-BCN:H films where the ability to impede Cu diffusion has also been demonstrated.[449,450] However while a-BN:H and a-BCN:H are less hygroscopic relative to B_2O_3, some reports of thin film delamination[451,452] and electrical instability[453] on exposure to ambient moisture have been reported for a-BN:H that could limit the utility of a-BN:H and a-BCN:H in low-*k*/metal interconnects.

Boron also forms several boron rich carbide and sub-oxide compounds.[454,455] At the atomic level, these materials are unique in that they are typically composed of interlinked B_{12} icosahedra with C or O either substituting for B in the icosahedra or forming intra-icosahedra linkages.[456,457] These compounds are structurally distinct from B_2O_3, BN, and BCN where B is incorporated in either trigonal/sp^2 or tetrahedral/sp^3 linkages with O, N and C.[458] Due to the strong covalent bonding forming the B_{12} icosahedra, B_4C and BO_x materials exhibit extremely high values of Young's modulus (>300 GPa) and hardness (>30 GPa) with relatively low values of dielectric constant ($\leq$5).[454,455,459] PECVD a-B_{4-5}C:H films have been reported with even lower optical dielectric constants (3-4),[460] and still compelling hardness and mass density values of $\sim$ 8 GPa[461] and 1.5–1.8 g/cm^3,[462] respectively. These values are extremely compelling for low-*k* DB applications, and further optimization of a-B_xC:H materials for low-*k* applications can be anticipated due to the ability of the B_{12} icosahedra to arrange themselves in many different distorted arrangements[463] similar to SiO_4 tetrahedra in SiO_2 and low-*k* a-SiOC:H materials.[14,15]

C network materials – DLC, a-C:H, and SAMS.—Although carbon is incorporated in many current low-*k* dielectric materials, few investigations of pure carbon materials for DB (or ES) applications have been reported. Diamond and diamond like carbon (DLC) films have a high mass density (3–3.5 g/cm^3)[464] and many excellent physical properties[465] with a relatively low dielectric constant of $\sim$ 5.7,[466] but are formed mostly under relatively extreme conditions unsuitable for metal interconnect fabrication.[465,467] Amorphous hydrogenated carbon (a-C:H) thin films can be deposited under less extreme conditions that are more suitable for interconnect fabrication, but exhibit greatly reduced properties in addition to dielectric constant.[468,469] To date, most a-C:H materials investigated for metal interconnect applications have been targeted primarily for low-*k* ILD or planarization applications.[470–472] However in one case, the Cu diffusion resistance of a k = 2.7 PECVD a-C:H film was investigated and no Cu diffusion was observed after annealing at 450C for 1 hr.[470] This limited result suggests that more research into a-C:H films as a potential DB is merited.

An additional challenge to the use of DLC and a-C:H films for low-*k* ILD, DB, and ES applications is the typically low resistivities reported.[465,467] In many cases, the low resistivity has been attributed to the formation of conductive sp^2 carbon clusters in the sp^3 DLC or a-C:H matrix.[464] Takabayashi has recently shown that by careful attention to the deposition parameters, sp^2 carbon cluster formation can be minimized and DLC/a-C:H films with low-*k* (<2.5) and high breakdown strength ($\sim$8 MV/cm) can be achieved.[473]

Another form of carbon more thoroughly investigated from a Cu and H_2O/O_2 diffusion barrier perspective is self-assembled monolayers (SAMS). SAMS are molecular assemblies of organic (typically linear) molecules that spontaneously adsorb and self-assemble on surfaces into ordered thin film domains.[474] Early investigations of SAMS have demonstrated them as effective Cu corrosion inhibitors in wire bonding[475] and other applications.[476] More recently, SAMS have been demonstrated as Cu diffusion barriers,[477–479] low-*k* ILD pore sealants,[480] Cu surface passivation layers,[481] and Cu/ILD adhesion promoters.[482,483] Due these successes and thicknesses <2–3 nm, SAMS are extremely attractive for meeting the ITRS forecast for <2 nm DBs. However in head-to-head comparisons with state-of-the-art TaN/Ta Cu diffusion barriers, SAMS have exhibited order of magnitude lower lifetimes in Cu-MIS TDDB testing indicating that SAMS may not be able to completely meet low-*k*/Cu interconnect reliability requirements.[477] In this regard, two challenges / areas of research needed for the use of SAMS in low-*k* metal interconnect applications are (1) the ability to withstand ion bombardment and thermal stresses from various downstream plasma processes,[484,485] and (2) diffusion barrier performance in the presense of inevitable surface defects and topography.

Mg and Al network materials.—Skipping over N and O (which are in the Si-O-C-N composition) and F (which is a network modifier for SiO_2 and Si_3N_4 similar to H),[16,486] the next network formers in the periodic table are Mg and Al. Both form stable oxide, nitride, and carbide compounds but generally have relatively high dielectrics constants of > 7.[408,487] In fact, MgO and Al_2O_3 have been extensively investigated as high-*k* gate dielectrics and capacitive elements for a variety of different devices.[488,489] However from a diffusion barrier perspective, the relatively high-*k* of these materials could be accommodated if they allow more aggressive thickness scaling relative to current DB materials in the Si-O-C-N system. In this regard, Majumder has recently evaluated the Cu diffusion barrier performance of 3 nm thick Al_2O_3 and even higher *k* HfO_2 ALD films.[490] X-ray diffraction measurements of Cu-MIS structures annealed at various temperatures showed these films to prevent Cu diffusion up to temperatures as high as 650°C.[490] These encouraging results indicate that an aggressively scaled high-*k* material could in some cases serve as a metal interconnect DB with minimal capacitance penalty. With respect to the ITRS goal of <2 nm DB, these results are also encouraging and should justify additional studies of high-*k* dielectrics as DBs at <2 nm thickness targets.

2D materials.—Although not compositionally unique relative to the prior materials reviewed, one new class of materials garnering significant interest as nanometer scale DBs are two dimensional (2D) materials such as graphene and boronitrene. Graphene has been demonstrated as an impermeable membrane for He[491] and both materials have been demonstrated as H_2O/O_2 barriers for preventing oxidation of polymers and metals such as Cu and Ni.[492,493] Recently graphene (G) has also been demonstrated as a Cu diffusion barrier in Cu-G-Si structures annealed at temperatures up to 750°C.[494] Given the atomic thick dimensions of graphene and boronitrene, these materials have great potential to meet the ITRS forecasted goal of a <1-2 nm DB. However as with SAMS and other materials, the performance of 2D materials will be greatly challenged by the presence of defects, topography, and material heterogeneities that exist on the surfaces of metal interconnect structures. Studies by Wlasny[495] and Schiver[496] have already shown that while at the macro scale graphene can prevent corrosion of Cu, defects and imperfections in the graphene can allow corrosion at the nano-scale that would not be acceptable in state-of-the-art metal interconnects.

*Alternate low-*k *ES materials.*— Due to continued delays in EUV lithography,[497] semiconductor manufacturers have been forced to implement various forms of pitch division patterning schemes.[498,499] In some cases, 4X multiple patterning schemes are being considered for <22 nm technology nodes.[500] To reduce some of the complexity of such pitch division / multiple pass patterning schemes, new ES / HM materials and deposition processes are being sought that either provide high or contrasting etch selectivities relative to other materials,[501] or can be selectively deposited / grown on pre-existing patterned structures.[502–504] The latter is beyond the scope of this article. However for the former, we biefly review below some of the ES/HM challenges associated with multiple patterning schemes and one material system that could be useful in this regard.

Four color problem.—In a typical pitch quatering patterning approach, multiple hardmask, backbone (BB), and spacer (SP) materials are utilized in conjuction with other photoresist and anti-reflection coating materials.[501] Such schemes require that all the materials involved have discrete and unique etch selectivities with respect to one another. Understanding all the associated etch selectivity requirements in such schemes is complex. However, some insight into how to parse and reduce the complexity of the pitch division etch selectivity requirements can be gained from map theory and the four color theorem of topology.[505]

The four color theorem elegantly states that only four colors are needed to color a two dimensional topological map such that no two regions (i.e. "countries") with a common border will have the same color.[506] Based on this theorem, one could anticipate that the etch selectivity requirements of any pitch division metal interconnect patterning scheme could be easily solvable with the availability of just four materials (i.e. BB, SP, ILD, and HM/ES) that exhibit distinct etch properties relative to one another, i.e. "colors." However, the challenges of finding this unique set of materials are two fold. First, the requirement of four materials with distinct etch properties implies the availability of 4 distinct etches to pattern and clear these materials and increases the complexity by at least a factor of two. The second challenge is that compositionally all of the BB, SP, ILD, HM, and ES materials typically utilized in metal interconnect fabrication schemes generally fall within the Si-O-C-N-H phase diagram. While Si, C, SiC, SiO_2, and Si_3N_4 as distinct thermodynamic chemical compounds could easily provide the four needed colors, the previously reviewed requirements on k and other material properties quickly forces one into a blurred window of a-SiO_xC_y:H, a-SiC_yN_z:H, and a-SiO_xN_z:H materials for the SP, ILD, and HM/ES layers. Using such compositionally similar materials further aggravates the challenge of finding four unique and selective etch chemistries.

The recent use of metal or semi-metallic materials (i.e. TiN)[507,508] as a hard mask in DD patterning schemes has added an additional color to address the pitch division four color problem. However, new (preferably low-k) dielectric materials outside of the Si-O-C-N phase are desired to help provide additional color and process latitude for pitch division schemes. In the previous section, we reviewed several potential low-k DB materials that fall outside the Si-O-C-N composition space. These materials could also prove useful as new ES, HM, or SP colors in pitch division patterning schemes. However in many cases, the etch behavior of these alternative materials in dry plasma etch processes utilized for interconnect fabrication has not been well characterized. Therefore in the following section, we focus only on aluminum based materials where a high resistance to various fluorinated plasma etches has been previously established in the literature.[509]

High-k Al_2O_3 and low-k AlOC:H.—In a previous section, we reviewed the use of Al_2O_3 as a potential high-k DB material.[490] From an ES perspective, Al_2O_3 and other Al containing compounds are attractive due to a demonstrated high resistance to fluorinated plasma etch chemistries.[509] The high resistance to etching by fluorine plasmas is largely due to the low volatility of the predominate AlF_3 etch products formed.[510] This extreme etch resistance can in turn allow the relatively high k of Al_2O_3 and other Al compounds to be mitigated as an ES by minimizing the thickness utilized as previously mentioned for DB applications. However for advanced single digit nanometer technology nodes, extreme thickness scaling may not be sufficient to mitigate the relatively high k of Al_2O_3. In this case, Al containing compounds with reduced values of k would be attractive.

In this regard, two approaches for reducing the dielectric constant of Al_2O_3 have been demonstrated in the literature. The first involves alloying relatively high-k Al_2O_3 with a lower k material such as SiO_2. Lim[511] and others[512,513] have shown that near continuous Al_2O_3-SiO_2 alloys and nano-laminates can be prepared by ALD and PEALD methods that span the full composition and dielectric permittivity window of these materials. Another approach similar to traditional low-k a-SiOC:H ILD materials is to form inorganic-organic hybrid AlOC:H films by ALD via substituting oxidizing sources such as H_2O, O_2, and O_3 with various organic acids or alcohols.[514–518] Although the low frequency dielectric constant and other important electrical properties for these hybrid materials have yet to be reported in the literature, prior studies have shown that these materials exhibit reduced mass densities,[514,515] refractive indexes,[517] and Young's modulus[518] implying that reduced values of k are likely. However, the reductions in mass density and Young's modulus also suggest that these materials may exhibit reduced diffusion barrier and etch resistance. This should be a subject of future research for these materials in addition to fully characterizing their electrical, mechanical, and thermal properties.

Conclusions and Final Remarks

In summary, we have reviewed the material property and intregrated functionality requirements for DB, CCL, and ES materials in low-k/metal interconnect structures, and illustrated the limitations that these requirements place on both k and thickness scaling for these layers. We have also reviewed the current state-of-the-art DB/CCL/ES materials with respect to the 2013 ITRS goals of <2 nm thick DB materials with k values of <3.0. These goals will be extremely challenging to meet using traditional deposition methods and materials with-in the Si-O-C-N phase diagram. In response, we have lastly reviewed several alternative low-k and low dimension materials that offer promise for meeting these goals and allowing continued interconnect dimensional scaling.

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