Effect of Low-K dielectric material on 63nm MLC (Multi-Level Cell) NAND Flash Cell Arrays

Mincheol Park, Jung-Dal Choi, Sung-Hoi Hur, Jong-Ho Park, Joon-Hee Lee, Jin-Taek Park, Jong-Sun Sel, Jong-Won Kim, Sang-Bin Song, Jung-Young Lee, Ji-Hwon Lee, Suk-Joon Son, Yong-Seok Kim, Soo-Jin Chai, Kyeong-Tae Kim and Kinam Kim
Semiconductor R & D Center, Samsung Electronics Co., LTD.
San#24, Nongseo-Ri, Giheung-Eup, Yongin-City, Gyunggi-Do, 449-711, Korea
Tel.:82-31-209-2587, Fax:82-31-209-3274, e-mail:mcpark.park@samsung.com

ABSTRACT

We investigate the effect of applying oxide spacer into MLC NAND flash memory with 63nm design rule. The oxide spacer is effective on reducing cell to cell coupling with its low-k dielectric constant. The uniform cell V_{th} distribution of 0.6V fulfilling the MLC operation is obtained while maintaining fast programming speed and sufficient cell current.

INTRODUCTION

NAND flash memory has given a promise of high-density cell integration, which is suitable for mass storage devices. As a result, the cell integration density of the NAND flash memory is increasing very rapidly [1] and is further enhanced by a factor of two by adopting MLC operation. In this paper, we present our study on MLC NAND flash memory with 63nm cell technology. Cell to cell coupling is minimized by applying the oxide spacer and optimizing the cell structure. The uniform cell V_{th} distribution of 0.6V fulfilling the MLC operation of the 63nm cell array is obtained without loss of programming speed and cell current.

KEY TECHNOLOGIES AND DEVICE CHARACTERISTICS

Fig.1 shows the schematic of MLC NAND flash memory cell arrays of 63nm design rule. There are 32 cells and 2 select transistors that are connected in series between bit-line contact and common source line.

The interference between neighboring cells due to floating gate coupling is one of the most important factors in MLC operation [3]. For MLC operation, the V_{th} shift by cell-to-cell coupling should be kept below 0.2V to maintain the distribution of the programmed cell state within 0.8V. Fig.2 shows a simulation result of V_{th} shift (ΔV_{th}) corresponding to floating gate height and spacer material, which affect the cell coupling significantly. Silicon oxide is more favorable than silicon nitride spacer in the respect of WL-WL cell coupling and BL-BL cell coupling. Fig. 3 shows the cross-sectional TEM image of cell transistors. Oxide spacer is incorporated into 63nm cell transistors while 90nm cell transistors use silicon nitride spacer. The simulation and measurement results of WL-WL cell coupling of both cell transistors are shown in Fig. 4. In case of 90nm cell transistor, the cell coupling increases abruptly as the gate to gate space is decreased below 40nm. However, by incorporating oxide spacer, the cell coupling of 63nm cell transistor is remained around 0.03 at the gate space of 30nm, which is equivalent to 0.15V V_{th} shift when the adjacent cell undergoes 5V V_{th} shift. It is seen that the measuring data of both cell transistors remain less than 0.01. This result confirms that oxide spacer is able to reduce the cell to cell coupling effectively, and adopting low-k dielectric material as a spacer facilitates the cell size reduction of NAND-type flash memory.

Fig.5 demonstrates the programming characteristics of the 63nm and 90nm cell transistors. Since both cells have the same coupling ratio with the floating gate height of 45nm and the tunnel oxide thickness of 61A, the programming speed of 63 nm cell is similar with the speed of 90nm cell. It is estimated that 3V programmed cell V_{th} can be achieved by applying 18V program voltage with 200μs pulse duration.

Fig.6 shows a comparison of fresh cell currents for single level cell (SLC) operation and multi level cell (MLC) operation. The 63nm cell current in worst condition is about 500nA for 1.0V bit-line voltage. Since the channel doping is focused on suppressing the leakage current which is severe in smaller cell, the on cell current of 63nm cell is quite small when compared to the 90nm cell current of 800nA. In MLC operation, both cells have the same current of 120nA for 1.0V bit-line voltage. Cell V_{th} adjustment for MLC operation makes the on cell currents be same.

V_{th} distributions of 63nm and 90nm cell arrays in MLC condition are shown in Fig.7. It is seen that, in spite of gate to gate space reduction, 63nm cell arrays possess narrower V_{th} distribution width. And, the uniform V_{th} distribution of three different program states of 63nm cell arrays indicates the negligible influence of cell to cell coupling. We conclude that this enhancement is mainly due to adopting oxide spacer.

CONCLUSION

The effect of applying oxide spacer into MLC NAND flash memory with 63nm design rule is investigated. By incorporating oxide spacer, we obtain less than 0.2V V_{th} shift by cell to cell coupling that leads to a uniform 0.6V V_{th} distribution of cell arrays. Cell current of 120nA and programming speed of 18V are obtained satisfying the MLC operation of 63nm cell array.

REFERENCES

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[3] J. D . Lee, et. al., "Effects of floating-gate interference on NAND flash memory cell operation," IEEE EDL., Vol. 23, No. 5, pp. 264-266, 2002.

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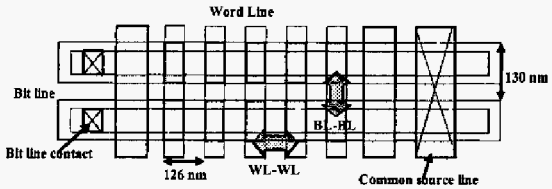


Fig.1. Schematic diagram of the cell layout and its dimension of the 63nm cell arrays. WL-WL and BL-BL directions are indicated.

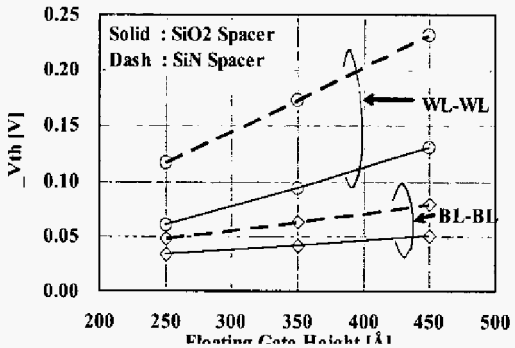
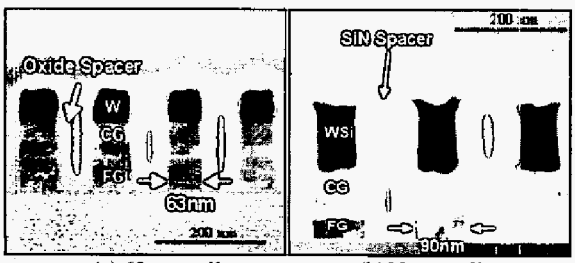


Fig.2. Simulation results of floating gate height dependency on cell-to cell coupling. ΔV_{th} is calculated in case of 10V V_{th} change of the adjacent cell



(a) 63 nm cell (b)90 nm cell

Fig.3. Cross-sectional TEM of the NAND string

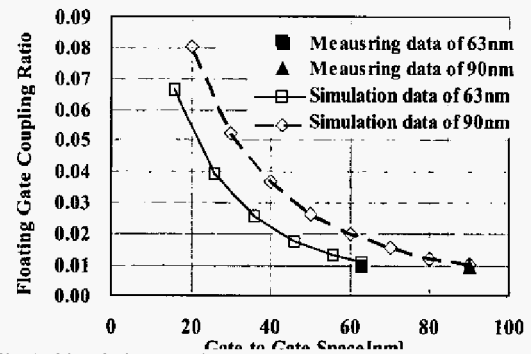


Fig.4. Simulation results of WL-WL cell coupling ratio as a function of gate-to-gate space dimensions for 63nm and 90nm cells. Both cells have same floating gate height of 45nm.

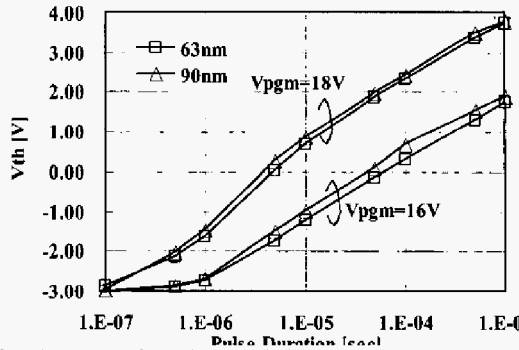


Fig.5 Programming Characteristics of 63nm and 90nm cells. The program voltage is estimated about 18V with 200μs programming at 3V threshold voltage.

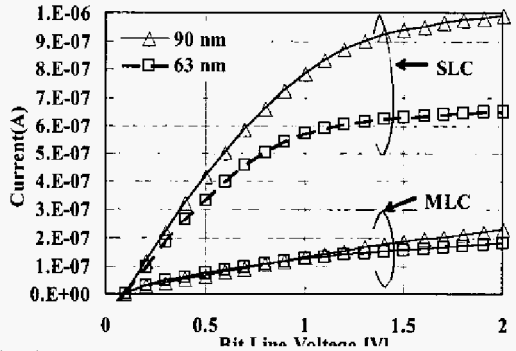


Fig. 6. "On" cell current characteristics at the temperature of 80°C. 63nm and 90nm cell in MLC condition have same current of 120nA while the cell current of 63nm cell in SLC condition is 200nA smaller than the current of 90nm cell.

	SLC	MLC
Selected Cell Vth	-2.0V	+0.9V
Selected Cell V_{WL}	0.0V	+1.1V
Unselected Cells Vth	+2.0V	+3.0V
Unselected Cells V_{WL}	+5.0V	+5.5V
Source Voltage	+0.1V	+0.1V

Table.1. Bias conditions for "On" cell current in Fig.6

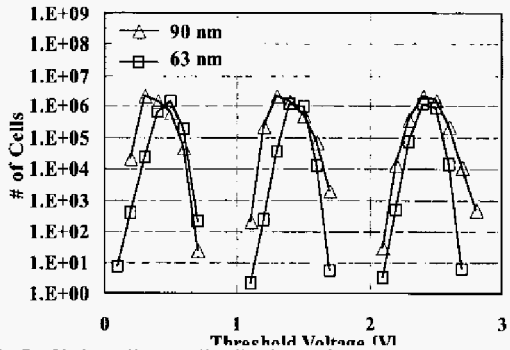


Fig.7. 8Mb cell V_{th} distribution of 63nm and 90nm cell arrays in MLC condition.