UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED.

Patent Owner.

Case No. IPR2025-01527

U.S. Patent No. 9,117,909 B2

PATENT OWNER'S PRELIMINARY RESPONSE PURSUANT TO 37 C.F.R. § 42.107(a)

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph C. McAlexander III
2002	Peter Van Zant, *Microchip Fabrication, A Practical Guide to Semiconductor Processing*, (4th ed. 2000)
2003	*Curriculum Vitae* of Joseph C. McAlexander III
2004	Collins Dictionary, https://www.collinsdictionary.com/us/dictionary/english/encompass
2005	Merriam-Webster, https://www.merriam-webster.com/dictionary/trench
2101	Website: Foundries to Grow Faster than Integrated Circuits in 2016 (https://marketrealist.com/2015/12/foundries-grow-faster-integrated-circuits-2016/)
2102	Website: Ranked: Seminconductor Foundries by Revenue Share (www.visualcapitalist.com/ranked-semiconductor-foundries-by-revenue-share/)
2103	Website: US Patent No. 9,117,909 B2 – Non-planar transistor – Google Patents https://patents.google.com/patent/US9117909B2/en?oq=9%2c117%2c909+
2104	Declaration of Paul Ahern Regarding Patent Owner's Request for Discretionary Denial of Institution

I. INTRODUCTION

The Petition should be denied because each of the four asserted grounds fails to disclose multiple limitations of the challenged claims of U.S. Patent Number 9,117,909 ("the '909 patent").

Grounds 1 and 2 (Lin and Liaw)

Grounds 1 and 2 fail to disclose or render obvious at least claim elements [1.a], [1.b], and [1.c]. First, Lin's alleged "isolation region" is between two alleged "active regions" rather than "encompass[ing] the active region," as recited in element [1.a]. Second, Lin's "active region" only includes a single trench, rather than having "a plurality of shallow trenches disposed… in the active region," as recited in element [1.b]. Third, Lin fails to disclose a "protruding structure" having "an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall" as recited in element [1.b]. Fourth, Lin's alleged "deep trench" does not have "a shoulder portion," as recited in element [1.c]. And Liaw does not remedy any of the deficiencies of Lin with respect to any of these claim elements.

Grounds 3 and 4 (Chang)

Grounds 3 and 4 fail to disclose or render obvious at least claim element [1.c]. Chang's alleged "shoulder portion" is in fact just the outer sidewall of the protruding structure. As such, it cannot constitute the claimed "shoulder portion" of the "deep trench," as required by element [1.c].

Accordingly, the Board should deny institution of the Petition.

II. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors. Ex. 2001, ¶17.

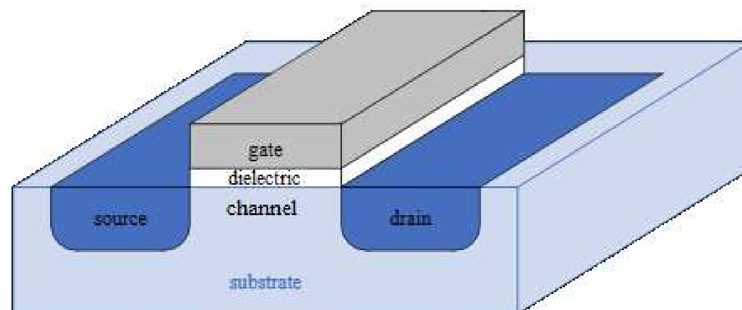
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2; Ex. 2001, ¶18. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3; Ex. 2001, ¶18.

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Ex. 2001, ¶19. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34; Ex. 2001, ¶19. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex.

2002 at 29; Ex. 2001, ¶19. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30; Ex. 2001, ¶19. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34; Ex. 2001, ¶19.

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. Ex. 2001, ¶20. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See*, *e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



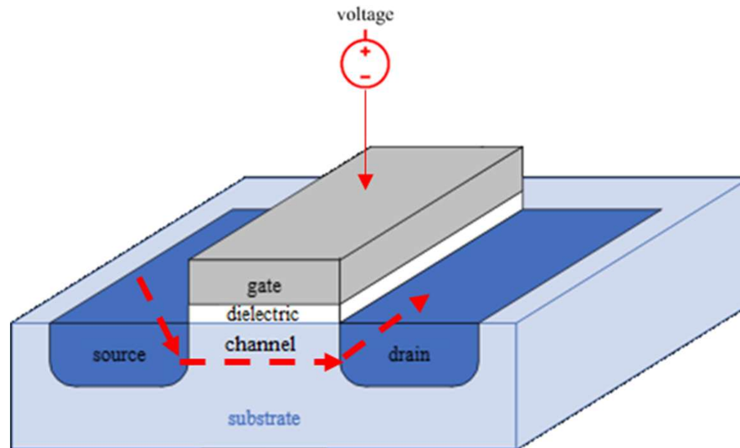
See, *e.g.*, Ex. 2002 at 510-511; Ex. 2001, ¶20.

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28; Ex. 2001, ¶21. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the

source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511; Ex. 2001, ¶21.

The gate is a conductor (or semiconductor) located above the channel. Ex. 2001, ¶ 22. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511; Ex. 2001, ¶22. When a voltage is applied to the gate, the dielectric prevents the "flow of charge" (current) between the gate and the channel, but the applied voltage results in the creation of a "field effect" in the channel. Ex. 2002 at 510-511; Ex. 2001, ¶22. This "field effect" either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511; Ex. 2001, ¶22.

As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Ex. 2001, ¶23. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current. Ex. 2001, ¶23.

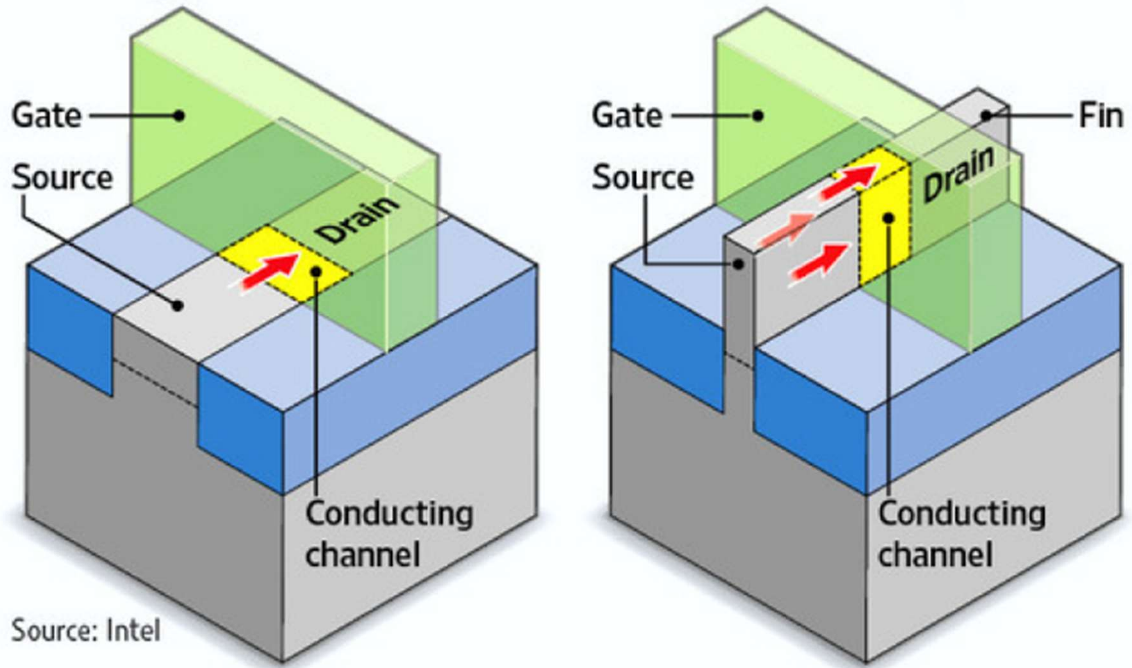


B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. Ex. 2001, ¶ 24. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. *Id*. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. *Id*. This desire led to the development of a new type of transistor, a "FinFET." Ex. 2001, ¶24.

The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a "planar" FET. Ex. 2001, ¶25. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. Ex. 2001, ¶25

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. Ex. 2001, ¶26. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



Ex. 2001, ¶26.

In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. Ex. 2001, ¶27. In the resulting fin field effect transistor ("FinFET"), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides. *Id*.

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. Ex. 2001, ¶28. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. *Id*. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. *Id*. This, too, increases the number of FinFET transistors that may fit onto a single chip. *Id*.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. Ex. 2001, ¶29.

In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13; Ex. 2001, ¶30.

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into

thin disks called "wafers." Ex. 2002 at 13-14; Ex. 2001, ¶35. A wafer acts as a semiconductor substrate on and in which transistors may be formed. Ex. 2001, ¶31.

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14; Ex. 2001, ¶32. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14; Ex. 2001, ¶32.

In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15; Ex. 2001, ¶33.

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. Ex. 2002 at 14; Ex. 2001, ¶34. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* Ex. 2002 at 29-31, 71; Ex. 2001, ¶34. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. Ex. 2001, ¶34.

Layering is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72; Ex. 2001, ¶35. The layers may be conductors,

semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72; Ex. 2001, ¶35.

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Ex. 2001, ¶36. Another way of adding a layer of material is to grow the material on the semiconductor substrate. *Id*. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. *Id*. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72; Ex. 2001, ¶36.

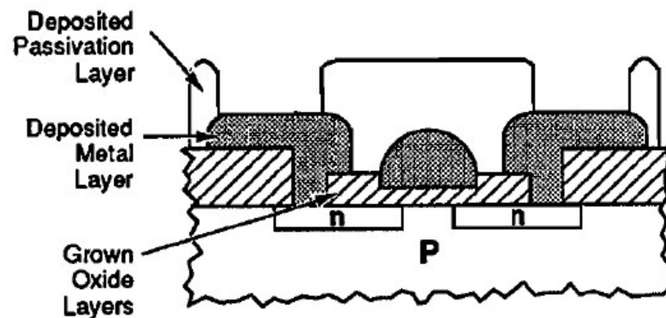


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

<u>**Patterning**</u> is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73; Ex. 2001, ¶37. This creates a pattern on the wafer surface. Ex. 2002 at 72-73; Ex. 2001, ¶37.

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73; Ex. 2001, ¶38. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

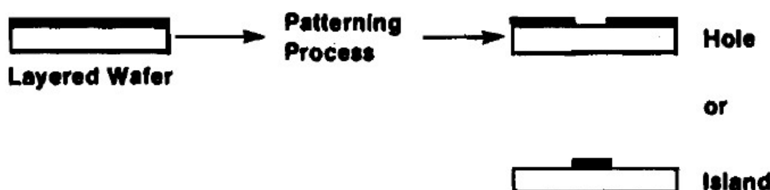


Figure 4.7 Patterning.

Ex. 2001, ¶38.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

> These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

Ex. 2002 at 73; Ex. 2001, ¶39.

III. THE CHALLENGED ’909 PATENT

The ’909 patent “is related to a method of forming a fin structure of a non-planar transistor, and more particularly, to a method of forming at least a fin structure

having nearly identical critical dimension (CD)." Ex. 1001, 1:13-16. To this end, the '909 patent provides a specific non-planar transistor:

> The non-planar transistor comprises a substrate, a plurality of second trenches, a sixth trench, an insulation layer, a conductive layer and a gate dielectric layer. The substrate has an active region and an isolation region, wherein the isolation region encompasses the active region. The second trenches are disposed in the substrate in active region, wherein a portion of the substrate between each two second trenches is defined as a second fin structure. The sixth trench is disposed in the substrate in the isolation region, wherein the sixth trench is deeper than the second trench. An insulation layer is disposed in the second trench and the sixth trench, wherein the insulation layer in the second trench is level with that in the sixth trench. A portion of the second fin structure that protrudes over the insulation layer is defined as a fin structure. The conductive layer is disposed on the fin structure. The gate dielectric layer is disposed between the fin structure and the conductive layer.

Ex. 1001, 1:61-2:10. Figure 13 illustrates the above-described non-planar transistor:

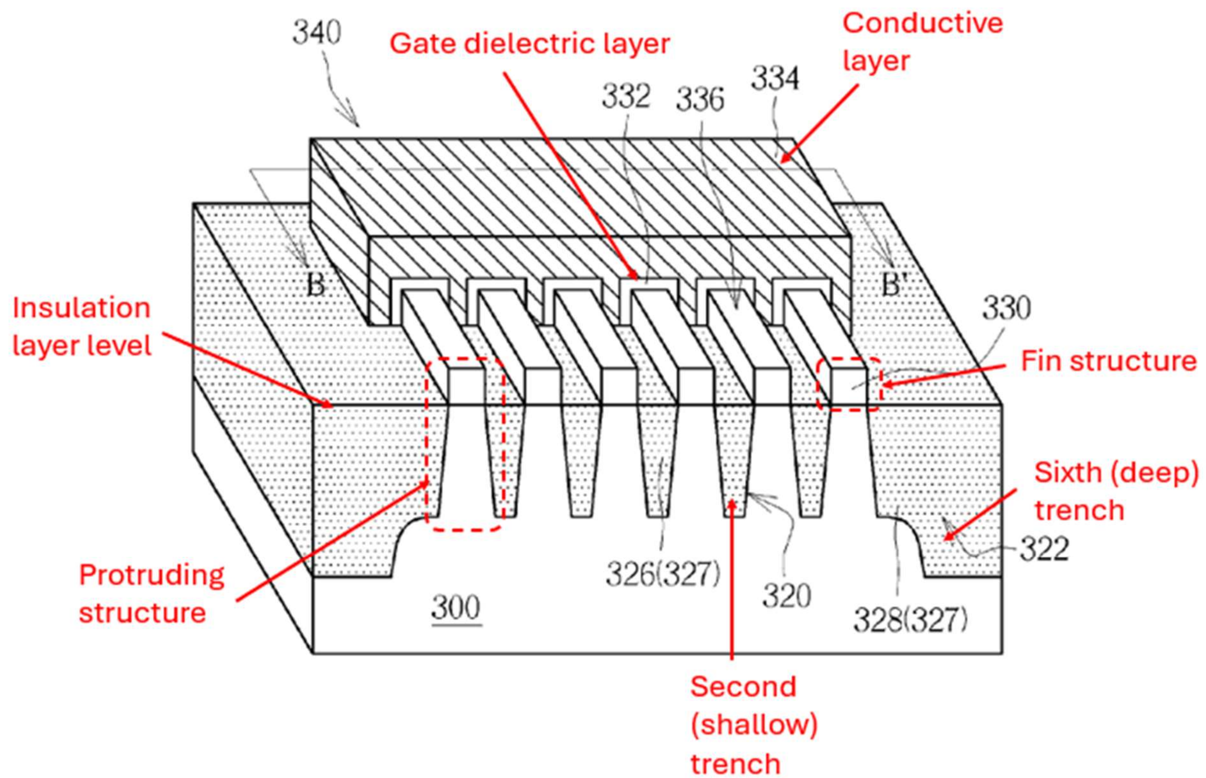


FIG. 13

Ex. 1001, Fig. 13 (annotated). The ’909 patent uses lexicography to define “fin structure” as “only refer[ring] to the upper portion of the second protruding structures 324 which has vertical sidewalls.” Specifically, “because the second protruding structures in conventional arts are formed by one single etching process, the second protruding structure in conventional arts is easy to have tapered sidewalls, especially those at the edge of the second protruding structures. Accordingly, the present invention uses two separated etching steps to form the second protruding structures 324. ***Since the fin structure 330 only refers to the upper portion of the***

second protruding structures 324 which has vertical sidewalls, the CD of the fin structure 330 can be on target and meet the desired value." *Id*., 4:46-55.

The above-described innovative aspects of the invention are embodied in all challenged claims via independent claim 1, which recites:

1. A non-planar transistor, comprising:

[1.a] a substrate having an active region and an isolation region, ***wherein the isolation region encompasses the active region***;

[1.b] ***a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall***;

[1.c] ***a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion;***

[1.d] an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench;

[1.e] a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure;

[1.f] a conductive layer disposed on the fin structure; and

[1.g] a gate dielectric layer disposed between the fin structure and the conductive layer.

Ex. 1001, claim 1 (annotated to identify claim elements).

IV. THE PETITION FAILS TO ESTABLISH THE REQUIRED LIKELIHOOD OF SUCCESS

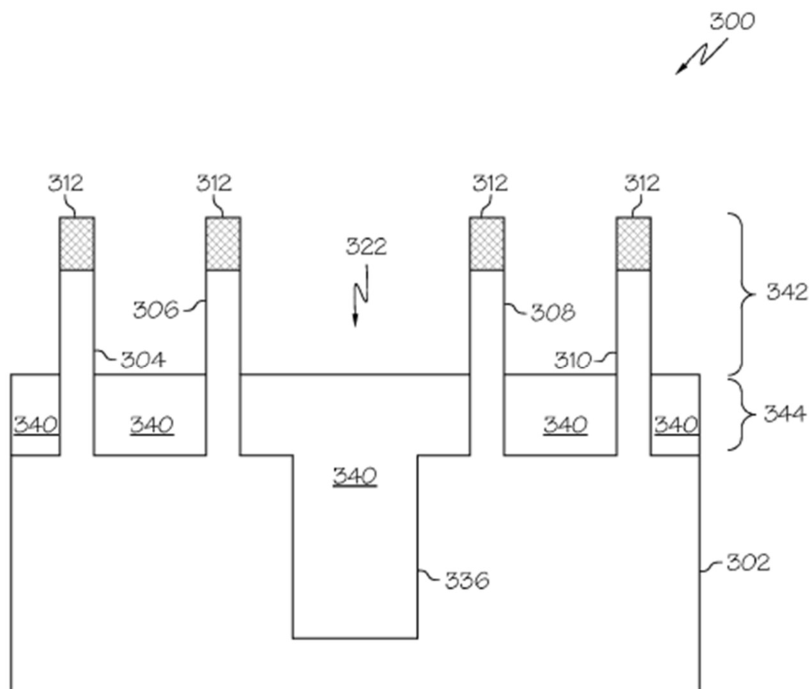
A. Grounds 1 and 2

In Ground 1, the Petition alleges the combination of Lin (Ex. 1004) and Liaw (Ex. 1003) renders obvious claims 1-4 and 6. Pet., 16. In Ground 2, the Petition alleges the combination of Lin, Liaw, and Chang (Ex. 1006) renders obvious claim 5, which depends from claim 1. Pet., 47. Both of these grounds fail because the Lin-Liaw combination does not disclose or render obvious elements [1.a], [1.b], [1.c], and [1.e]. Additionally, the Petition fails to set forth an adequate motivation to combine Lin and Liaw.

1. Ground 1 Fails To Disclose Or Render Obvious "Wherein The Isolation Region Encompasses The Active Region" (Element [1.a])

The Petition alleges that "[a]s illustrated in Figure 10 [], Lin discloses an isolation region (gap 322) comprising an isolation trench 336 formed in bulk silicon substrate 302." Pet., 26. Thus, the Petition alleges that Lin's "gap 322" constitutes an "isolation region." However, even if this is true, Lin's "gap 322" does not "encompass[] the active region" as required by element [1.a]. See Ex. 2004 ("[t]o encompass a place means to completely surround or cover it"). As shown below in

Lin's Figure 10, Lin's "gap 322" is ***between*** two active regions (regions with fins), rather than encompassing the active region, as required by the challenged claims.



Ex. 1004, Fig. 10; *see also id.* at 3:46-47 (describing "isolation regions between adjacent FinFET devices formed on a bulk semiconductor substrate").

In contrast, in the '909 patent, "the second region 402 is disposed between the first region 400… so that the second region 402 encompasses the first region 400." Ex. 1001, 2:43-45. In the above quote, the "second region 402" is the isolation region and the "first region 400" is the active region. *Id.*, 6:2-4 ("An active region such as the first region 400 and an isolation region such as the [second] region 402 are defined on the substrate 300."); Ex. 2001, ¶44. As shown in the '909 patent's

Figure 1, and as recited in claim 1, the isolation region 402 encompasses (or surrounds) the active region 400:

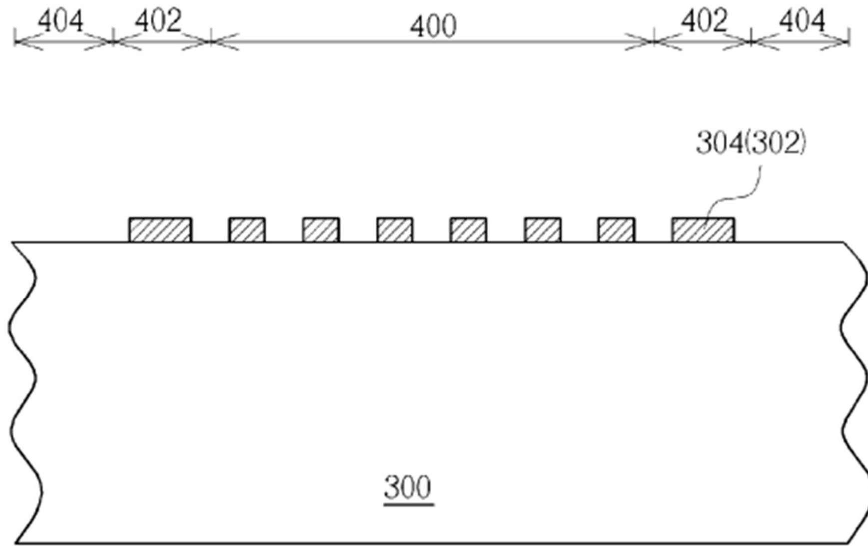


FIG. 1

Ex. 1001, Fig. 1; Ex. 2001, ¶44.

Recognizing this defect in Lin, the Petition argues, without support, that in Lin's Figure 10, there are additional alleged isolation regions on either side of the active regions:

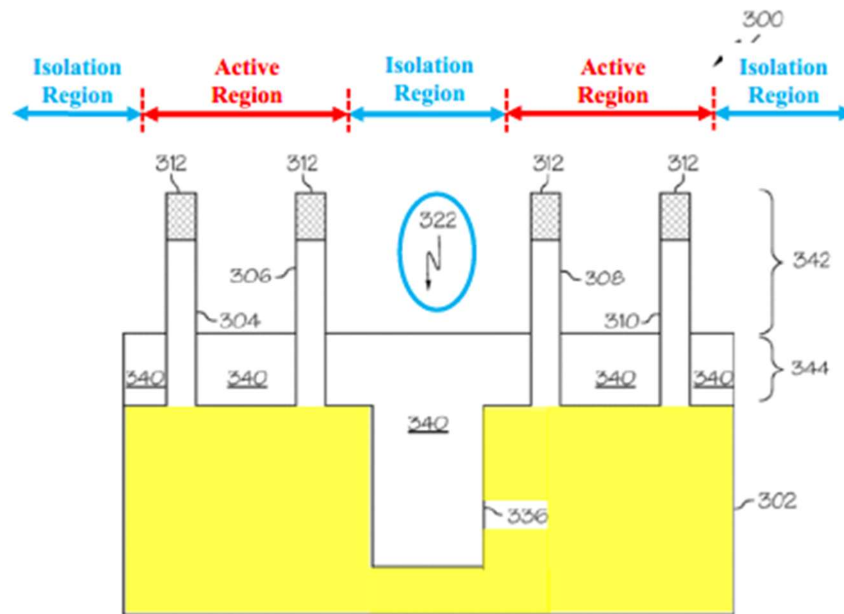


FIG. 10

Pet., 25 (annotated Ex. 1004, Fig. 10). This is pure speculation, and in fact, contradicts the Petition's own argument that Lin's "gap 322" is an isolation region because it includes an "isolation trench 336." Lin's device does not include isolation trenches on the outside of the active regions, only in between them, as clearly shown in Figure 10 and as described in Lin's specification. Ex. 2001, ¶45.

The Petition also alleges that Liaw discloses this limitation because it discloses that "trenches 210 may be continuous and surrounding the semiconductor fin 212." Pet., 27 (citing Ex. 1005, 3:50-52). However, this disclosure in Liaw refers to trenches surrounding a single fin 212, which corresponds to the '909 patent's shallow trenches disposed in the active region and surrounding each individual protruding structure, rather than the '909 patent's deep trench disposed in the

isolation region. Ex. 2001, ¶46. Thus, Liaw similarly fails to disclose or render obvious "wherein the isolation region encompasses the active region," as recited in element [1.a].

Accordingly, neither Lin nor Liaw disclose or render obvious element [1.a], either alone or in combination.

2. Ground 1 Fails To Disclose Or Render Obvious "A Plurality Of Shallow Trenches Disposed In The Substrate In The Active Region, Wherein A Portion Of The Substrate Between Each Two Shallow Trenches Is Defined As A Protruding Structure" (Element [1.b])

The Petition alleges that Lin's Figure 10 discloses or renders obvious "a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure." Pet., 28-30. The Petition includes the following annotated Lin Figure 10 identifying multiple alleged "shallow trenches" on each alleged "active region":

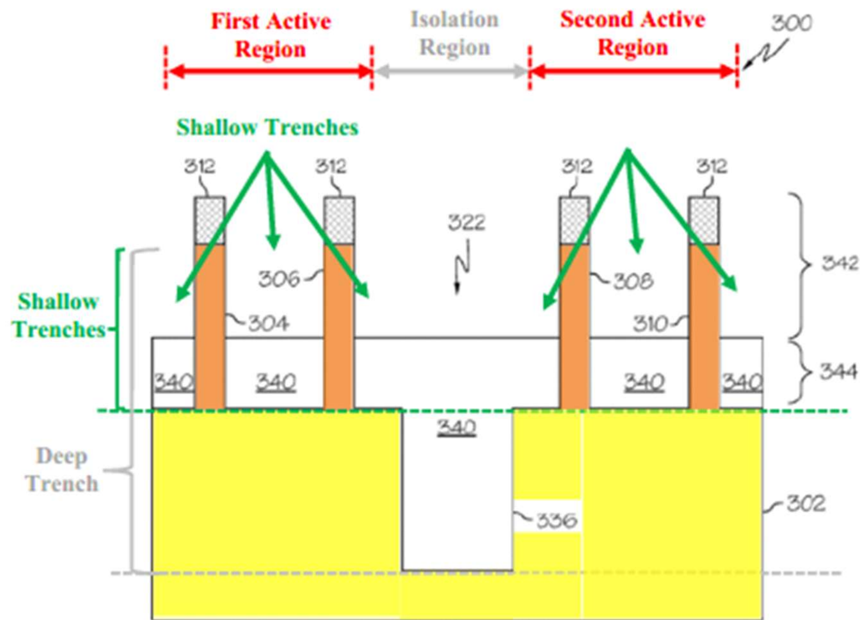


FIG. 10

Pet., 29 (showing annotated Ex. 1004, Fig. 10). But the Petition's annotations are misleading—the Petition labels the "active region" as including space to the left of the left protrusion and to the right of the right protrusion and identifies these spaces as "shallow trenches." The areas outside of the protrusions that the Petition points to as "shallow trenches" are not "trenches" because a trench inherently has two sides, rather than one:

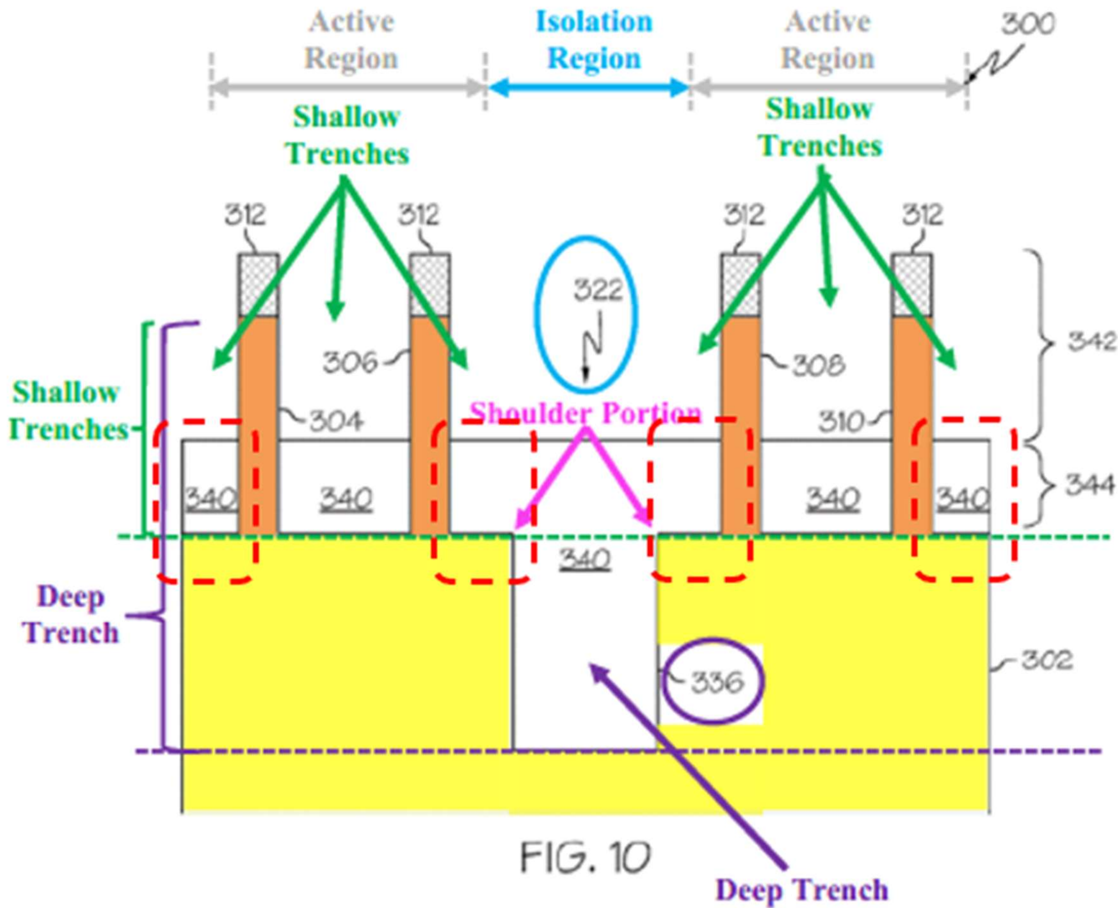
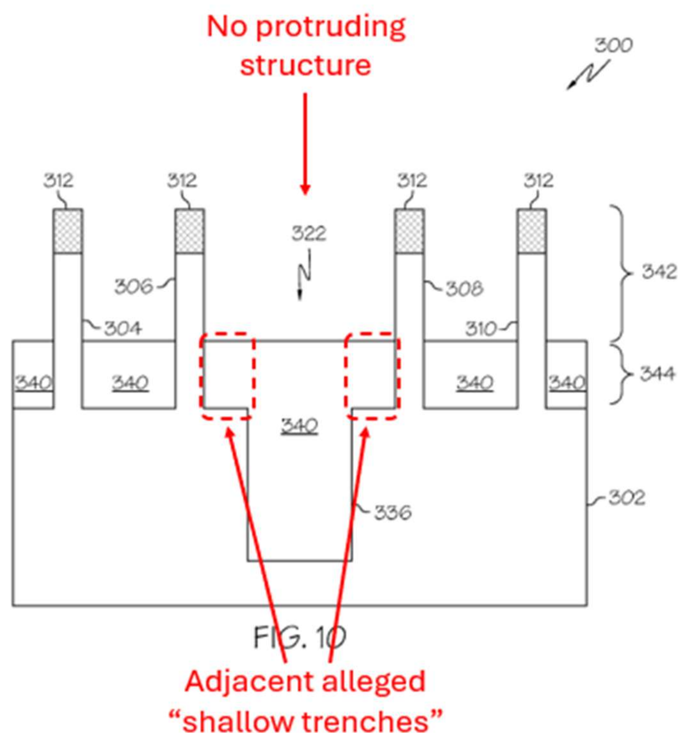


FIG. 10

Pet., 29 (additional annotations added); Ex. 2001, ¶48; *see* Ex. 2005 (defining "trench" as "a long cut in the ground"). Further, the Petition's theory requires that the active region extends an arbitrary distance past the outer boundaries of the protruding structures. A POSA would have understood, however, that the areas outside of the protruding structures are not part of the "active region," because those protruding structures act as the conducting channels between the source and drain regions. Ex. 2001, ¶48; *see also supra* § II.B.

Thus, Lin fails to disclose or render obvious "a plurality of shallow trenches disposed in the substrate in the active region," as recited in element [1.b].

Moreover, even assuming for the sake of argument that the Petition is correct that those areas constitute the claimed "shallow trenches," Lin fails to satisfy another requirement of element [1.b]—that "a portion of the substrate between each two shallow trenches is defined as a protruding structure." In this case, the portion between the two "inner" alleged shallow trenches would not be defined as a protruding structure:



Ex. 1004, Fig. 10 (annotated); Ex. 2001, ¶49.

Thus, Lin fails to disclose or render obvious "a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure," as recited in element [1.b]. The Petition relies solely on Lin for this claim language. Pet., 28-31 (relying on Liaw for only the "sidewall" limitations). Accordingly, Ground 1 fails to disclose or render obvious element [1.b].

3. Ground 1 Fails To Disclose Or Render Obvious "the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall" (Element [1.b])

The '909 patent discloses and claims a protruding structure having an upper portion with a "substantially vertical sidewall" and a lower portion with a "tilted sidewall." Petitioner's expert asserts, without support, that such protrusions were "well-known" prior to the '909 patent. Pet. 5. But Petitioner's Ground 1 does not include any such protruding structure. Instead, Petitioner amalgamates the upper portion of Lin's fin with the lower portion of Liaw's fin. This contrived combination fails in at least two different ways.

First, Lin does not actually describe protrusions "having a substantially vertical sidewall." Ex. 2001, ¶52. Petitioner cites to col. 6, lines 49-54 of Lin as disclosure of this limitation. Pet., 31. That section of Lin, however, includes no description of the shape of Lin's protruding structure, let alone any disclosure of

"substantially vertical sidewalls." Nothing in the text of Lin suggests that its fins have substantially vertical sidewalls. Ex. 2001, ¶52. Without actual support in the text of Lin, Petitioner relies on Fig. 10 of Lin. The visual appearance of components in patent figures, however, ***cannot*** be relied upon as evidence of the features' shapes. *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343 (Fed. Cir. 2013) (holding that the visual appearance of unscaled figures "cannot be relied upon" as evidence that a structure is "longer than it is wide," i.e., "elongated").

Even if Lin did describe a protruding structure with a "substantially vertical" upper portion, Petitioner's combination of Lin with Liaw would also fail. Petitioner argues that "a POSA would have been motivated to modify Lin's fabrication method to form one or more of Lin's protrusions 304, 306, 308, and 310 (the "protruding structure") using the etching parameters set forth in Liaw." Pet., 32-33. It's not enough to simply modify Lin with Liaw's process, because Liaw's protruding structure does not have an upper portion with a "substantially vertical" sidewall. Rather, the sidewall of the upper portion of Liaw's protruding structure is also tilted:

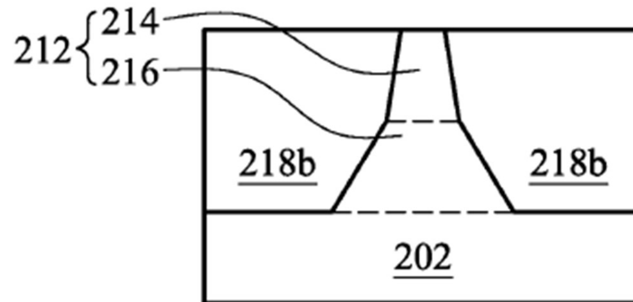


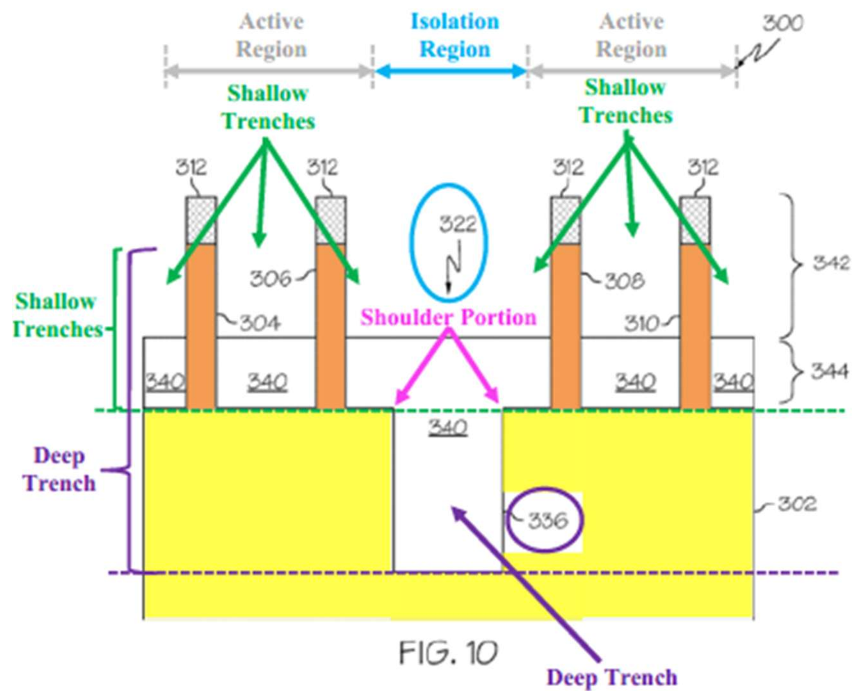
FIG. 5B

Ex. 1005, Fig. 5B; Ex. 2001, ¶53.

As such, Petitioner's amalgamated protruding structure must include the upper portion (with purported substantially vertical sidewall) of Lin with the lower portion (with tilted sidewall) of Liaw. Ex. 2001, ¶54. Petitioner's expert does not provide any explanation of why a POSA would use Lin's process to create the upper portion of the fin, and then switch to Liaw's process for the lower portion of the fin.

4. Ground 1 Fails To Disclose Or Render Obvious "Wherein The Deep Trench… Has A Shoulder Portion" (Element [1.c])

The Petition alleges that Lin's "isolation trench 336 also includes '*a shoulder portion*' at both the top left and top right corners—e.g., where the sidewalls of isolation trench 336 meet the upper surface of substrate 302." Pet., 34.



Pet., 34 (showing annotated Ex. 1004, Fig. 10). The challenged claims require that the claimed "deep trench" (including the "shoulder portion") is "disposed in the substrate in the isolation region." However, according to the Petition's apparent interpretation, Lin's alleged "shoulder portion" would include at least part of one of the alleged "shallow trenches," which the Petition alleges is part of the active region. Ex. 2001, ¶56. Thus, the Petition's arguments regarding Lin's alleged "shallow trenches" directly contradict its own arguments regarding Lin's alleged "shoulder portion." *Id*.

The Petition's Ground 1 relies solely upon Lin for element [1.c]. Pet., 33-35. Accordingly, because Lin fails to disclose or render obvious "wherein

the deep trench… has a shoulder portion," Ground 1 fails to disclose or render obvious element [1.c].

5. Ground 2 Fails For The Same Reasons As Ground 1

Ground 2 adds the Chang reference to address an additional limitation of dependent claim 5, which depends from independent claim 1. Pet., 47-48. Ground 2 does not provide any further analysis regarding claim 1. Pet., 47-53. Thus, Ground 2 fails for the same reasons as Ground 1.

B. Grounds 3 and 4

In Ground 3, the Petition alleges that Chang (Ex. 1006) renders obvious claims 1-3, 5, and 6. Pet., 53 In Ground 4, the Petition alleges the combination of Chang and Liu (Ex. 1009) renders obvious claim 4, which depends from claim 1. Pet., 71. Both of these grounds fail because Chang does not disclose or render obvious element [1.c].

1. Ground 3 Fails To Disclose Or Render Obvious "A Deep Trench Disposed In The Substrate In The Isolation Region, Wherein The Deep Trench Is Deeper Than The Shallow Trenches And Has A Shoulder Portion" (Element [1.c])

The Petition alleges that Chang's Figure 11 embodiment includes "a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion." Pet., 62-66. The Petition identifies Chang's alleged "isolation region," "deep trench," and "shoulder portion" as follows:

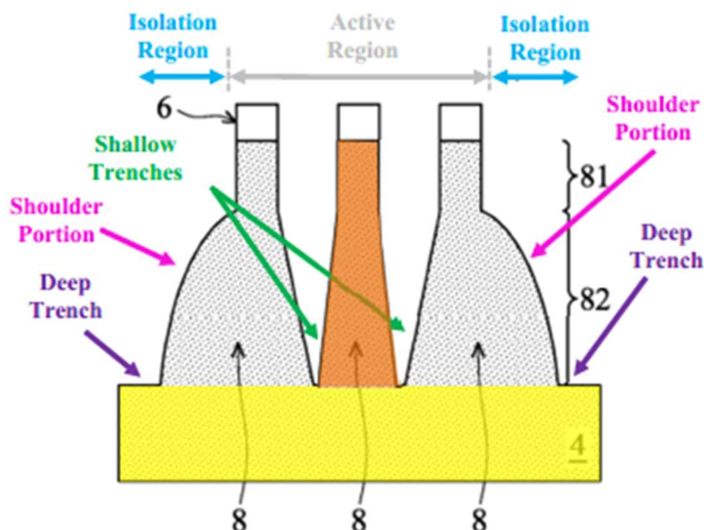
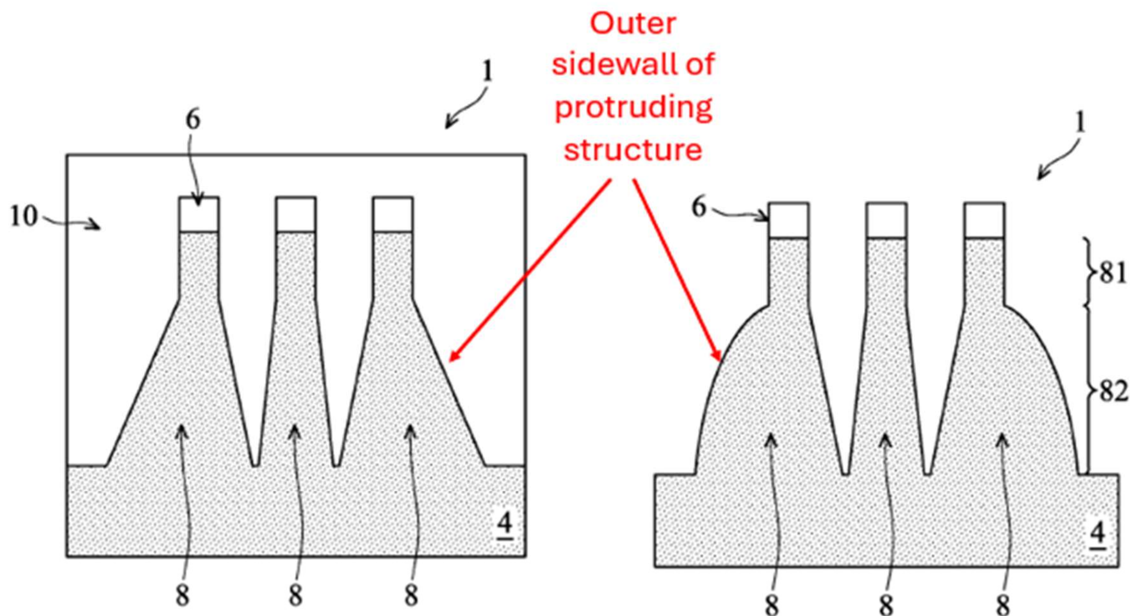


FIG. 11

Pet., 63 (showing annotated Ex. 1006, Fig. 11). But the Petition's interpretation of Chang contradicts Chang's disclosure, which reveals that what the Petition alleges is the "shoulder portion" of the "deep trench" is really just "the outer sidewall of the lower portions 82 of the outermost fins 8," which "are formed to have a non-constant slope." Ex. 1006, 6:38-40. This becomes apparent when comparing Chang's main embodiment (see Figs. 5-9) with its Figure 11 embodiment. For example, in Figure 6b (below left), the outer sidewalls of the outermost fins are straight but tilted. In Figure 11 (below right), that same outer sidewall is curved.



Ex. 1006, Figs. 6b and 11 (annotated). But regardless of the shape, the fact remains that it is still the outer sidewall of the protruding structure, rather than the "shoulder portion" of a "deep trench disposed… in the isolation region," as recited by element [1.c]. Ex. 2001, ¶60. In contrast, in the '909 patent, the shoulder portion of the deep trench is separate from the tilted sidewall of the protruding structures, showing that these are separate elements in the claimed device, rather than the shoulder portion being part of the protruding structure's sidewall:

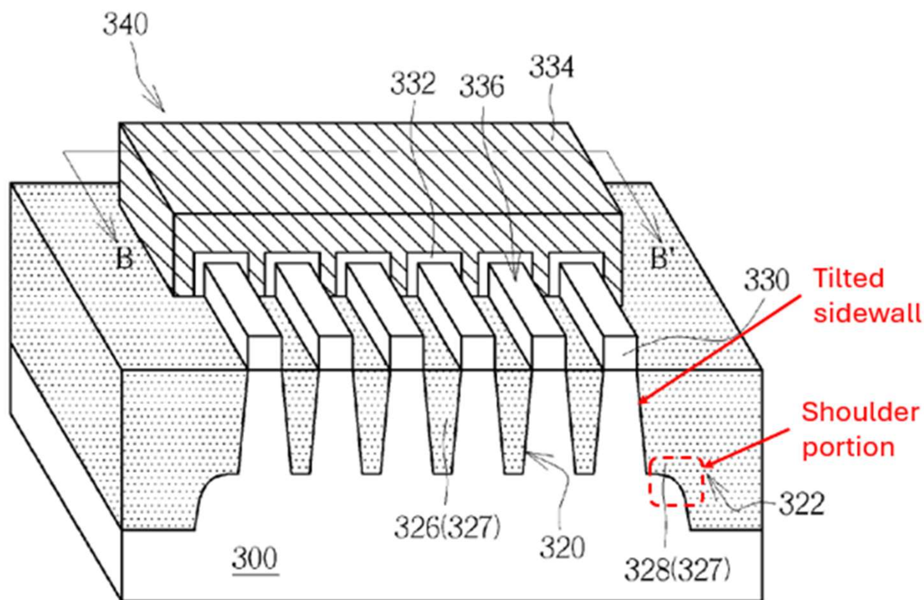


FIG. 13

Ex. 1001, Fig. 13 (annotated); Ex. 2001, ¶60; *see also* Ex. 1002, 90 (May 25, 2015, amendment adding "shoulder portion" limitation).

That the shoulder portion of the deep trench is separate from the protruding structure is clear from the '909 patent's process for forming the shallow and deep trenches. Ex. 2001, ¶61. First, as shown below, in Figure 9, "[a]t least one etching process is performed by using the patterned photoresist layer 316 as a mask to sequentially pattern the ARC layer 314, the auxiliary mask layer 312, and then remove the mask layer 302 and the first protruding structure 310 in the second region 402." Ex. 1001, 5:6-11. Moreover, "the etching process further removes the

substrate 300 in the second region 402 and the third region 404, thereby forming a fifth trench 309 in the second region 402 and the third region 404." *Id.*, 5:11-14.

FIG. 9

Id., Fig. 9. That is, in Figure 9, the upper portions of the protruding structures—the portions with vertical sidewalls—are formed. Ex. 2001, ¶62. Then, "[a]s shown in FIG. 10, an etching process is performed by using the patterned mask layer 302 as a mask to simultaneously deepen the first trenches 306 and the fifth trench 309. In the first region 400, each first trench 306 is deepened to form a second trench 320. In the second region 402 and the third region, the fifth trench 309 is deepened to form a sixth trench 323." Ex. 1001, 5:16-23.

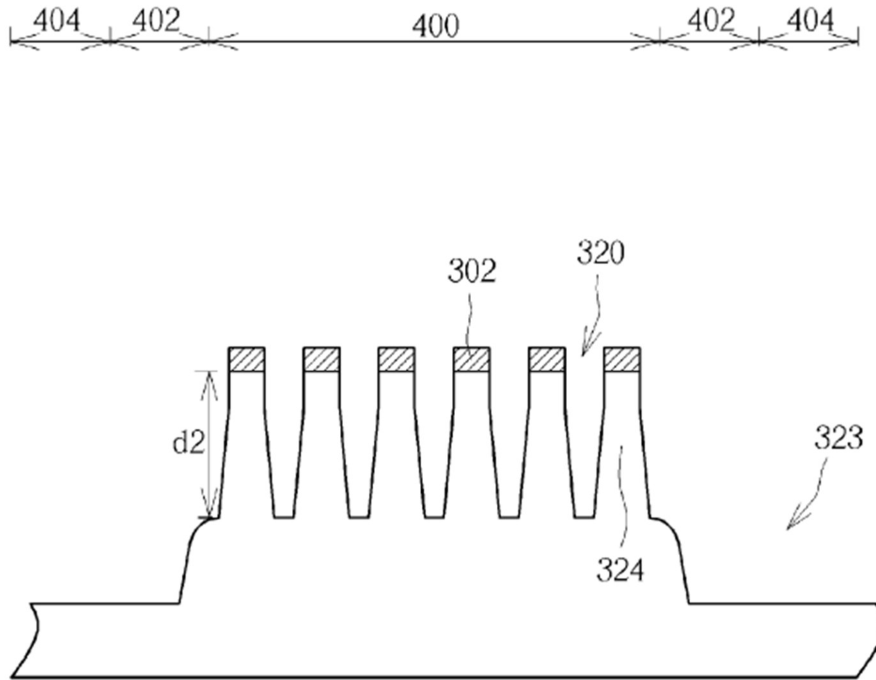


FIG. 10

Id., Fig. 10. As can be observed by comparing Figures 9 and 10, the lower portions of the protruding structures—the portions with tilted sidewalls—are formed in the active region 400. Ex. 2001, ¶62. And separately, the deep trench (including the shoulder portion) are formed in the isolation region 402 and 404. *Id*.

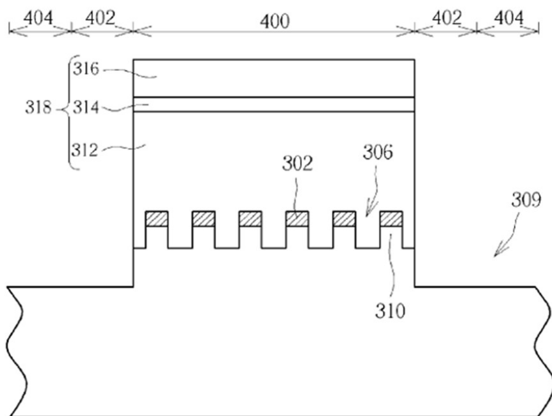


FIG. 9

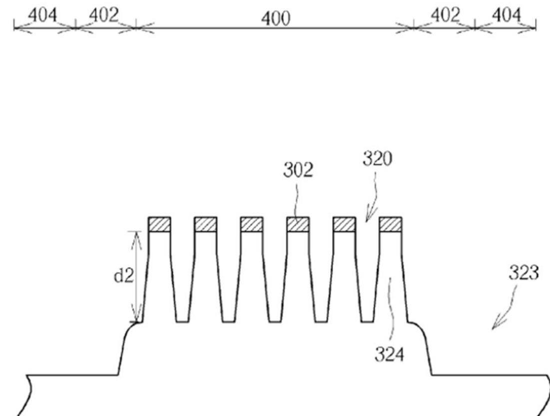


FIG. 10

Compare Ex. 1001, Fig. 9 *with id*., Fig. 10. Thus, the '909 patent clearly distinguishes between the outer sidewall of the protruding structure and the shoulder portion of the deep trench. Ex. 2001, ¶62.

This distinction is critical because the challenged claims require that the "deep trench" (including the "shoulder portion") is "disposed… in the isolation region." Contrary to the Petition's annotations of Chang's Figure 11, the Petition's alleged "shoulder portion" is part of the active region because it is a part of the protruding structure. Ex. 2001, ¶63. As such, what the Petition identifies as the "shoulder portion" of the "deep trench" does not meet the requirements of element [1.c].

The Petition's arguments regarding the "shoulder portion" are further undercut by the Petition's own prior arguments regarding element [1.b]. The Petition alleges that the inner sidewalls of Chang's outermost protruding structures meet element [1.b]'s requirement that "the protruding structure has… a lower portion having a tilted sidewall":

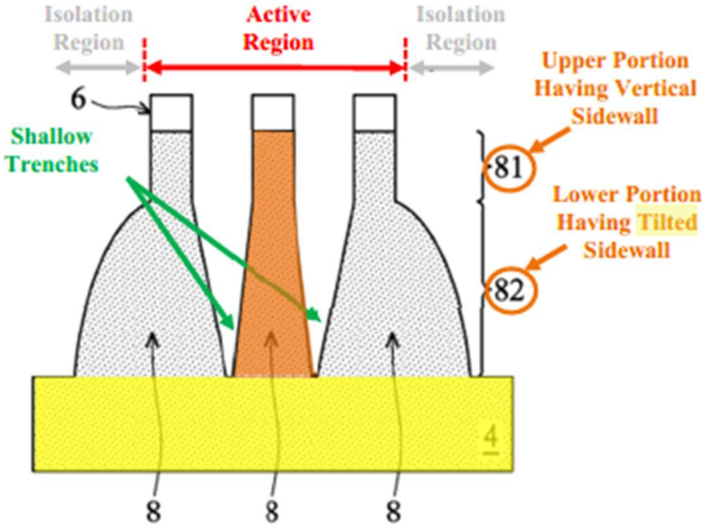
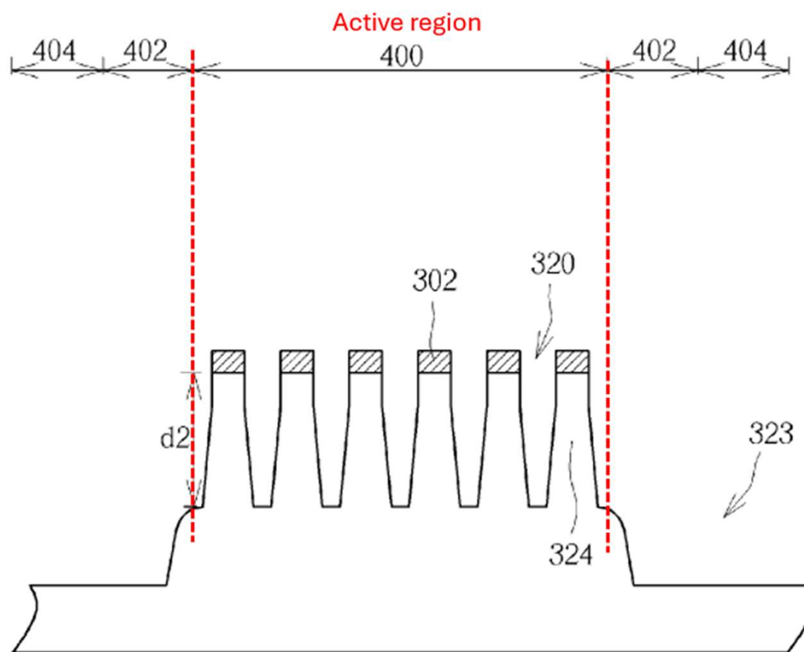


FIG. 11

Pet., 60 (showing annotated Ex. 1006, Fig. 11). If this is correct, then logically, the outer sidewall must also be part of the claimed "lower portion" of the protruding structure and thus is in the active region. Ex. 2001, ¶64; *see also* Ex. 1001, Fig. 10 (showing that active region 400 includes outer sidewall of outer protruding structures). That the outer sidewall is in the active region is confirmed by the '909 patent's Figure 10:



Ex. 1001, Fig. 10 (annotated) (showing that active region 400 includes outer sidewall of outer protruding structures). Thus, the Petition's allegations that the "active region" includes only the "upper portion" of the protruding structure makes no sense—the Petition's interpretation of Chang is clearly a contrived attempt to meet the claim language rather than based on Chang's disclosure. Ex. 2001, ¶64.

Accordingly, Ground 3 fails to disclose or render obvious element [1.c].

2. Ground 4 Fails For The Same Reasons As Ground 3

Ground 4 adds the Liu reference to address an additional limitation of dependent claim 4, which depends from independent claim 1. Pet., 71. Ground 4 does not provide any further analysis regarding claim 1. Pet., 71-77. Thus, Ground 4 fails for the same reasons as Ground 3.

V. CONCLUSION

For the above reasons, the Petition should be denied.

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 5,173. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

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CERTIFICATE OF SERVICE

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