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A New $CBrF_3$ Process for Etching Tapered Trenches in Silicon

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ABSTRACT

A new process for etching trenches in bulk silicon for the generation of trench capacitors in highly integrated DRAM's is reported. Trenches, 1 μm wide and up to 2 μm deep, were etched in RIE mode with $CBrF_3$ using a single wafer etcher. The trenches have very smooth sidewalls. The slope of the sidewall can easily be controlled by the RF power. The possibility of tapering the trench in bulk silicon is attributed to the low selectivities of the process with regard to the oxide mask, leading to enhanced sputter etch of the mask.

Anisotropic dry etching processes for the generation of trenches in bulk silicon are intensively developed for highly integrated DRAM's. Deep trenches are used in these devices for trench capacitors to replace planar capacitors; thereby higher integration without capacitance loss can be achieved (1, 2). To obtain uniform thickness and quality of the dielectric, the trench must have very smooth sidewalls and a rounded bottom. Therefore, the etching process must not lead to enhanced etch attack at the rim of the trench bottom, a phenomenon called "trenching" (3). Furthermore the sidewalls must be slightly tapered to allow for complete subsequent refilling of the trench without voids. In this paper, a new dry etching process for bulk silicon that meets all of the requirements is reported.

Experimental

For the experiments, a single wafer etcher, Alcatel GIR 200, was used. The etching chamber was loaded with wafers via a vacuum loadlock. The chamber itself and the electrodes consist of anodized aluminum. The wafers were put one after another on the powered electrode and thus processed in RIE mode.

The process gas comes into the chamber through holes in the grounded top electrode acting as a gas shower. The electrode spacing was adjusted to 150 mm for optimum etch rate uniformity.

We chose $CBrF_3$ as the process gas for it forms polymer sidewall films that are mainly responsible for etch anisotropy. The chamber walls had to be kept at a temperature of 40°C to obtain best reproducibility of the process.

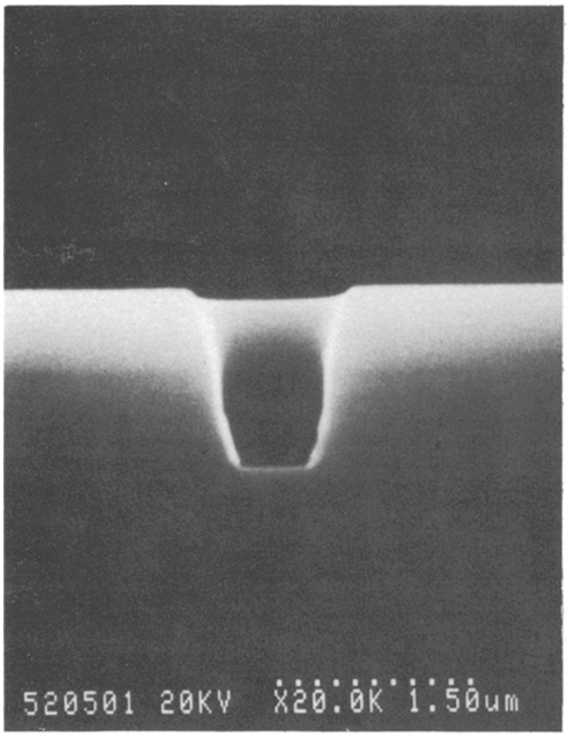


Fig. 1. Trench profile for RF = 250W

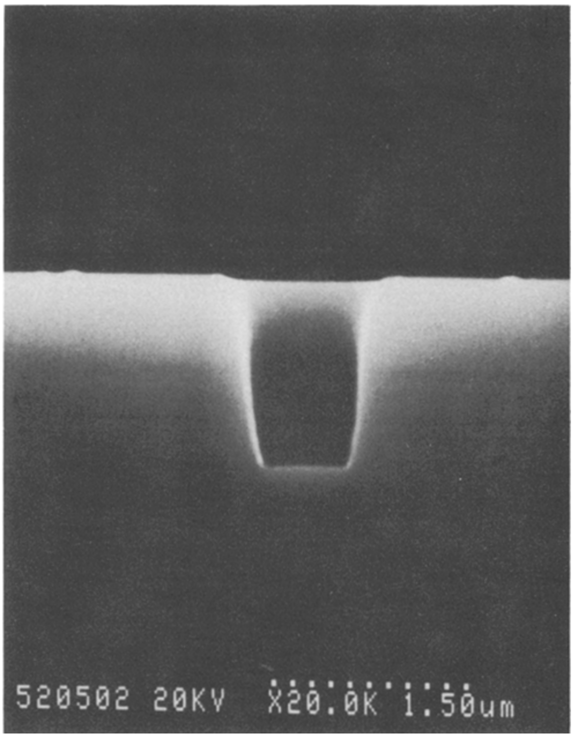
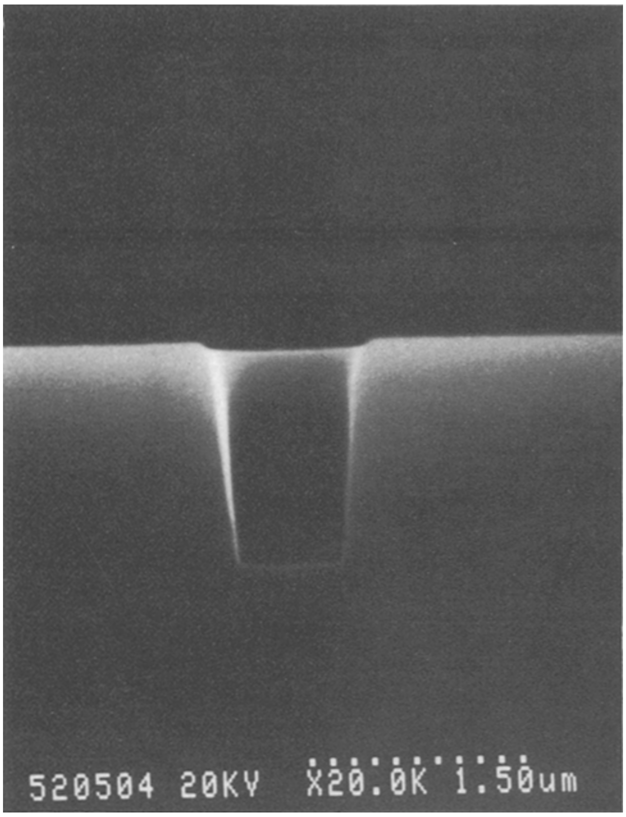


Fig. 2. Trench profile for RF = 200W



For the etching mask, 700 nm of CVD oxide (TEOS) was used. The oxide mask was structured in an AME 8111 batch etcher (Applied Materials). Photoresist had to be stripped prior to the trench etching process to avoid photoresist reticulation. During the trench etching process, the erosion of the oxide mask was monitored by a laser interferometer. The process was stopped when the thickness of the remaining oxide mask was 50-100 nm.

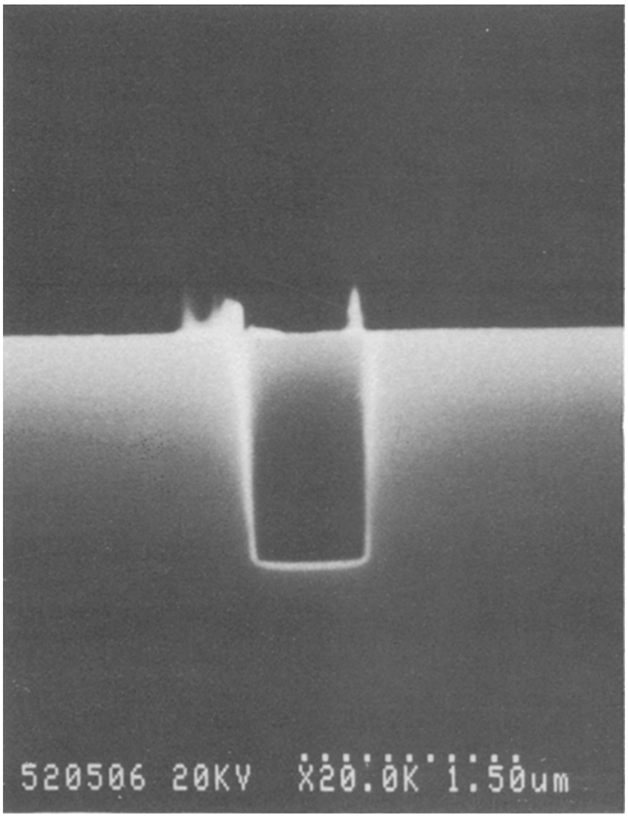


Fig. 4. Trench profile for RF = 75W

The wafers were of p-type silicon with a resistivity of 20 Ω-cm; they are 4 in. in diameter and had (100) orientation.

Results

Optimum trench profiles were obtained with a $CBrF_3$ gas flow of 30 standard cm^3/min and a pressure of 2 Pa (15 mtorr) at RF power levels ranging from 75 to 250W (Fig. 1-4). All these profiles have in common the required smooth sidewalls and rounded bottoms. They differ appreciably, however, in the slope of the trench sidewall. The profile obtained at the highest applied RF power, which was system-limited, has strongly tapered sidewalls. The slope of the sidewall increases continuously with decreasing RF power. The profiles obtained at 75W have nearly vertical sidewalls. Trenches etched at even lower RF power levels are not suited for capacitor cells; due to small bias voltages and low directionality of the ions, the sidewalls of these trenches show appreciable bowing (Fig. 5).

The experiments were done at the lowest gas pressure that could be achieved with the equipment. At higher gas pressures the trench sidewalls showed irregularities like steps, surface roughness, and bowing. The gas flow had only minor influence on the profiles; the etch rates increased slowly with increasing flow; a flow of 30 sccm of $CBrF_3$ was chosen to obtain optimum etch rate uniformity. The etch rate uniformity of all processes reported here was less than 10% with regard to both trench depth and oxide erosion.

Discussion

For the understanding of the process that leads to tapering of the trenches, it is useful to consider the dependence of both the silicon etch rate and the selectivity to SiO_2 on the applied RF power (Fig. 6). The etch rate for bulk silicon increases strongly with increasing RF power, whereas the selectivity to the oxide mask decreases with RF power due to enhanced nonselective physical sputtering by ions. The selectivity is rather small over the whole range of applied RF power.

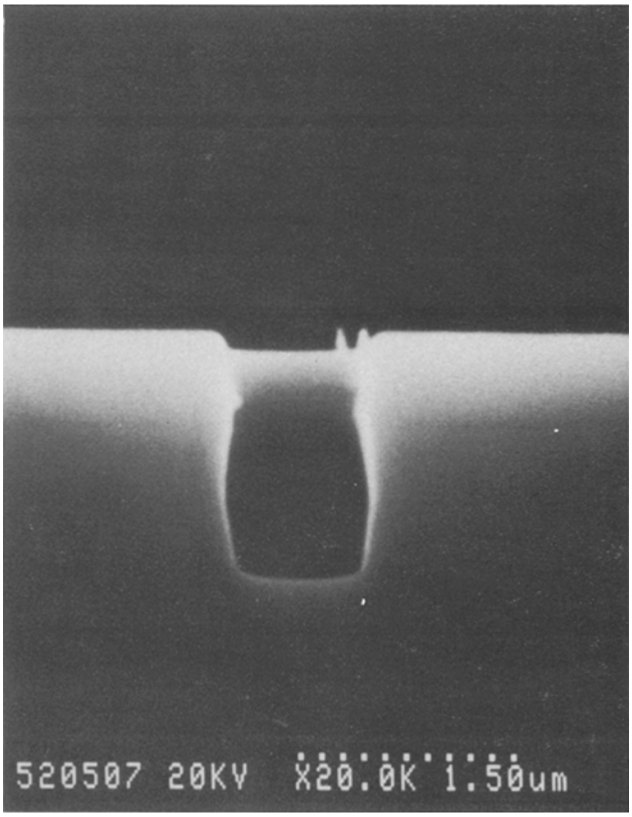


Fig. 5. Typical trench profile obtained at very low RF power levels (≲50W).

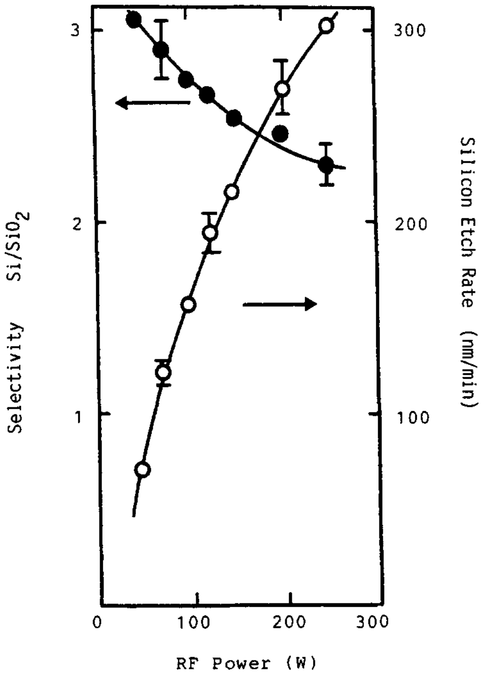


Fig. 6. Dependence of selectivity and silicon etch rate on RF power

Since the oxide mask has nonvertical sidewalls prior to trench etching the low selectivity to SiO_2 has direct influence on the trench profile obtained at different RF power levels. The smallest angle of slope is obtained at the highest applied RF power.

It increases continuously with decreasing RF power or what is equivalent with increasing selectivity to SiO_2. Thus, trench sidewall tapering may be adjusted by oxide mask erosion via physical sputtering. In our case, the angle of sidewall slope ranges from nearly 90° to 76° when the RF power is varied from 75 to 250W (Fig. 7). The taper mechanism of this low selectivity silicon trench etching process is similar to low selectivity oxide etching processes (4) where enhanced photoresist erosion is used to taper the sidewalls of the underlying oxide layer.

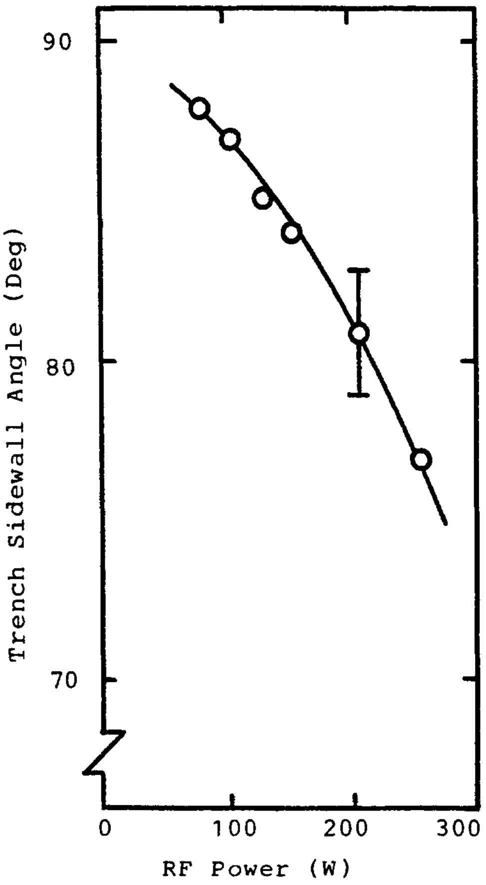


Fig. 7. Dependence of the sidewall slope on RF power

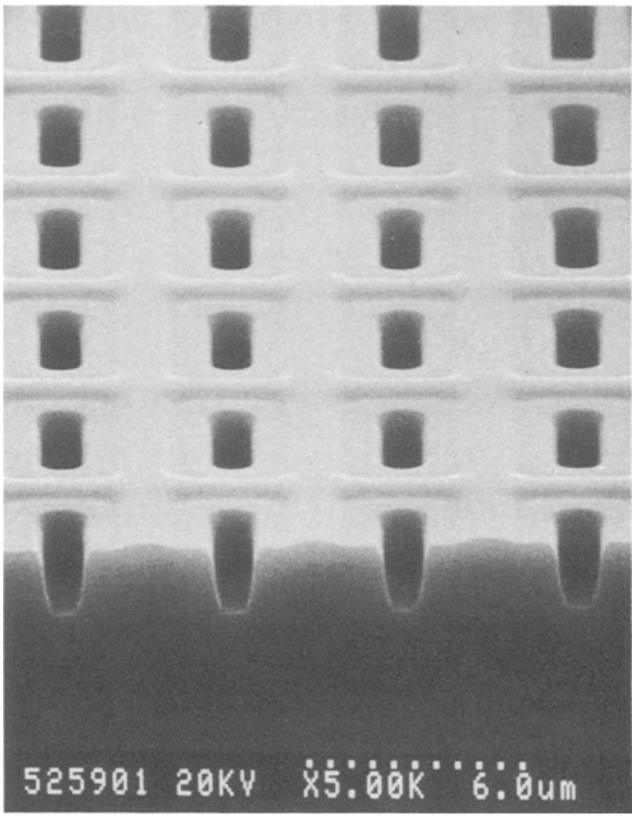


Fig. 8. Memory field with 2 μm deep trenches etched with RF = 125W and 1.5 μm oxide mask.

For pre-etch oxide angles ranging from 84° to 86° we observed no change of the etched profiles; at appreciably smaller pre-etch oxide angles an increased tapering of the trench profiles must, however, be expected.

Still deeper trenches could be achieved by using thicker oxide masks. A memory field with 2 μm deep trenches, which were etched with the same set of process parameters as the profile shown in Fig. 3, is presented in Fig. 8. The shown trenches are isolated from each other by the standard LOCOS technique.

We think that the smooth sidewalls of the observed trench profiles must be attributed to both the process gas and the applied RF power regime. $CBrF_3$ is well known for buildup of plasma-induced polymer films that protect the sidewalls from lateral etch attack leading to a very anisotropic etch. At the applied RF power levels the attack of the reactive ions is strongly directed perpendicularly to the wafer surface without leading to the "trenching" that is observed with chlorine-based chemistries (3).

Using CCl_4 we obtained much less reproducible processes all of which exhibited a tendency to bowing of the trench sidewalls. Changes in process parameters had only a minor influence on the profiles. Due to these reasons and because of its carcinogenic by-products we replaced the CCl_4 process by a $CBrF_3$ process.

Summary

It has been demonstrated that the new $CBrF_3$ process is a very promising process for etching trench cells for highly integrated DRAM's. The obtained profiles are well suited for this application; they have straight and slightly tapered sidewalls and a rounded bottom. Due to the special low selectivity etching process with $CBrF_3$ chemistry, the slope of the sidewall can be varied easily by the applied RF power. The $CBrF_3$ process substitutes a formerly used CCl_4 process which may lead to carcinogenic by-products.

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Variable Profile Contact Etching Using Bilayer Planarized Photoresist

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ABSTRACT

Contacts have been etched in 1 μm thick 10% phosphorus-doped pyroglass masked with bilayer planarized photoresist with slopes controllably varied from about 60° to 80°. The slope is controlled by varying the power, reactant chemistry, etch time, and etcher coolant temperature, and is independent of feature size. The relative dependence of the slope, the contact size, and the etch rate on the above parameters is presented. Test structures have been used to compare sloped contacts to control contacts with vertical profiles, and the metal step coverage, punch-through, and gate dielectric integrity data correlate to the measured profiles.

One of the most important steps in a silicon integrated circuit fabrication technology is the formation of contacts between the first metal level and the silicon junctions. Typically, these contacts are made by dry etching through a dielectric, typically silicon dioxide either with or without phosphorus and/or other dopants. Single layer positive photoresist normally serves to mask the contact openings during etching, but contacts approaching 1 μm and smaller may require a multilevel planarized photoresist system to improve the quality of the lithography.

Contact etching must satisfy a variety of requirements, many of which have conflicting solutions. First, contacts must provide a low electrical resistance path between the metallization and the silicon. This generally requires large area contacts etched deeply into the silicon. Etching too deeply results in junction shorting due to electromigration of aluminum into and through the junction (1). This is commonly known as contact electromigration. Among other effects, making contacts too large results in reduced isolation voltage if the contact edge encroaches too closely into the isolation region; or in shorting of the metal to the polysilicon gate, if too much dielectric is removed adjacent to the gate.

In addition, serious reliability problems arise if the profile of the contact is too steep. In this case, the aluminum is thinned where it crosses this step, and electromigration results in a metal open and premature failure of the part (2). Various planarization schemes have been proposed and implemented to solve the step coverage problem. Such schemes as metal pillars and metal-filled contacts are complex, not widely used, and are not the subject of this work.

The simplest approach for obtaining good step coverage is to slope the walls of the contact. One widely used technique is to use a heavy phosphorus or boron/phosphorus doping in the dielectric over the contacts. Following contact etching an anneal cycle is used that causes the dielectric to flow slightly, thus rounding the corners of the etched contact and providing a partial planarization (3). This is a widely used approach and can be well controlled, but by itself may not provide enough planarization to assure the desired aluminum step coverage.

Another popular approach for achieving good step coverage is to use a partial wet etch, which is isotropic, followed by an anisotropic dry etch. This typically slopes the top edge of the contact, while the bottom portion is vertical. This can give very good step coverage, but difficulty may be encountered in controlling the wet etch and in getting good wetting, especially with very small contacts. In addition, a number of other techniques for producing sloped profiles using dry etch processes have been developed (4-6). Typically, these processes seek to slope the photoresist and then use controlled erosion of the photoresist to induce a controlled slope in the etched contact. Sometimes the various techniques described above are combined to achieve the desired result.

A major problem with sloped profile contact etching is ensuring a uniform resist slope, especially for varied feature sizes (6). A further problem with sloped resist processes is that continued etching of the contact results in a continued growth in the contact diameter, although this can be alleviated somewhat by using a two-step etch process (5).

In this paper, we report the development of a sloped etch process using multilevel photoresist. Sloped etch processes using multilevel resist have previously been reported (7, 8). These techniques are known as cantilevered mask techniques. In these instances, a noneroding mask is spaced above the substrate by an undercut polymer layer. The resulting profile after the oxide etch tends to be sloped. The slope depends to first order on the thickness of the spacer layer and to second order on the etch recipe. In addition, the preparation of the cantelever mask requires two etch steps in addition to the actual oxide etch: etching the nonerodable mask anisotropically, and etching the spacer layer isotropically. The technique reported in this paper does not require additional dry etch steps. Although the mechanism of sloping is resist erosion, the resist begins with a vertical profile. The erosion can be controlled by varying the parameters of the etch process itself, resulting in contact profiles that controllably vary from about 60° to 80° (measured from the horizontal) depending upon the recipe chosen. We demonstrate the relative dependence of the slope, contact

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