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Present and Future of Si-based Transistor Technology for Memories

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Nanotechnology is named as a promising research area for the semiconductor technology to be extended or replaced by it. Since the silicon based devices such as NAND Flash memory, DRAM, SRAM, and CPUs are scaled down below 100 nm entering into the nanoscale regime late 1990s, in the middle of 2005, we are already facing the appearance of sub 50 nm technology in production. In this paper, we introduce recent technology development activities in Samsung to realize the sub 50 nm technologies into the devices such as SRAM, DRAM, and Flash memories as well as the high performance logic devices. RCAT (Recessed Cell Array Transistor), PiFET (Partially-insulated MOSFET) and FinFET, McFET (Multi channel FET), MBCFET (Multi-Bridge Channel MOSFET), and Twin Silicon Nanowire MOSFET (TSNWFET) are the 3-dimensional structure CMOS transistors to be introduced for nanoscale applications.

Introduction

The requirement of memory, one of the fundamental elements, for the rapid IT industry growth has been dramatically increased as shown in Fig.1. The device development speed has been accelerated to meet the market demand since sub 100 nm technology has been used for mass production in 2002. With the achievement of this technology trend, the digital equipment industry grows fast and we are being able to enjoy the plentitude of almost 16 gigabytes memory capacity as illustrated in Fig. 2.

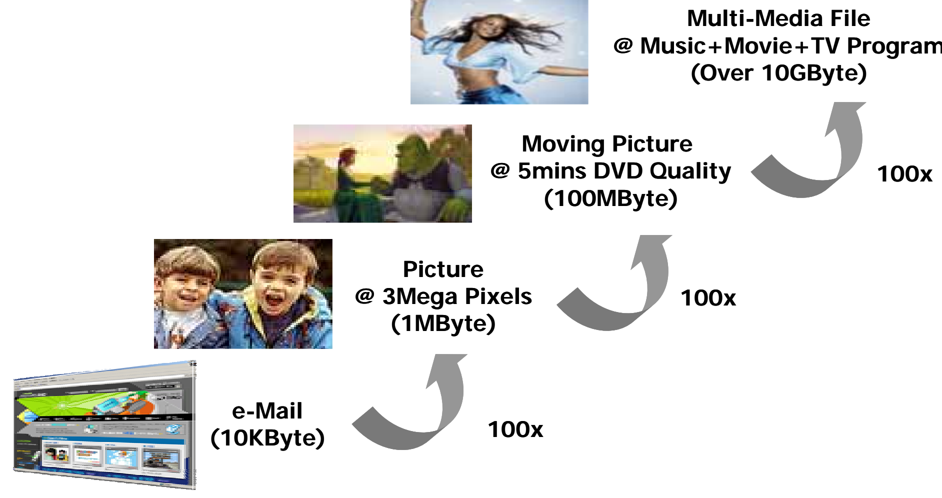

Figure 1. Information density increases by 100 times in sequence driving explosive demand for semiconductors.

TSMC EX1014
U.S. Patent No. 9,117,909 B2

Figure 2. With 16 gigabytes of memory, we can enjoy up to 4 series of DVD titles or 4000 songs with MP3 quality.

However, transistor, the basic element for Si based devices, is facing a barrier in the use of conventional planar CMOS technology due to its physical limit to the scaling. In this paper, we introduce various non-planar transistor development activities in Samsung to be implemented into sub 50 nm devices. This development is to extend the use of Si based transistor down to sub 20 nm technology nodes. It would act as a bridge for the future devices to enter into the nanotechnology era as illustrated in Fig.3.

As the transistor gate length scales down below 45 nm, short channel effects such as DIBL (Drain Induced Barrier Lowering),Vt (Threshold voltage) roll-off, and short HCL (Hot Carrier Lifetime), are crucial to the device fabrication. Many efforts to extend the use of planar transistor, such as strained Si, high-k dielectric, and elevated S/D (Source/Drain) are introduced. However, planar transistor structure is predicted to come to the end around 30nm technology node (1).

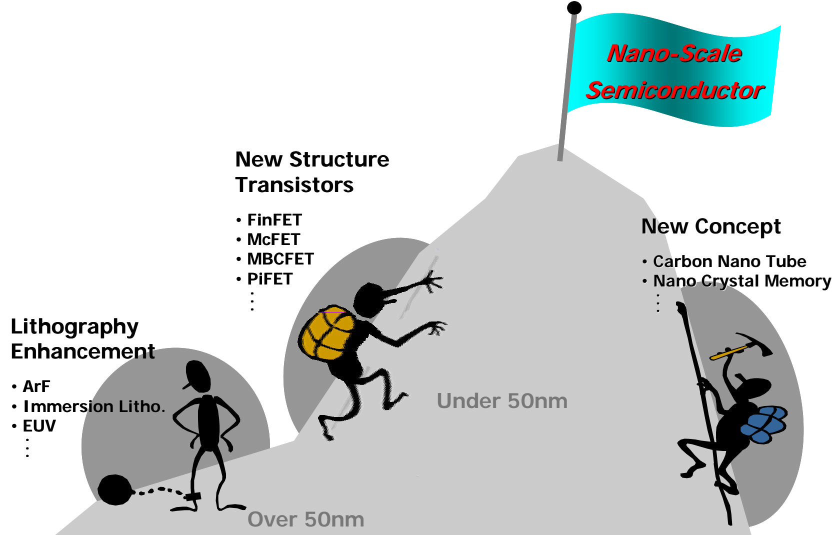

Figure 3. For the nanoscale semiconductor fabrication, new material, structure, concept are required in addition to fine patterning technologies.

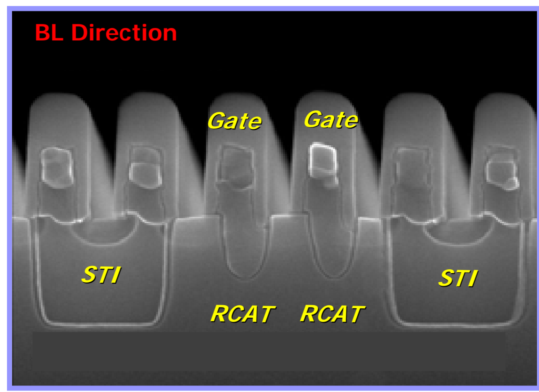

Figure 4. To overcome the scaling limit in DRAM cell transistor below 100nm, the channel region is recessed enlarging the gate length.

To overcome the scaling limit of planar Si CMOS transistor, 3 dimensional transistor structures have been introduced. Among them are RCAT (2), TSM (Twin SONOS Flash Memory) cell transistor (3,4), PiFET (5,6), FinFET (Fin shape FET) (7-9), McFET (10,11), MBCFET (12-15), and TSNWFET (16).

RCAT is a quasi-planar MOSFET enlarging the gate length. PiFET is a quasi-SOI transistor to control the channel and S/D depth effectively without demerits of SOI MOSFET. FinFET is the first highly manufacturable 3 dimensional non-planar transistor with fin shape channels. Various application examples of FinFET to memory devices have been reported (17-22). McFET is a further advanced form of FinFET having twin fin channels without using any sophisticated lithography tools. All the non-planar transistors show excellent electrical characteristics even though there are still some difficult tasks to be implemented to conventional CMOS processes. MBCFET that has two 20 nm thin Si bodies with surrounding gate shows the best transistor performance exceeding the ITRS (International Technology Roadmap for Semiconductors) prediction. From now on we will introduce these newly developed silicon based nanoscale CMOS transistors in detail.

Nanoscale Planar MOSFETs

In this chapter, we show planar MOSFET structures to be extended down to 50 nm technology node.

RCAT (Recessed Cell Array Transistor)

The newly developed recess channel array transistor of DRAM cell is shown in Fig. 4. Recessing the transistor channel, the gate length in small area is effectively enlarged so that not only the Vt distribution of RCAT is improved over the planar transistor but the drain induced barrier lowering (DIBL) is also reduced. This RCAT technology makes possible the DRAM scaling down to 50 nm technology node.

TSM (Twin SONOS Memory) Cell Transistor

While data storage of 2 bits per cell is popular in Flash memories, SONOS type Flash memory is an ultimate shape of Flash memory without floating gate. However, in

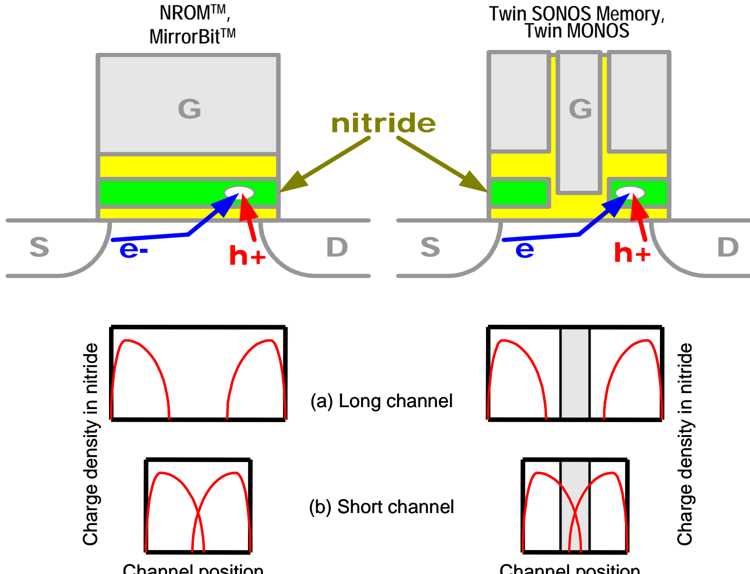

Figure 5. Non-volatile SONOS type Flash memory is facing the scaling limit due to the charge interaction along the gate. Twin SONOS memory cell transistor can be a breakthrough technology to overcome the limit.

NOR type SONOS memory, program is performed with CHI (Channel Hot Carrier Injection) with high drain voltage to enhance the program speed. For this purpose, the gate length should be large enough so that the transistor punchthrough voltage is larger than the program voltage. In addition, since the 2 bits/cell operation requires large enough separation of the programmed charges at the source and drain region, charge interaction in the nitride, charge trapping layer replacing the floating gate limits the gate length scale as illustrated in Fig.5. ITRS (International Technology Roadmap of Semiconductor) 2003 predicts the SONOS Flash Memory devices cannot be scaled down below 140 nm of the gate length even at the 20 nm NVM technology. Fig.6 shows our newly developed TSM cell transistor having physically separated nitride storage nodes at the source and drain regions and the gate oxide thickness at the transistor center is so thin that the transistor can be scaled down without punchthrough problem down to the total gate length of 80 nm. With this scheme, the excellent data retention time has been obtained as shown in Fig.7.

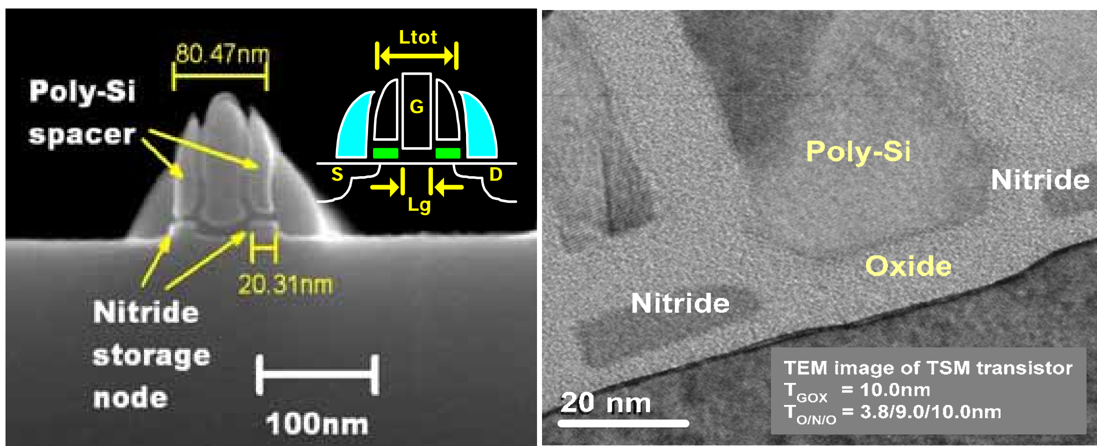

Figure 6. Using TSM cell transistor, SONOS type Flash memory can be scaled down below 80 nm without any charge interaction issues having better gate controllability.

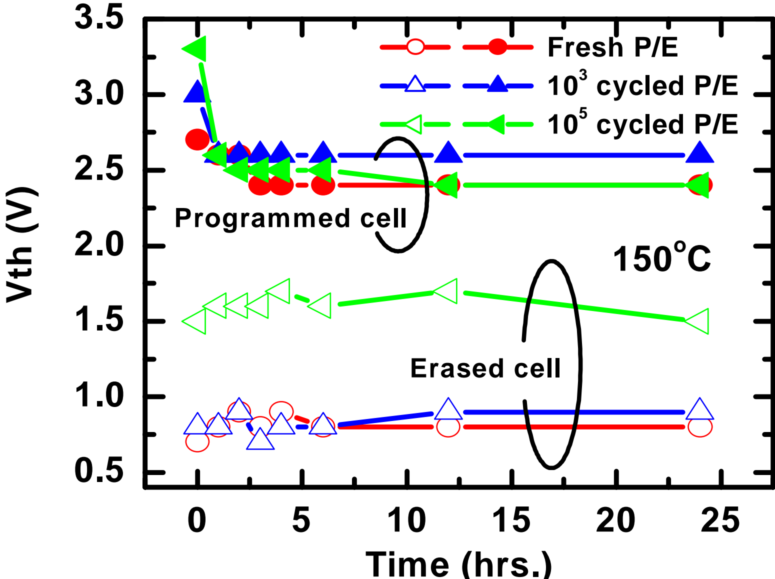

Figure 7. TSM cell shows reasonable program and erase Vth as well as excellent data retention time more than 24 hrs at 150°C.

PiFET (Partially insulated MOSFET)

As an effort to extend the planar MOSFET structure below 100 nm, SOI (Silicon On Insulator) wafer had been introduced. Using SOI wafer with thin silicon on SiO_2 layer, the channel Si region is thinned down to eliminate bulk punchthrough leakage path, while the shallow junction depth is obtained by the self-limited dopant diffusion as well. In this section, we demonstrate a PiCAT (PiFET Cell Array Transistor) structure that has PiOX, a buried oxide layer, to block the junction leakage current path physically. Using this PiCAT structure, improved DIBL characteristic, self-limited shallow junction, and reduced junction capacitance owing to its structural benefit have been obtained.

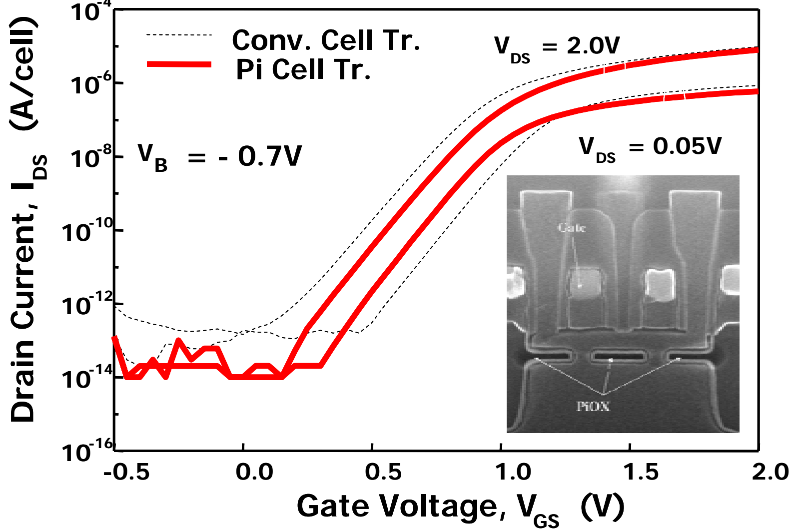

Figure 8. Self-limiting junction depth of piFET helps the PiCAT to show improved DIBL over the conventional ones.

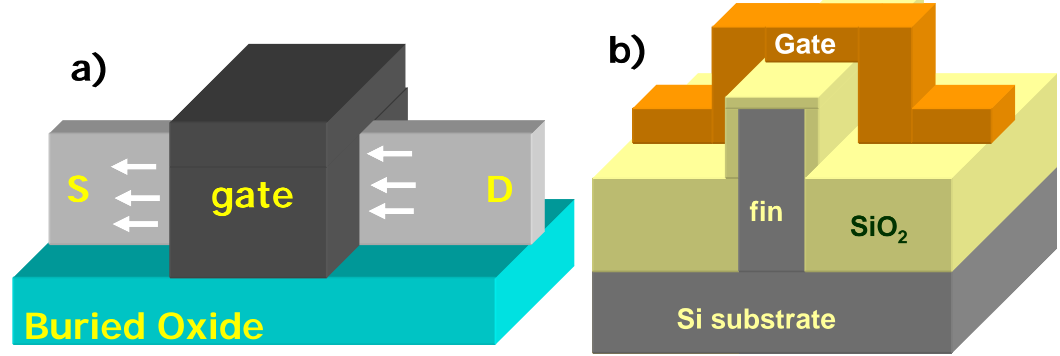

Figure 9. a) FinFET fabricated on SOI (Silicon On Insulator) waer, b) Body-Tied FinFET on Bulk Si. Body-Tied FinFET has several benefits such as eliminating floating-body, better heat dissipation, low cost, etc over FinFET on SOI.

The cross-sectional SEM picture of PiCAT for the fully integrated 80 nm 512M DRAM and the transistor characteristics are shown in Fig. 8. Using this unique process technology, the Si channel is tied to the silicon substrate so that the floating body problem of the SOI MOSFET is avoided.

3D MOSFETs for sub 50 nm Scaling

In this chapter, we show several 3 dimensional MOSFET structures that would be useful for the technology node below 50 nm down to 10 nm.

FinFETs (Fin shape MOSFETs)

Various FinFET structures, as illustrated in Fig. 9-a such as Omega-gate (23), Tri-gate (24), Dual-Gate UTB (Ultra-Thin Body), are introduced for the application below 50 nm technology node due to its good SCE immunity resulted from the excellent gate controllability with thin Si on Oxide (SOI).
We had introduced body-tied FinFETs fabricated on bulk Si instead of SOI wafer with the benefits of low wafer cost, good heat dissipation characteristic, and the elimination of floating body effect. Fig. 9-b shows schematic illustration of the body-tied FinFET.

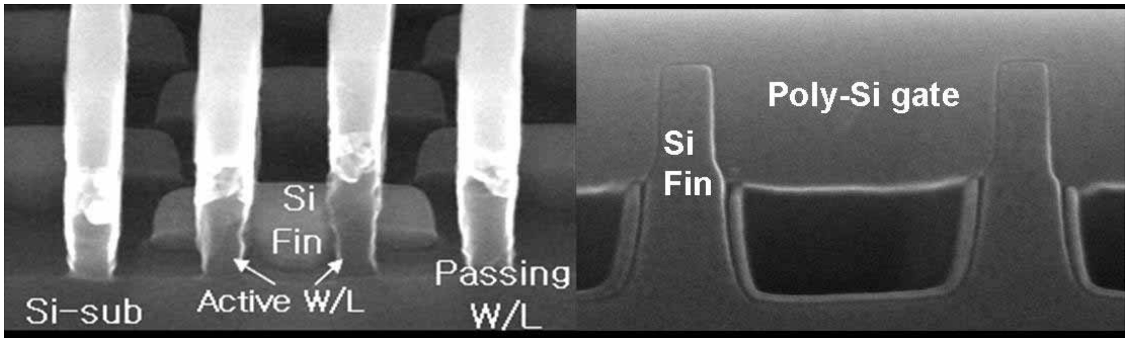

Figure 10. Body-Tied FinFET is adopted for DRAM cell array transistor application.

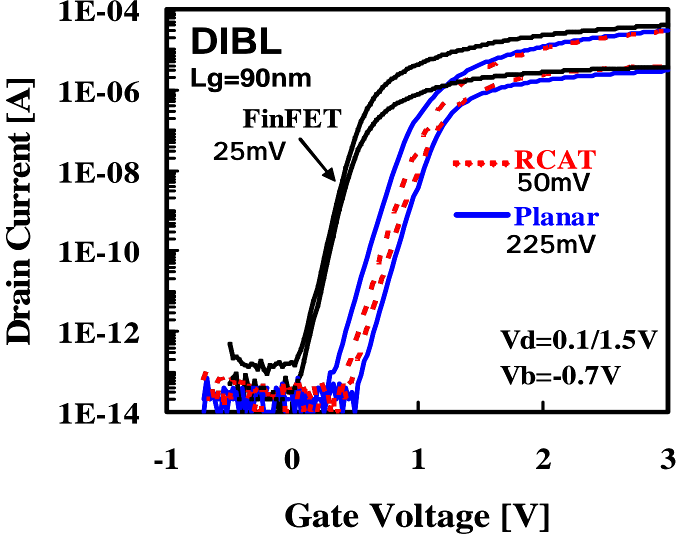

Figure 11. Due to the excellent short channel effect of FinFET, full-processed 512M 90 nm DRAM FinFET cell array transistor shows drain induced barrier lowering as low as 25 mV/V.

Fig. 10 shows the application of FinFET to fully working 90 nm 512M DRAM. Cell array transistors are made by FinFET, while the peripheral circuitries are still made by conventional planar transistors for convenience of analysis. In Fig. 11, we can clearly see that the body-tied FinFET DRAM cell transistor has superior transistor characteristics such as DIBL, subthreshold swing, and current drivability, over RCAT and planar transistors.

FinFET application to NOR Flash memory is shown in Fig. 12. With round fin, uniform tunnel oxide is formed around the fin. Fig. 13 shows that the major benefit of using FinFET to NOR cell transistor, punchthrough margin, is achieved with FinFET that is crucial to hot carrier program. The NOR Flash memory fabricated with FinFET shows programmed state of 7.2 V under the bias condition of Vgs = 10 V, Vds = 4.0 V, and Vb = -0.5V. Erase is performed at Vgb = 16 V for 10 msec. Under this program/erase conditions, Vth window (sensing margin) more than 3 V, endurance characteristics up to 10^5 program/erase cycling, 4.4 V sensing margin after 10^5 cycle endurance are achieved. In addition, data retention of programmed Vth shift of only 0.6 V at 300 °C for 12 hours is obtained. In spite of the above excellent performance of FinFET, FinFET cell has an inherent demerit of lower coupling ratio than planar one. However, the elongated channel

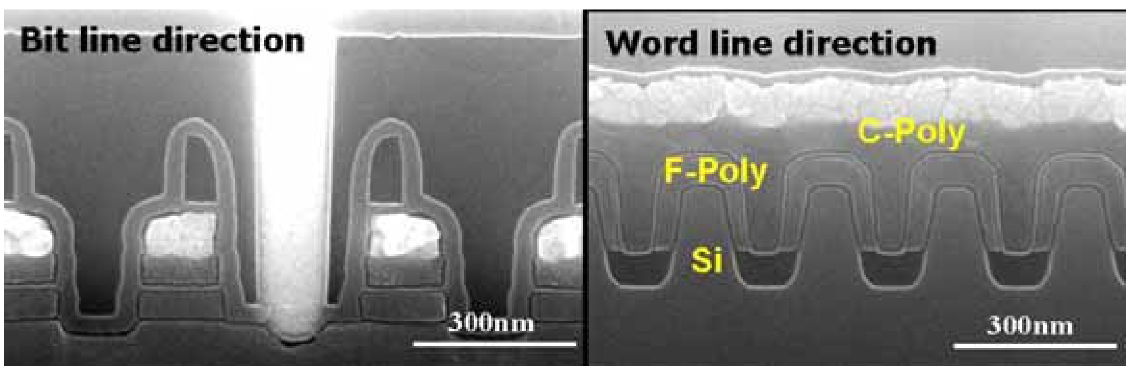

Figure 12. FinFET NOR Flash cell transistor

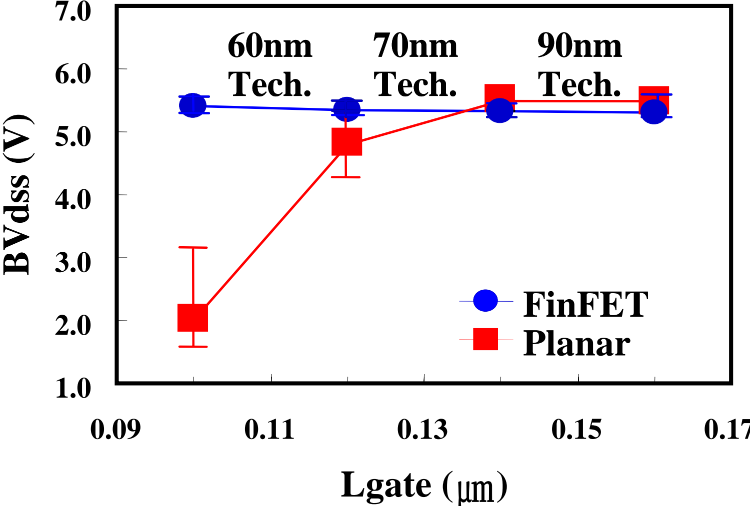

Figure 13. FinFET NOR Flash cell transistor is free from the transistor punchthrough down to 60 nm technology node that is expected to use 100 nm gate length.

width has a significant benefit on the erase Vth distribution. The coupling ratio variation, that is one of the key factors of erase Vth variation, can be dramatically reduced due to the almost same effective active width along the scaling in FinFET structure. As the cell scales down, FinFET would be an essential transistor for NOR flash. This feature would surpass the demerit of coupling ratio lowering.

FinFET SONOS Flash memory that is believed as a successor of floating gate NAND Flash is shown in Fig. 14. Combining FinFET and SONOS scheme, the issues such as interference between floating gates and worst on-cell current can be eliminated effectively. Fabricated FinFET SONOS cells show very uniform Vth distribution compared to floating gate flash cells that is smaller than 0.7 V. This result is owing to insensitivity of active width variation by widening effective channel width with tall fin structure and no coupling interference nature of SONOS device. Vth distributions of initial, programmed, and erased cells on chip are excellent without abnormal tail bits after program and erase operation. Table 1 shows the comparison of several FinFET SONOS schemes showing the excellence of body-tied FinFET SONOS.

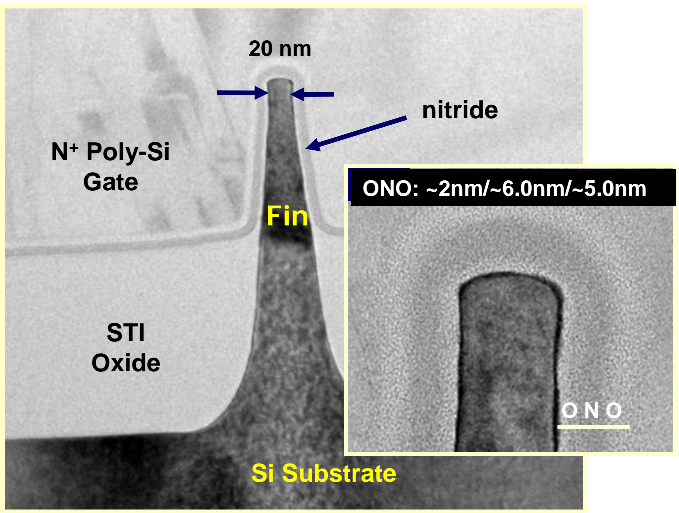

Figure 14. FinFET SONOS Flash cell transistor

TABLE I. Comparison of FinFET SONOS. SONOS FinFET fabricated on Bulk Si shows the best performance among the FinFET SONOS memories.

	IEDM, 2003 [1]	VLSI, 2004 [2]	IEDM, 2004
Structure [1] P. Xuan, *et al*, IEDM 2003 [2] M. Specht, *et al*, VLSI 2004	SOI FinFET	SOI FinFET	Bulk FinFET
Gate length	350 nm	30 nm	50 nm
Fin Width	30 nm	20 nm	30 nm
ONO	3nm/6.8nm/4.8nm	3nm/4nm/4.8nm	~2nm/~6nm/~5nm
ΔV_{TH}	~2.0V	~1.0V	*>4.5V*
Program speed	~2.5V @ 10ms/10V	–	*4.1V @1μs/12V*
Erase speed	2.3V @ 10ms/-12V	–	*4.0V @50μs/-12V*
Retention	>1.4V @ 10yrs	>1.1V @ 10yrs	*>2.4V @ 10yrs*
Endurance	> 10^5	> 10^3	> 10^4

McFET (Multi channel FET)

As an extended technology of FinFET, we successfully developed McFET that has, using conventional CMOS silicon processes, twin fins doubling the fin numbers in the same area as shown in Fig. 15. McFET is fabricated without any patterning limit, while it is hard to have narrower pitch than the design rule due to the patterning limit of lithography tools. In addition, since McFET has the thin fin only at the channel regime without hurting the source and drain contact active area, any parasitic resistance issues do not arise. Using McFET structure, drive current is increased 4~5 times with excellent short channel effect immunity. Fig. 16 shows that both of the n-ch and p-ch MOSFETs with McFET scheme are excellent in the transistor characteristics such as DIBL (Drain Induced Barrier Lowering), SS (Subthreshold Swing), and drive current. In addition, using mid-gap work function TiN metal gate to the thin FinFET, symmetric threshold voltage is obtained in both n-ch and p-ch MOSFETs. Fig. 17 shows that the McFET characteristics are uniform across the 8 inch wafer representing the uniform thin fin formation. We applied the McFET scheme to the 80 nm high performance 6T SRAM cell to successfully obtain the excellent Static Noise Margin of 310 mV and 350 mV at 0.8 V

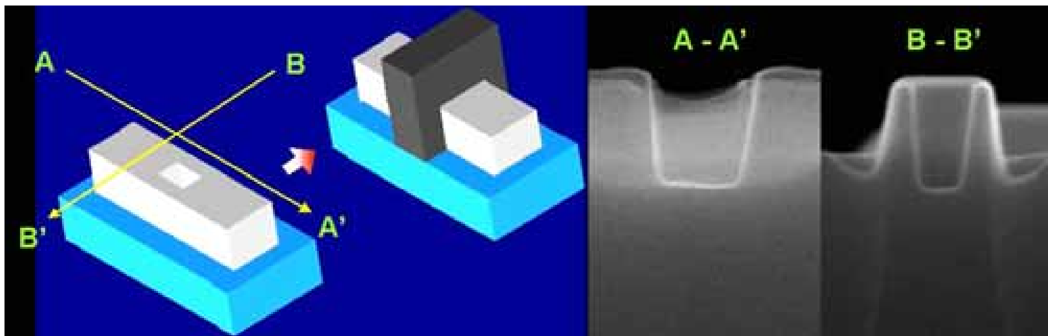

Fig. 15 Schematic view and SEM images of McFET

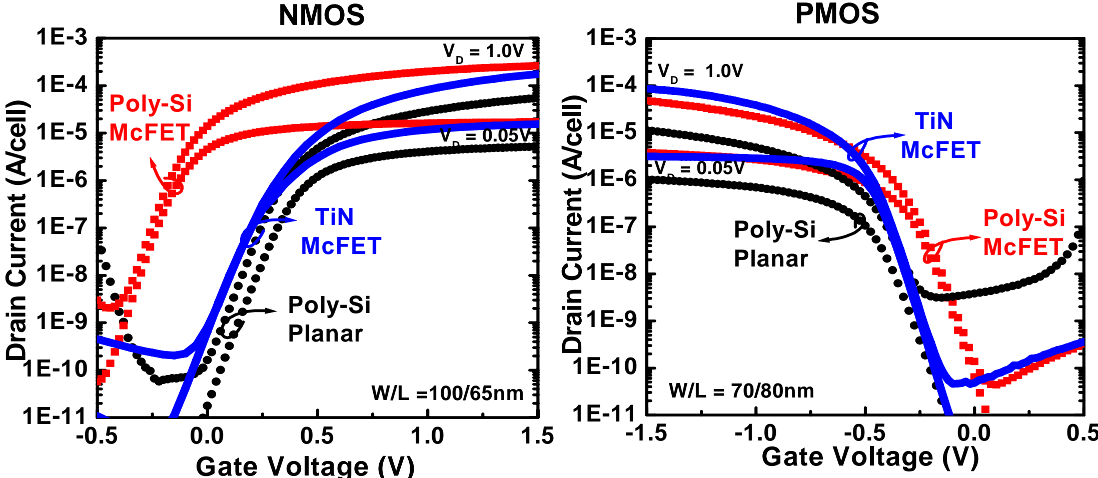

Fig. 16 n-ch and p-ch McFETs show excellent DIBL, subthreshold swing, and large drive current for both N[+]poly-Si and TiN metal gates. Using TiN gate to thin Si-body McFET, symmetric low enough Vtn and Vtp are obtained.

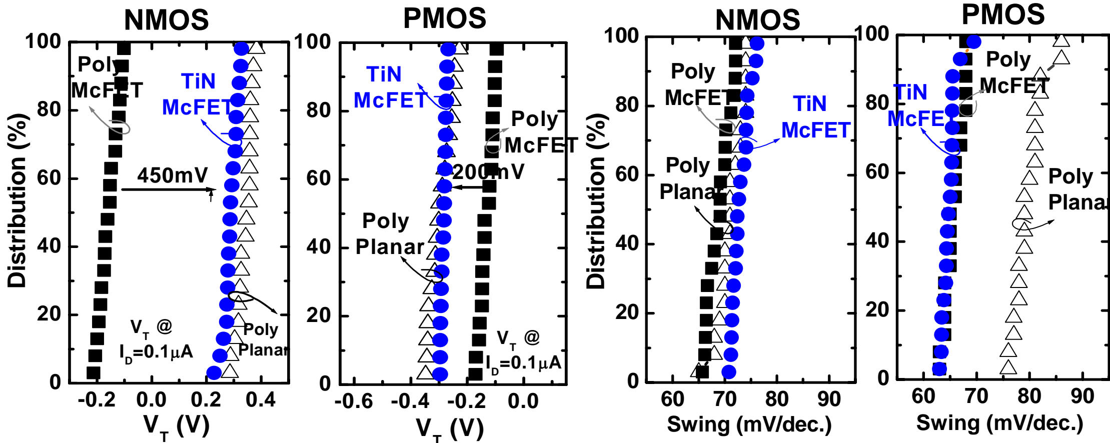

Fig. 17 TiN gate McFET shows optimal threshold voltages for both n-ch and p-ch MOSFETs as well as low and uniform subthreshold swing.

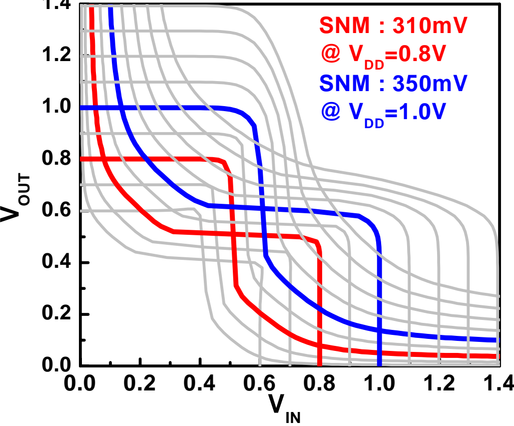

Fig. 18 The operation of SRAM cell inverter made by n-ch and p-ch McFETs show extremely large static noise margin of 310 mV even at Vdd = 0.8 V.

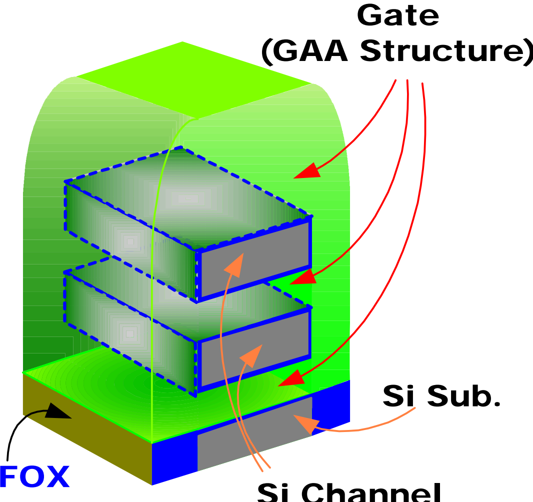

Fig. 19 Schematic diagrams of MBCFET. Multiple silicon channels are stacked to enhance the current drivability. Gate is surrounding the channel Si bridges resulting in excellent gate controllability.

and 1.0 V, respectively as shown in Fig. 18. This SNM is superior to the one of planar SRAM cell that is about 170 mV.

MBCFET (Multi-Bridge Channel MOSFET)

In this section, we introduce a novel MBCFET fabricated on bulk silicon substrate. MBCFET have several benefits originated from its vertically stacked surrounding gate structure as shown in Fig. 19. First of all, the current improvement far exceeds the gate capacitance increase due to the mobility enhancement that is resulted from the inversion charge volume inversion and reduced vertical electric field in the channel region. Secondly, it has an excellent immunity to the short-channel effect down to 30 nm gate length with 2 nm thick gate oxide and without any halo implantation, that suppresses off-leakage current and enables the MBCFET to operate at low Vdd and low Vt, resulting in mobility enhancement. Thirdly, its area efficiency is excellent stacking the channels vertically, that makes it possible to increase the driving current without any junction capacitance increment. Lastly, all of its gate lengths are same. It cannot be realized without our newly developed damascene gate process.

Similar to other multi-channel transistors, however, our early developed MBCFET also had the threshold voltage control issue due to the ultra thin silicon bridge thickness causing very low threshold voltage with large off-leakage current. While gate work function engineering is required for CMOS application, to simplify and improve the manufacturability of the dual-metal gate process, we introduce further developed a highly manufacturable CMOS MBCFET process including a simple elevated flat source/drain and single-metal gate process that is shown in Fig. 20. The multi-bridge-channels are completely surrounded by the gate, while typical gate oxide and Si channel thicknesses are 2.2nm and 17nm, respectively. Fig. 21 shows that the MBCFET with two 17nm thick silicon bridges has excellent symmetry of n-ch and p-ch MBCFETs so that CMOSFET is realized with the single metal gate at the thin Si bridge MBCFETs. In addition, the n-ch

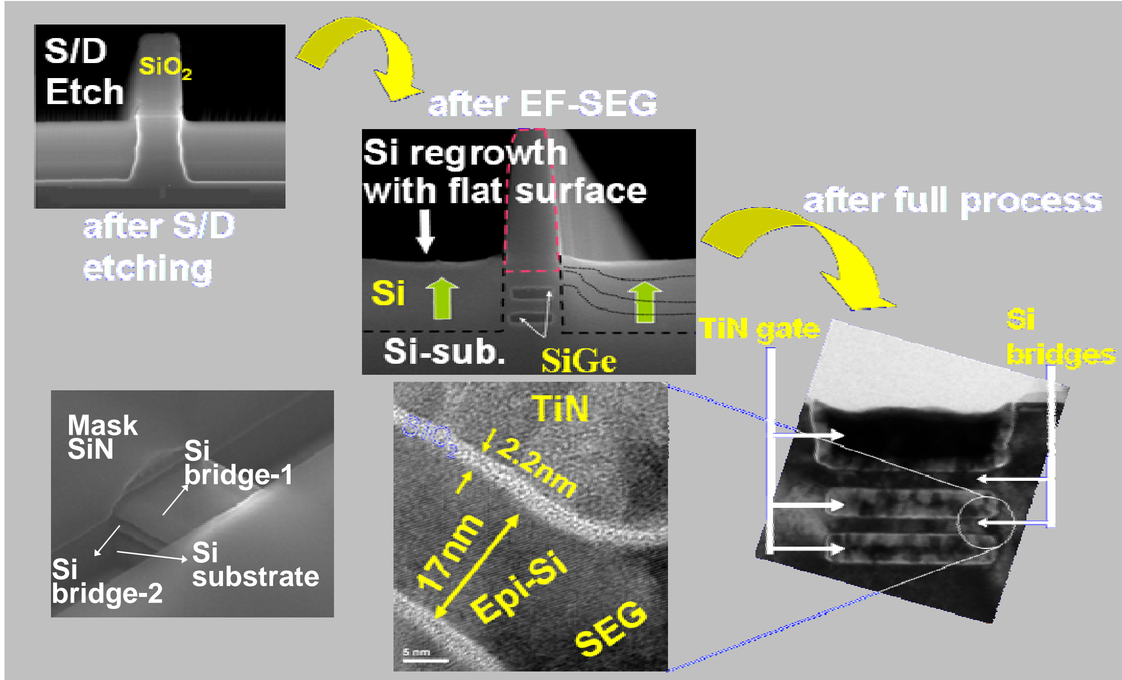

Fig. 20 SEM images of MBCFET. TiN gate is surrounding the two silicon channel bridges. Si channel thickness is 17nm and gate oxide is 2.2nm thick SiO_2.

and p-ch MBCFETs show excellent transistor characteristics of subthreshold swing less than 70 mV/dec and DIBL less than 35 mV/V even at the small gate length of 25 nm and 30nm for n-ch and p-ch MBCFETs, respectively. The drive current was 2.65 mA/um and 1.44 mA/um at V_{DD} =1.0 V for n-ch and p-ch MOSFETs, respectively. These are the MOSFET driving currents far exceeding the expectation of ITRS roadmap2003.

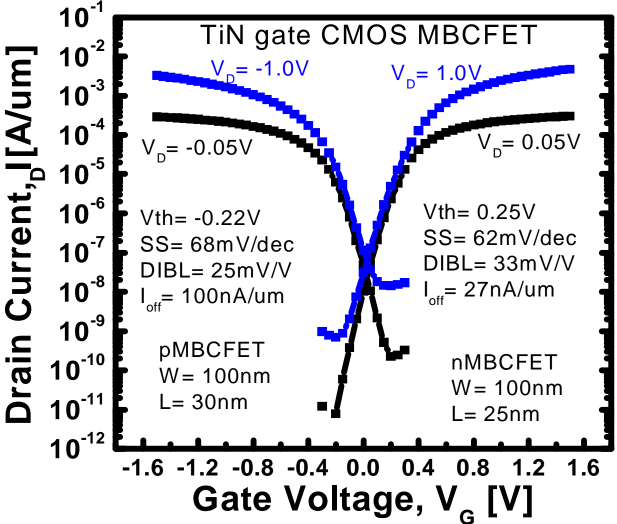

Fig. 21 Symmetric threshold voltage is achieved with mid-gap TiN gate. DIBL and SW are extremely low for both n-ch and p-ch MBCFETs even at the gate length of 25nm.

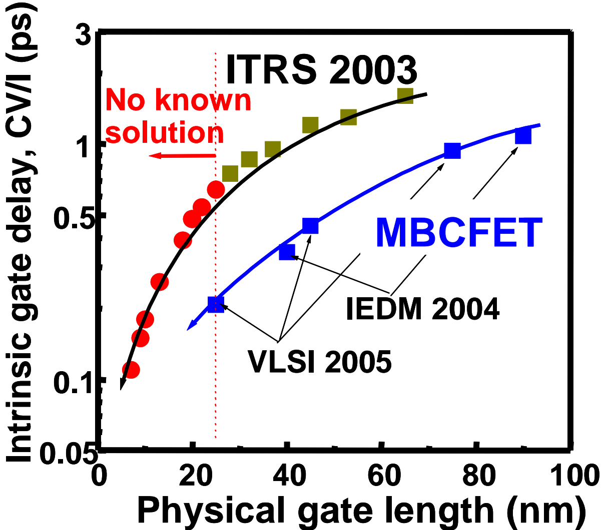

Fig. 22 MBCFET is a breakthrough device to overcome the scaling limit far exceeding the ITRS expectation.

Fig. 22 compares the propagation delay prediction of an inverter to the ITRS roadmap prediction. Even with the gate length of 50 nm, we could meet the goal that is predicted without any known solution to achieve. Moreover, with 25 nm gate length, the requirement of propagation delay for 2013 is achieved with our MBCFET. This result is obtained due to the mobility enhancement effect of surrounding gate and the inversion charge volume inversion effect of ultra-thin Si channel scheme of the MBCFET as shown in Fig. 23.

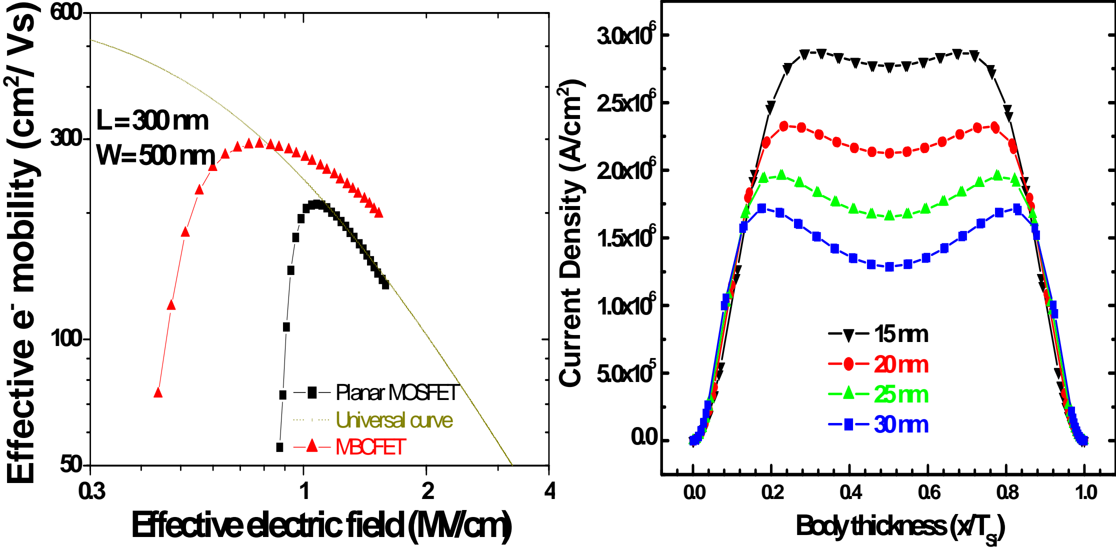

Fig. 23 Using thin silicon bridges and surrounding gate in MBCFET, benefits such as volume inversion and mobility enhancement are realized enhancing the circuit performance.

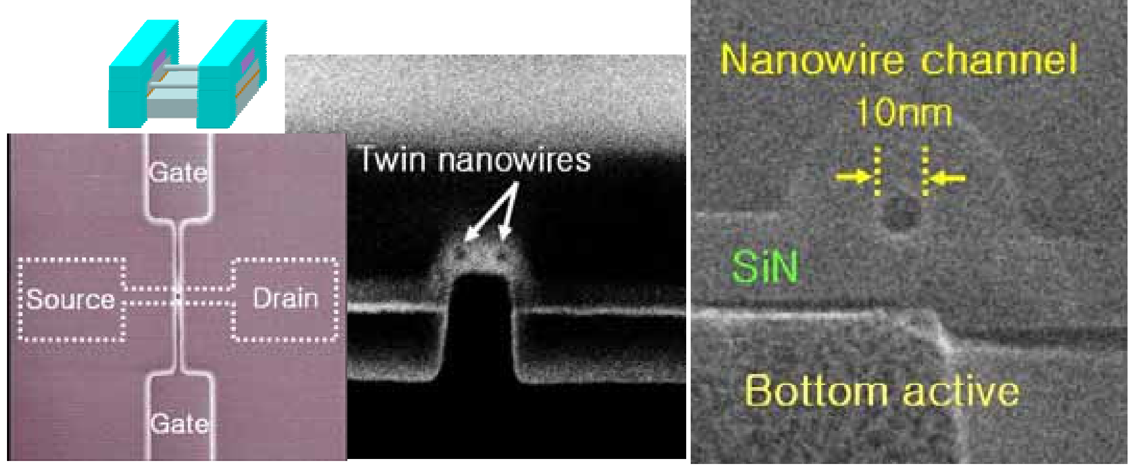

Fig. 24 Top view and cross sectional SEM images of Si nanowire with d=10nm and damascene-gate Lg=30nm.

Twin Silicon Nanowire MOSFET (TSNWFET)

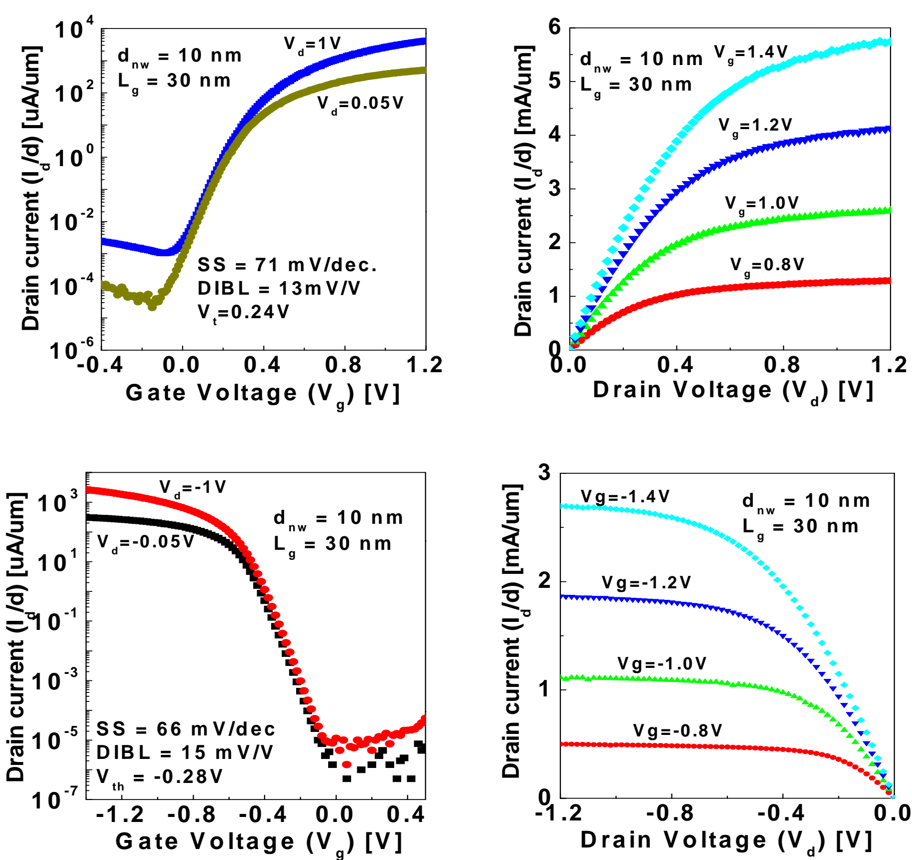

Fig. 22 Excellent SS and DIBL for both n-ch and p-ch TSNWFETs with symmetric Vtn = 0.24 V and Vtp = -0.28 V using mid-gap TiN gate and thin Si nanowire of d = 10 nm.

As transistor scaling approaches to the end of technology roadmap, various new-concept transistors have been reported as a candidate mentioned above. Si nanowire transistor (SNWT) has been focused among those new transistors due to its improved transport property and CMOS process compatibility (25-27). Fig. 24 shows our newly developed high-performance gate-all-around (GAA) twin SNWFET (TSNWFET) fabricated on bulk Si wafer with conventional CMOS processes eliminating the process difficulties and unexpectedly low current drivability of previous works (16).

We could confirm that the gate-all-around (GAA) the silicon nanowire channel fabricated on bulk Si wafer using self-aligned damascene-gate process with TiN metal gate let us achieve the increased transistor drive current as well as excellent subthreshold swing and DIBL with negligible threshold voltage roll-off down to 30nm gate length. This highly manufacturable MOSFETs using silicon nanowire of 5nm radius, namely TSNWFETs show 2.64 mA/μm and 1.11 mA/μm at Vd=Vg=1V, Lg=30nm for n-ch and p-ch, respectively, while the transistor width is counted d=10nm as shown in Fig. 25. These achievements far exceed the ITRS roadmap requirements without any help of emerging research materials.

Summary

We introduce newly developed nanoscale CMOS transistors based on silicon technology to overcome the scaling limits such as area, physics, lithography, etc. For the scaling od planar transistors down to 50 nm, RCAT, PiFET, and Twin SONOS Memory cell transistors are developed. As the scaling of transistors is required further below 50 nm, 3 dimensional structure transistors such as FinFET, McFET, MBCFET, and TSNWFET are newly developed to overcome the physical scaling limits. Using these technologies, with nanotechnology implementation, we believe that the Si based CMOS transistor can be scaled down to 10nm with manufacturability and reliability.

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