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(54) **MULTI-FIN DEVICE AND METHOD OF MAKING SAME**

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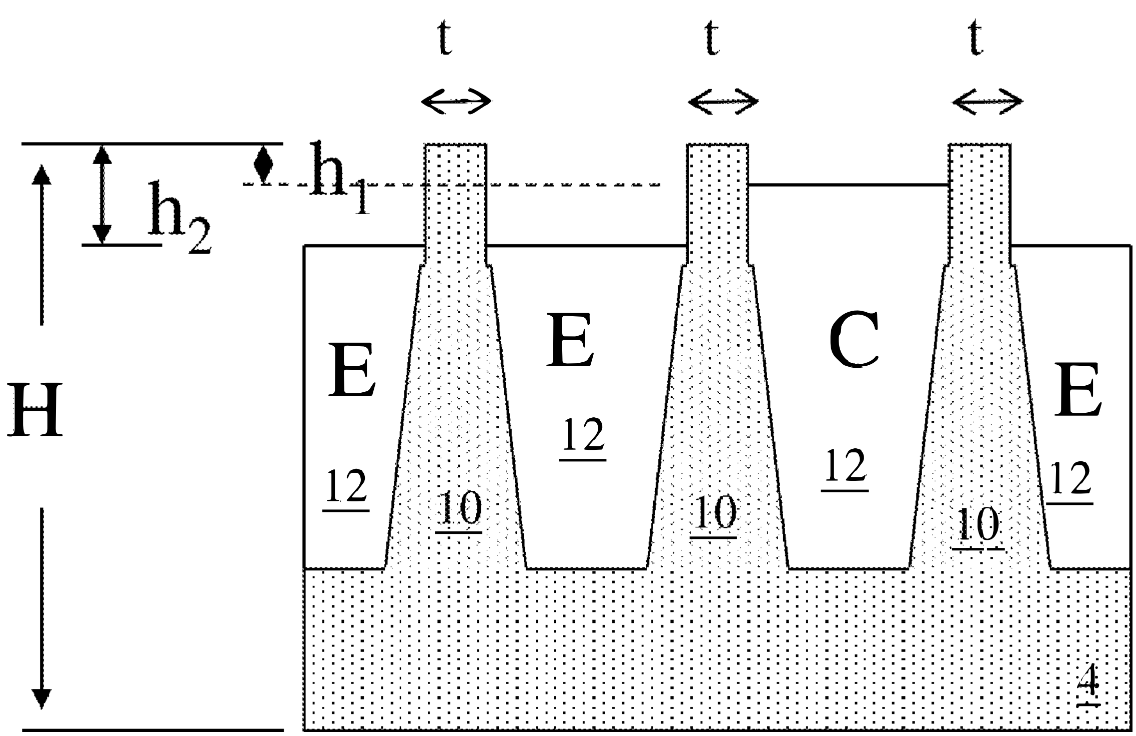
(57) **ABSTRACT**

A multiple-fin device includes a substrate and a plurality of fins formed on the substrate. Source and drain regions are formed in the respective fins. A dielectric layer is formed on the substrate. The dielectric layer has a first thickness adjacent one side of a first fin and having a second thickness, different from the first thickness, adjacent an opposite side of the fin. A continuous gate structure is formed overlying the plurality of fins, the continuous gate structure being adjacent a top surface of each fin and at least one sidewall surface of at least one fin. By adjusting the dielectric layer thickness, channel width of the resulting device can be fine-tuned.



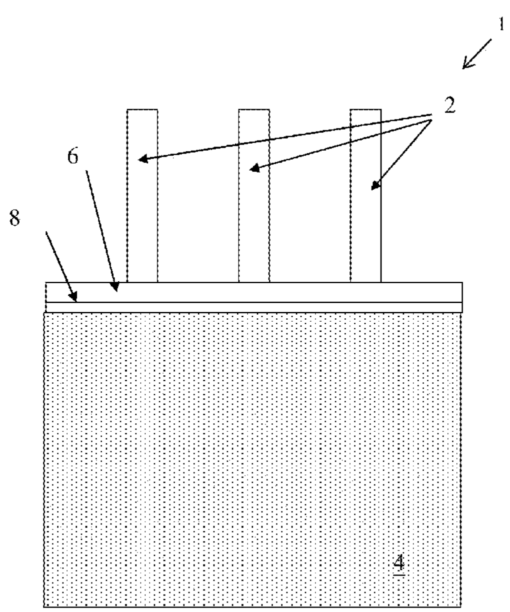


FIG. 1b

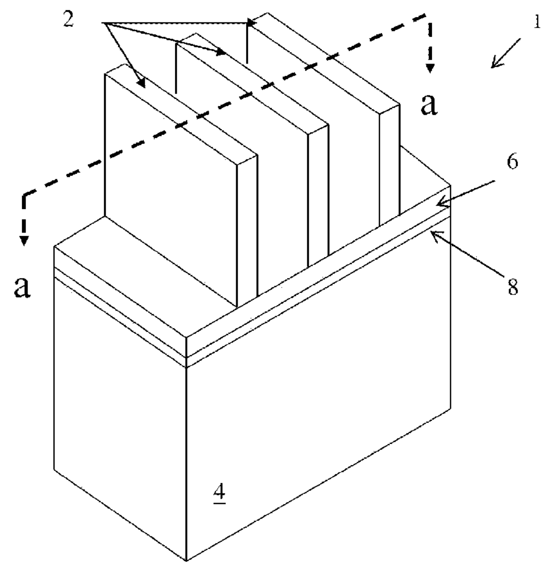


FIG. 1a

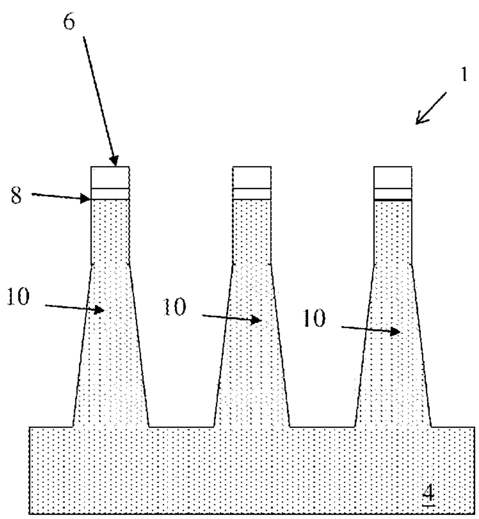


FIG. 2b

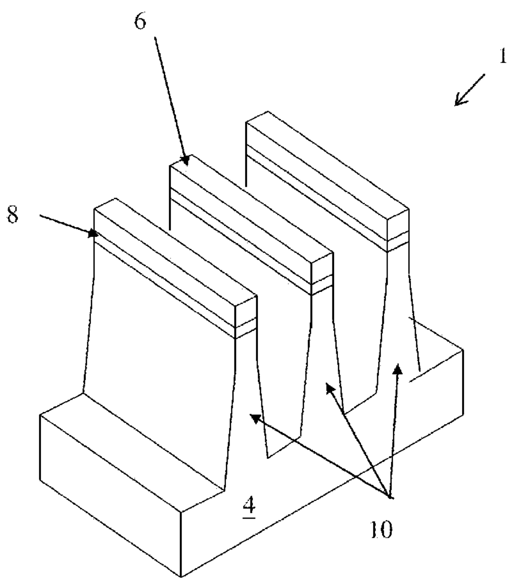


FIG. 2a

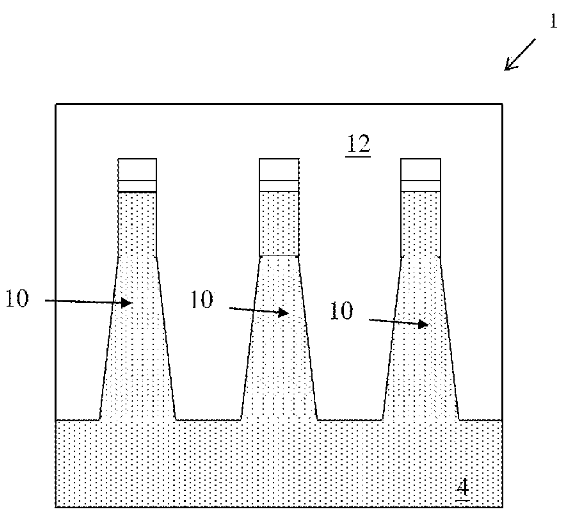


FIG. 3b

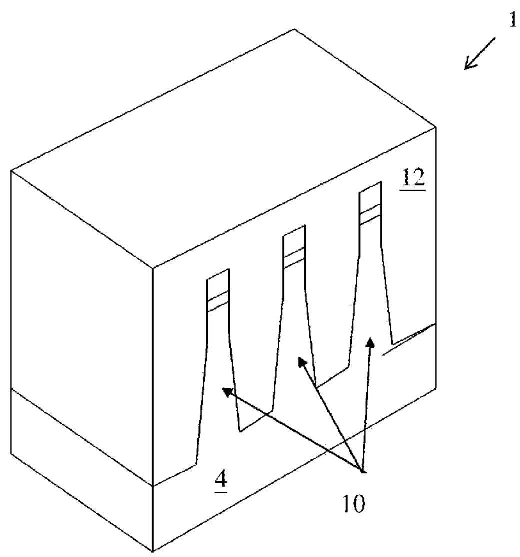


FIG. 3a

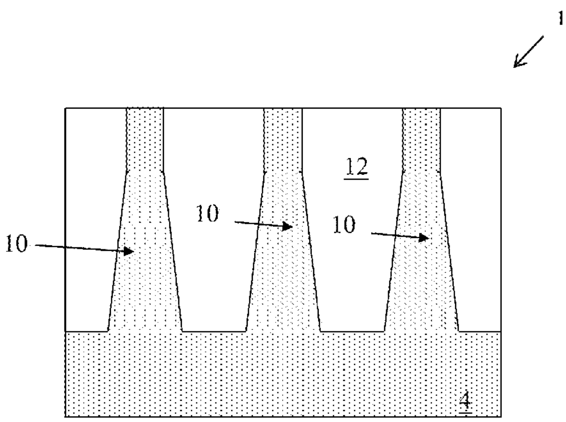


FIG. 4b

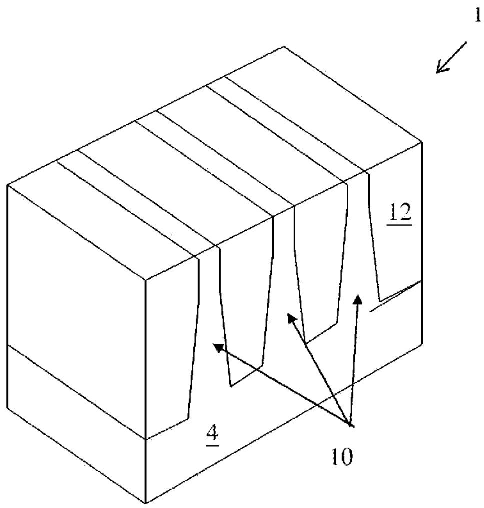


FIG. 4a

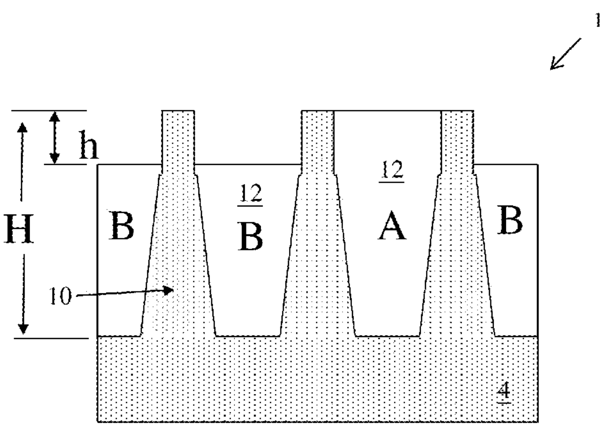


FIG. 5b

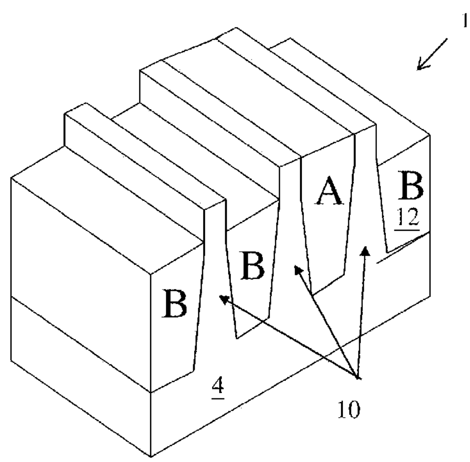


FIG. 5a

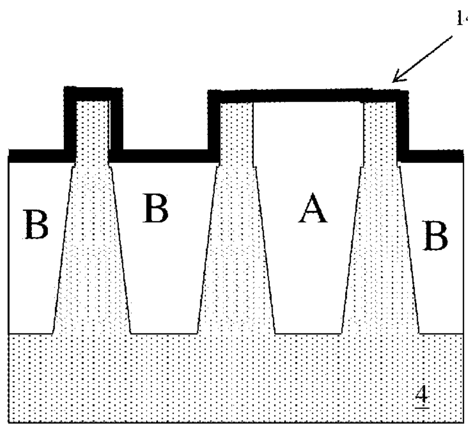


FIG. 6b

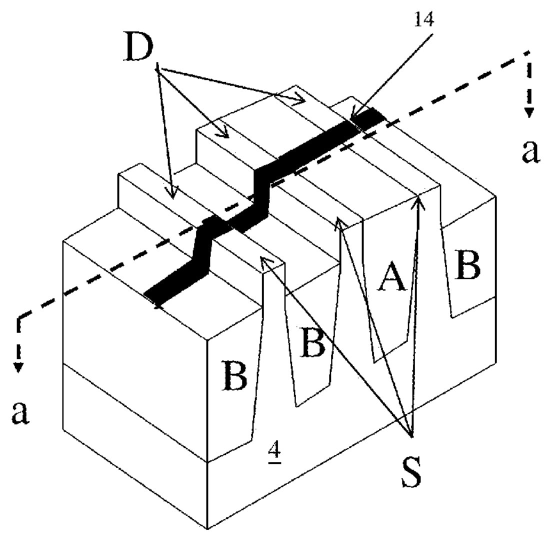


FIG. 6a

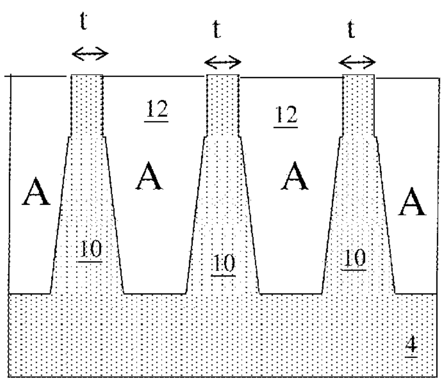


FIG. 6c

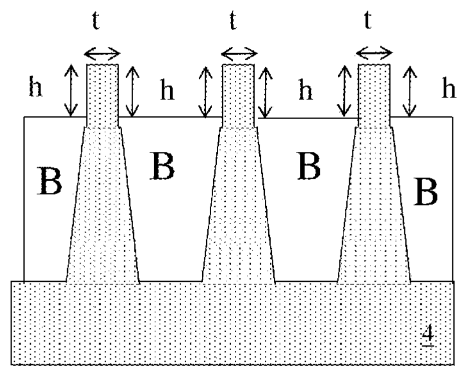


FIG. 6d

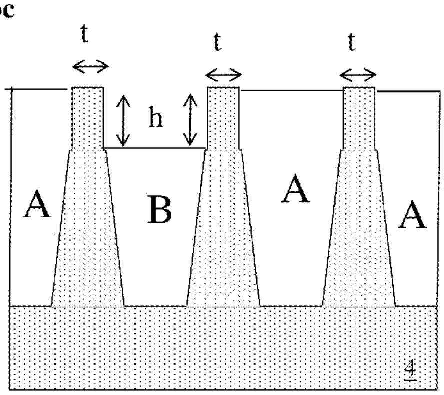


FIG. 6e

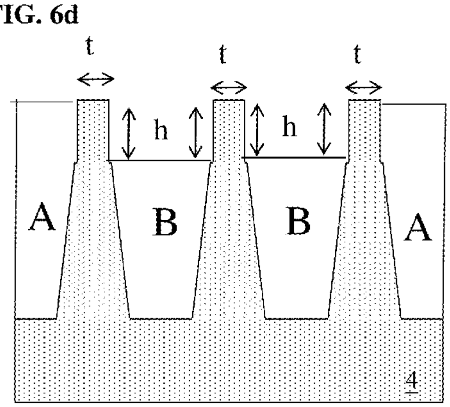


FIG. 6f

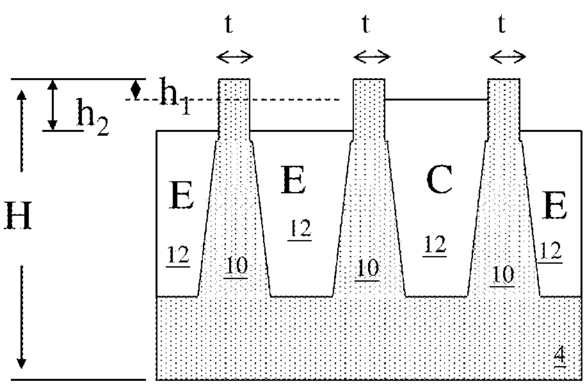


FIG. 7b

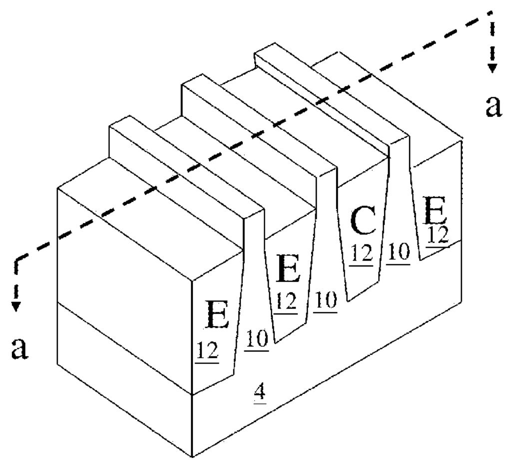


FIG. 7a

MULTI-FIN DEVICE AND METHOD OF MAKING SAME

BACKGROUND

[0001] The so-called Fin field effect transistor (FinFET) device is becoming increasingly popular for high performance, low dimension integrated circuits. Because the gate wraps around the channel region on three sides, FinFETs provide excellent channel control with small critical dimensions. On the other hand, the very nature of the FinFET structure makes it difficult to adjust or tune the channel width of a typical FinFET device. Since various device performance parameters, such as driving current (I_{Dsat}) are related to channel width, it is disadvantageous that channel width cannot be readily tuned or adjusted. What is needed then, is a FinFET structure and methods of making same that overcome the shortcomings in the conventional arts.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0003] FIGS. **1***a*-**6***b* illustrate various stages in the manufacture of an embodiment 1;

[0004] FIGS. **6***c*-**6***f* illustrate alternative approaches to adjusting dielectric layer thickness in an embodiment; and

[0005] FIGS. **7***a*-**7***b* illustrate an alternative embodiment of the structure illustrated in FIGS. **6***a* and **6***b*, respectively.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0006] FIG. **1***a* illustrates, in perspective view, an intermediate stage in the manufacture of a Fin field effect transistor (FinFET) device **1**. FIG. **1***b* illustrates the structure in cross-sectional view along the line indicated as a-a in FIG. **1***a*. In the illustrated embodiments, FinFET **1** will extend across several fins, and more specifically three fins, as will be explained in greater detail below. In the intermediate stage of manufacture illustrated in FIG. **1***a*, a patterned photo-sensitive layer **2** has been formed on a substrate **4**. More precisely, patterned photo-sensitive layer **4**, such as a photoresist or the like, is formed atop hard mask **6**, which in turn is atop pad oxide **8**, which in turn is atop substrate **4**. Hard mask **6** may be silicon nitride, silicon oxynitride, or the like. Pad oxide layer **8** may be silicon oxide and their formations are well known.

[0007] Substrate **4** may be a bulk substrate such as a bulk silicon wafer. Alternatively, substrate **4** may be simply a top semiconductor layer of a compound wafer, such as a silicon-on-insulator substrate. In yet other embodiments, substrate **4** may be either a bulk substrate or a top layer of a compound wafer comprising Ge, SiGe, a III-V material such as GaAs, InAs, a II-VI material such as ZeSe, ZnS, and the like, typically epitaxially grown. It is believed the III-V or II-VI materials may be particularly advantageous for forming illustrative devices because of the beneficial strain properties that can be derived from using III-V or II-VI properties, such as InAs, ZnS, and the like.

[0008] As illustrated in FIGS. **2***a* and **2***b* (wherein FIG. **2***a* continues the perspective view and FIG. **2***b* continues the cross-sectional view of FIGS. **1***a* and **1***b*, respectively), the pattern of patterned photo-sensitive layer **4** is transferred into hard mask **6**, pad oxide **8**, and substrate **4** using well known etching processes the details of which are not necessary for understanding the invention and hence are not repeated herein. During this pattern transfer process, patterned photo-sensitive layer **2** may be entirely consumed as indicated by FIGS. **2***a* and **2***b*. In some embodiments, patterned photo-sensitive layer **2** is not entirely consumed, but rather remaining portions of patterned photo-sensitive layer **2** are removed using, e.g., an oxygen plasma or so-called ash process. The resulting structure includes a plurality of fins **10** formed in substrate **4**. Each fin of the plurality of fins **10** has a sidewall, a portion of the sidewall being substantially orthogonal to a major surface of the substrate **4**, and a lower portion of the sidewall being non-orthogonal to the major surface of the substrate. These fins **10** serve as the fin structure for the to-be-formed FinFET device **1**. In some embodiments substrate **4** is etched to a depth, meaning fins **10** are formed to a height, of from about 40 nm to about 80 nm. In one specific embodiment, fins **10** are formed to a height of about 60 nm.

[0009] Turning now to FIG. **3**, an oxide layer **12** is blanket deposited on device **1**. Oxide layer **12**, sometimes referred to as shallow trench isolation oxide or just shallow trench isolation, may be deposited by, e.g., a chemical vapor deposition (CVD) process, by a spin-on-glass process, or the like using process steps that are known to those skilled in the art. Optionally and prior to forming oxide **12**, a thermal oxidation of fins **10** may be undertaken to repair damage that occurred to the sidewalls during the etching step (illustrated in FIGS. **2***a* and **2***b*).

[0010] A CMP step is employed to thin oxide layer **12** back to the level of the tops of fins **10**, as illustrated in FIGS. **4***a* and **4***b*. Note that patterned hard mask **6** and patterned pad oxide **8** are removed in the CMP step. The process parameters for a CMP step are well known in the art and hence are not repeated herein for the sake of brevity and clarity. In some embodiments, after the CMP process, the step of forming a plurality of fins **10** on a substrate **4** may further comprise a process selected from the group consisting essentially of etching fins into a substrate and epitaxially growing fins on a substrate, and combinations thereof. Thus, the plurality of fins may be selected from the group consisting essentially of an epitaxial material, the substrate material, and combinations thereof.

[0011] FIG. **5***a* illustrates the next stage in the manufacturing process, wherein oxide layer **12** is further thinned back. Oxide layer **12** can be thinned back in a variety of ways. In one embodiment, oxide layer **12** is thinned back by a diluted hydrofluoric acid (DHF) treatment or a vapor hydrofluoric acid (VHF) treatment for a suitable time. Note in particular that oxide layer **12** is selectively thinned back, as illustrated by the notations A (indicating portions of oxide layer **12** that have not been thinned back) and B (indicating portions of oxide layer **12** that have been thinned back). This selective thinning can be accomplished by covering portion A of oxide layer **12** with a protective layer, such as a photoresist layer, during the etch back process.

[0012] In the embodiment illustrated in FIG. **5***b*, fin **10** extends a distance H above the surface of substrate **4** and extends a distance h above the thinned back portions B of oxide layer **12**. In illustrative embodiments, $1/4 < h/H < 1/3$ for the B regions. It is believed that this ratio of the extension of fins **10** above oxide layer **12** in the B regions provides for a desirable channel width, as will be explained further below.

[0013] Next, a single continuous gate structure is formed over the three fins **10**, as illustrated in FIGS. **6***a* and **6***b*. Also illustrated in FIG. **6***b* is the formation of source regions S and drain regions D within respective fins **10**. In one embodiment, forming source and drain regions includes implanting dopants into the respective fins. In another embodiment, forming source and drain regions comprises etching fins into a substrate and epitaxially growing source and drain regions on a substrate. One skilled in the art will recognize the multiple process steps for forming gate structure **14**, which includes formation and patterning of a gate dielectric and formation and patterning of a gate electrode. Such details are not necessary for an understanding of the present invention and the gate dielectric and electrode are referred to collectively herein as the gate structure **14**. Likewise, the details of forming doped source and drain regions are known and are the details are not repeated herein for the sake of clarity. In this instance, a first metal layer may be continuous and overlying the three source regions to form source region of one finFET device. Further, a second metal layer may be continuous and overlying the three drain regions to form drain region of one finFET device.

[0014] Those of skill in the art will recognize that channel length and channel width are two significant parameters for a transistor, including for a finFET device such as illustrative device **1**. Channel length is substantially equal to the distance between the source S and drain D regions. In the illustrated embodiment, the use of multiple fins and particularly multiple fins having varying heights as a result of the varying thickness of oxide layer **12** between the fins, has no impact on channel length. In other words, the different oxide layer **12** thicknesses between the fins does not impact the distance between the source S and drain D, or the channel length. Channel length impacts such transistor performance as, e.g., switching speed.

[0015] Channel width also impacts device performance, such as the driving current of the device. As an example, I_{DSAT} can be fine-tuned by adjusting the channel width. By varying the thickness of oxide layer **12** between fins, and hence varying the height of fins **10** above the oxide layer, the overall channel width of the resulting finFET can be modified. This is explained in greater detail with regard to FIGS. **6***c* through **6***f*.

[0016] Referring first to FIG. **6***c*, an end-point embodiment is illustrated in which oxide layer **12** is not etched back at all between fins **10**. In this embodiment, the total channel width (after gate structure **14** is formed) will be equal to the thickness t of the fins **10**. In this instance, with three fins **10** ganged together to form one finFET device (i.e. with a single gate structure **14** continuous and overlying the three fins **10** such as illustrated in FIG. **6***b*), the total channel width would be equal to 3t. This structure is effectively equivalent to a planar transistor device. By contrast, FIG. **6***d* illustrates the other end-point embodiment, in which oxide layer **12** is uniformly etched back between all fins **10**. In this embodiment, the total channel width will be equal to the thickness t of each fin plus 2 times the height h of each fin (because the gate structure will overlie both sidewalls of each fin, each having a height h and the top of each fin, having a thickness t). In the illustrated embodiment, the channel width would be equal to 3t+6h. While such a structure might be beneficial in that it is easy to lay out a three fin structure, e.g., in an equivalent area to a planar transistor of similar characteristics, the multiple fin structure might have excessive drive current which can negatively impact desired performance.

[0017] FIG. **6***e* illustrates another embodiment structure wherein drive current is modified by having oxide layer **12** of varying thickness between the fins. Note that in the embodiment of FIG. **6***e*, oxide layer **12** is etched back between one pair of fins **10** (the leftmost and center fin), but is not etched back between the other pair of fins **10** (the rightmost and center fin), for example. In this case, the drive current of the resulting structure will be 3t+2h, as only two sidewalls of the fins are exposed for gate structure **14** (not shown, but illustrated in FIG. **6***b*) to overlie.

[0018] FIG. **6***f* illustrates yet another embodiment, wherein gate oxide **12** is etched back between both pairs of fins, but not on the outer edges of the outside fins. In this illustrated example, the total channel width is equal to 3t+4h. One skilled in the art will recognize various other configurations that can be employed to fine tune the channel width by adjusting the oxide layer **12** thickness bordering the various fins **10**.

[0019] In the embodiments illustrated in FIG. **6** (which includes FIGS. **6***a* through **6***f*), oxide layer **12** is either etched is some regions (regions B) or remains totally un-etched in other regions (regions A). In other embodiments, further fine tuning can be obtained by etching back certain regions of oxide layer **12** by a first amount and etching back other regions of oxide layer **12** by a second greater amount. FIGS. **7***a* and **7***b* illustrate one such embodiment.

[0020] FIG. **7***a* illustrates in perspective view and FIG. **7***b* illustrates in cross sectional view an embodiment in which the portions of oxide layer **12** denoted as C as protected (e.g., covered with a photoresists, a hard mask, a sacrificial layer, or the like) during a first etch back step in which portions of oxide layer **12** denoted as E are partially etched back. In a next process step, portions C are exposed and oxide layer **12**, including portions C and E, is further etched back to the levels shown in FIGS. **7***a* and **7***b*. In this case, the left most fin **10** extends a height of h_2 above oxide layer **12** whereas the two rightmost fins extend a height h_2 above oxide layer **12** on their respective outer sidewalls (because oxide layer **12** is at a thickness of "E" on the outer regions of the fins) and extend a lesser height of h_1 above oxide layer **12**, having a thickness of "C" along their respective inner sidewalls. Assuming fins **10** have a thickness of t, the total channel width for the embodiment illustrated in FIG. **7** is $3t+4\ h_2+2\ h_1$.

[0021] Although the present embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. As but a few examples, although a finFET device extending across three fins is shown, the teachings of the present disclosure would apply equally to a finFET extending across two fins, or extending across four or more finds. Likewise, other multi-gate devices, such as w-gate devices, omega-gate devices, and the like are within the contemplated scope. Additionally, even further fine tuning of channel length can be obtained by extending the above described two etch back process (FIG. **7**) to a three etch back process wherein oxide layer **12** could be three different heights, resulting in fins with up to three different sidewall fin heights. This teaching could be further extending to four or more different oxide layer thicknesses by adding additional etch back and masking steps. It is important to note that the present teaching would apply equally to fins that are epitaxially grown as it does to fins that are etched into a substrate.

[0022] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A device comprising:

a substrate;

a plurality of fins formed on the substrate;

source and drain regions formed in the respective fins;

a dielectric layer formed on the substrate, the dielectric layer having a first thickness adjacent one side of a first fin and having a second thickness, different from the first thickness, adjacent an opposite side of the fin; and

a continuous gate structure overlying the plurality of fins, the continuous gate structure being adjacent a top surface of each fin and at least one sidewall surface of at least one fin.

2. The device of claim **1** wherein the device is a finFET device.

3. The device of claim **1** comprising:

a first fin having a first sidewall covered by the dielectric layer and a second sidewall that extends above the dielectric layer;

a second fin having both a first and second sidewall that extends above the dielectric layer; and

wherein the gate structure conformally overlies the second sidewall of the first fin and the first and second sidewalls of the second fin.

4. The device of claim **1** wherein each fin of the plurality of fins has a top surface having a thickness t and at least one sidewall having a height h above the dielectric layer, wherein a channel is formed in the plurality of fins, the channel having a channel width defined by sum of the thicknesses t and the sum of the heights h.

5. The device of claim **1** wherein at least one fin of the plurality of fins has two sidewalls extending above the dielectric layer.

6. The device of claim **1** includes three or more fins.

7. The device of claim **1** wherein the first thickness of the dielectric layer is equivalent to a height above the substrate of the fin.

8. The device of claim **1** wherein the plurality of fins selected from the group consisting essentially of an epitaxial material, the substrate material, and combinations thereof.

9. The device of claim **1** wherein each fin of the plurality of fins a sidewall, a portion of the sidewall being substantially orthogonal to a major surface of the substrate, and a lower portion of the sidewall being non-orthogonal to the major surface of the substrate.

10. A transistor comprising:

a first semiconductor fin in a dielectric layer, the first semiconductor fin having a first sidewall extending a first distance above the dielectric layer, a top surface, and a second sidewall extending a second distance over the dielectric layer;

a second semiconductor fin in the dielectric layer, the second fin having a first sidewall extending the first distance above the dielectric layer, a top surface, and a second sidewall extending the first distance above the dielectric layer;

a gate structure overlying the first and second semiconductor fins, wherein the gate structure contacts the first semiconductor fin on the top surface and at least one sidewall and contacts the second semiconductor fin on the top surface and at least one sidewall;

a source region distributed in the first and second semiconductor fins; and

a drain region distributed in the first and second semiconductor fins.

11. The transistor of claim **10** further comprising a third semiconductor fin in the dielectric layer, the third semiconductor fin having a first sidewall extending the first distance above the dielectric layer, a top surface, and a second sidewall extending the first distance above the dielectric layer.

12. The transistor of claim **10** wherein the second distance is equal to zero.

13. The transistor of claim **10** wherein the gate structure includes a gate dielectric and a gate electrode.

14. The transistor of claim **10** wherein the transistor includes a channel region in the first and second fins and wherein the channel region has a channel width that is equal to the sum of the two top surface thicknesses and the sum of the distances by which the first and second sidewalls of the first semiconductor fin extend above the dielectric layer and the sum of the distances by which the first and second sidewalls of the second semiconductor fin extend above the dielectric layer.

15. A method of forming a transistor comprising:

forming a plurality of fins on a substrate;

forming source and drain regions in the plurality of fins;

forming a dielectric layer between the fins;

adjusting a thickness of the dielectric layer between at least two of the plurality of fins; and

forming a continuous gate structure on the fins and dielectric layer.

16. The method of claim **15** wherein the step of forming a plurality of fins on a substrate comprises a process selected from the group consisting essentially of etching fins into a substrate and epitaxially growing fins on a substrate, and combinations thereof.

17. The method of claim **15** wherein the step of adjusting a thickness of the dielectric layer includes:

covering a portion of the dielectric layer; and

etching back a not covered portion of the dielectric layer.

18. The method of claim **17** further including:

uncovering the covered portion of the dielectric layer.

19. The method of claim **18** further including:

etching back the uncovered portion of the dielectric layer; and

further etching back the not covered portion of the dielectric layer.

20. The method of claim **15** wherein forming source and drain regions includes implanting dopants into the respective fins.

* * * * *