UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

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Case IPR2025-01527
U.S. Patent No. 9,117,909

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# DECLARATION OF PROF. SAYEEF SALAHUDDIN, PH.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 9,117,909

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a. [1.P]: A non-planar transistor, comprising:....................64

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c. [1.b] a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall;........................76

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1. Independent Claim 1..............................................................113

a. [1.P]: A non-planar transistor, comprising:..................113

b. [1.a] a substrate having an active region and an isolation region, wherein the isolation region encompasses the active region;................................................................114

c. [1.b] a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall; ......................121

d. [1.c] a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion; ............................125

e. [1.d] an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench; ......................................................131

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I, Sayeef Salahuddin, hereby declare as follows.

# I. INTRODUCTION

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Ltd. ("TSMC"; "Petitioner") for the above-captioned *inter partes* review (IPR). I am being compensated for my time in connection with this IPR at my standard consulting rate, which is $400 per hour.

2. I understand that this Declaration accompanies a petition for IPR involving U.S. Patent No. 9,117,909 ("the '909 patent") (EX1001), which resulted from U.S. Patent Application No. 14/470,957 ("the '957 application"), filed on August 28, 2014. I understand that the '909 patent alleges a priority date of April 16, 2013. I refer to this date throughout this Declaration.

3. I have been retained by TSMC to study and provide my opinions on the technology claimed in, and the patentability or unpatentability of, claims 1-6 of the '909 patent ("the challenged claims"). This declaration is directed to the challenged claims of the '909 patent, and sets forth the opinions I have formed, the conclusions I have reached, and the bases for each. For purposes of this declaration, I was not asked to provide any opinions that are not expressed herein.

4. In preparing this Declaration, I have reviewed the '909 patent and each of the documents cited herein, in light of general knowledge in the art before April 16, 2013. I am familiar with the technology described in the '909 patent as of

April 16, 2013. I have reviewed and am familiar with the specification of the ’909 patent. I understand that the ’909 patent has been provided as EX1001. I will cite to the specification using the following formats: EX1001, ’909 patent, 1:1-10 (long form) and EX1001, 1:1-10 (short form). These example citations both point to the ’909 patent specification at column 1, lines 1-10.

5. In formulating my opinions, I have relied upon my experience, education, and knowledge in the relevant art. In formulating my opinions, I have also considered the viewpoint of a person of ordinary skill in the art (“POSA”) (i.e., a person of ordinary skill in the semiconductor field, as defined further below in Section VII.C) prior to April 16, 2013. It is my opinion that each of the challenged claims of the ’909 patent is unpatentable for at least the reasons I discuss below.

6. I am over 18 years of age. I have personal knowledge of the facts stated in this declaration and could testify competently to them if asked to do so.

## II. GROUNDS OF UNPATENTABILITY

7. In forming my opinions about the ’909 patent, I have considered the following grounds of unpatentability. Based on my review of the prior art references that form the basis of these grounds, it is my opinion that claims 1-6 of the ’909 patent would have been obvious to a person of ordinary skill in the art (“POSA”) as of April 16, 2013.

| Ground | Basis | Claims | Reference(s) |
|---|---|---|---|
| 1 | § 103 | 1-4, and 6 | Lin and Liaw |
| 2 | § 103 | 5 | Lin, Liaw and Chang |
| 3 | § 103 | 1-3, 5, and 6 | Chang |
| 4 | § 103 | 4 | Chang and Liu |

8. I have been asked to consider how a POSA would have understood the challenged claims in light of the disclosures of the ’909 patent. I also have been asked to consider how a POSA would have understood the prior art references Lin, Liaw, Chang, and Liu. Further, I have been asked to consider and provide my technical review, analysis, insights, and opinions regarding whether a POSA would have understood that the combinations of the prior art references listed in the table above render obvious claims 1-6 of the ’909 patent.

## III. MY BACKGROUND AND QUALIFICATIONS

9. My academic and professional pursuits are closely related to the subject matter of the ’909 patent. I have over 20 years of experience in advanced semiconductor research, especially in device physics, device design, material synthesis, nanoscale fabrication, and testing. My research at the University of California, Berkeley in the aforementioned areas led to more than 100 publications in the most prestigious journals. Based on my education and work experience, I am

well qualified to serve as a technical expert in this matter.

10. I received a Bachelor of Engineering (B.E.) degree in Electrical and Electronics Engineering in 2003 from the Bangladesh University of Engineering and Technology in Dhaka, Bangladesh. I also received a Doctor of Philosophy (Ph.D.) degree in Electrical and Computer Engineering in 2007 from Purdue University in West Lafayette, Indiana.

11. Following my Ph.D. degree, I worked as a Post-doctoral Research Associate at Purdue University. In 2008, I joined University of California, Berkeley as an Assistant Professor and was later promoted to Associate Professor in 2014 and to Professor in 2017.

12. Currently, I am the TSMC Distinguished Chair Professor[1] of Electrical Engineering and Computer Sciences at the University of California Berkeley. My current research interests relate to the following areas: (i) negative capacitance effect in ferroelectric materials and negative capacitance transistors; (ii) thin film ferroelectricity; (iii) spintronics and nanomagnetic logic computing;

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[1] The TSMC Distinguished Chair is an endowed chair at the University of California Berkeley. Chair holders are selected by the Dean of the College of Engineering. TSMC has no say in choosing the holder of the chair, nor does it constitute any obligation of loyalty to or sponsorship from TSMC.

(iv) electrical driven ferromagnetic resonance free from external magnetic field; and (v) two-dimensional semiconductors and quantum tunneling effect in low dimensional materials and devices.

13. I co-directed the ASCENT Center, which is jointly funded by the Semiconductor Research Corporation (SRC), a consortium composed of major semiconductor companies around the world, and the United States Defense Advanced Research Agency (DARPA). I was selected as a member of a panel to advise the U.S. government on advanced semiconductor manufacturing through DARPA. Further, I received the Inventor Recognition Award by the SRC.

14. I was elected a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), the American Physical Society (APS), and American Association for Advancement of Science (AAAS) for my contributions to semiconductor devices. I am a member of the Technical Advisory Board of the Natcast, the operator of the National Semiconductor Technology Center. My work on semiconductor devices was also recognized by the Presidential Early Career Award for Scientists and Engineers by President Barack Obama.

15. In addition, I have consulted for leading semiconductor companies, such as Sandisk Corporation (now part of Western Digital Corporation) on advanced two-dimensional (2D) and three-dimensional (3D) memory design, semiconductor process innovation, and semiconductor fabrication. In this role, I

reviewed process flows, process recipes, lithography, and material integration issues, as well as their impact on the device and system level. Based on my review, I advised Sandisk Corporation on optimizing these areas. Further, I have advised on device reliability issues that may arise from certain semiconductor processing. Additionally, I have consulted for advanced semiconductor companies in the context of Front End of the Line (e.g., transistor level) process integration, where I reviewed process flows, recipes, and material integration issues. Similarly, I have consulted on fin field effect transistor (FinFET) fabrication processes, heteroepitaxy and conformal synthesis of materials for advanced transistor fabrication, and simulation of structures and current flow for advanced transistors. In this work, I also reviewed process flows, recipes, and training materials.

16. Further, I am an advisor of Sunrise Memory Corp., a startup company commercializing innovative 3D memory solutions. At Sunrise3D, I led the design of the memory bit cell and advised on process innovations. I conceived multiple process integration solutions for 3D device structures and established Design of Experiments (DOE) for optimization. In addition, I am a co-founder at Sonera Magnetics, a company developing innovative device solutions for augmented/virtual reality. I have 15 patents (including granted and pending applications) in the area of advanced semiconductor devices and technology.

17. I have authored or co-authored over 150 technical papers, in technical

journals and conferences in my field of expertise and have been the inventor or co-inventor of over 20 patents. I have supervised over 20 doctoral students, over 20 post-doctoral researchers, and over 150 undergraduate students in research areas in material physics and electronic applications. I received the NSF CAREER Award and the IEEE Nanotechnology Council Early Career Award in 2012, the Army Research Office (ARO) Young Investigator Program Award and the Air Force Office of Scientific Research Young Investigator Award in 2013, the Presidential Early Career Award for Scientist and Engineers in 2016, the IEEE George E Smith Award in 2019, and the IEEE Andrew Grove Award in 2025.

18. A full list of my research and professional experience, my consultant and work experience, and other activities and awards is further detailed in my curriculum vitae (CV), which I understand is being included as Exhibit 1012.

## IV. LIST OF DOCUMENTS CONSIDERED

19. In formulating my opinions, I have relied upon my training, knowledge, and experience that are relevant to the '909 patent. I have also considered all of the references cited in this Declaration, including the documents listed below. All citations to the documents listed below in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

| Exhibit No. | Description |
|---|---|
| 1001 | U.S. Patent No. 9,117,909 to Kuo et al. ("'909 patent") |

| Exhibit No. | Description |
|---|---|
| 1002 | Prosecution History of U.S. Patent No. 9,117,909 to Kuo et al. |
| 1004 | U.S. Patent No. 7,994,020 to Lin et al. ("Lin") |
| 1005 | U.S. Patent No. 8,629,512 to Liaw ("Liaw") |
| 1006 | U.S. Patent No. 8,546,891 to Chang et al. ("Chang") |
| 1009 | U.S. Patent Application Pub. No. 2013/0056826 to Liu et al. ("Liu") |
| 1010 | U.S. Patent No. 9,368,388 to Liaw ("Liaw-388") |
| 1011 | U.S. Patent Application Pub. No. 2013/0045580 to Cho ("Cho") |
| 1012 | *Curriculum Vitae of Dr. Sayeef Salahuddin* |
| 1013 | U.S. Patent Application Pub. No. 2011/0068405 to Yuan et al. ("Yuan") |
| 1014 | Park, D., et al., "Present and Future of Si-based Transistor Technology for Memories," *ECS Transactions*, 2(11):11-26 (2006) ("Park") |
| 1015 | U.S. Patent No. 7,148,120 to Chen et al. ("Chen-120") |
| 1016 | U.S. Patent No. 7,611,950 to Kim ("Kim") |
| 1018 | U.S. Patent Application Pub. No. 2007/0148979 to Lee et al. (Lee-979) |
| 1019 | U.S. Patent No. 6,413,802 to Hu et al. ("Hu") |
| 1020 | Chau, R., et al., "Silicon nano-transistors and breaking the 10 nm physical gate length barrier," 61st Device Research Conference. Conference Digest, Salt Lake City, UT, USA, 123-126 (2003) ("Chau") |
| 1021 | Colinge, J., et al.," FinFETs and Other Multi-Gate Transistors," Springer (2008) ("Colinge") |
| 1022 | Hu, C., "Modern Semiconductor Devices for Integrated Circuits," 1st ed. (2009) (Excerpt) ("Hu-2009") |
| 1023 | Huang, X., et al., "Sub 50-nm FinFET: PMOS," International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318), Washington, DC, USA, 67-70 (1999) ("Huang") |

| Exhibit No. | Description |
|---|---|
| 1024 | Bohr, M. et al., "Intel's Revolutionary 22nm Transistor Technology," available at http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf (accessed through https://newsroom.intel.com/press-kits/intel-22nm-3-d-tri-gatetransistor-technology/), ("Bohr") |
| 1025 | Kundu, S., et al., "Nanoscale CMOS VLSI Circuits: Design for Manufacturability," 1st ed. (2010) ("Kundu") |
| 1026 | Huang, X., et al., "Sub-50 nm P-channel FinFET," IEEE Transactions on Electron Devices, 48(5):880-886 (2001) ("Huang-2001") |
| 1027 | U.S. Patent No. 7,172,943 to Yeo et al. ("Yeo") |
| 1028 | Park, T., et al., "Fabrication of body-tied FinFETs (Omega MOSFETs) using bulk Si wafers," 2003 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, Japan, 135-136 (2003) ("Park-2003") |
| 1029 | Wolf, S. and Tauber, R., "Silicon Processing For The VLSI Era," Vol. 2, Lattice Press (1990) ("Wolf.") |
| 1030 | U.S. Patent No. 8,110,466 to Shieh et al. ("Shieh") |
| 1031 | Shamiryan, D., et al. "Dry etching process for bulk finFET manufacturing," Microelectron. Engineering, 86(10):96-98 (2009) ("Shamiryan") |
| 1032 | U.S. Patent Application Pub. No. 2012/0049294 to Chen et al. ("Chen-294") |
| 1033 | Engelhardt, M., et al. "A new $CBrF_3$ process for etching tapered trenches in Silicon," Journal of Electrochemical Society: Solid-State Science and Technology, 134(8):1985-1988 (1987) ("Engelhardt") |

| Exhibit No. | Description |
| --- | --- |
| 1034 | Makovejev, S., et al. "Improvement of high-frequency FinFET performance by fin width engineering," 2012 IEEE International SOI Conference (SOI), Napa, CA, USA, 2012, pp. 1-2 |
| 1035 | Jan, C., et al. "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate,<br>Optimized for Ultra Low Power, High Performance and High Density SoC Applications," 2012 International Electron Devices Meeting, San Francisco, CA, USA, 2012, pp. 3.1.1-3.1.4 |
| 1036 | U.S. Patent Application Pub. No. 2012/0001197 to Liaw et al. ("Liaw-197") |
| 1037 | U.S. Patent Application Pub. No. 2014/0131813 to Liaw et al. ("Liaw-813") |

20. To the best of my knowledge, the above-mentioned documents and materials are true and accurate copies of what they purport to be. An expert in the field would reasonably rely on them to formulate opinions such as those set forth in this declaration.

## V. LEGAL STANDARDS FOR MY ANALYSIS

21. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '909 patent are patentable, I have been told that I am obliged to follow existing law.

22. I have been told that a patent may not be obtained, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was

made to a person having ordinary skill in the art to which said subject matter pertains. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

23. When considering the issues of obviousness, I have been told that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

24. I have been told that the relevant time for considering whether a claim would have been obvious to a POSA is the time of alleged invention, which I have been asked to assume is just before the alleged earliest claimed priority date of the ’909 patent (i.e., April 16, 2013).

25. I have been told that a prior art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary

skill in the art would have employed at the time of invention.

26. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation

of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

27. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a POSA. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of a POSA. In addition, I have been told that the inferences and creative steps a POSA would have employed are also relevant to the obviousness inquiry.

28. I have been told the reasons a POSA would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

29. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a POSA would have implemented a

predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a POSA would have had good reason to pursue those known options.

30. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

31. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a POSA would have applied the prior art to obtain the claimed invention.

32. I have been told that when there is a known technique to address a

known problem using prior art elements according to their established functions, then a POSA would have had a motivation to combine.

33. I have been informed that, in an obviousness analysis, the prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

34. I understand that certain objective indicia can be important evidence as to whether a patent is obvious or nonobvious. Such indicia include: (1) commercial success of products covered by the patent claims; (2) a long-felt need for the invention; (3) failed attempts by others to make the invention; (4) copying of the invention by others in the field; (5) unexpected results achieved by the invention as compared to the closest prior art; (6) praise of the invention by the infringer or others in the field; (7) the taking of licenses under the patent by others; (8) expressions of surprise by experts and those skilled in the art at the making of the invention; and (9) the patentee proceeded contrary to the accepted wisdom of the prior art. At this point, I am not aware of any secondary indicia of non-obviousness. But, I reserve the right to review and opine on any evidence of

objective indicia of nonobvious that may be presented during this proceeding.

35. I also understand that "obviousness" is a legal conclusion based on the underlying factual issues of the scope and content of the prior art, the differences between the claimed invention and the prior art, the level of ordinary skill in the prior art, and any objective indicia of non-obviousness. For that reason, I am not rendering a legal opinion on the ultimate legal question of obviousness. Rather, my testimony addresses the underlying facts and factual analysis that would support a legal conclusion of obviousness or non-obviousness, and when I use the term obvious, I am referring to the perspective of one of ordinary skill at the time of invention.

## VI. STATE OF THE ART

36. The '909 patent describes a "method of forming a fin structure" and a corresponding "structure of a non-planar transistor." EX1001, Abstract. The claims of the '909 patent recite this non-planar transistor (e.g., fin field-effect transistor (FinFET)) in terms of four general concepts: the transistor having (i) a gate structure; (ii) active regions, (iii) shallow and deep trench isolation regions; and (iv) one or more protrusions having both a vertical upper portion sidewall and non-vertical lower portion sidewall. But as I explain below, each of these concepts, and combinations thereof, were well known before the '909 patent's earliest possible priority date.

### A. Non-Planar Transistors Having A Gate Structure Were Well Known

37. At the time of the ’909 patent, a FinFET—a type of non-planar transistor—having a gate structure was well-known, which is also acknowledged by the ’909 patent. EX1001, 1:26-36.

38. Traditionally, metal–oxide–semiconductor field-effect transistors (MOSFETs) were recognized as two-dimensional, or planar, transistors containing a source region, a drain region, a channel region through which electrons flow from the source to the drain, and a gate structure to control the flow of electrons. The demand for continued miniaturization of semiconductor devices drove a need for MOSFETs to evolve from these traditional planar MOSFET structures, as MOSFETs scaled to channel lengths below 100 nm suffer from short-channel effects, such as off-state leakage and drain-induced barrier-lowering and reduced gate control over the channel regions. EX1019, 1:25-31; EX1020, 124; EX1021, 2.

39. In the early 1980s, researchers started exploring new MOSFET structures which led to the development of 3-dimensional, non-planar FET structures. These non-planar FET structures were called by many names including the “fully Depleted Lean-channel TrAnsistor” (DELTA), double-gate FET, tri-gate FET, Π gate FET, and the Ω gate FET. EX1020, 125; EX1021, 8-15; EX1022, 280-282. In 1999, researchers at UC Berkeley coined a generic term to describe

these non-planar FETs—"FinFET." EX1023, 67. The term "Fin" refers to the 3-dimensional semiconductor protrusion present in these non-planar transistors, as described below.

40. The figures below show a side-by-side comparison of a planar MOSFET (below left) and a non-planar MOSFET (i.e., FinFET) (below right), which were presented in a May 2011 Intel presentation. EX1024, 4, 7. In the planar MOSFET, source and drain regions are formed in a substrate, a gate structure is formed on the substrate, and a channel region is formed in the substrate portion underneath the gate and between the source and drain regions. In contrast, in the FinFET, the channel region and the source and drain regions are formed on the substrate along with the gate structure. In the FinFET, the portion of the protrusion above the oxide layer is called a "fin," the gate structure is formed wrapped around a portion of the fin, the channel region is formed in the fin portion underneath the gate structure, and the source and drain regions are formed in the fin portions on either side of the channel region. "The dimensions of the fin dictate the channel length of the [FinFET]." EX1025, 5.

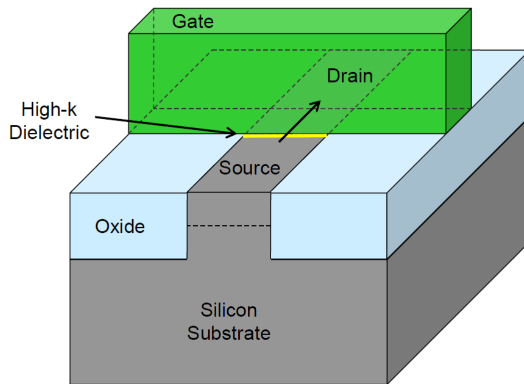



**Figure on page 4 of EX1024.**

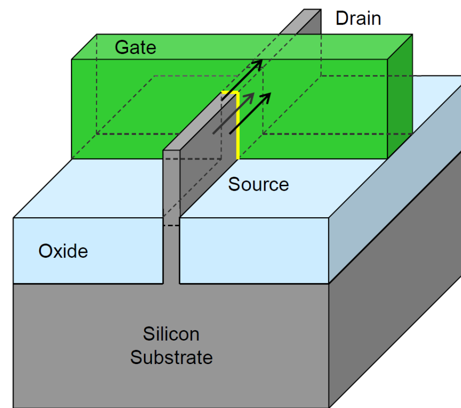



**Figure on page 7 of EX1024.**

41. Both the FETs have similar gate structures, which include gate dielectric layers (shaded yellow) and gate electrodes (shaded green). Both of the gate structures perform similar operations—control electron flow in the channel regions. However, the FinFET gate structure has better control over the channel regions than the planar MOSFET gate structure, as the FinFET gate structure exerts control on the channel region from multiple sides of the fins. EX1019, 1:52-55; EX1025, 6.

42. FinFETs with gate structures having gate dielectric layers and gate electrodes were developed in the early 2000s by major semiconductor companies like Intel, IBM, TSMC, and Samsung. EX1020, 123-126; EX1026, 881-882; EX1027, Abstract; EX1028, 135-136. For example, a TSMC patent to Yeo et al., filed in 2003, discloses a FinFET having a gate structure, as illustrated in annotated Figure 3 below:

**EX1027, FIG. 3 (annotated).**

43. Yeo discloses "a semiconductor fin 134 [(highlighted in orange)] formed in a portion of a bulk semiconductor substrate 132 [(highlighted in yellow)]. A gate dielectric 144 [(highlighted in gray)] overlies a portion of the semiconductor fin 134 and a gate electrode 146 [(highlighted in brown)] overlies the gate dielectric 144." EX1027, Abstract. Yeo further discloses that the "semiconductor fin 134 includes a doped source region 138 and a doped drain region 140. The source and drain regions 138 and 140 sandwich a channel region 142. A gate dielectric 144 overlies the channel portion 142 of the semiconductor fin 134, as shown in FIG. 3." EX1027, 4:33-37.

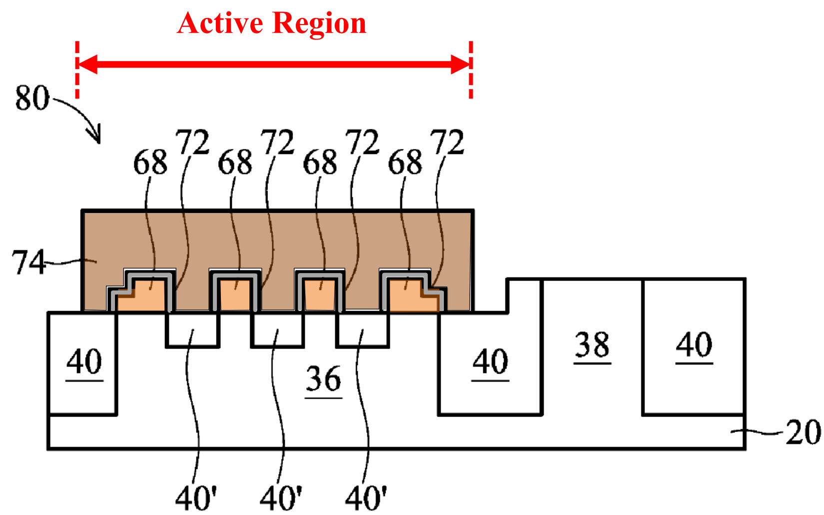
### B. Non-Planar Transistors Having Active Regions Were Well Known

44. FinFETs having active regions were well known prior to the '909

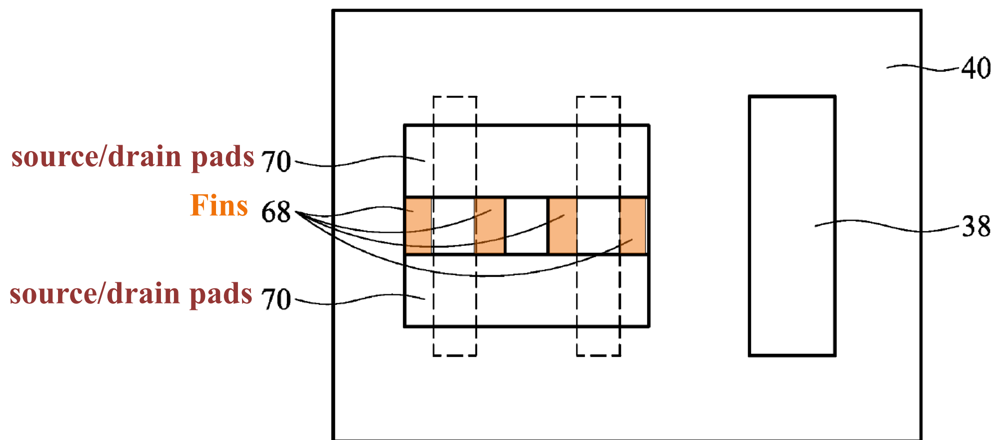
patent.

45. As early as 1990, Wolf described the active regions of a planar MOSFET as "those [regions] in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions." EX1029, 299. As the basic elements and operation of the planar MOSFET are similar to that of the non-planar FinFET, the semiconductor industry adopted the term "active region" to define the source, drain, and channel regions of the FinFET. And, as fins of the FinFET include the source, drain, and channel regions, the FinFET region that includes the protrusions are often referred to as the active region (or active area) of the FinFET, as illustrated and described in the examples below.

46. For example, in a patent filed in 2010, Shieh describes a FinFET 80 having an active region, as illustrated in annotated Figures 14B and 15 below. EX1030. Shieh discloses that "fins 68 [(highlighted in orange)] and source/drain pads 70 are formed in active region 36." EX1030, 4:62-63. Shieh explains that "an active region of the FinFET…includes the source/drain regions and (semiconductor) fins for forming channel regions of the FinFET." EX1030, 2:40-42. Shieh further discloses that "gate dielectric 72 [(highlighted in gray)] and gate electrode 74 [(highlighted in brown) are formed] on the surfaces and side walls of fins 68." EX1030, 5:3-5.



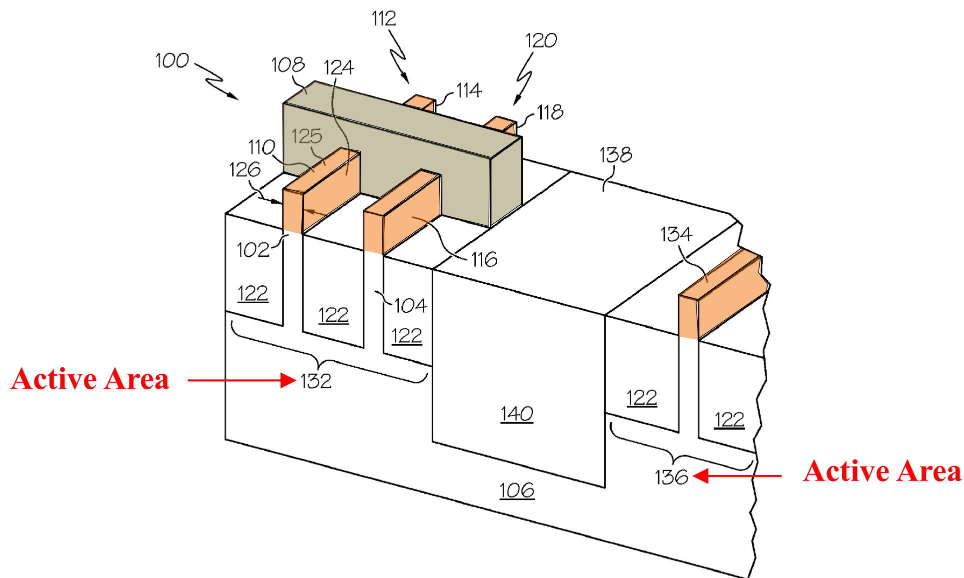

**EX1030, FIG. 15 (annotated).**




**EX1030, FIG. 14B (annotated).**

47. In another example, Cho describes, in a patent filed in 2011, an integrated circuit 100 with FinFETs having active areas, as illustrated in annotated Figure 1 below. EX1011. Cho discloses an active area 132 having fins (portions of

protrusions 102 and 104 above oxide layer 122 highlighted in orange) and an active area 136 having a fin (portion of protrusion 134 above oxide layer 122 highlighted in orange). EX1011, ¶14. Cho further discloses that "[a] gate electrode 108 [(highlighted in brown)] overlies the two fins [in active area 132] and is electrically insulated from the fins by a gate insulator (not illustrated)." EX1011, ¶14.




**EX1011, FIG. 1 (annotated).**

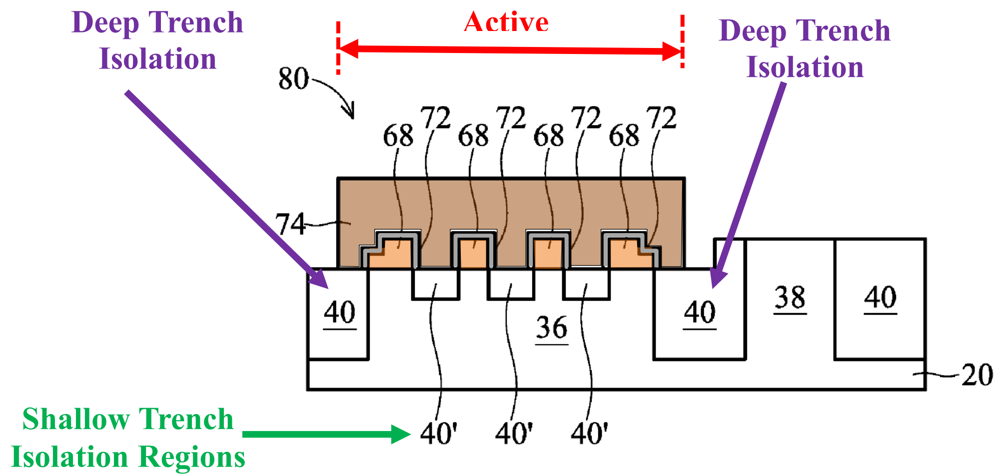
## C. Non-Planar Transistors Having Shallow and Deep Trench Isolation Regions Were Well Known

48. FinFETs having shallow and deep trench isolation regions were well known prior to the '909 patent.

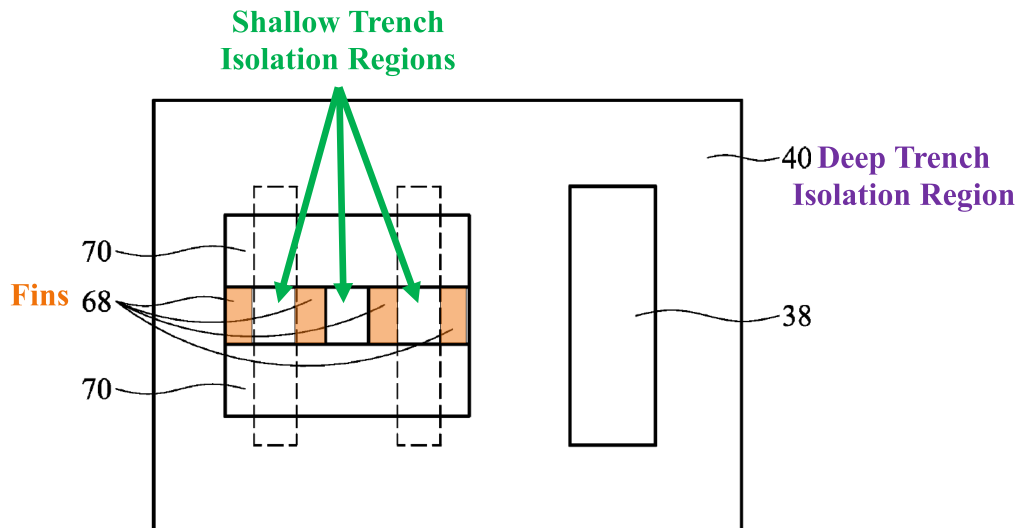
49. Multiple FinFETs located near one another (as is common in

microchips having millions of FinFETs) are electrically isolated from each other by "trenches" between adjacent FinFETs and/or between protrusions. Two types of trench isolation regions are most commonly used in semiconductor devices with FinFETs formed on bulk silicon substrates. EX1011, ¶4, EX1032, ¶14. One is the shallow trench isolation region and the other is the deep trench isolation region. The shallow trench isolation regions are typically formed between protrusions in an active region of a FinFET to electrically isolate the protrusions from each other. EX1011, ¶4, EX1032, ¶14. In contrast, the deep trench isolation regions are formed surrounding the active region of the FinFET to electrically isolate the FinFET from adjacent FinFETs or other active regions formed on the same substrate. EX1011, ¶4, EX1032, ¶14. Also, the deep trench isolation regions are formed deeper into the substrate than the shallow trench isolation regions. Such semiconductor devices with FinFETs having shallow trench isolation regions and deep trench isolation regions were well known prior to the '909 patent, as illustrated and described in the examples below.

50. For example, in a patent filed in 2010, Shieh describes a FinFET 80 having shallow trench isolation regions and deep trench isolation regions, as illustrated in annotated Figures 14B and 15 below.




**EX1030, FIG. 15 (annotated).**

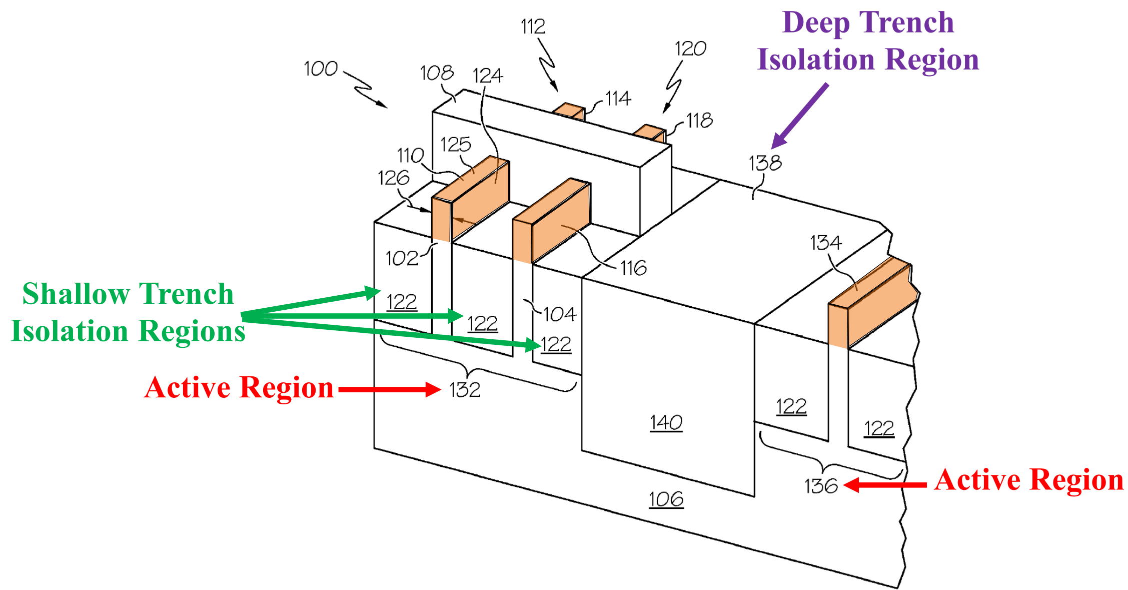



**EX1030, FIG. 14B (annotated).**

51. Figure 15 illustrates a cross-sectional view of FinFET 80 and Figure 14B illustrates a top view of FinFET 80 prior to the formation of gate dielectric 72 (highlighted in gray) and gate electrode 74 (highlighted in brown) in Figure 15.

Shieh discloses that "fins 68 [(highlighted in orange)] and source/drain pads 70 are formed in active region 36….[and] gate dielectric 72 and gate electrode 74 [are formed] on the surfaces and side walls of fins 68" EX1030, 4:62-63, 5:3-5. Shieh further discloses that insulation regions 40' are formed in shallow trenches 66 and insulation regions 40 are formed in deep trenches 34, which are deeper than trenches 66. EX1030, 3:40-43, 4:53-60. Also, Shieh explains that trenches 34 including insulation regions 40 "encircle (in the top view) active region 36," as illustrated in Figure 14B. EX1030, 3:31-32. Thus, the insulation regions 40' form the shallow trench isolation regions of FinFET 80 and the insulation regions 40, surrounding active region 36, form the deep trench isolation regions of FinFET 80.

52. In another example, Cho describes, in a patent filed in 2011, an integrated circuit 100 with FinFETs having shallow trench isolation regions and deep trench isolation regions, as illustrated in annotated Figure 1 below. Cho discloses an active area 132 having fins (portions of protrusions 102 and 104 above oxide layer 122 highlighted in orange) and an active area 136 having a fin (portion of protrusion 134 above oxide layer 122 highlighted in orange). EX1011, ¶14. Cho further discloses "[d]eep trench isolation region 138, filled with an insulating material 140 provides electrical isolation between active areas 132 and 136" and "[o]xide layer 122 forms electrical isolation between fins 102 and 104." EX1011, ¶14.




**EX1011, FIG. 1 (annotated)**

### D. Non-Planar Transistors Having Protrusions Comprising Both a Vertical Upper Portion Sidewall and Non-Vertical Lower Portion Sidewall Were Well Known

53. FinFETs having one or more protrusions with both a vertical upper portion sidewall and non-vertical lower portion sidewall were well known prior to the ’909 patent.

54. During the development of FinFETs on bulk silicon substrates in the early 2000s, one of the challenges encountered was the formation of isolation regions between protrusions having only vertical sidewalls. The high aspect ratio of the gaps between the vertical protrusions made the filling of insulating layers with minimal defects (e.g., voids) in the gaps challenging. This led to the development of protrusions with vertical upper portion sidewalls and non-vertical

lower portion sidewalls to minimize defects in the isolation regions.

55. For example, in a 2009 paper, Shamiryan describes "a method to manufacture bulk fins for finFET [that] consist of two parts: the straight top of 125 nm height which is used as a fin and a sloped bottom of 200 nm one that facilitates the trench filling," as illustrated in Figure 1c below. EX1031, Abstract.

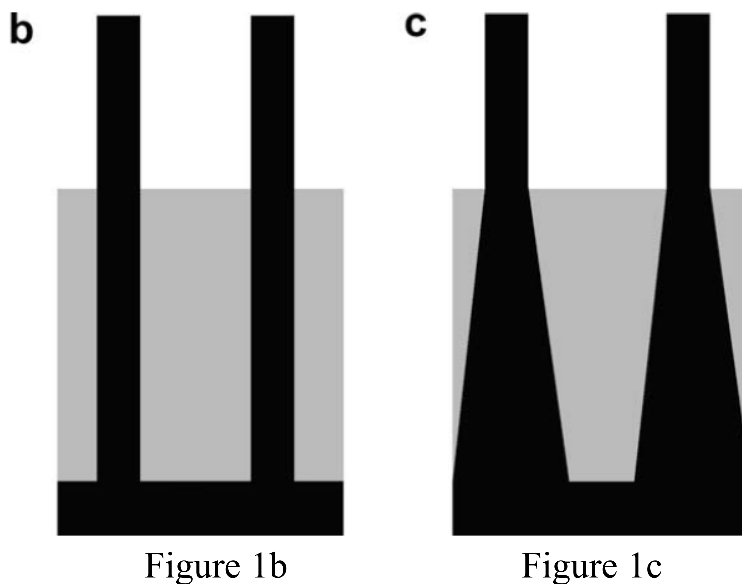


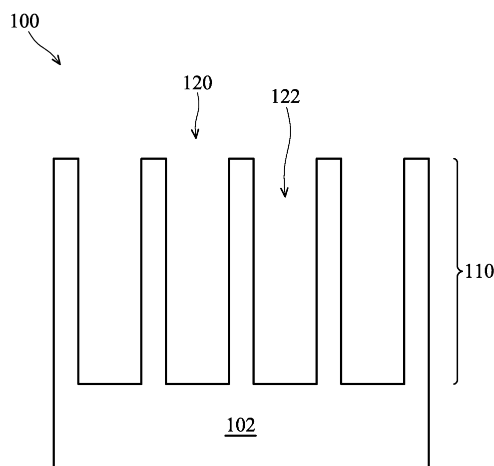

Figure 1b Figure 1c

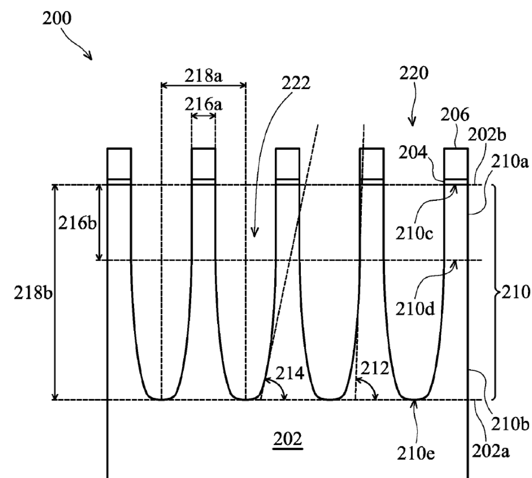
**EX1031, FIGS. 1b-c.**

56. Shamiryan explains that "filling the space between fins with conventional dielectric used for STI…is more challenging in bulk finFET because of its trench shape with vertical walls," as illustrated in Figure 1b. EX1031, 96. To overcome this gap filling challenge, Shamiryan "propose[d] a combination of vertical fin (top part) and sloped STI-like bottom as illustrated in Fig. 1c."

EX1031, 96. Shamiryan explains that "[t]he top vertical part provides the desired electrical performance, while the sloped bottom facilitates the filling." EX1031, 96.

57. In another example, Yuan describes, in a patent filed in 2010, a FinFET 200 having protrusions 210 with vertical upper portions 210a and tapered lower portions 210b (shown in Figure 2D reproduced below) for better gap-fill performance than FinFETs 100 with vertical protrusions 110 (shown in Figure 1A reproduced below). EX1013.




**EX1013, FIGS. 1A, 2D.**

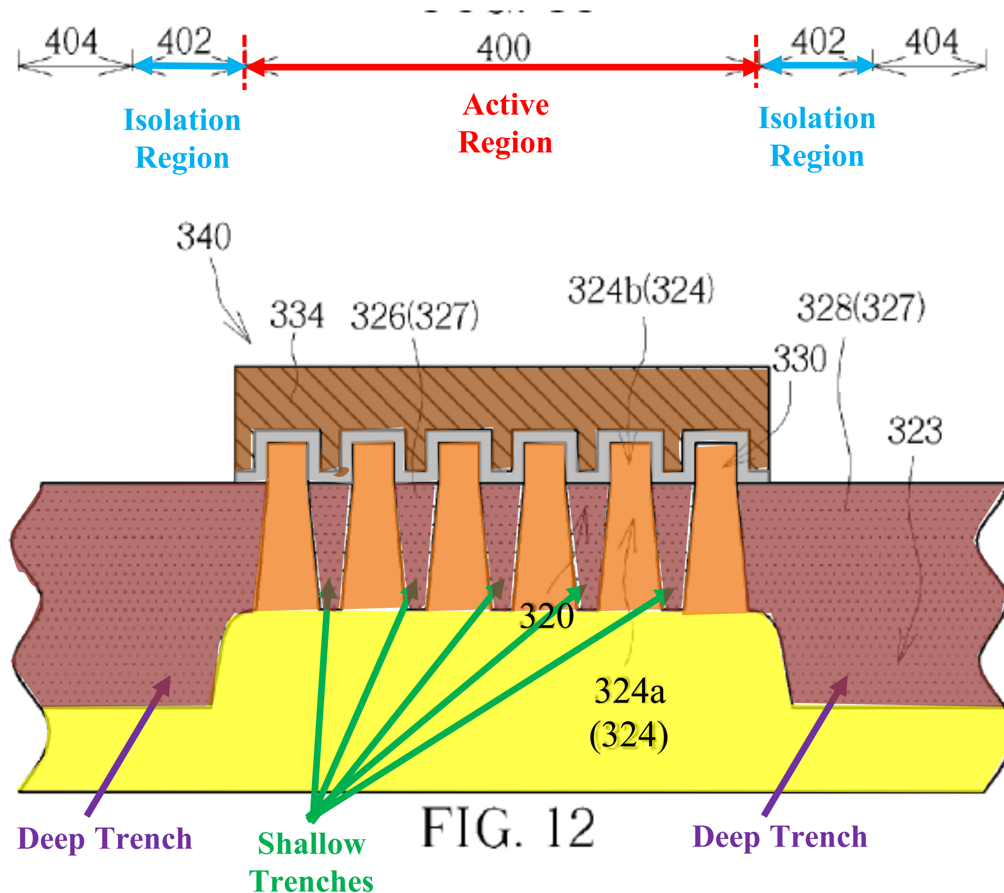
58. Yuan explains that "[o]ne of the challenges [of FinFET fabrication] is forming recess-free isolation structures" because the "dielectric material [of the isolation structures] may comprise a plurality of deep []recesses [] due to the high aspect ratio of the plurality of trenches" between the protrusions of the FinFET.

EX1013, ¶5. To overcome this challenge, Yuan discloses forming tapered protrusions 210 with vertical upper portions 210a and tapered lower portions 210b. Yuan further discloses that "upper portion 210a of each fin structure 210 has sidewalls that are substantially perpendicular to the major surface 202a of the substrate 202 and a top surface 210c." EX1013, ¶17. And, the "lower portion 210b of each fin structure 210 has tapered sidewalls on opposite sides of the upper portion 210a and a base 210e….[and] the tapered regions of the lower portion 210b of each fin structure 210 is preferably at an angle 214 in the range of 60 degrees to 85 degrees to the major surface 202a of the substrate 202." EX1013, ¶18. Yuan explains that "a plurality of trenches 222 formed between the tapered fin structures 210 [of FinFET 200] have lower aspect ratio than the plurality of trenches 122 formed between the vertical fin structures 110 [of FinFET 100]. The lower aspect-ratio trenches 222 have better gap-fill performance than the higher aspect-ratio trenches 122." EX1013, ¶18.

## VII. THE '909 PATENT

### A. Overview of the '909 Patent

59. The '909 patent generally discloses a "method of forming a fin structure of a non-planar transistor." EX1001, 1:13-16. Figure 12 (below) illustrates an example of the non-planar transistor.




**EX1001, FIG. 12 (annotated).**

60. Referring to Figure 12, the '909 patent discloses that "non-planar transistor 340 includes a substrate 300 [(annotated in yellow)], at least a protruding structure 324 [(annotated in orange)], a gate dielectric layer 332 [(not labeled in Figure 12, but nonetheless annotated in gray above)], a gate 334 [(annotated in brown)], a source/drain region 336, at least a fin-STI 326 and an STI 323." EX1001, 5:65-6:2. The '909 patent also discloses that the "gate 334 is disposed on the fin structure 330 and the gate dielectric layer 332 is disposed between the gate 334 and the fin structure 330." EX1001, 6:13-15, 5:63-64. The fin structure 330

refers to the upper portion 324b of the protruding structure 324 that protrudes over the fin-STI 326, as shown in Figure 12 above. EX1001, 4:7-11, 4:52-54.

61. The ’909 patent further discloses that “[a]n active region [(annotated in red)] such as the first region 400 and an isolation region such as the third region 402 are defined on the substrate 300. At least a second trench 320 [(annotated with green arrows and text)] is disposed in the active region and a sixth trench 323 [(annotated with purple arrows and text)] is disposed in the isolation region, wherein the sixth trench 323 is deeper than the second trench 320. An insulation layer 327 [(annotated in maroon)] is disposed in the second trench 320 and the sixth trench 323, wherein the insulation layer 327 in the second trench 320 (fin-STI 326) is level with that in the sixth trench 323 (STI 328)” EX1001, 6:2-11.

62. Moreover, the “fin structure 330 is disposed between each of the two second trenches 320 and protrudes over the fin-STI 326.” EX1001, 6:11-13. The “protruding structure 324 has an upper portion 324b having a substantial vertical sidewall, and a lower portion 324a having a tilted sidewall….In one embodiment, an upper surface of the insulation layer 327 is level with the boundary between the upper portion 324b and the lower portion 324a. In another embodiment, the upper surface of the insulation layer 327 is higher than the lower portion 324a.” EX1001, 6:15-24.

### B. Prosecution History Summary

63. The application that became the ’909 patent issued after receiving two non-final office actions. EX1002, ’909 Patent Prosecution History, 61-65, 82-86. In a first office action on November 28, 2014, the Examiner rejected independent Claim 1 under §102(a)(1) as being anticipated by U.S. Patent No. 7,247,887 to King et al. EX1002, 63-65. And, in its response, Applicant amended independent Claim 1 by adding that “the protruding structure has an upper portion having a substantial vertical sidewall and a lower portion having a titled sidewall,” without identifying any deficiencies in King, EX1002, 75.

64. Following Applicant’s amendment, the Examiner issued a second office action on March 12, 2015, in which the Examiner again rejected independent Claim 1 under §103 over King in view of U.S. Patent No. 8,946,829 to Wann et al. EX1002, 83-86. In response to the second office action, Applicant again chose not to argue that the references applied by the Examiner failed to disclose or render obvious any claim feature—including the protruding structure having “an upper portion having a substantial vertical sidewall and a lower portion having a titled sidewall.” Instead, Applicant again amended independent Claim 1 by adding that the deep trench “has a shoulder portion”—a feature that was not claimed until being added as a new dependent claim in response to the November 28, 2014 office action. EX1002, 76, 90. Following the second amendment to

independent Claim 1, the Examiner issued a notice of allowance on June 2, 2015. EX1002, 97-99.

65. But, as I discuss below, all of the claimed concepts—including the shoulder portion of the deep trench—were well known before the ’909 patent. In my opinion, if any of the prior art references applied herein been before the Examiner during prosecution, the ’909 patent would not have been allowed.

### C. Level of Ordinary Skill in the Art

66. I have been informed that a person of ordinary skill in the art (“POSA”) is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

67. I have been instructed to assume a POSA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

68. In my opinion, a POSA in reference to the ’909 patent would have had a master’s degree in electrical engineering, physics chemistry, materials science, or related fields and three years of work experience in semiconductor manufacturing, including planar transistors. Additional education could substitute for professional experience, and additional work experience/training could substitute for formal

education.

69. I have not analyzed the priority date of the ’909 patent, but I note that the alleged earliest claim to priority is April 16, 2013. Because all the prior art discussed in this Declaration predates April 16, 2013, I have been asked for simplicity to treat April 16, 2013 as the priority date for the ’909 patent. I have also treated this date as the date from which to assess the knowledge available to a POSA.

70. I am well qualified to determine the level of ordinary skill in the art. I am very familiar with the technology of the ’909 patent during the April 2013 timeframe. As mentioned above, by 2013, I had obtained a Ph.D. in Electrical and Computer Engineering from Purdue University, was working as an Assistant Professor at the University of California, Berkeley, and had acquired extensive experience relating to the design and manufacturing of semiconductors, including FinFETs. I thus also qualify as a POSA for the ’909 patent.

71. Regardless of whether I use “I” or a “POSA” during my technical analysis below, all of my statements and opinions are always to be understood to be based on how a POSA would have understood or read a document at the time of the alleged invention.

### D. Claim Construction

72. I have been told that, in an *inter partes* review, all claim terms must

be given their ordinary and customary meaning as understood by a POSA at the time of the invention, in light of the specification and the prosecution history of the patent. Solely for the purposes of this Declaration in this *inter partes* review proceeding, I submit that all claim terms should receive their plain and ordinary meaning in the context of the ’909 patent specification.

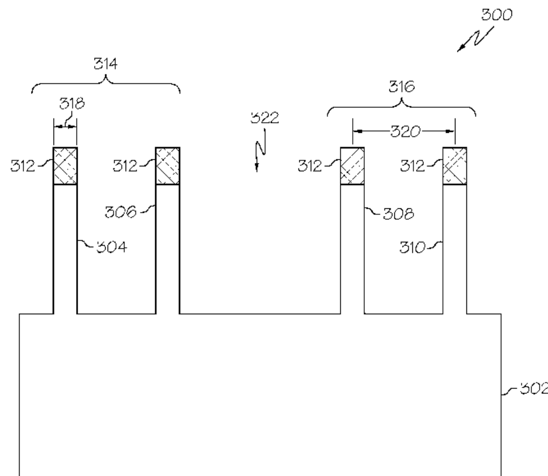
## VIII. OVERVIEW OF THE APPLIED REFERENCES

### A. Lin

73. Lin (EX1004) was filed on July 21, 2008, and issued on August 9, 2011. Lin is directed to forming FinFETs having trench isolation. EX1004, Title, 1:10-11. In my opinion, Lin is analogous art because Lin is in the same field of endeavor as the ’909 patent and reasonably pertinent to at least one problem the ’909 patent purports to address—the formation of FinFETs. EX1001, 1:40-42, 5:63-64; EX1004, 1:10-11.

74. Similar to the ’909 patent, Lin describes a “method of manufacturing a semiconductor device structure, such as a FinFET device structure.” EX1004, Abstract. Referring to Figure 3 reproduced below, Lin discloses that the method begins by “providing a substrate [302] comprising a bulk semiconductor material, a first conductive fin structure [304 and 306] formed from the bulk semiconductor material, and a second conductive fin structure [308 and 310] formed from the bulk semiconductor material. The first conductive fin structure [304 and 306] and the

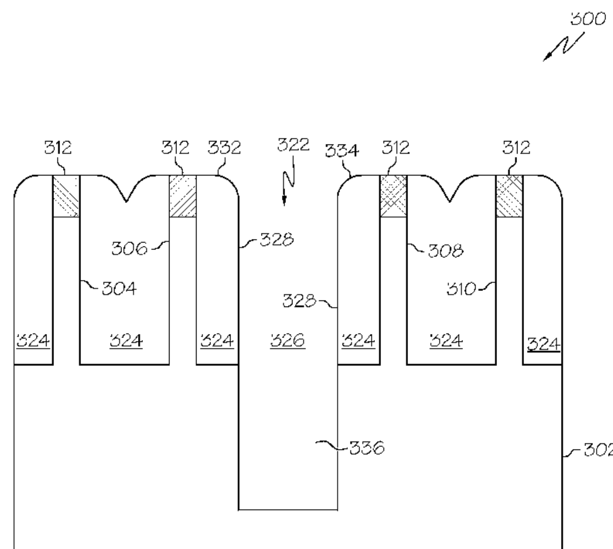
second conductive fin structure [308 and 310] are separated by a gap [322].” EX1004, Abstract. In several instances, Lin refers to protrusions 304, 306, 308, and 310 as “conductive fins,” “fins,” and/or “fin structure[s].” EX1004, Abstract, 1:23-54, 4:1-25. Regardless of the terminology used, a POSA would have understood from Lin’s teachings that protrusions 304, 306, 308, and 310 are exemplary embodiments of well-known semiconductor fins used in known FinFETs. EX1004, 1:23-54, FIGS. 1, 2. Moreover, as I explain below, in my opinion a POSA would have understood that each of Lin’s protrusions 304, 306, 308, and 310 represents the claimed “*protruding structure*” and the upper section 342 of each protrusion that protrudes above dielectric material 340 represents the claimed “*fin structure*.”




**EX1004, FIG. 3.**

75. Lin further discloses that the method continues with an “etching step [that] etches the bulk semiconductor material … to form an isolation trench [336]

in the bulk semiconductor material," specifically in the gap 322, as shown in Figure 6 reproduced below. EX1004, Abstract.




**EX1004, FIG. 6.**

76. Subsequently, a "dielectric material [340] is formed in the isolation trench [336], … over the first conductive fin structure [304 and 306], and over the second conductive fin structure [308 and 310]." EX1004, Abstract. Lin discloses that at least a portion of the dielectric material 340 is then "etched away to expose an upper section of the first conductive fin structure [304 and 306] and an upper section of the second conductive fin structure [308 and 310], while preserving the dielectric material [340] in the isolation trench [336]," as shown in Figure 10 reproduced below. EX1004, Abstract. Lin explains that "[f]ollowing these steps, the fabrication of the devices is completed in a conventional manner." EX1004, Abstract.

FIG. 10

**EX1004, FIG. 10.**

## B. Chang

77. Chang (EX1006) was filed on February 29, 2012, and issued on October 1, 2013. Chang is directed to forming FinFETs with different protrusion profiles. EX1006, Title. In my opinion, Chang is analogous art because Chang is in the same field of endeavor as the ’909 patent and reasonably pertinent to at least one problem the ’909 patent purports to address—the formation of FinFETs. EX1001, 1:40-42, 5:63-64; EX1006, 11:3-4.

78. Again similar to the ’909 patent, Chang describes “a method for forming a FinFET device,” and various resulting FinFET devices. EX1006, 11:3-4. An intermediate stage of fabrication of one of Chang’s many example FinFETs is illustrated in Figures 9a and 9b below.

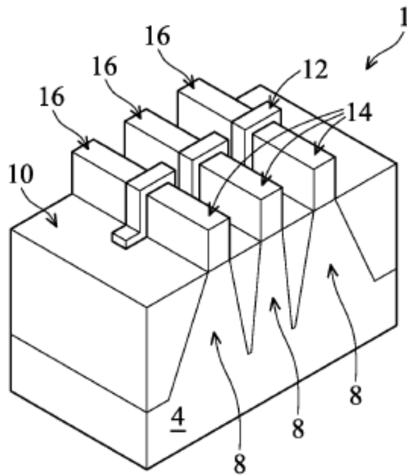



FIG. 9a

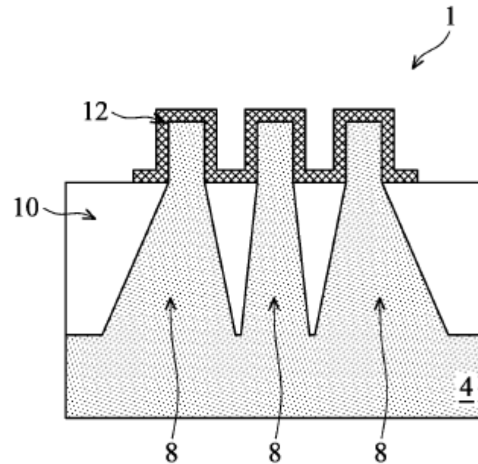



FIG. 9b

**EX1006, FIGS. 9a-b.**

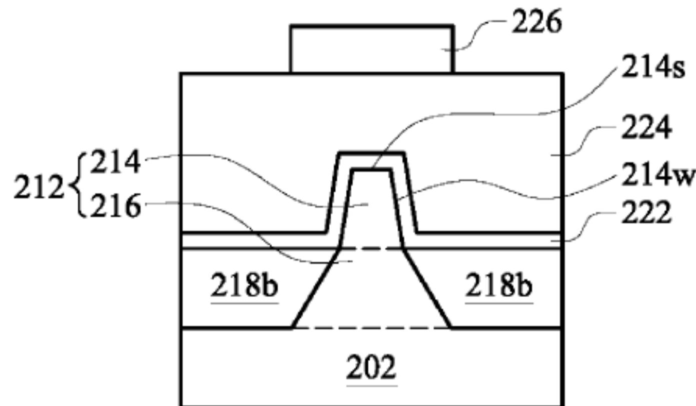
79. Chang discloses that its FinFET device includes a first protrusion 8 that is laterally adjacent to a second protrusion 8." EX1006, Abstract. In several instances, Chang refers to each protrusion 8 as a "semiconductor fin." EX1006, Abstract, 3:26-40. As I explain below, regardless of the terminology used, a POSA would have understood that each of Chang's protrusions 8 represents the claimed "*protruding structure*" and the upper portion of each protrusion 8 that protrudes above dielectric material 10 represents the claimed "*fin structure*." Chang explains that "[t]he first semiconductor fin [8] and the second semiconductor fin [8] may have profiles to minimize defects and deformation." EX1006, Abstract. Specifically, the lower portions of the first and second protrusions 8 may have a flared profile that is wider at the bottom than the upper portions of the first and

second protrusions 8. EX1006, Abstract. Chang also discloses that trenches on the outer edges of the outermost protrusions may be etched deeper than trenches in between the protrusions. EX1006, 4:3-5. Subsequently, "dielectric material 10 is blanket deposited on the FinFET 10." EX1006, 4:30-31. Chang further discloses that "FIGS. 9*a* and 9*b* illustrate the formation of the gate structure 12 over the fins 8," where "gate structure 12 may include a gate dielectric layer (not shown), [and] a gate electrode (not shown)." EX1006, 4:61-64.

### C. Liaw

80. Liaw (EX1005) was filed on May 21, 2012, and issued on January 14, 2014. Liaw is directed to forming FinFETs with a gate stack. EX1005, Title, 1:14-15. In my opinion, Liaw is analogous art because Liaw is in the same field of endeavor as the '909 patent and reasonably pertinent to at least one problem the '909 patent purports to address—the formation of FinFETs. EX1001, 1:40-42, 5:63-64; EX1005, 2:11-14.

81. Liaw describes "a method of fabricating a gate stack of a Fin Field Effect Transistor (FinFET)," where the FinFET comprises "a tapered gate stack 230." EX1005, 1:51-53, 2:28-31. An intermediate stage of fabrication of Liaw's FinFET with a tapered gate stack is illustrated in Figure 7B reproduced below.




**EX1005, FIG. 7B.**

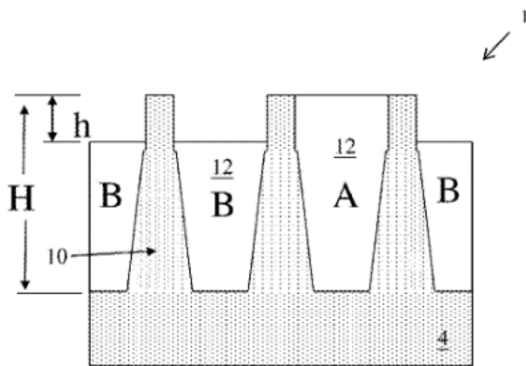
82. Referring to Figure 7B, Liaw discloses that its FinFET includes a protrusion 212 with an upper portion 214 and a lower portion 216, wherein the lower portion 216 has tapered sidewalls. EX1005, 8:20-24. In several instances, Liaw refers to protrusion 212 as a "fin." EX1005, 8:20-24, 3:22-33. As I explain below, regardless of the terminology used, a POSA would have understood that Liaw's protrusion 212 represents the claimed "*protruding structure*" and the upper portion 214 of protrusion 212 that protrudes above insulating regions 218b represents the claimed "*fin structure*." Liaw further discloses that its "FinFET further includes a gate dielectric [222]" covering the upper portion 214 of protrusion 212 and "a conductive gate strip [224] traversing over the gate dielectric." EX1005, Abstract.

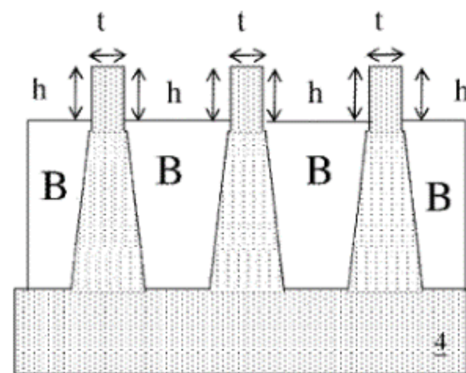
**D. Liu**

83. Liu et al. (EX1009) was filed on September 1, 2011, and published on

March 7, 2013. Liu is directed to forming FinFETs with multiple protrusions. EX1009, Title, Abstract. In my opinion, Liu is analogous art because Liu is in the same field of endeavor as the ’909 patent and reasonably pertinent to at least one problem the ’909 patent purports to address—the formation of FinFETs. EX1001, 1:40-42, 5:63-64; EX1009, ¶6.

84. Liu discloses methods for fabricating a FinFET device 1. EX1009, ¶6. Liu discloses that FinFET device 1 “includes a substrate and a plurality of fins formed on the substrate.” EX1009, Abstract. Liu also discloses that as part of its FinFET fabrication method, a “dielectric layer is formed on the substrate,” which can have one or more different thicknesses. EX1009, Abstract. An intermediate step in the fabrication of two of Liu’s example FinFETs is illustrated in Figures 5b and 6d reproduced below.




**EX1009, 5B, 6d.**

85. Liu explains that “[b]y adjusting the dielectric layer thickness, channel

width of the resulting device can be fine-tuned." EX1009, Abstract. Liu further discloses that a "continuous gate structure is formed overlying the plurality of fins, the continuous gate structure being adjacent a top surface of each fin and at least one sidewall surface of at least one fin." EX1009, Abstract.

## IX. GROUNDS OF UNPATENTABILITY

86. In my opinion, claims 1-6 are unpatentable for at least the reasons set forth below. In providing my analysis, I refer to the '909 patent claim limitations using the claim mapping in the Claims Appendix, which can be found in Section IX of this Declaration.

### A. Ground 1: The combination of Lin and Liaw renders obvious claims 1-4 and 6.

#### 1. A POSA would have been motivated to combine Lin and Liaw.

87. In my opinion, both Lin and Liaw are in the same field of endeavor – fabrication of FinFETs. As I explain below in Sections IX.A.1.a and IX.A.1.b, in my opinion a POSA would have been motivated (a) to modify Lin's method of fabricating protrusions with Liaw's method of fabricating protrusions with tapered sidewalls in lower portions of the protrusions, and (b) to incorporate Liaw's method of fabricating a gate stack of conductive gate strip and gate dielectric into Lin's FinFET fabrication method.

##### a. A POSA would have been motivated to modify Lin's protrusions to incorporate Liaw's manufacturing

**techniques to form protrusions having lower portions with tapered sidewalls.**

88. In my opinion, a POSA would have been motivated to modify Lin's FinFET fabrication process with Liaw's method of protrusion formation to modify Lin's protrusions to have lower portions with tapered sidewalls, similar to Liaw's protrusions.

89. Referring to Figures 3 and 10 (reproduced below), Lin discloses a method of fabricating a FinFET with protrusions having upper sections ("upper portion") and bases ("lower portion"):

> A **method of manufacturing** a semiconductor device structure, such as **a FinFET device structure**, is provided. The method begins by providing a substrate **comprising** a bulk semiconductor material, **a first conductive fin structure** formed from the bulk semiconductor material, and **a second conductive fin structure** formed from the bulk semiconductor material.

EX1004, Abstract.[2]

> FIG. 3 illustrates semiconductor device structure 300 in a state **after the formation of a plurality of conductive fins 304, 306, 308, and 310** from bulk silicon substrate 302, and after formation of silicon nitride caps 312 on the top of the fins. The combination of a conductive fin and its overlying nitride cap may be referred to herein as a "**conductive fin structure**."

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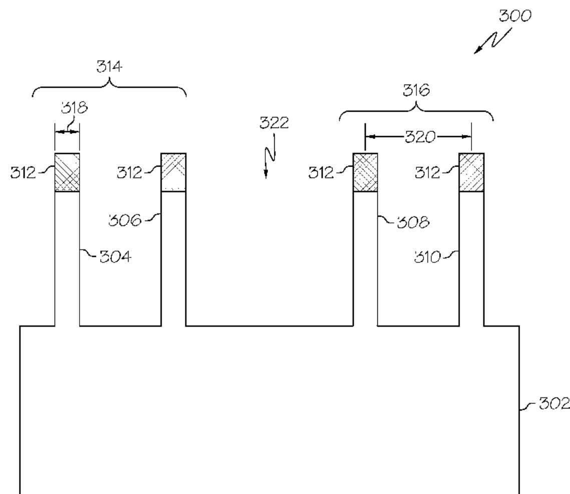
[2] Bold emphasis added unless otherwise noted.

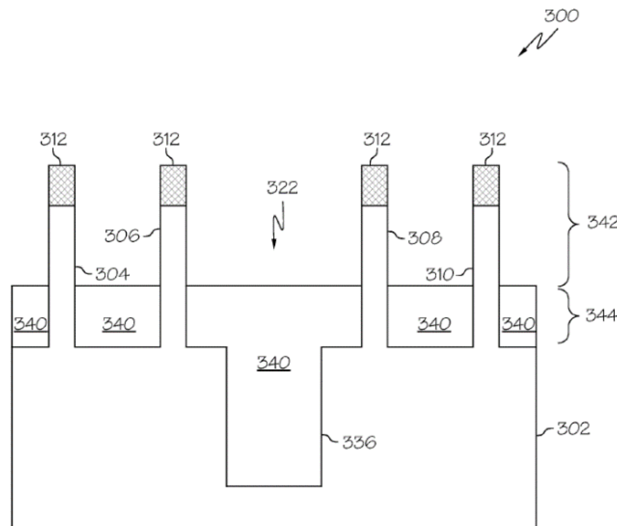
EX1004, 4:1-5.

> Referring to FIG. 10, the etching of dielectric material 340 exposes **an upper section 342 of each conductive fin structure**. In other words, silicon nitride caps 312 and the upper lengths of the conductive fins become exposed due to the etching of dielectric material 340 to a remaining height relative to the conductive fins. … Moreover, a layer 344 of the dielectric material 340 is retained at **the base of the conductive fins**.

EX1004, 6:49-58.




**EX1004, FIG. 3.**




**EX1004, FIG. 10.**

90. As I discussed above in Section VIII.A, in several instances, Lin refers to protrusions 304, 306, 308, and 310 as "conductive fins," "fins," and/or "fin structure[s]." EX1004, Abstract, 1:23-54, 4:1-25. And, regardless of the terminology used, a POSA would have understood that each of Lin's protrusions 304, 306, 308, and 310 represents the claimed "*protruding structure*" and the upper section 342 of each protrusion that protrudes above dielectric material 340 represents the claimed "*fin structure*." Each of Lin's protrusions 304, 306, 308, and 310 are shown in Figures 3 and 10 (reproduced above) to have vertical sidewalls along both its upper section 342 and base. Lin discloses forming these protrusions 304, 306, 308, and 310 with "well known techniques and process steps," such as "techniques and steps related to photolithography and patterning, sidewall image transfer, etching, material growth, material deposition, [and] surface

planarization." EX1004, 4:7-11. But Lin does not explicitly disclose how these techniques and process steps are performed, nor does Lin explicitly disclose how these techniques and process steps would impact the dimensions and sidewall profiles of the upper sections 342 and bases of the protrusions 304, 306, 308, and 310.

91. Lin further discloses that the "dimensions [of the conductive fins 304, 306, 308, and 310] are provided to establish a convenient and realistic frame of reference, and that the actual dimensions of a practical embodiment of semiconductor device structure 300 might vary." EX1004, 4:37-41. But Lin does not explicitly disclose why these dimensions would vary, nor discloses how these dimensions and sidewall profiles of the upper sections 342 and bases of the protrusions 304, 306, 308, and 310 could be varied. Moreover, Lin does not disclose why a practitioner would want to vary these dimensions.

92. Nevertheless, in my opinion, a POSA would have understood that varying the parameters of the different processes provided by Lin for the formation of the protrusions 304, 306, 308, and 310 could be used to vary the dimensions and sidewall profiles of the upper sections 342 and bases of the protrusions 304, 306, 308, and 310. Thus, in my opinion, a POSA would have been motivated to look to other prior art references, such as Liaw, for teachings on how to vary the dimensions of semiconductor device structure 300, including that of the

protrusions 304, 306, 308, and 310, and on how varying these dimensions would impact the fabrication process control and characteristics of semiconductor device structure 300.

93. Referring to Figures 3A and 3B (reproduced below), Liaw discloses a method of fabricating a FinFET with a protrusion 212 having upper and lower portions 214 and 216:

> Referring to FIGS. 3A, 3B, and 3C, and step 104 in FIG. 1, after formation of the openings 208 in the photo-sensitive layer 206, the structure in FIGS. 3A, 3B, and 3C is produced by **forming a fin 212 in the substrate 202**…. In the depicted embodiment, **the semiconductor fin 212 comprises an upper portion 214 and a lower portion 216** (separated by the dashed line [in FIG. 3B]).

EX1005, 3:22-25, 3:40-42.

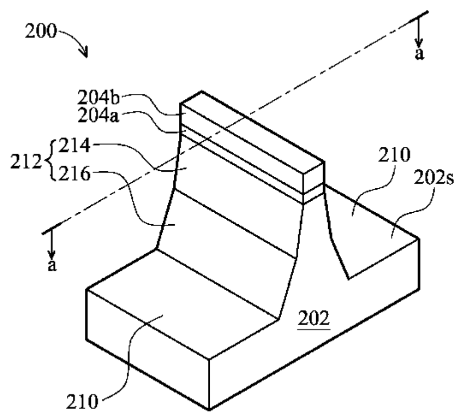


FIG. 3A

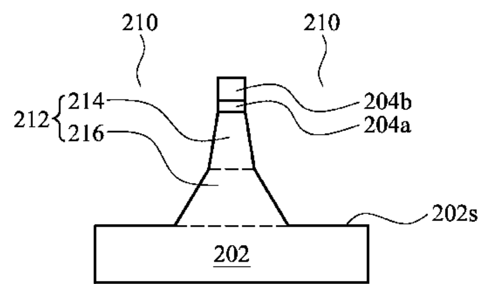


FIG. 3B

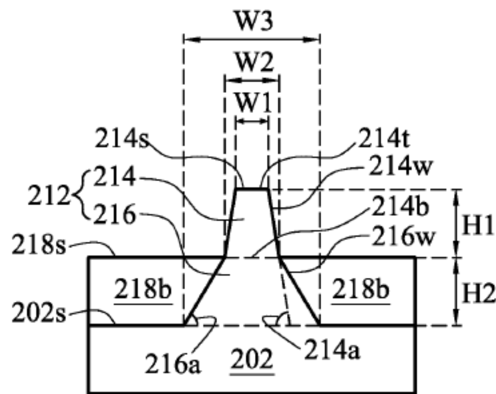
**EX1005, 3A-B.**

94. Referring to Figure 6B (reproduced below), Liaw further discloses forming the upper portion 214 and the lower portion 216 with tapered sidewalls

and forming the lower portion 216 with a more rigid and larger volume than the upper portion 214:

> In the depicted embodiment, the fin 212 through an opening in the insulation region 218b to a first height H1 above the second surface 218s, wherein the base 214b of an upper portion 214 (shown by the dashed line [in FIG. 6B]) of the fin 212 is broader than the apex 214t, wherein **the upper portion 214 has first tapered sidewalls 214w** and top surface 214s (or defined as a third surface 214s). … In some embodiments, the semiconductor fin 212 further comprises a lower portion 216 extending downward from the base 214b to the first surface 202s has a second height H2. **The lower portion 216 has third tapered sidewalls 216w**. In at least one embodiment, an angle 216a of the third tapered sidewalls 216w to the first surface 202s is from about 60 degrees to 85 degrees. In some embodiments, a difference between a maximum width $W_3$ of the third tapered sidewalls 216w and the maximum width $W_2$ of the first tapered sidewalls 214w is in the range of about 3 nm to 10 nm. In yet another embodiment, a ratio of the first height H1 to the second height H2 is from about 0.2 to 0.5.

EX1005, 5:7-13, 5:26-37.




**EX1005, FIG. 6B.**

95. As I discussed above in Section VIII.C, in several instances, Liaw refers to protrusion 212 as a "fin." EX1005, 8:20-24, 3:22-33. And, regardless of the terminology used, a POSA would have understood that Liaw's protrusion 212 represents the claimed "*protruding structure*" and the upper portion 214 of protrusion 212 that protrudes above insulating regions 218b represents the claimed "*fin structure*." Liaw explains that the tapered design of protrusion 212 (shown in Figure 6B above) is an improvement on the typical protrusion design of FinFETs that are "fabricated with a thin vertical 'fin' (or fin structure) extending from a substrate," a design which can "increase[] the likelihood of device instability and/or device failure." EX1005, 1:24-40. Moreover, Liaw explains that by "[h]aving more rigid volume [in the lower portion 216] than the upper portion 214, the lower portion 216 can avoid fin 212 deformation of the FinFET 200 due to high stress in the insulation regions 218*b*." EX1005, 5:37-40.

96. In my opinion, at least based on the above teachings of Liaw, a POSA would have recognized the benefits—improved performance and stability—of forming protrusions with tapered lower portions in FinFETs. Moreover, in my opinion, a POSA would have understood that Liaw's protrusion design of tapered lower portion 216 provides an improvement over Lin's protrusions 304, 306, 308, and 310, which have vertical sidewalls along both their upper sections 342 and bases.

97. Besides, well before Liaw (and the '909 patent), it was well known in the field of FinFET technology that having protrusions with tapered lower portions improved FinFET fabrication process control. Because, the tapered lower portions assist in filling in gaps with minimal defects (e.g., voids) between adjacent protrusions as gaps with a lower aspect ratio between tapered protrusions than that between vertical protrusions are consistently filled in with a dielectric material during isolation region formation, which improves device performance predictability and control.

98. For example, as I discussed in Section VI.D above, Shamiryan reported "a method to manufacture bulk fins for finFET[, in which each of]…[t]he bulk fins consist of two parts: the straight top one which is used as a fin and a sloped bottom one that facilitates the trench filling," as shown in Figure 1c reproduced below. EX1031, 98. Shamiryan explains that "filling the space between

fins with conventional dielectric used for STI…is more challenging in bulk finFET because of its trench shape with vertical walls," as shown in Figure 1b reproduced below. EX1031, 96. But, with "a combination of vertical fin (top part) and sloped STI-like bottom[,] as illustrated in Fig. 1c[,] … [t]he top vertical part provides the desired electrical performance, while the sloped bottom facilitates the filling." EX1031, 98.

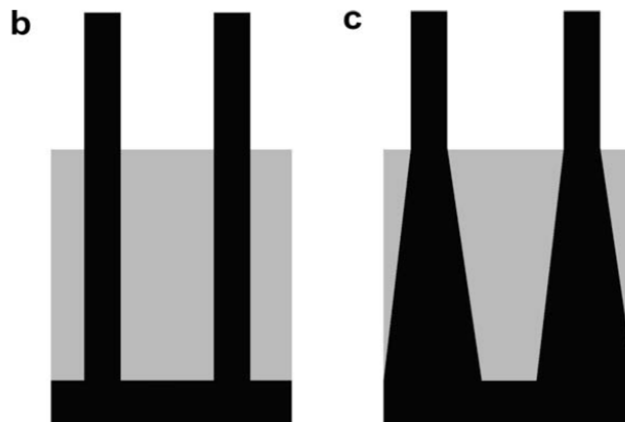



Figure 1b Figure 1c

**EX1031. FIGS. 1b-c.**

99. In another example, as I discussed in Section VI.D above, Yuan discloses forming a FinFET 200 having protrusions 210 with vertical upper portions 210a and tapered lower portions 210b (shown in Figure 2D reproduced below) for better gap-fill performance than FinFETs 100 with vertical protrusions 110 (shown in Figure 1A reproduced below). EX1013. Yuan explains that "a plurality of trenches 222 formed between the tapered fin structures 210 [of FinFET 200] have lower aspect ratio than the plurality of trenches 122 formed between the

vertical fin structures 110 [of FinFET 100]. The lower aspect-ratio trenches 222 have better gap-fill performance than the higher aspect-ratio trenches 122." EX1013, ¶18.

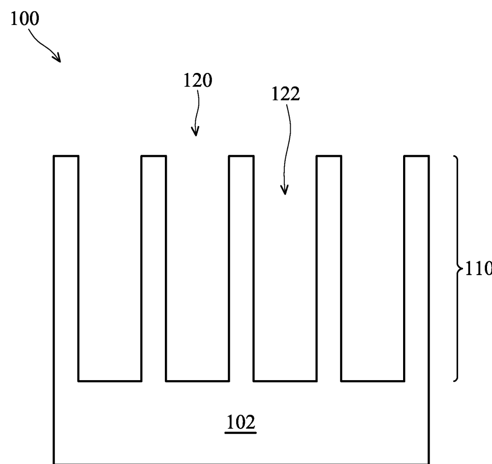



FIG. 1A ( PRIOR ART )

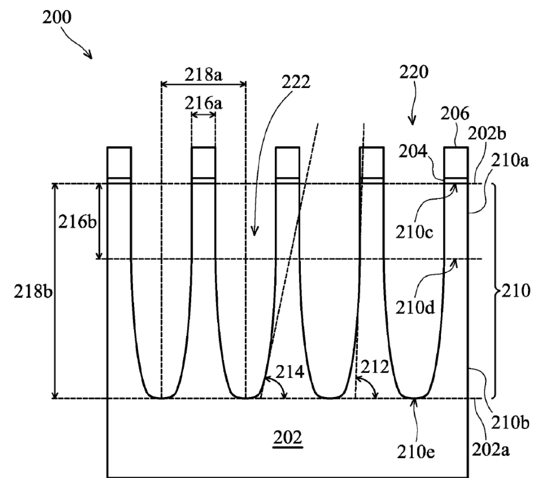



FIG. 2D

**EX1013, FIGS. 1A, 2D.**

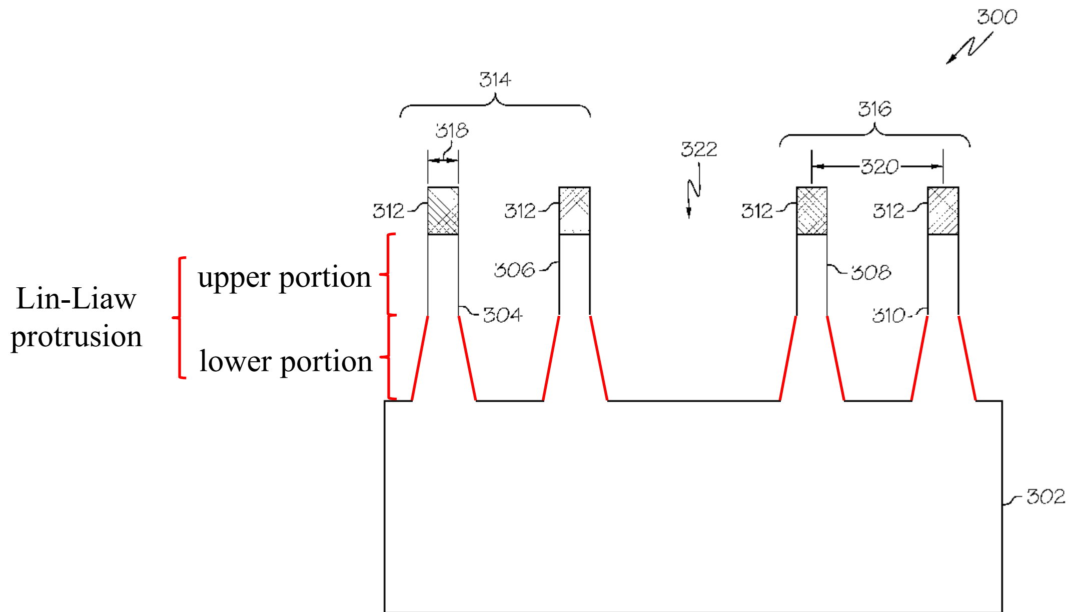
100. Thus, in my opinion, to achieve the benefits of having protrusions with tapered lower portions in FinFETs, a POSA would have been motivated to modify Lin's method of forming protrusions 304, 306, 308, and 310 with Liaw's method of forming protrusions 212 with tapered lower portions 216. That is, in my opinion, it would have obvious to a POSA to modify Lin to use techniques and processing steps to form protrusions having upper portions with vertical sidewalls (as taught by Lin's upper sections 342) and lower portions with tapered sidewalls (as taught by Liaw's lower portions 216).

101. Similar to Lin, Liaw discloses a method of fabricating a FinFET,

which includes a process for forming protrusions on a substrate using photolithography and etching processes. *Compare* EX1004, Abstract, 4:1-11 *with* EX1005, Abstract, 3:7-42. Thus, in my opinion, a POSA would have recognized that Liaw's techniques are applicable to and compatible with Lin's fabrication process, and that modifying Lin's semiconductor device structure 300 to include protrusions having a lower portion with tapered sidewalls would have required minimal modifications to Lin's fabrication process. In my opinion, in the combined Lin-Liaw system, it would have been obvious to a POSA to incorporate Liaw's etching process—a process specifically identified in Lin as being suitable for forming its protrusions (EX1004, 4:7-11)—in Lin's fabrication process to form the lower portions of one or more of Lin's protrusions 304, 306, 308, and 310.

102. As a result, in my opinion, Lin's modified protrusion formation process would include two etching processes—(1) a first etching process, as taught by Lin, performed on Lin's bulk silicon substrate 302 to form an upper portion with vertical sidewalls, and (2) a second etching process, as taught by Liaw, performed on Lin's bulk silicon substrate 302 after the formation of the upper portion to form a lower portion with tapered sidewalls. This modified process would result in one or more protrusions ("Lin-Liaw protrusions") having an upper portion with vertical sidewalls (as taught by Lin) and a lower portion with tapered sidewalls (as taught by Liaw), as I illustrate in a modified version of Lin's Figure 3

(with annotations) below. In my opinion, a POSA would not have experienced any unreasonable technical hurdles in implementing these modifications, as incorporating the second etching process into Lin's protrusion formation process would require nothing more than modifying the known etching process parameters, such as etching gas flow rates, etching temperature, etching pressure, and etching bias of Lin's protrusion formation process.




**EX1004, FIG. 3 (modified and annotated).**

103. In my opinion, a POSA would have been further motivated to combine Lin and Liaw because both are in the same general field of FinFET fabrication, and address the same problem—formation of a semiconductor device structure having dimensions that are closely controlled so as to produce reliable performance. EX1004, 1:23-41, 3:29-44; EX1005, 1:19-40, 5:37-40. Lin and Liaw

are thus analogous art to each other and to the ’909 patent. Accordingly, a POSA would have had a reasonable expectation of success in modifying Lin to use techniques and processing steps to form protrusions having a lower portion with tapered sidewalls, as taught by Liaw.

104. It is also my opinion that a POSA would have understood that modifying Lin’s fabrication method to use Liaw’s etching process would merely amount to combining prior art elements (Lin’s semiconductor device fabrication methods and Liaw’s etching process) according to known methods (implementing Liaw’s etching process to form the lower portions of one or more of Lin’s protrusions 304, 306, 308, and 310) to yield predictable results (e.g., the formation of one or more of Lin’s protrusions having an upper portion with vertical sidewalls and a lower portion with tapered sidewalls).

#### b. A POSA would have been motivated to incorporate Liaw’s conductive gate strip and gate dielectric into Lin’s semiconductor device.

105. As I discussed above in Section IX.A.1.a, Lin discloses methods of manufacturing a semiconductor device structure, such as FinFET. EX1004, Abstract. Lin further discloses that its methods are applicable to, and are intended to be used for fabricating transistor devices with gate structures having conductive gate electrodes and gate insulators (or gate dielectric):

> The techniques and technologies described herein may be utilized to

> fabricate MOS transistor devices, including NMOS transistor devices, PMOS transistor devices, and CMOS transistor devices. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to any semiconductor device that includes a conductive gate electrode (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate.

EX1004, 3:18-28.

106. Moreover, Lin illustrates FinFETs 100 and 200 with gate structures 110 and 208 (EX1004, 1:29-36, FIGS. 1 and 2), but Lin does not illustrate a gate structure with a conductive gate electrode or a gate insulator (or a gate dielectric) in any of its figures, nor does Lin explicitly disclose how the conductive gate electrode and gate insulator can be formed. Though, in my opinion, a POSA would have understood that FinFETs generally include a gate structure wrapped around one or more fins (*See,* EX1004, 1:29-36, FIG. 2), a POSA would have nonetheless looked to other prior art references, such as Liaw, for guidance on how to form such gate structures having a conductive gate electrode and gate insulator.

107. Similar to Lin, Liaw discloses a method of fabricating a FinFET with a gate structure. But, Liaw additionally discloses that the method includes steps of forming the gate structure with a conductive gate strip and a gate dielectric wrapped around a semiconductor fin:

> The description relates to a **gate stack of a fin field effect transistor (FinFET)**. … The FinFET further includes a fin disposed through an opening in the insulation region to a first height above the second surface, where a base of an upper portion of the fin is broader than a top of the upper portion, wherein the upper portion has first tapered sidewalls and a third surface. The FinFET further includes **a gate dielectric** covering the first tapered sidewalls and the third surface and **a conductive gate strip traversing over the gate dielectric**, where the conductive gate strip has second tapered sidewalls along a longitudinal direction of the fin.

EX1005, Abstract.

> **a method 100 of fabricating a gate stack of a fin field effect transistor (FinFET)** according to various aspects of the present disclosure. The method 100 begins with step 102 in which a substrate is provided. The method 100 continues with step 104 in which a fin is formed in the substrate, wherein a base of an upper portion of the fin is broader than an apex of the upper portion, wherein the upper portion has first tapered sidewalls and a top surface. The method 100 continues with **step 106 in which a gate dielectric covering the first tapered sidewalls and the top surface is formed**. The method 100 continues with **step 108 in which a conductive gate strip traversing over the gate dielectric is formed**, wherein the conductive gate strip has second tapered sidewalls along a longitudinal direction of the fin.

EX1005, 2:11-23.

108. Liaw further discloses that step 108 of forming the conductive gate

strip includes patterning and etching a conductive gate electrode layer on the gate dielectric layer:

> Then, as depicted in FIGS. 7A and 7B, and step 108 in FIG. 1, the **gate electrode layer 224 is formed over the gate dielectric 222**…. In some embodiments, the **gate electrode layer 224 comprises a metal** selected from a group of W, Cu, Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr…. In some embodiments, a layer of photoresist is formed over the gate electrode layer 224 by a suitable process, such as spin-on coating, and patterned to form a patterned photoresist feature 226 over the gate electrode layer 224 by a proper lithography patterning method. The patterned photoresist feature 226 can then be transferred using a dry etching process to the underlying layers (i.e., the gate dielectric 222 and gate electrode layer 224) to form a gate stack along the longitudinal direction of the fin 212. **The patterned gate electrode layer is referred to a conductive gate strip**.

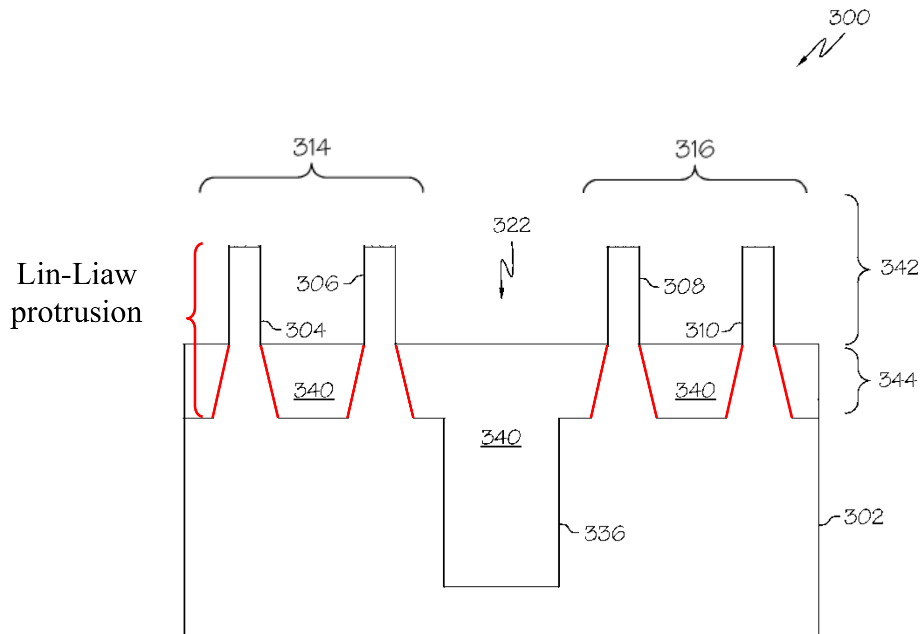
EX1005, 6:9-11, 22-25, 36-45.

109. In my opinion, a POSA would have understood that Liaw's teachings are built on the general understanding that a functioning FinFET requires a gate electrode and a gate dielectric around a semiconductor fin. Moreover, Liaw discloses that when its conductive gate strip 224b and gate dielectric 222 are formed, the resulting gate stack "can help to form a fully depleted fin when the FinFET is in on-state, thereby improving DIBL and sub-threshold leakage of the FinFET 200 and thus upgrading device performance." EX1005, 6:57-64, 7:38-43,

7:60-65. Thus, in my opinion, based on Liaw's teachings, a POSA would have been motivated to further modify Lin's FinFET fabrication process (in addition to the modification of Lin's protrusion formation process discussed in Section IX.A.1.a above) to incorporate Liaw's method of forming a conductive gate strip and a gate dielectric on a fin. Moreover, a POSA would have recognized that Liaw's techniques for forming its conductive gate strip and gate dielectric are not only applicable to and compatible with Lin's fabrication process, but are specifically intended to be used with Lin's semiconductor device structure. Besides, it would have been obvious to a POSA that modifying Lin's fabrication process to incorporate Liaw's method of forming conductive gate strip and gate dielectric would have required minimal modifications.

110. In my opinion, to incorporate Liaw's method of forming a conductive gate strip and a gate dielectric into Lin's fabrication process, the additional steps of forming a gate dielectric over the upper portions (defined as fins) of Lin-Liaw's protrusions (after the nitride caps 312 are removed), and forming a conductive gate strip over the gate dielectric would be included in Lin's fabrication process. More specifically, as I illustrate with modified versions 1-3 of Lin's Figure 10 (with annotations) below, in the combined Lin-Liaw system, Lin's modified fabrication process would include the additional sequential steps of: (1) removing Lin's nitride caps 312 by an etching process after the formation of Lin's dielectric material 340,

as illustrated in modified version 1 of Lin's Figure 10 below, (2) forming a gate dielectric ("Lin-Liaw gate dielectric") on the upper sections 342 of Lin-Liaw's protrusions (as taught by Liaw's gate dielectric 222), as illustrated in modified version 2 of Lin's Figure 10 below, (3) forming a gate electrode layer ("Lin-Liaw gate electrode") on the gate dielectric layer (as taught by Liaw's gate electrode layer 224), as illustrated in modified version 2 of Lin's Figure 10 below, and (4) etching the gate dielectric and gate electrode layer to form conductive gate strips ("Lin-Liaw conductive gate strip"; as taught by Liaw's conductive gate strip 224b), as illustrated in modified version 3 of Lin's Figure 10 below. These additional steps would then result in the formation of a completed FinFET having both a conductive gate strip and a gate dielectric, as intended by Lin. EX1004. 3:18-28.




**Modified Version 1 of Figure 10 of EX1004 (annotated).**

300
314
316
Lin-Liaw gate electrode
Lin-Liaw gate dielectric
Lin-Liaw protrusion
342
344
340
340
340
336
302

FIG. 10

**Modified Version 2 of Figure 10 of EX1004 (annotated).**

300
314
316
Lin-Liaw conductive gate strip
Lin-Liaw gate dielectric
322
Lin-Liaw protrusion
342
344
340
340
340
336
302

FIG. 10

**Modified Version 3 of Figure 10 of EX1004 (annotated).**

111. In my opinion, a POSA would not have experienced any unreasonable

technical hurdles in implementing these modifications because techniques for forming a conductive gate strip and a gate dielectric were well known and compatible with Lin's method. Thus, a POSA would have had a reasonable expectation of success in incorporating these modifications in Lin's fabrication process, as taught by Liaw. In this manner, a POSA would have understood that modifying Lin's fabrication process to explicitly include steps for forming a conductive gate strip and a gate dielectric would merely amount to combining prior art elements (Lin's semiconductor device fabrication methods and Liaw's techniques for forming its conductive gate strip and gate dielectric) according to known methods (forming a gate dielectric over the fins (after the nitride caps 312 are removed), and forming a conductive gate strip over the gate dielectric) to yield predictable results (e.g., the formation of a completed FinFET having both a conductive gate strip and a gate dielectric).

### 2. Independent Claim 1

#### a. [1.P]: A non-planar transistor, comprising:

112. Lin discloses "[a] method of manufacturing a semiconductor device structure, such as **a FinFET device structure**." EX1004, Abstract, 1:9-11, 1:58-60, FIG. 10. In my opinion, a POSA would have understood that a FinFET (fin

field-effect transistor) device structure is an example of a "*non-planar transistor*"[3], as it was well known before the '909 patent that "FinFET is the first highly manufacturable 3 dimensional non-planar transistor with fin shape channels." EX1014, 13; EX1001, 5:63-64.

113. Therefore, in my opinion, a POSA would have understood that Lin discloses "*[a] non-planar transistor*."

**b. [1.a] a substrate having an active region and an isolation region, wherein the isolation region encompasses the active region;**

114. In my opinion, Lin discloses "*a substrate having an active region and an isolation region*." Below, I reproduce Figure 10 of Lin with the "*substrate*" highlighted in yellow, "*active region[s]*" annotated in red, and the "*isolation region*" annotated in blue.[4] Referring to Figure 10, Lin discloses that "semiconductor device structure 300 utilizes a bulk semiconductor substrate, such as a bulk silicon **substrate 302**. … and bulk silicon substrate 302 is subsequently

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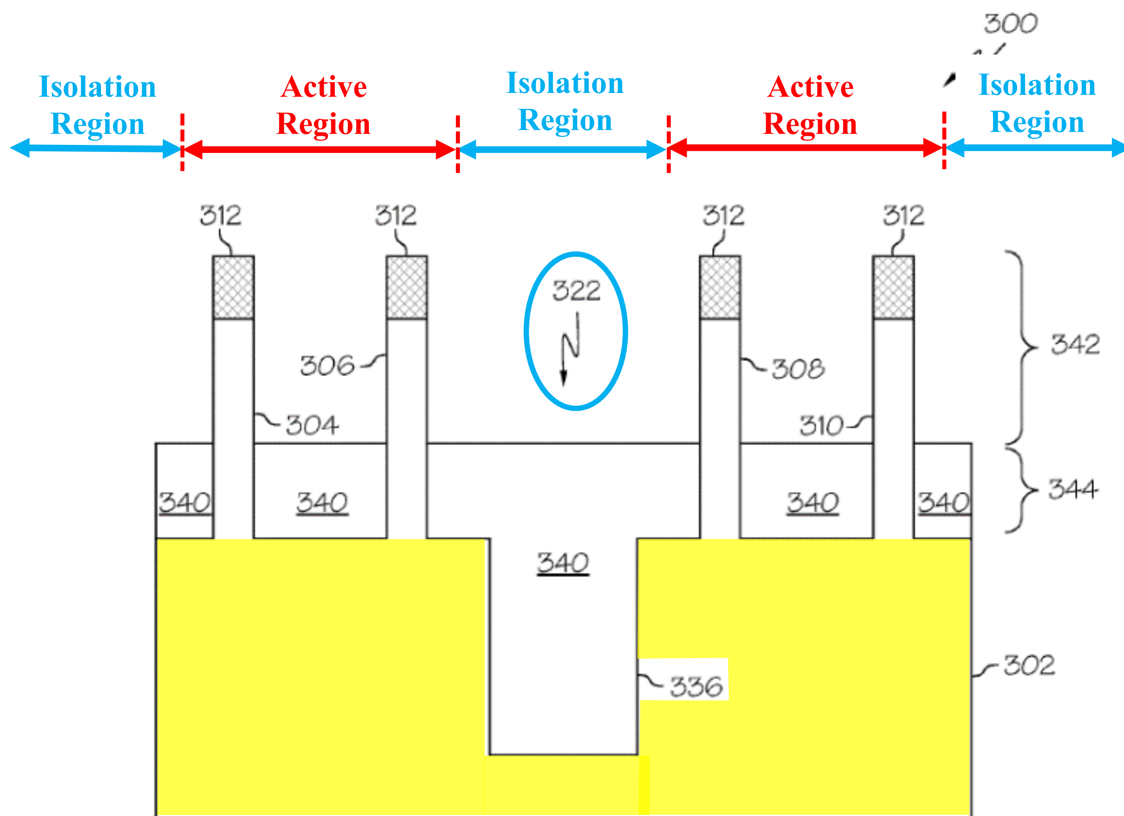
[3] Throughout the Declaration, claim language from the '909 patent is identified in italics, and language quoted from other exhibits is identified using regular font.

[4] The isolation region annotations in Figure 10 assume that there are not additional protrusions immediately to the left of protrusion 304 and to the right of protrusion 310.

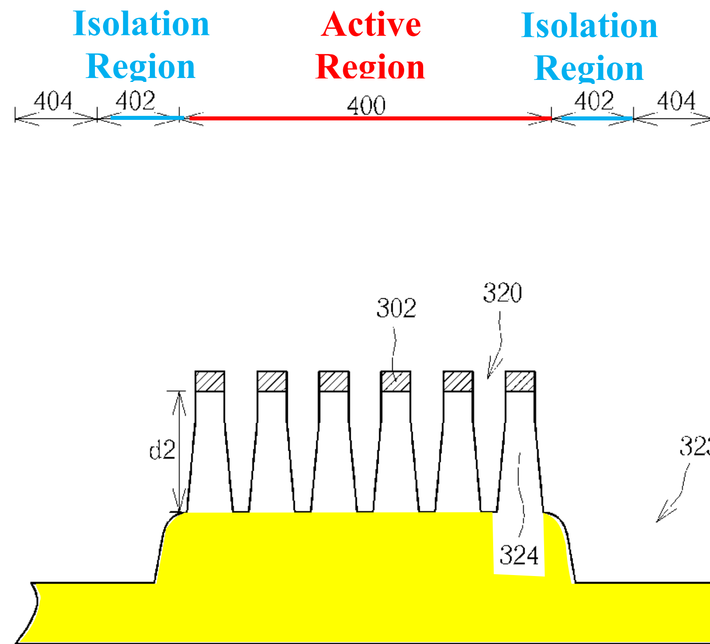
doped in an appropriate manner to form **active regions**." EX1004, 3:57-59, 3:62-65. Lin further discloses that "[t]he techniques and technologies described herein can be utilized to form **isolation regions** between adjacent FinFET devices formed on a bulk semiconductor substrate." EX1004, 3:45-47.




**EX1004, FIG. 10 (annotated).**

115. The term "*active region*" is not defined in the '909 patent. Instead, the '909 patent merely describes "*an active region*" with respect to the elements contained therein—i.e., as including (i) shallow trenches; and (ii) protruding structures residing between the shallow trenches 320, as shown in Figure 10 of the

’909 patent (reproduced and annotated) below. EX1001, 1:64-2:2, FIG. 10 (active region 400). The “*active region*” is not described as having any other defining characteristics in the ’909 patent.




**EX1001, FIG. 10 (annotated).**

116. In my opinion, a POSA would have understood that Lin’s active regions are comprised of the same elements as in the ’909 patent. Referring to Figure 10 above, Lin’s substrate 302 includes first and second active regions. The first active region includes protrusions 304 and 306, as well as the areas immediately adjacent thereto. EX1004, FIG. 10. The second active region includes protrusions 308 and 310, as well as the areas immediately adjacent thereto. EX1004, FIG. 10. Because Lin’s active regions of substrate 302 include the same

elements as the "*active region*" in the '909 patent, in my opinion, a POSA would have understood that each of Lin's active regions disclose, or render obvious, the claimed "*active region*."

117. Besides, it was well-known prior to the '909 patent that active regions include one or more protrusions. For example, as I discussed in Section VI.B above, Cho discloses that active areas include one or more protrusions extending upwardly from a semiconductor substrate. EX1011, ¶¶26, 6, 8, 14, Abstract, FIG. 1. In another example, as I discussed in Section VI.B above, Shieh discloses a method for forming FinFETs and explains that "an active region of the FinFET…includes the source/drain region and (semiconductor) fins for forming channel regions of the FinFET." EX1030, 2:40-42. Thus, in my opinion, a POSA would have understood that each of Lin's active regions of substrate 302 represent the claimed "*active region*."

118. Similarly, in my opinion, a POSA would have understood that Lin's isolation region (gap 322) represents the claimed "*isolation region*." The '909 patent again does not define the term "*isolation region*," and merely describes "*an isolation region*" with respect to the element contained therein—i.e., as including a trench deeper than the trenches included in the active region. EX1001, 2:2-4, FIG. 10 (isolation region 402).

119. Lin's isolation region of substrate 302 is comprised of the same

element as in the ’909 patent. Referring to Figure 10 above, Lin discloses an isolation region (gap 322) comprising “an isolation trench 336 in the bulk silicon substrate 302.” EX1004, 5:36-38, FIG. 10. Because Lin’s isolation region comprises the same element as the “*isolation region*” in the ’909 patent, in my opinion, a POSA would have understood that Lin’s isolation region discloses or renders obvious the claimed “*isolation region*.”

120. Lin further discloses that “*the isolation region encompasses the active region*.” Again, the ’909 patent does not explain what it means that its isolation region “*encompasses*” its active region. Nonetheless, in my opinion, a POSA would have understood that Lin’s isolation region “*encompasses*” its active regions. Indeed, Lin discloses that the purpose of isolation trench 336 in the isolation region is to “electrically isolate the two adjacent device structures from one another.” EX1004, 6:54-57. Lin also explains that the adjacent device structures are comprised of a first set of protrusions 304 and 306 (forming the first active region), and a second set of protrusions 308 and 310 (forming the second active region), respectively. EX1004, 4:11-25. A POSA would have understood that to effectively electrically isolate the two devices (or protruding structures) in the first and second active regions, isolation trench 336 would have to encompass each of the devices (or protruding structures) in the first and second active regions.

121. Besides, it was well known prior to the ’909 patent to fabricate

semiconductor devices with isolation regions surrounding active regions, similar to Lin. For example, Liaw discloses a method of forming a FinFET with its active region having protrusions that are "**surrounded** by the isolation region." EX1010, 1:39-44, claims 1 and 18. Liaw explains that it was known to design a "FinFET [that] comprises an isolation region formed in a substrate, a reverse T-shaped fin formed in the substrate, wherein a bottom portion of the reverse T-shaped **fin is enclosed by the isolation region**…." EX1010, Abstract.

122. In another example, as I discussed in Section VI.C above, Cho discloses forming a FinFET with active areas and forming isolation regions surrounding the active areas:

> An isolation hard mask is deposited and patterned overlying the plurality of fins and is used as an etch mask to **etch trenches in the substrate defining a plurality of active areas**, each of the plurality of active areas including at least a portion of at least one of the fins. The **trenches are filled with an insulating material** to isolate between adjacent active areas.

EX1011, Abstract, ¶¶6, 14.

123. In a further example, as I discussed in Section VI.C above, Shieh discloses forming a FinFET with an active region and forming an isolation region encircling the active region:

> The patterned hard mask 30 is then used to pattern substrate 20,

> resulting in trenches 34. The regions of substrate 20 covered by hard mask 30 are left un-recessed, forming active region 36 and large-pitch active region 38, while the uncovered portions are recessed. **The resulting trenches 34 may encircle (in the top view) active region 36** and large-pitch active region 38…. A dielectric material is then filled into trenches 34, followed by a chemical mechanical polish (CMP) to remove the excess dielectric material over silicon nitride layer 22, leaving insulation regions 40.

EX1030, 3:27-33, 3:40-43, FIGS. 4, 5B, 14B, 15.

124. Moreover, Lin explains that electronic isolation is achieved by "form[ing] isolation regions **between** adjacent FinFET devices formed on a bulk semiconductor substrate." EX1004, 3:45-47. Thus, a POSA would have understood that as more of Lin's devices in active regions are formed in a repeating pattern on Lin's bulk substrate 302, the isolation regions would naturally be formed between adjacent devices to isolate each device from adjacent devices on all four sides of the device. As a result, each device in the active region would be encompassed by an isolation region. Such isolation regions between repeating patterns of devices in active regions were well known to a POSA in the field of FinFET technology. For example, Jan discloses forming a system-on-chip (SoC) with a repeating pattern of logic transistors having protruding structures (active regions) and a repeating pattern of high-voltage I/O transistors having protruding structures on a substrate, as shown in Figure 2 (reproduced and annotated) below. EX1035, 3.1.1-3.1.2, FIG.

2. A POSA would have understood that for the SoC to function effectively, each of these transistors in the repeating patterns would be electrically isolated from adjacent transistors on all four sides with isolation regions.

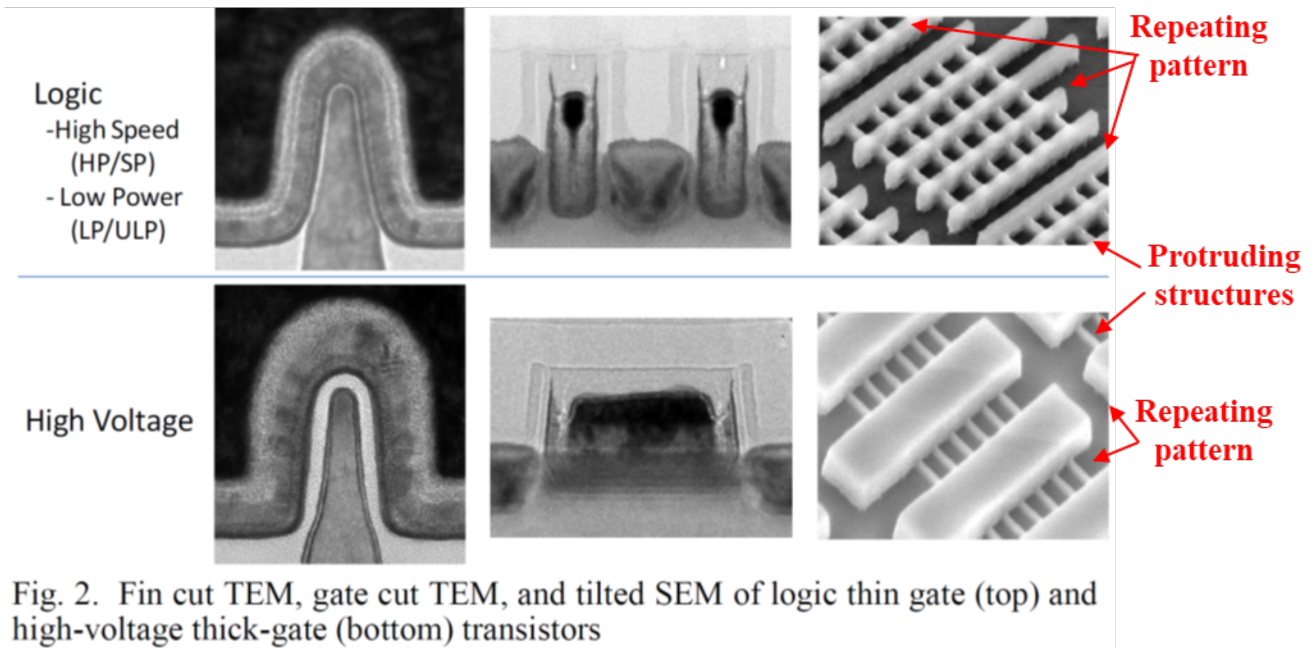
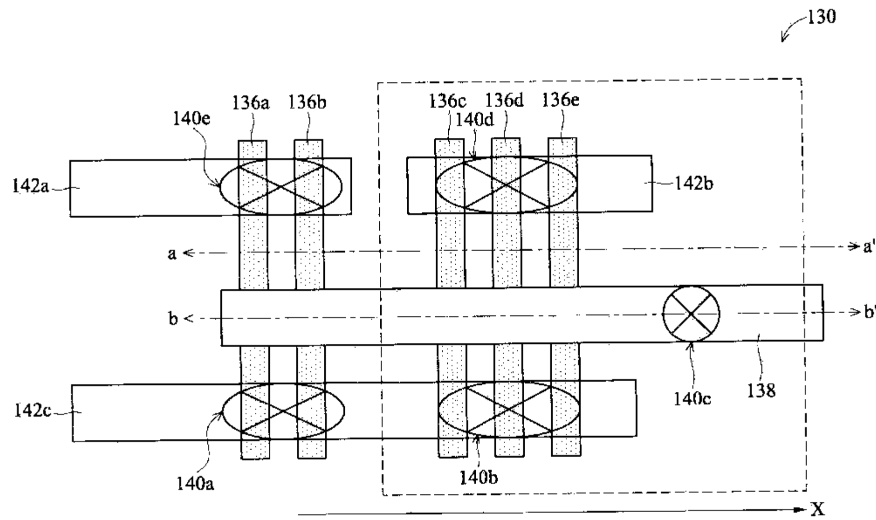



Fig. 2. Fin cut TEM, gate cut TEM, and tilted SEM of logic thin gate (top) and high-voltage thick-gate (bottom) transistors

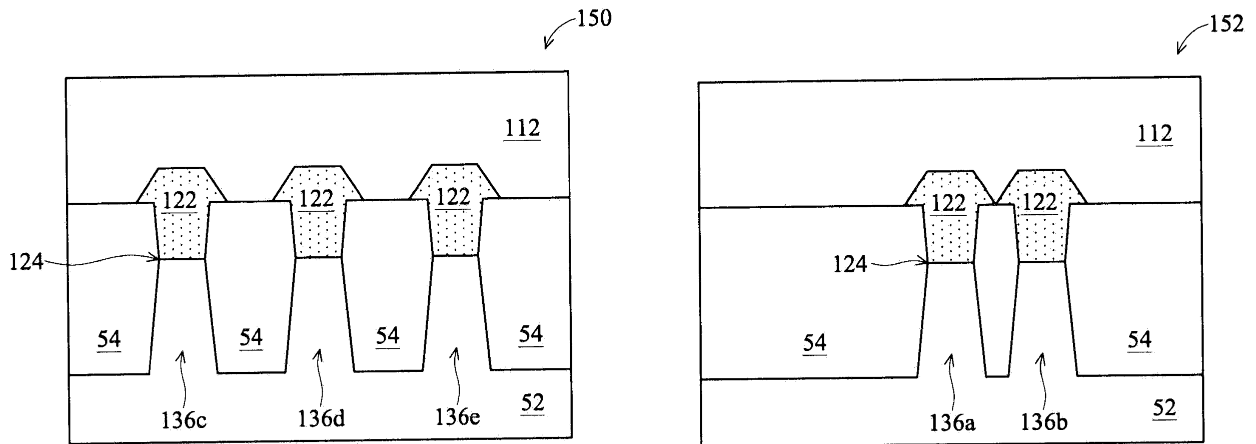
**EX1035, FIG. 1 (annotated)**

In another example, Liaw-197 discloses a **portion** of an SRAM cell having n-type FinFETs (active regions) with protrusions 136a and 136b and p-type FinFETs (active regions) with protrusions 136c-136e, as shown in Figures 5 and 10-11 reproduced below. EX1036, ¶35, FIG. 5. Liaw-197 further discloses that isolation features 54 electrically isolate the p-type FinFETs 150 with protrusions 136c-136e from the n-type FinFETs 152 with protrusions 136a and 136b, as shown in Figures 10-11 below. EX1036, ¶37, FIGS. 10-11. A POSA would have understood that Liaw-197's complete SRAM cell would have a repeating pattern of these n- and p-

type FinFETs and that these different types of FinFETs in the repeating pattern would be electrically isolated from adjacent FinFETs on all four sides with isolation features 54.



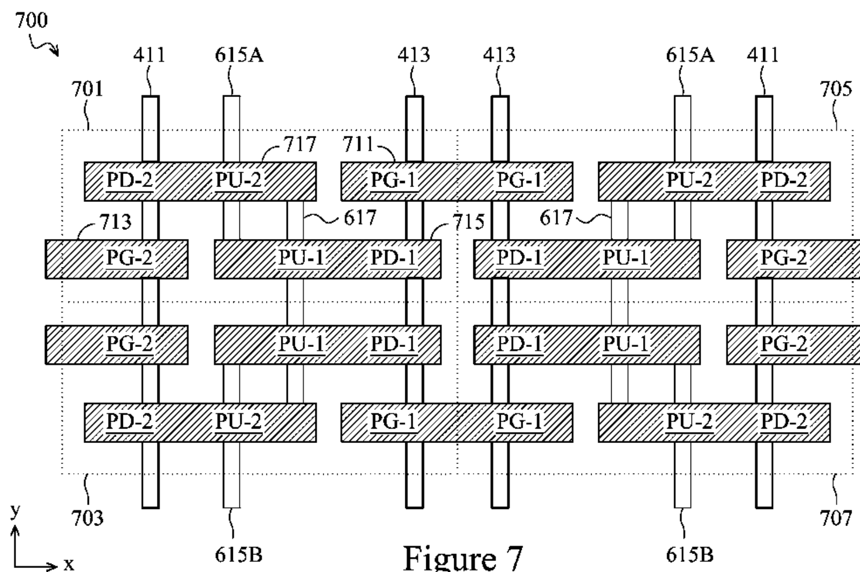

**EX1036, FIG. 5**




**EX1036, FIGS. 10 and 11**

In a further example, Liaw-813 discloses forming an array of SRAM cells 701,

703, 705, and 707 having FinFETs with protrusions 411, 413, 615A, 615B, and 617, as shown in Figure 7 reproduced below. EX1037, ¶53, FIG. 7. A POSA would have understood that each of these protrusions 411, 413, 615A, 615B, and 617 would be electrically isolated from adjacent protrusions on all four sides with isolation regions.




**EX1037, FIG. 7**

As such, in my opinion, a POSA would have understood that Lin discloses or renders obvious "*the isolation region encompasses the active region*."

125. To the extent that an argument is made that Lin does not disclose or render obvious that its isolation region "*encompasses*" its active region—which I would disagree with—in my opinion, Liaw discloses this limitation. Liaw discloses that "trenches 210 may be **continuous and surrounding the semiconductor fin 212** (shown in FIG. 3C)." EX1005, 3:50-52, 4:65-5:1, FIGS. 3C, 6C. While Liaw

only illustrates a single protrusion 212 in its figures, Liaw discloses that its teachings are applicable to FinFETs having multiple protrusions. EX1005, 1:34-37. Based on Liaw's teachings, in my opinion, a POSA would have found it obvious to form Lin's isolation trench 336 in the isolation region to be continuous and surrounding each active region including each region's protrusions (e.g., Lin's first active region having protrusions 304 and 306 and Lin's second active region having protrusions 308 and 310), as taught by Liaw. This proposed combination would have achieved Lin's goal of "electrically isolate[ing]" adjacent device structures from one another, particularly when Lin's substrate 302 includes multiple adjacent devices in active regions in a repeating pattern. EX1004, 6:54-57.

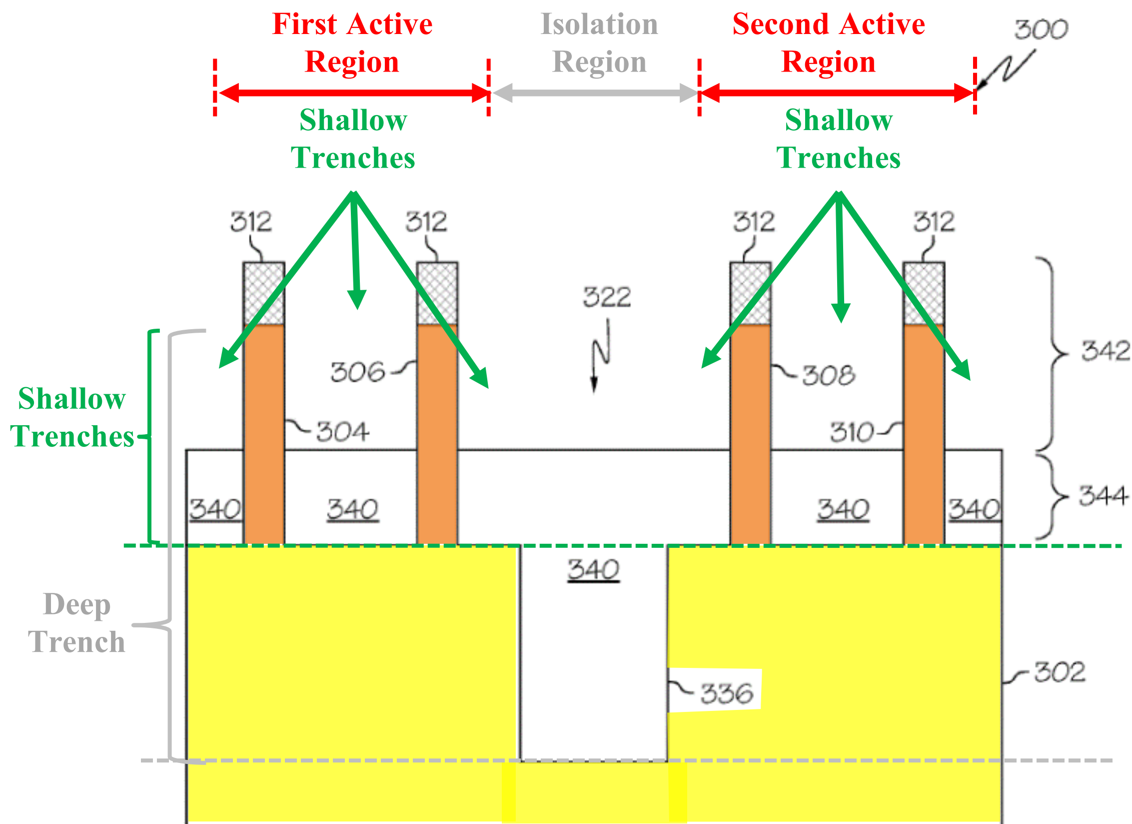
126. In my opinion, a POSA would have understood that modifying Lin's fabrication method to use Liaw's trench formation process would merely amount to combining prior art elements (Lin's fabrication process and Liaw's process of forming trenches that surround protrusions) according to known methods (forming a trench that is continuous and surrounds each active region) to yield predictable results (e.g., the formation of an isolation region that encompasses each adjacent device (active region) on Lin's substrate 302).

127. Therefore, in my opinion, a POSA would have understood that Lin both alone and in combination with Liaw discloses and renders obvious "*a*

*substrate having an active region and an isolation region, wherein the isolation region encompasses the active region*."

**c. [1.b] a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall;**

128. In my opinion, Lin discloses "*a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure*." Below, I reproduce Figure 10 of Lin with the "*active region[s]*" annotated with red arrows and texts, the "*plurality of shallow trenches*" annotated with green arrows and texts, and each "*protruding structure*" highlighted in orange.



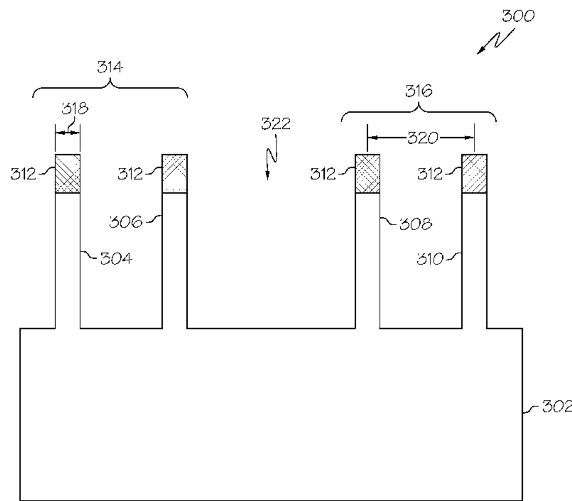

**EX1004, FIG. 10 (annotated).**

129. As I discussed in Section IX.A.2.b above, Lin discloses that substrate 302 includes a first active region comprising protrusions 304 and 306, as well as the areas immediately adjacent thereto, and a second active region comprising protrusions 308 and 310, as well as the areas immediately adjacent thereto. EX1004, FIG. 10, 4:14-17 (disclosing that each active region "may include any number of fins," and thus any number of adjacent areas forming said fins). In my opinion, a POSA would have understood that these areas immediately adjacent to protrusions 304, 306, 308, and 310 represent "*trenches*," and that each of

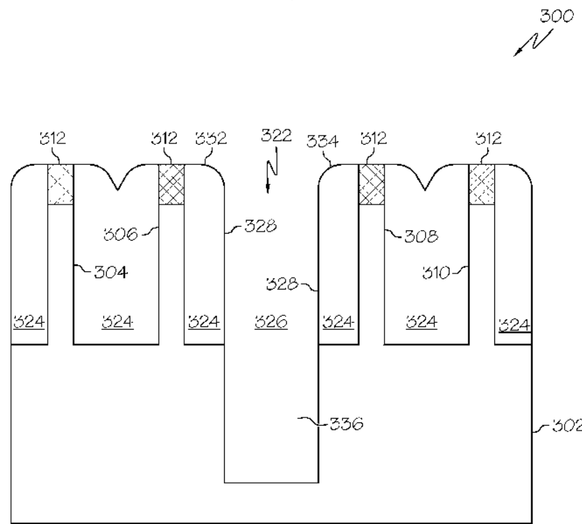
protrusions 304, 306, 308, and 310 represents "*a protruding structure*."

130. Lin also discloses that the areas ("*trenches*") between, and immediately adjacent to protrusions 304, 306, 308, and 310 are also "*disposed in the substrate*": FIGS. 3-10 "illustrate[] semiconductor device structure 300 in a state after the **formation of a plurality of conductive fins 304, 306, 308, and 310 from bulk silicon substrate 302**." EX1004, 4:1-11 (also disclosing the protrusions etched from substrate 302).

131. Moreover, a POSA would have understood that the areas ("*trenches*") between, and immediately adjacent to fins 304, 306, 308, and 310 represent "*a plurality of shallow trenches*." Because, Lin discloses that after performing an etching step on substrate 302 to form these areas and protrusions 304, 306, 308, and 310 (as shown in Figure 3 of Lin reproduced below), an additional etching step is performed on substrate 302. This additional "etching step **deepens recess 326** into bulk silicon substrate 302 **to form isolation trench 336**," as shown in Figure 6 of Lin (reproduced below). EX1004, 5:29-42. As isolation trench 336 is deeper than the areas between, and immediately adjacent to protrusions 304, 306, 308, and 310, in my opinion these areas represent the claimed "*shallow trenches*."




**EX1004, FIG. 3.**

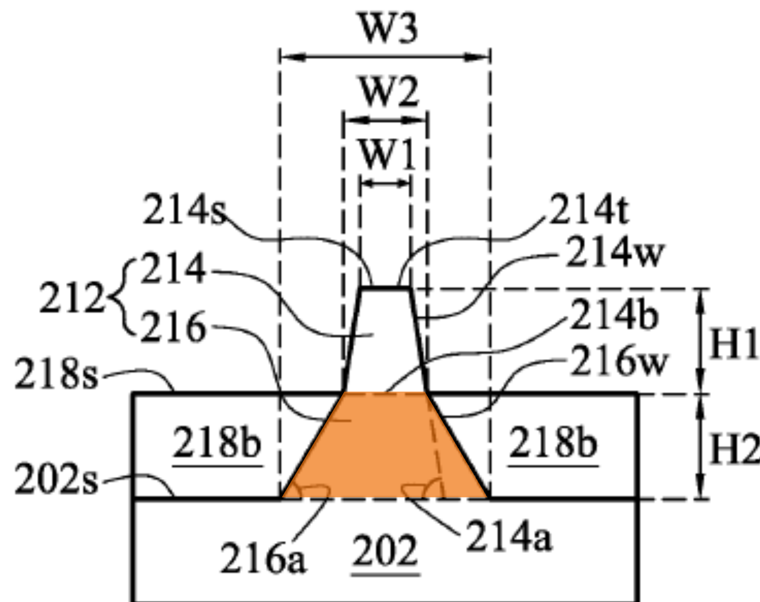



**EX1004, FIG. 6.**

132. Referring back to Figure 10 of Lin above, each of protrusions 304, 306, 308, and 310 ("*the protruding structure*") includes an upper section 342, which has "*a substantially vertical sidewall*." EX1004, 6:49-54. However, Lin does not explicitly disclose that one or more of protrusions 304, 306, 308, and 310 ("*the protruding structure*") also has "*a lower portion having a tilted sidewall*." In

my opinion, Liaw discloses this limitation.

133. Below, I reproduce Figure 6B of Liaw with the "*lower portion [of the protruding structure] having a tilted sidewall*" annotated in orange. As I discussed in Section IX.A.1.a above, Liaw discloses a method of fabricating a FinFET with a protrusion having upper and lower portions. More specifically, Liaw discloses that its FinFET includes a "**fin [that] comprises a lower portion** extending downward from the base of the upper portion to the first surface and having a second height, wherein **the lower portion has second tapered sidewalls**." EX1005, 8:20-24, 5:26-40, claim 16, 17.




**EX1005, FIG. 6B (annotated).**

134. As I discussed in Section IX.A.1.a above, a POSA would have been

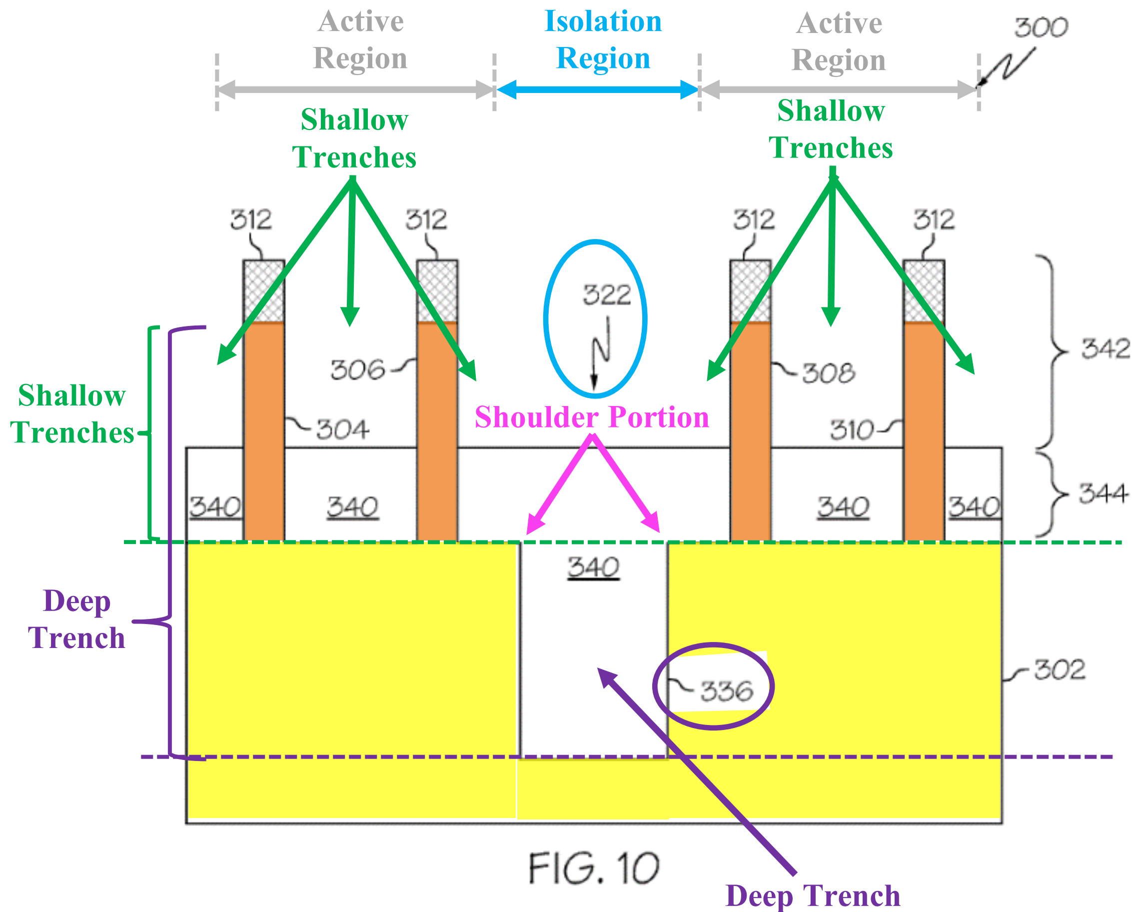
motivated to modify Lin's fabrication process to form one or more of Lin's protrusions 304, 306, 308, and 310 ("*the protruding structure*") using Liaw's etching process. This modification would result in the formation of Lin-Liaw protrusions having an upper portion with vertical sidewalls (as taught by Lin) and a lower portion with tapered sidewalls (as taught by Liaw), as I illustrated in a modified version of Lin's Figure 3 in Section IX.A.1.a above. That is, the lower portions of one or more of Lin's protrusions—e.g., the portions disposed within layer 344 of dielectric material 340—would be modified to include tapered sidewalls, as taught by Liaw.

135. Therefore, in my opinion, a POSA would have understood that the combination of Lin and Liaw discloses and renders obvious "*a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall*."

#### d. [1.c] a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion;

136. In my opinion, Lin discloses "*a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion*." Below, I reproduce Figure 10 of Lin with the

"*isolation region*" annotated with blue arrows and texts, the "*shallow trenches*" annotated with green arrows and texts, and the "*deep trench*" annotated with purple arrows and texts.

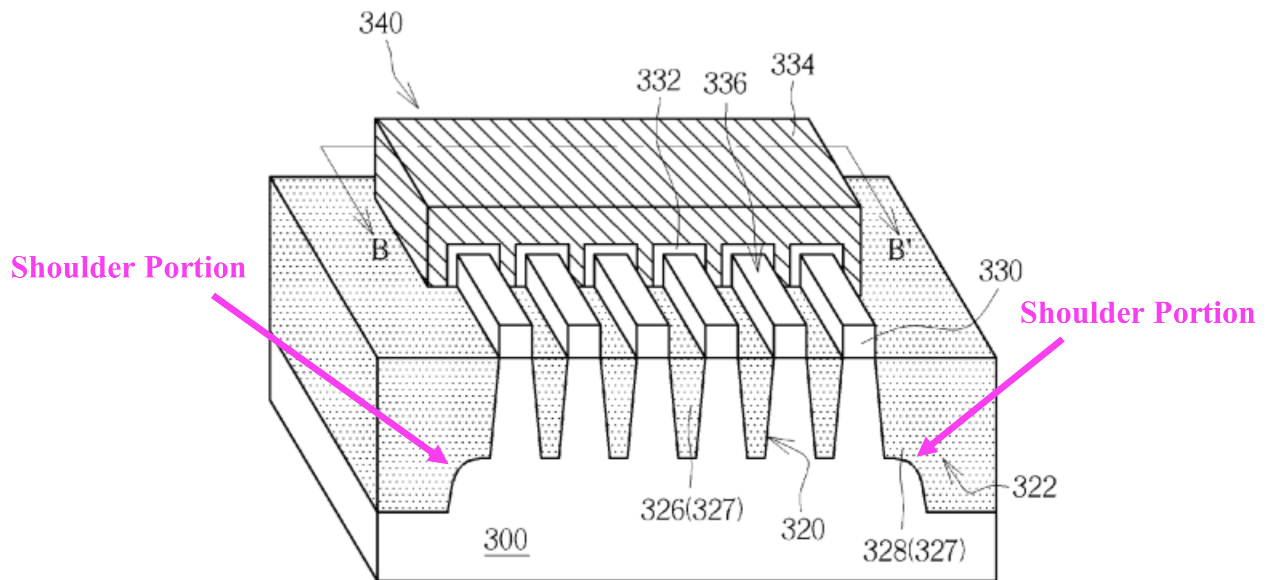



**EX1004, FIG. 10 (annotated).**

137. Referring to Figure 10 above, Lin discloses and illustrates an isolation region (gap 322) comprising "an **isolation trench 336 in the bulk silicon substrate 302**." EX1004, 5:36-38, FIG. 10. As I discussed in Section IX.A.2.c above, Lin discloses that after performing an etching step on substrate 302 to form areas ("*the shallow trenches*") between protrusions 304, 306, 308, and 310, an

additional etching step is performed on substrate 302. This additional "etching step **deepens recess 326** into bulk silicon substrate 302 **to form isolation trench 336.**" EX1004, 5:29-42. As isolation trench 336 is deeper than the areas ("*the shallow trenches*") between, and immediately adjacent to protrusions 304, 306, 308, and 310, in my opinion a POSA would have understood that isolation trench 336 is "*a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches*."

138. Referring to Figure 10 above, Lin further illustrates that isolation trench 336 ("*the deep trench*") has "*a shoulder portion*" (annotated with pink arrows and texts) at both the top left and top right corners, where the sidewalls of isolation trench 336 meet the upper surface of substrate 302. In my opinion, these top left and right corners represent the claimed "*shoulder portion[s]*" as they are in substantially similar locations as the alleged shoulder portions in Figure 13 (annotated and reproduced below) of the '909 patent. Applicant relied on Figure 13 of the '909 patent for support when adding the "*shoulder portion*" and "*the shoulder portion includes a round corner*" (claim 5) limitations to the claims during prosecution. *See* EX1002, 94-95.



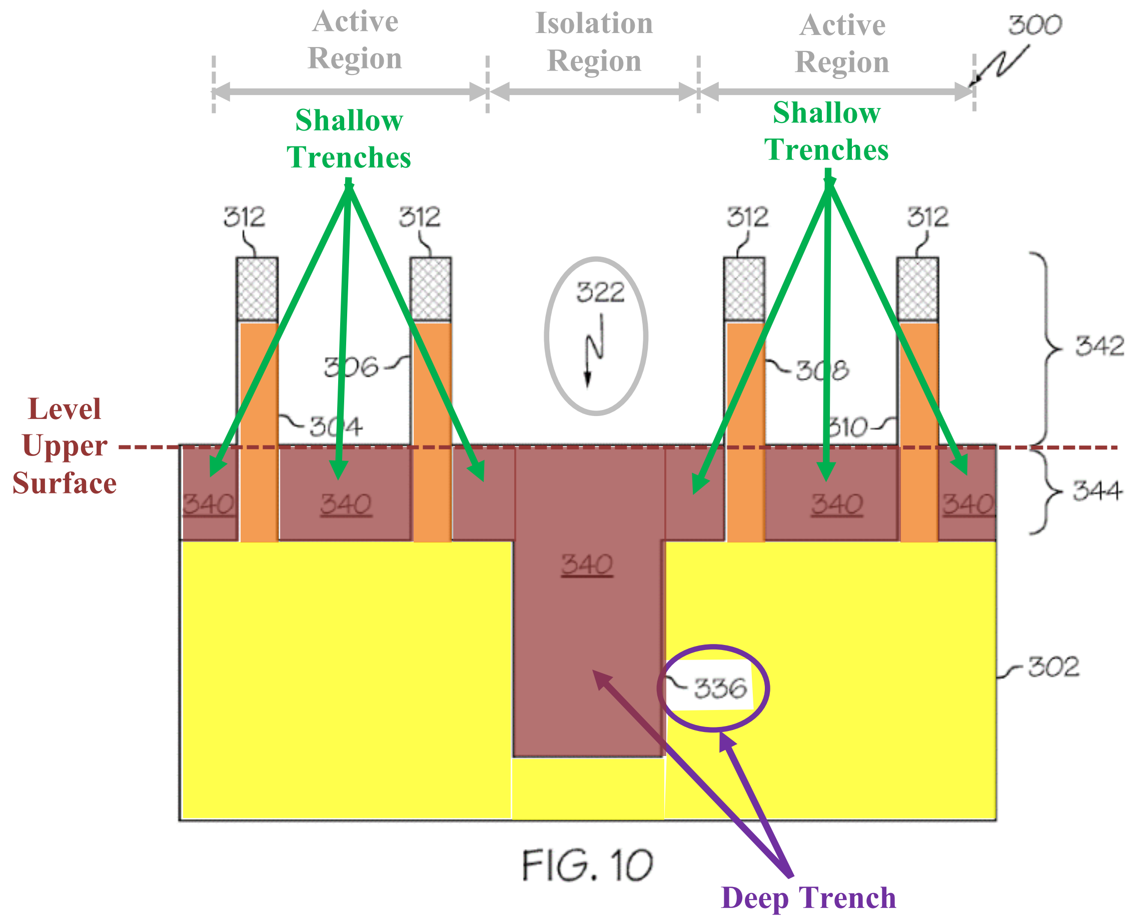

**EX1001, FIG. 13 (annotated).**

139. Therefore, in my opinion, a POSA would have understood that Lin discloses "*a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion*."

**e. [1.d] an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench;**

140. In my opinion, Lin discloses "*an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench*." Below, I reproduce Figure 10 of Lin with the "*shallow trenches*" annotated with green

arrows and texts, the "*deep trench*" annotated with purple arrows and texts, and the "*isolation layer*" having a uniform upper surface highlighted in maroon.



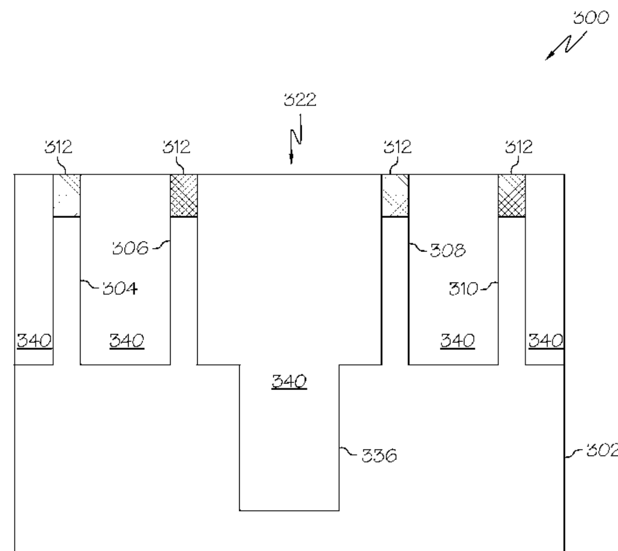

**EX1004, FIG. 10 (annotated).**

141. Referring to Figure 9 of Lin (reproduced below), Lin discloses depositing a dielectric material 340 ("*an insulation layer*") after the formation of areas ("*the shallow trenches*") between protrusions 304, 306, 308, and 310 and the formation of the isolation trench 336 ("*the deep trench*"):

> In practice, **a dielectric material 340 can be formed in isolation trench 336, over conductive fins 304, 306, 308, and 310, over silicon nitride caps 312,**

> **and over bulk silicon substrate 302** using, for example, an appropriate deposition technique such as chemical vapor deposition. In certain embodiments, **the dielectric material 340 is silicon dioxide** deposited using tetraethyl orthosilicate (TEOS) as a silicon source (commonly referred to as TEOS oxide). **FIG. 9 illustrates the condition of semiconductor device structure 300 after deposition of dielectric material 340**, and after dielectric material 340 has been polished or planarized. For example, chemical mechanical polishing may be performed to polish the TEOS oxide to the height of the conductive fin structures.

EX1004, 6:17-31.




**EX1004, FIG. 9.**

142. As Lin explains that its dielectric material 340 is silicon oxide and Lin discloses that "an insulator material [is] … an oxide (preferably, silicon oxide)," a POSA would have understood that Lin's dielectric material 340 represents "*an insulation layer*." EX1004, 4:56-61. Moreover, Lin confirms that the dielectric

material 340 "serves to electrically isolate" adjacent devices on the substrate 302. EX1004, 6:54-57, claim 12. Thus, in my opinion, a POSA would have understood that Lin discloses "*an insulation layer disposed in the shallow trenches and the deep trench.*"

143. Referring to Figure 10 of Lin above, Lin further discloses uniformly recessing the height of the dielectric material 340 ("*the insulation layer*") in the areas ("*the shallow trenches*") between protrusions 304, 306, 308, and 310 ("*protruding structure*") and in the isolation trench 336 ("*the deep trench*"):

> **after the formation of dielectric material 340** as shown in FIG. 9, this example **continues by reducing the height of dielectric material 340**. FIG. 10 depicts the state of semiconductor device structure 300 after at least a portion of dielectric material 340 has been removed. In preferred embodiments, dielectric material 340 is removed during a timed endpoint etch that selectively etches the TEOS oxide material while leaving the conductive fins, the caps 312, and bulk silicon substrate 302 substantially intact. In this regard, **the duration of the etching step is controlled** to achieve the desired remaining height of the TEOS oxide material, and **such that the layer of dielectric material 340 is uniformly recessed**. Referring to FIG. 10, the etching of dielectric material 340 exposes an upper section 342 of each conductive fin structure. In other words, silicon nitride caps 312 and the upper lengths of the conductive fins become exposed due to the etching of dielectric material 340 to a remaining height relative to the conductive fins. **Notably, the dielectric material 340 that resides in isolation trench 336 is**

> **preserved.** This serves to electrically isolate the two adjacent device structures from one another. Moreover**, a layer 344 of the dielectric material 340 is retained at the base of the conductive fins**.

EX1004, 6:36-58.

144. In my opinion, at least based on the above teachings of Lin and the illustration of the uniform top surface of dielectric material 340 in Figure 10 of Lin, a POSA would have understood that "*an upper surface*" of dielectric material 340 ("*the insulation layer*") in the areas ("*the shallow trenches*") between protrusions 304, 306, 308, and 310 is "*level*" with that in the isolation trench 336 ("*the deep trench*").

145. Therefore, in my opinion, a POSA would have understood that Lin discloses "*an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench*."

#### f. [1.e] a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure;

146. In my opinion, Lin discloses this limitation for the same reasons as I discussed above for claim limitations [1.b] and [1.d]. For example, as I discussed in Sections IX.A.2.c and IX.A.2.e above, each of Lin's protrusions 304, 306, 308, and 310 represents "*a protruding structure*" and an upper section 342 of each protrusions 304, 306, 308, and 310 is exposed by the etching of dielectric material

340. EX1004, 6:49-50, FIGS. 3-10. As the upper section 342 ("*a portion*") of each protrusions 304, 306, 308, and 310 ("*the protruding structure*") "*protrudes over*" the dielectric material 340 ("*an insulation layer*"), the upper section 342 of each protrusions 304, 306, 308, and 310 represents the claimed "*fin structure*." Therefore, in my opinion, Lin discloses "*a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure*."

#### g. [1.f] a conductive layer disposed on the fin structure; and

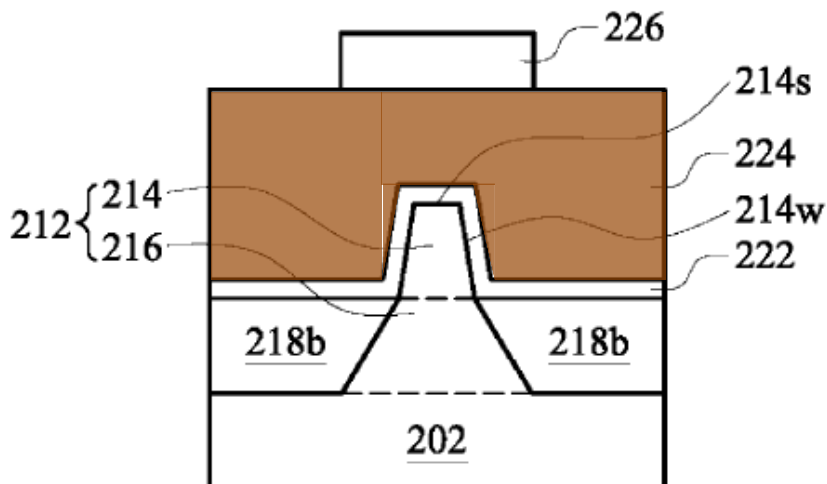
147. As I discussed above in Section IX.A.1.b, Lin discloses methods of manufacturing a semiconductor device structure (e.g., FinFET), which are applicable to, and are intended to be used for fabricating transistor devices with gate structures having conductive gate electrodes and gate insulators (or gate dielectric):

> The techniques and technologies described herein may be utilized to fabricate MOS transistor devices, including NMOS transistor devices, PMOS transistor devices, and CMOS transistor devices. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to an**y semiconductor device that includes a conductive gate electrode** (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate.

EX1004, 3:18-28.

148. Moreover, Lin illustrates FinFETs 100 and 200 with gate structures 110 and 208 (EX1004, 1:29-36, FIGS. 1 and 2), but Lin does not illustrate such a conductive gate electrode in any of its figures, nor does Lin explicitly disclose how the conductive gate electrode can be formed. Nevertheless, a POSA would have understood that Lin's FinFETs would include a conductive gate electrode, or would have found it obvious that Lin's FinFETs would include a conductive gate electrode because a gate electrode is one of the key elements of a FinFET. As I discussed above in Section IX.A.1.b, Liaw provides such teaching—guidance on how to form such conductive gate electrodes on fin structures that protrude over insulation regions.

149. Below, I reproduce FIG. 7B of Liaw with the "*conductive layer*" highlighted in brown.




**EX1005, FIG. 7B (annotated).**

150. Referring to Figure 7B above, Liaw discloses that "**gate electrode layer 224** is formed over the gate dielectric 222" and the "gate electrode layer 224 **cover[s] the upper portion 214 of the semiconductor fin 212** … [or] … the upper portion 214 of more than one semiconductor fin 212 (not shown), so that the resulting FinFET comprises more than one fin." EX1005, 6:9-17, FIGS. 7A, 7B, Section IX.A.1.b. Liaw further discloses that "the gate electrode layer 224 comprises a metal selected from a group of W, Cu, Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr" and explains that its "gate electrode layer is referred to a conductive gate strip." EX1005, 6:23-25, 6:44-45, Section IX.A.1.b. Thus, in my opinion, a POSA would have understood that Liaw's gate electrode layer 224 represents "*a conductive layer*."

151. As I discussed in Section IX.A.1.b above, based on Liaw's teachings, a POSA would have been motivated to modify Lin's FinFET fabrication process to incorporate Liaw's method of forming gate electrode layer 224. A POSA would have found it obvious to combine Liaw's gate electrode layer 224 with Lin's semiconductor device structure 300 to dispose gate electrode layer 224 over one or more of the upper sections 342 of Lin-Liaw's protrusions, as taught by Liaw, to form the resulting structures as I illustrated with modified versions 1-3 of Lin's Figure 10 in Section IX.A.1.b above.

152. In my opinion, the proposed Lin-Liaw combination merely makes

explicit a well-known fabrication step that is already contemplated and specifically intended in Lin. EX1004, 3:18-28. A POSA would have known that a functioning FinFET requires a gate electrode around a semiconductor fin. As I discussed in Section VI.A above, FinFETs with gate structures having gate electrodes were well known since the early 2000s and were developed by major semiconductor companies like Intel, IBM, TSMC, and Samsung. EX1020, 123-126; EX1026, 881-882; EX1027, Abstract; EX1028, 135-136.

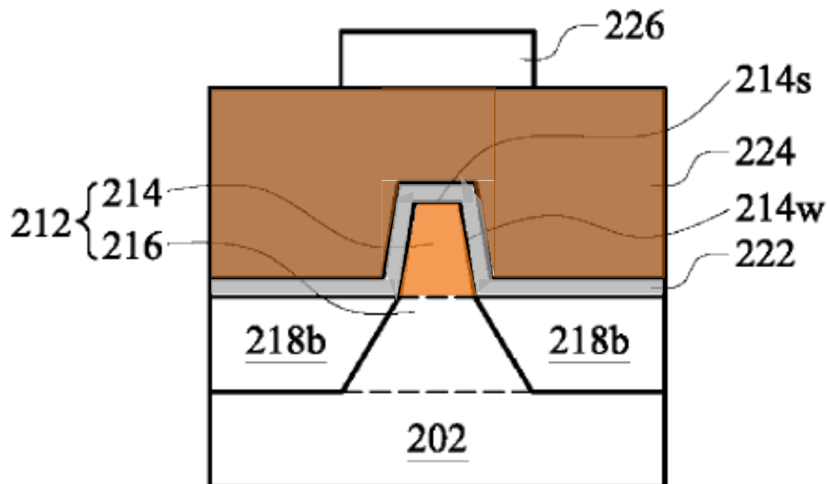
153. Therefore, in my opinion, a POSA would have understood that the combination of Lin and Liaw discloses and renders obvious "*a conductive layer disposed on the fin structure*."

#### h. [1.g] a gate dielectric layer disposed between the fin structure and the conductive layer.

154. Lin discloses that its described "techniques and technologies … may be utilized to fabricate MOS transistor devices," which refers "to any semiconductor device that includes **a conductive gate electrode** (whether metal or other conductive material) that is **positioned over a gate insulator** (whether oxide or other insulator) **which, in turn, is positioned over a semiconductor substrate**." EX1004, 3:18-28. Thus, a POSA would have understood that Lin's fabrication process is intended to be used to form devices having a gate insulator. But, Lin does not illustrate such a gate structure with a gate insulator (or a gate

dielectric) in any of its figures, nor does Lin explicitly disclose how the gate insulator can be formed. Nevertheless, a POSA would have understood that Lin's FinFETs would include a gate insulator, or would have found it obvious that Lin's FinFETs would include a gate insulator because a gate insulator is one of the key elements of a FinFET. As I discussed above in Section IX.A.1.b, Liaw provides such teaching—guidance on how to form such gate structures having a gate dielectric between a conductive gate electrode and a fin structure.

155. Below, I reproduce FIG. 7B of Liaw with the "*gate dielectric layer*" highlighted in gray, the "*conductive layer*" highlighted in brown, and the "*fin structure*" highlighted in orange.




**EX1005, FIG. 7B (annotated).**

156. Referring to Figure 7B above, Liaw discloses "**forming a gate dielectric 222 to cover** the first tapered sidewalls 214*w* and the third surface 214*s*

of **the upper portion 214 [of protrusion 212]**." EX1005, 5:48-54, FIGS. 7A, 7B. Subsequently, "**gate electrode layer 224 is formed over the gate dielectric 222**." EX1005, 6:9-13, FIGS. 7A, 7B.

157. As I discussed in Section IX.A.1.b above, based on Liaw's teachings, a POSA would have been motivated to modify Lin's FinFET fabrication process to incorporate Liaw's method of forming gate dielectric 222. A POSA would have found it obvious to combine Liaw's gate dielectric 222 with Lin's semiconductor device structure 300 to dispose gate dielectric 222 between one or more of the upper sections 342 of Lin-Liaw's protrusions and Liaw's gate electrode layer 224, as taught by Liaw, to form the resulting structures as I illustrated with modified versions 1-3 of Lin's Figure 10 in Section IX.A.1.b above.

158. In my opinion, the proposed Lin-Liaw combination merely makes explicit a well-known fabrication step that is already contemplated and specifically intended in Lin. EX1004, 3:18-28. A POSA would have known that a functioning FinFET requires a gate dielectric around a semiconductor fin. As I discussed in Section VI.A above, FinFETs with gate dielectric disposed between gate electrode and fin structures were well known since the early 2000s and were developed by major semiconductor companies like Intel, IBM, TSMC, and Samsung. EX1020, 123-126; EX1026, 881-882; EX1027, Abstract; EX1028, 135-136.

159. Therefore, in my opinion, a POSA would have understood that the

combination of Lin and Liaw discloses and renders obvious "*a gate dielectric layer disposed between the fin structure and the conductive layer*."

### 3. Dependent Claim 2: wherein the upper portion has a height between 200 and 400 angstroms.

160. Lin discloses that "[f]or certain embodiments, the conductive fins are about 40-70 nm [(400-700 angstroms)] high." EX1004, 4:35-36. A POSA would have understood that, at least in the embodiments where the entire protrusion height is 400 angstroms, any portion of the protrusion—including the upper portion—would necessarily be less than 400 angstroms. Therefore, in my opinion, a POSA would have found it obvious that in such embodiments, the upper portion of protrusions 304, 306, 308, and 310 would have a height less than 400 angstroms.

161. Also, in my opinion, a POSA would have found it obvious to fabricate these upper portions of the protrusions with a height of more than 200 angstroms, as taught by Liaw. Referring to Figure 6B (reproduced below), Liaw discloses that "[i]n some embodiments, a first height $H_1$ of upper portion 214 [of protrusion 212] above the second surface 218s is in the range of about 20 to 50 nm [(200 to 500 angstroms)]". EX1005, 5:23-25.

FIG. 6B

**EX1005, FIG. 6B.**

162. This disclosure of a protrusion with upper portion H1 having a height between 200 and 500 angstroms has significant overlap with the claimed range of "*between 200 and 400 angstroms*." Thus, in view of the above, in my opinion, the Lin-Liaw combination renders obvious claim 2.

#### 4. Dependent Claim 3: wherein the lower portion has a height between 1000 and 2000 angstroms.

163. Referring to Figure 6B (reproduced above), Liaw discloses:

> In some embodiments, a first height $H_1$ of upper portion 214 above the second surface 218s is in the range of about 20 to 50 nm. In some embodiments, **the semiconductor fin 212 further comprises a lower portion 216** extending downward from the base 214b to the first surface 202s **has a second height $H_2$.** … In yet another embodiment, **a ratio of the first height $H_1$ to the second height $H_2$ is from about 0.2 to 0.5**.

EX1005, 5:23-37.

164. Based on the values of the first height $H_1$ and the ratio between the first height $H_1$ to the second height $H_2$, a POSA would have understood that the second height $H_2$ would be in the range of about 40 to 250 nm, i.e., between 400 and 2,500 angstroms, which overlaps the claimed range of "*between 1000 and 2000 angstroms.*" Thus, in my opinion, the Lin-Liaw combination renders obvious claim 3.

**5. Dependent Claim 4: wherein the upper surface of the insulation layer is higher than the lower portion.**

165. In my opinion, the Lin-Liaw combination renders obvious claim 4. Referring to Figure 6B (reproduced above), Liaw discloses that the top surface 218b of the insulation regions 218b can be higher or lower than the base 214b of the upper portion 214 of protrusion 212: "In one embodiment, the base 214b may be coplanar with the second surface 218s, although **the base 214b may also be higher or lower than the second surface 218s**." EX1005, 5:13-16. Thus, in my opinion, a POSA would have understood that the top surface 218b of insulation regions 218b would necessarily be "*higher*" than lower portion 216 of protrusion 212 in instances where base 214b of upper portion 214 of protrusion 212 is lower than the top surface 218b of insulation regions 218b.

166. For reasons similar to those I discussed in Section IX.D.1 below, a POSA would have been motivated to modify Lin's fabrication process to form its

dielectric material 340 with an upper surface higher than the lower portion of the Lin-Liaw protrusions, as taught by Liaw. In my opinion, a POSA would have understood that the thickness of Lin's dielectric material 340 is merely a matter of design choice. Moreover, a POSA would have found it obvious to implement the upper surface of Lin's dielectric material 340 to be higher than the lower portion the Lin-Liaw protrusions because such implementation represents selecting one of a finite number of identified, predictable upper surface heights (e.g., in-line with, above, or below the top surface of the lower portion of the Lin-Liaw protrusions).

167. Furthermore, a POSA would have understood that such an implementation would ensure that the gate electrode and the gate dielectric are wrapped only around the upper sections 342 of the Lin-Liaw protrusions, which are narrower than the lower portions of the Lin-Liaw protrusions. A POSA would have known that having the gate electrode and the gate dielectric on the narrower upper sections 342 would result in improved gate control for Lin's FinFET. EX1034, 2 ("As [fin width] $W_{fin}$ shrinks, the gate control over the channel improves.")

#### 6. Dependent Claim 6: wherein each of the fin structures has a same size.

168. Lin discloses that "**[t]he conductive fins** in each set are formed such that they **have a uniform pitch and a uniform fin thickness**. In practice, the fin

pitch and thickness will typically be the same for both conductive fin sets 314 and 316." EX1004, 4:26-29, 1:37-40, 3:37-40. In my opinion, Lin's disclosure of uniform protrusions still applies to the combined Lin-Liaw structure, because the claimed "*fin structures*" merely refer to the "*portion of the protruding structure that protrudes over the insulation layer*." EX1001, 6:48-49. Thus, in my opinion, the Lin-Liaw combination renders obvious claim 6.

### B. Ground 2: The combination of Lin, Liaw, and Chang renders obvious claim 5.

#### 1. A POSA would have been motivated to combine Lin, Liaw, and Chang.

169. In my opinion, a POSA would have been motivated to modify the combined FinFET fabrication process of Lin and Liaw ("Lin-Liaw fabrication process"), as I discussed in Section IX.A1, to incorporate Chang's etching process for forming deep trenches with curved corner and sidewall profiles.

170. As I discussed in Section IX.A.1 above, Lin-Liaw fabrication process teaches a method of manufacturing a FinFET with Lin-Liaw protrusions. Lin discloses that the formation of its protrusions 304, 306, 308, and 310 are followed by an additional anisotropic etching process that "deepens recess 326 into bulk silicon substrate 302 to form isolation trench 336." EX1004, 5:29-42. The isolation trench 336 is illustrated in Lin's figures as having substantially sharp top corners where the sidewalls of isolation trench 336 meet the upper surface of substrate 302.

EX1004, FIGS. 8-10. But Lin does not explain any significance in having substantially sharp corners at the top left and right edges of isolation trench 336, as opposed to other well-known corner profiles (e.g., curved profiles), let alone in forming such sharp corners using an anisotropic etching process.

171. In my opinion, a POSA would have understood that the sharp top corners of isolation trench 336 shown in Lin's figures are for illustrative purposes. A POSA would have known that, in practice, such sharp top corners are challenging to achieve in trenches using an anisotropic etching process, particularly in deep trenches like Lin's isolation trench 336. Because, despite the vertical directional etching of the anisotropic etching process during the trench formation, there is some amount of lateral etching (i.e., undercutting) that occurs during the anisotropic etching process. This lateral etching is even more evident when deep trenches like Lin's isolation trench 336 are formed. And, a POSA would have known that such lateral etching would lead to rounding of the top trench corners during the trench formation process. For example, Engelhardt reported the formation of deep trenches in silicon substrate using an anisotropic etching process that resulted in the deep trenches having trench profiles with rounded top trench corners. EX1033, FIGS. 1-2, 1985.

172. Moreover, in my opinion, a POSA would have understood that the isotropic wet etch used in Lin to remove the oxide materials 324 following the

formation of isolation trench 336 (EX1004, 6:3-6) could itself result in a rounding of the top left and right corners of isolation trench 336. EX1018, ¶31 ("the recesses 37 beneath the undercuts 36 are subjected to an isotropic etching process, thereby making top corners of the recesses 37 rounded.").

173. To the extent that an argument is made that Lin does not render obvious rounded trench corners—which I would disagree with—in my opinion, a POSA would have understood that using an anisotropic etching process for trench formation and forming substantially sharp corners where the sidewalls of isolation trench 336 meet the upper surface of substrate 302 are merely matters of design choice. In my opinion, this understanding is also supported by the '909 patent, which does not mention the shoulder portion of its deep trench outside of the claims themselves, nor does it discuss the shoulder portion having a specific profile, or any conceivable reason for implementing one shoulder portion profile over another. Thus, in my opinion, a POSA would have been motivated to look to other prior art references, such as Chang, for teachings on what etching processes could be used to form a deep trench like Lin's isolation trench 336, and what trench corner profiles could be achieved.

174. Referring to Figures 4b and 11 (reproduced and annotated below), Chang discloses a method of fabricating a FinFET with a plurality of protrusions and deep trenches with curved sidewall profiles, which form boundaries with

sidewalls of lower portions of the outermost protrusions:

> In FIGS. 4 a and 4 b, **the exposed areas of semiconductor substrate 4 are etched to form the upper portions 81 of the fins 8.** In an embodiment, an anisotropic plasma dry etch process is conducted in a plasma etch chamber. The etchant gas may contain SF6, CF4, NF3, the like, or combinations of these. The etch process may be a time-controlled process, and continue until the upper portions 81 reach a predetermined height $h_1$ from about 5 nm to about 50 nm and a width $w_1$ from about 5 nm to 40 nm. … The embodiment in FIG. 11 may begin formation as shown in FIGS. 1 a through 4 b. After the formation of the upper portions 81 of the fins 8, **the curved profile of the lower portions 82 may be formed by an etch process**. In an embodiment, **the etch process is a plasma dry etch process** conducted in the same plasma etch chamber as the etch process for the upper portions 81. **To form the curved profile of the lower portions 82, the etch process may include varying the process parameters of the etch process during the etch process.** The time variable process parameters may include the gas flow ratio of etchant gas to passivation gas, the plasma source power, the substrate bias voltage, the bottom plate temperature, or the like.

EX1006, 3:26-34, 6:52-64.

> FIG. 11 illustrates a third embodiment in which **the outer sidewall of the lower portions 82 of the outermost fins 8 are formed to have a non-constant slope**. In this embodiment, the slope of the outer sidewall is smaller at the top of the lower portion 82 and gradually increases towards the bottom of the lower portion 82.

EX1006, 6:38-44.

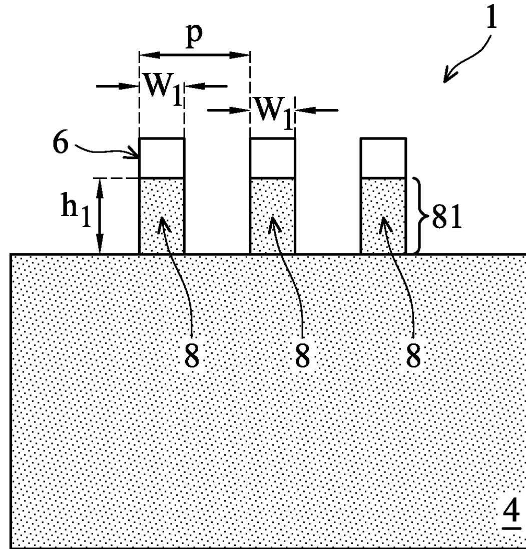
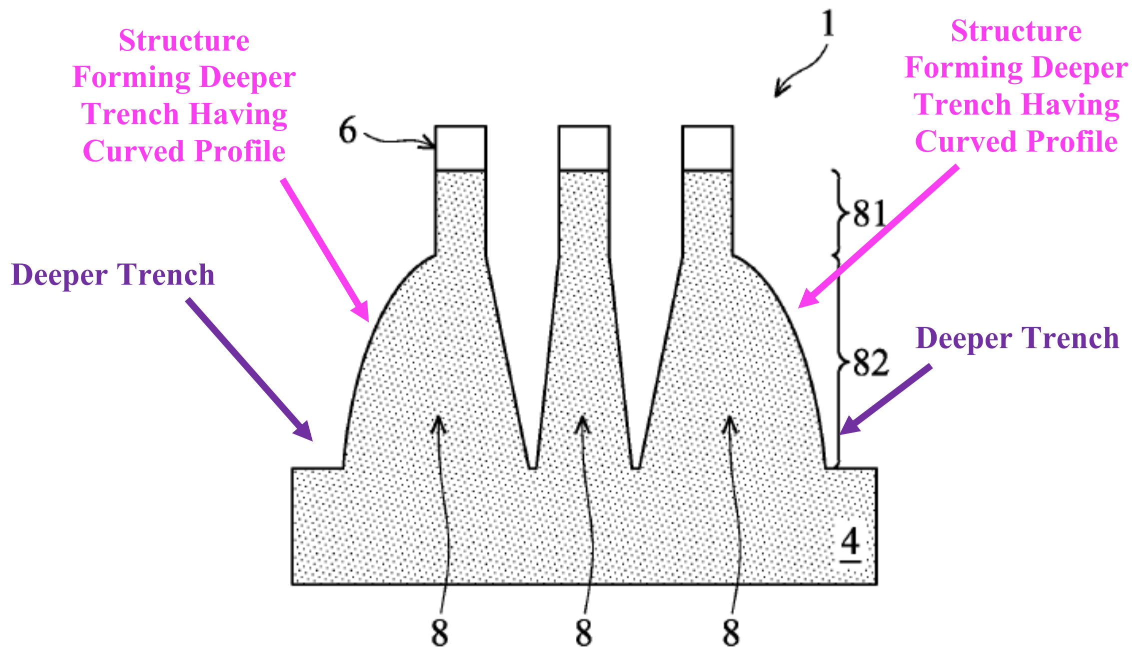



FIG. 4b

**EX1006, FIG. 4b.**




**EX1006, FIG. 11 (annotated).**

175. As I discussed above in Section VIII.B, in several instances, Chang refers to each protrusion 8 as a "semiconductor fin." EX1006, Abstract, 3:26-40. And, regardless of the terminology used, a POSA would have understood that each of Chang's protrusions 8 represents the claimed "*protruding structure*" and the upper portion 81 of each protrusion 8 represents the claimed "*fin structure*." Chang further discloses that the inner trenches between the lower portions 82 of adjacent protrusions 8 are formed with a height $h_3$, which is lower than the height $h_2$ of the outermost trenches. Thus, a POSA would have understood the inner trenches are shallow trenches and the outermost trenches are deep trenches. EX1006, 4:3-5,

10:12-13, FIG. 5b.

176. Chang explains that the disclosed sidewall profiles of the lower portions 82, including the curved sidewalls that form boundaries of the deep trenches, "may help to minimize the deformation and defects of the fins 8 caused by the depositing of a dielectric material [10] between and around the fins 8 of the FinFET device 1." EX1006, 4:15-23. In my opinion, at least based on the above teachings of Chang, a POSA would have recognized the benefits—improved performance and stability—of forming Lin's deep isolation trench 336 with curved profiles (e.g., "*a round corner*"). Besides, well before Chang (and the '909 patent), the benefits of having trenches with curved corner profiles were well known. For example, Chen discloses that "trench rounded corners at the top and bottom portions are produced with improved rounding profiles which advantageously reduces electric field strength at the corners thereby reducing current (charge) leakage and device degradation." EX1015, 4:32-36.

177. In another example, Kim discloses that

> [T]he sharp profile of the substrate may induce the electric field concentration and silicon lattice stress at the upper corners of the trench. As a result, the performance of the transistor may be deteriorated…. It is, therefore, an object of the present invention to provide a method for improving the profile of the semiconductor substrate in the vicinity of top corners of the isolation trench. The electric field concentration and

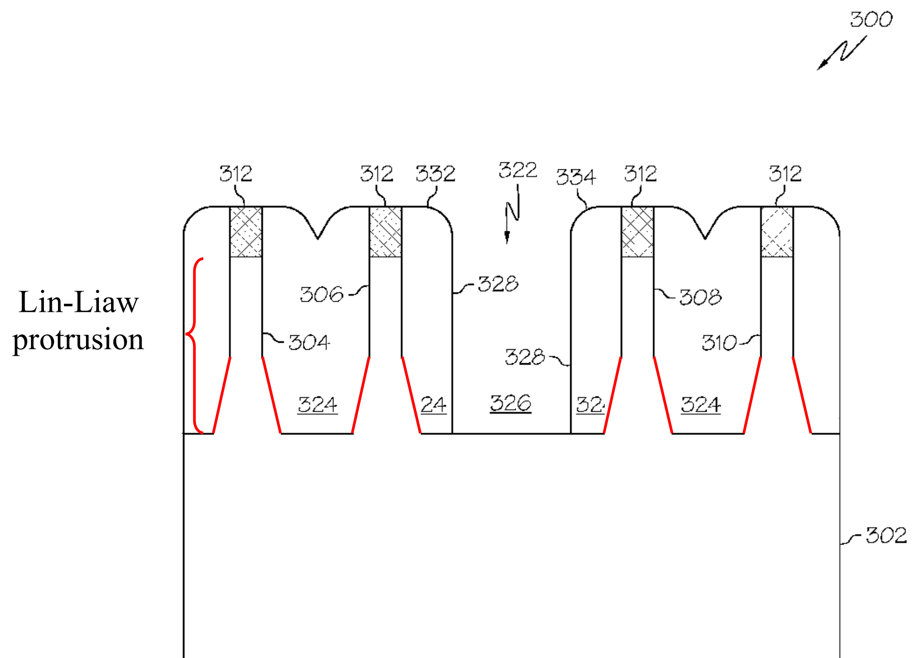
> silicon lattice damage in the vicinity of top corners of the isolation trench can be effectively prevented. … To achieve the above objects, an embodiment of a method for forming shallow trench isolation in a semiconductor device, according to the present invention, comprises the steps of: … (b) forming a trench in the substrate by etching the pad nitride, the pad oxide and the substrate; … and (d) rounding the exposed portion of the top corners of the trench by a wet chemical etch.

EX1016, 2:26-39, 2:43-52.

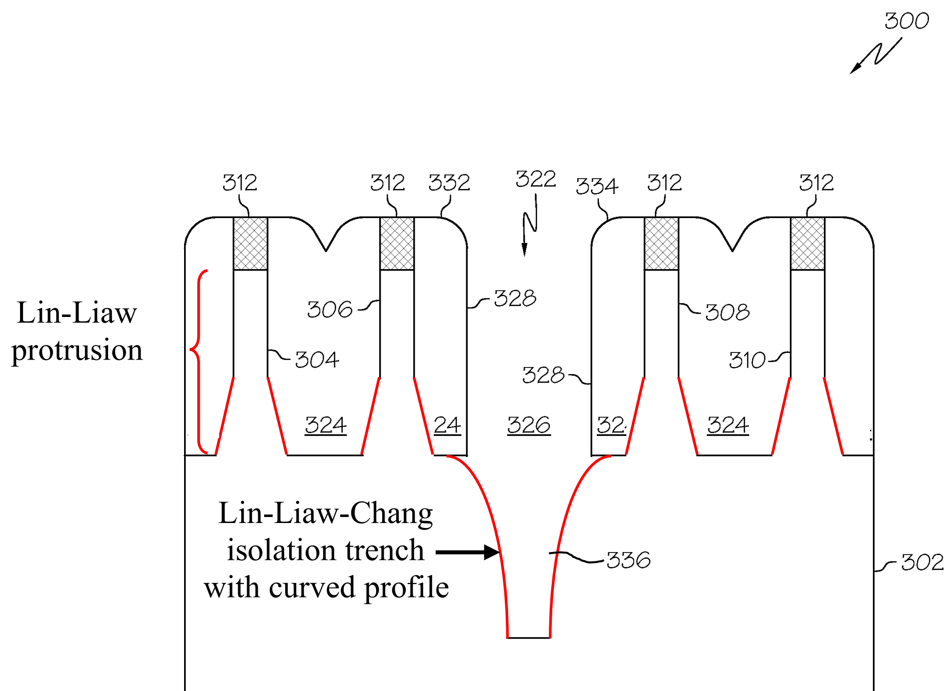
178. Thus, in my opinion, to achieve the benefits of having trenches with curved profiles in FinFETs, a POSA would have been motivated to modify the Lin-Liaw fabrication process to incorporate the techniques and processing steps of Chang to modify the shoulders (i.e., top corners) of Lin's isolation trench 336 to have curved profiles. Similar to Lin and Liaw, Chang discloses that its fabrication method can be used to form a FinFET, and can employ a photolithography process and/or an etching process. *Compare* EX1004, Abstract, 4:7-11; EX1005, Abstract, 3:7-42 *with* EX1006, Abstract, 2:9-20, 3:26-4:11. Thus, in my opinion, a POSA would have recognized that Chang's techniques are applicable to and compatible with the Lin-Liaw fabrication process, and that modifying the combined semiconductor device structure of Lin and Liaw (as shown in modified version 1 of Figure 10 in Section IX.A.1.b above) to have Lin's isolation trench 336 with curved or rounded shoulders would have required minimal modifications. A POSA

would have also recognized that such modification would have provided trench shoulder rounding in addition to the rounding of the shoulders that may already be provided by Lin's isotropic wet etch during the removal of Lin's oxide materials 324 following the formation of isolation trench 336.

179. In my opinion, in the combined Lin-Liaw-Chang system, it would have been obvious to a POSA to incorporate Chang's plasma dry etch process—used for forming the curved sidewall profiles of the lower portions 82—into Lin-Liaw fabrication process to form the shoulders of Lin's isolation trench 336. As a result, in my opinion, in the modified Lin-Liaw fabrication process, Lin's anisotropic etching process would be substituted with Chang's plasma dry etch process for etching the exposed substrate 302 of Lin-Liaw structure, as I illustrate in a modified version of Lin's Figure 5 (with annotations) below. This would result in the shoulders and sidewalls of Lin's isolation trench 336 to be formed with curved profiles, as taught by Chang, as I illustrate in a modified version of Lin's Figure 6 (with annotations) below.




**EX1006, FIG. 5 (modified and annotated).**




**EX1006, FIG. 6 (modified and annotated).**

180. In my opinion, forming the shoulders of Lin's isolation trench 336 with curved profiles would have been obvious based on the teachings of Chang at least because Chang implements its curved profiles on structures that form the boundary of the deeper trenches. EX1006, FIG. 11. Therefore, applying these techniques to the Lin-Liaw structure would similarly result in the structures (as illustrated in modified version of Lin's Figure 6) that form the boundary of isolation trench 336 to have a similar curved profile.

181. Moreover, because using a plasma dry etch process represents selecting one of a finite number of identified, predictable etch processes for use during isolation trench formation in semiconductor fabrication, a POSA would have found it obvious to use a plasma dry etch process (or similar process) in the formation of Lin's isolation trench 336, as taught by Chang. In my opinion, a POSA would not have experienced any unreasonable technical hurdles in implementing these modifications. In my opinion, a POSA would have also been motivated to substitute Chang's plasma dry etch process for Lin's anisotropic etching process, since it is merely a simple substitution of one known process for another to obtain predictable results.

182. A POSA would have been motivated to combine Lin, Liaw, and Chang because they are all in the same general field of FinFET fabrication, and address the same problem—formation of a semiconductor device structure having

dimensions that are closely controlled so as to produce efficient and reliable performance. EX1004, 1:23-41, 3:29-44; EX1005, 1:19-40, 5:37-40; EX1006, 1:6-20, 4:15-18. Lin, Liaw, and Chang are thus analogous art to each other and to the ’909 patent. Accordingly, in my opinion, a POSA would have had a reasonable expectation of success in modifying the Lin-Liaw fabrication process to use techniques and processing steps to form the shoulders of Lin’s isolation trench 336 with curved profiles, as taught by Chang.

183. Also, in my opinion, a POSA would have understood that modifying the Lin-Liaw fabrication process to use Chang’s plasma dry etch process would merely amount to combining prior art elements (the Lin-Liaw fabrication process and Chang’s plasma dry etch process) according to known methods (implementing Chang’s plasma dry etch process to form the shoulders of Lin’s isolation trench 336) to yield predictable results (e.g., forming the shoulders of Lin’s isolation trench 336 with curved profiles).

#### 2. Dependent Claim 5: wherein the shoulder portion includes a round corner.

184. As I discussed in Section IX.A.2.d above, Lin discloses isolation trench 336 (“*a deep trench*”) that includes “*a shoulder portion*” at both the top left and top right corners, where the sidewalls of isolation trench 336 meet the upper surface of substrate 302. EX1004, FIG. 10. Lin further discloses that isolation

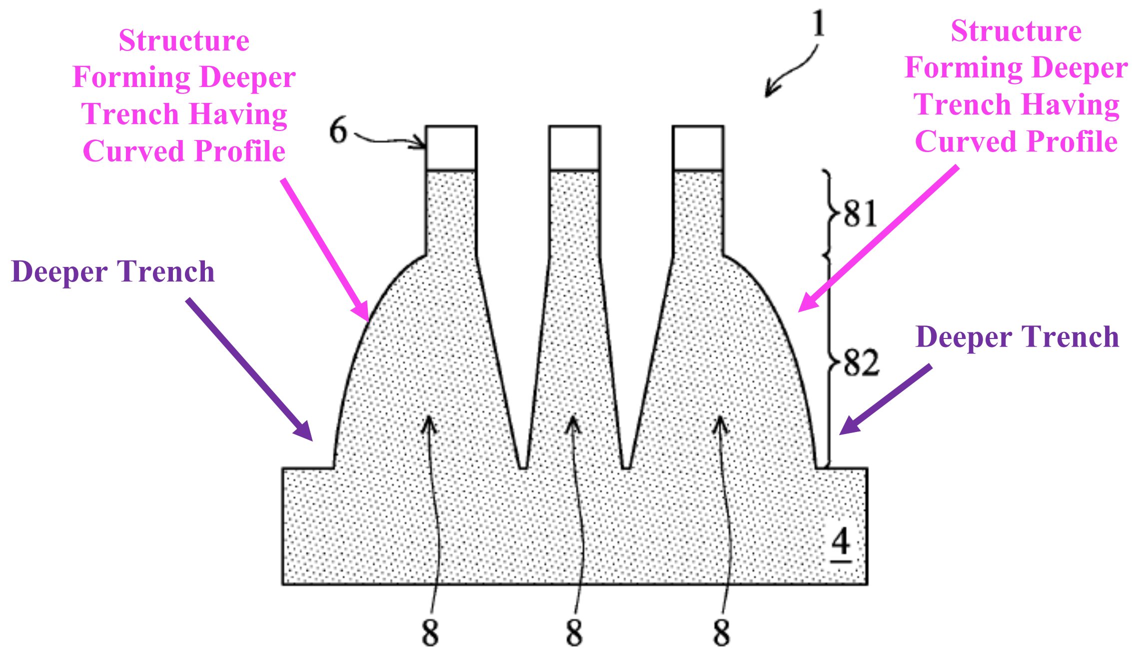
trench 336 is formed by performing an anisotropic etching process on substrate 302. EX1004, 5:29-42, FIGS. 5-6. Based on the teachings of Lin, in my opinion, it would have been obvious to a POSA that the "*shoulder portions*" of Lin's isolation trench 336 would have rounded corners.

185. In my opinion, a POSA would have understood that the sharp top corners of isolation trench 336 shown in Lin's figures are for illustrative purposes. A POSA would have known that, in practice, such sharp top corners are challenging to achieve in trenches using an anisotropic etching process, particularly in deep trenches like Lin's isolation trench 336. Because, despite the vertical directional etching of the anisotropic etching process during the trench formation, there is some amount of lateral etching (i.e., undercutting) that occurs during the anisotropic etching process. This lateral etching is even more evident when deep trenches like Lin's isolation trench 336 are formed. And, a POSA would have known that such lateral etching would lead to rounding of the top trench corners during the trench formation process. For example, Engelhardt reported the formation of deep trenches in silicon substrate using an anisotropic etching process that resulted in the deep trenches having trench profiles with rounded top trench corners. EX1033, FIGS. 1-2, 1985.

186. To the extent that an argument is made that Lin does not disclose or render obvious that "*the shoulder portion includes a round corner*"—which I

would disagree with—in my opinion, a POSA would have looked to Chang (or another prior art reference), which discloses this limitation to achieve the benefits of having trench shoulder (i.e., trench top corner) that "*includes a round corner*," as I discussed in Section IX.B.1 above.

187. Below, I reproduce Figure 11 of Chang with the curved lower portions 82 of the outermost sidewalls annotated with pink arrows and texts, and the deeper trenches annotated with purple arrows and texts. Referring to Figure 11, as I discussed in Section IX.B.1 above, Chang discloses that the outermost trenches are deeper having a height $h_2$ and the inner trenches between the lower portions 82 of adjacent protrusions 8 are shallower having a height $h_3$ "that is less than the height $h_2$" of the outermost trenches. EX1006, 4:3-5, 10:12-13, FIG. 5b. Chang further discloses that "**the outer sidewall of the lower portions 82 of the outermost fins 8 are formed to have a non-constant slope**. In this embodiment, the slope of the outer sidewall is smaller at the top of the lower portion 82 and gradually increases towards the bottom of the lower portion 82." EX1006, 6:38-44. That is, the outer sidewalls of the lower portions 82 of the outermost protrusions 8, which form the boundaries of the deeper trenches have curved profiles, as illustrated in Figure 11. EX1006, 6:53-55 ("the **curved profile of the lower portions** 82.").




**EX1006, FIG. 11 (annotated).**

188. For at least the reasons discussed in Section IX.B.1 above, in my opinion, a POSA would have been motivated to form Lin's isolation trench 336 ("*the shoulder portion*") with each of the top left and top right corners having a curved profile ("*a round corner*"), as taught by Chang.

189. Thus, in view of the above, in my opinion, the Lin-Liaw-Chang combination renders obvious claim 5.

### C. Ground 3: Chang renders obvious claims 1-3, 5, and 6.

#### 1. Independent Claim 1

##### a. [1.P]: A non-planar transistor, comprising:

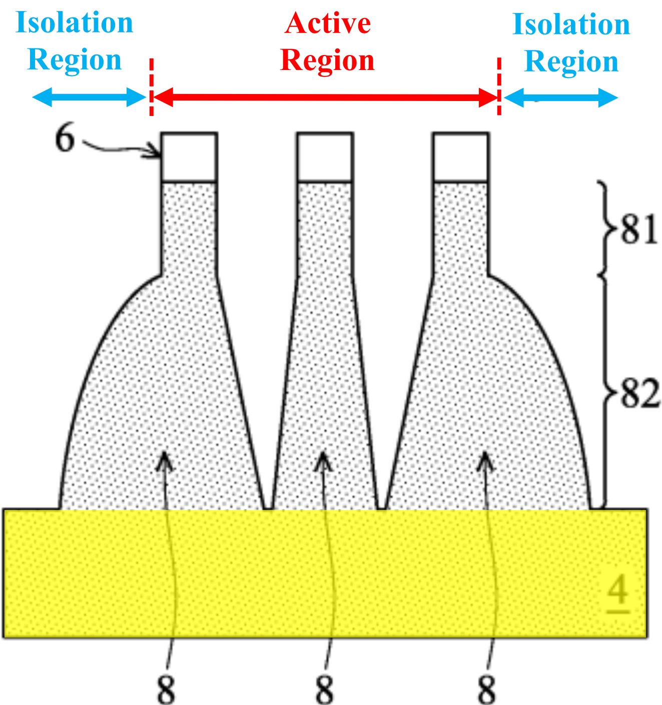
190. Chang discloses "a method for forming a **FinFET device**," and

various resulting FinFET devices. EX1006, 11:3-4, Abstract, 10:18-31, FIGS. 9a, 9b, claim 1. In my opinion, a POSA would have understood that a FinFET device is an example of a "*non-planar transistor*", as it was well known before the '909 patent that "FinFET is the first highly manufacturable 3 dimensional non-planar transistor with fin shape channels." EX1014, Park, 13; EX1001, 5:63-64.

191. Therefore, in my opinion, a POSA would have understood that Chang discloses "*[a] non-planar transistor*."

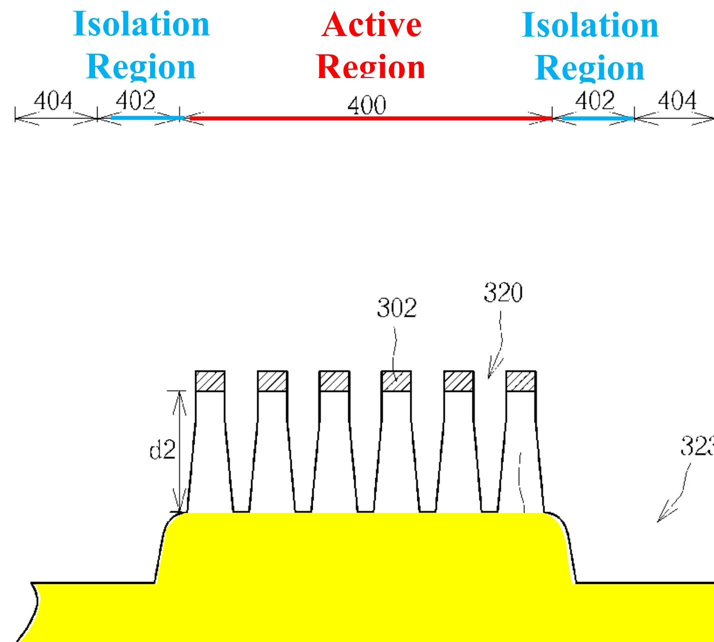
#### b. [1.a] a substrate having an active region and an isolation region, wherein the isolation region encompasses the active region;

192. In my opinion, Chang discloses "*a substrate having an active region*." Below, I reproduce Figure 11 of Chang with the "*substrate*" highlighted in yellow, the "*active region*" annotated with red arrows and texts, and the "*isolation region*" annotated with blue arrows and texts. Chang disclose "a method for forming a FinFET device … [with] a plurality of semiconductor fins over a **semiconductor substrate**." EX1006, 11:3-5. Referring to Figure 11, Chang further discloses that its FinFET device includes "trenches between the lower portions [of the fins]," where the outermost trenches are deeper having a height $h_2$ and the inner trenches between the lower portions 82 of adjacent protrusions are shallower having a height $h_3$ "that is less than the height $h_2$" of the outermost trenches. EX1006, 4:3-5, 10:8-13, FIG. 5b.




**EX1006, FIG. 11 (annotated).**

193. As I previously discussed in Section IX.A.2.b above, the ’909 patent does not define the term “*active region*.” Instead, the ’909 patent merely describes “*an active region*” with respect to the elements contained therein—i.e., as including (i) shallow trenches; and (ii) protruding structures residing between the shallow trenches, as shown in Figure 10 of the ’909 patent (reproduced and annotated) below. EX1001, 1:64-2:2, FIG. 10 (active region 400).




**EX1001, FIG. 10 (annotated).**

194. In view of the ’909 patent, Chang discloses “*a substrate having an active region*” consistent with how the term active region is used in the ’909 patent. As I discussed above, Chang’s substrate includes a region comprising a plurality of protrusions and shallow trenches there between, which are the same elements as the “*active region*” in the ’909 patent. Thus, in my opinion, a POSA would have understood that the region of Chang’s substrate comprising the plurality of protrusions and shallow trenches discloses, or renders obvious, the claimed “*active region*.”

195. Moreover, a POSA would have understood that the region comprising the plurality of protrusions is an “*active region*” because Chang discloses that there

are dopants in the protrusions. EX1006, 5:27-30. A POSA would have understood that the presence of doped regions in a substrate is an indication that these regions constitute active regions. EX1004, 3:62-65 ("substrate 302 is subsequently doped in an appropriate manner to form **active regions**"). Besides, it was well known prior to the '909 patent that active regions include one or more protrusions. For example, as I discussed in Section VI.B above, Cho discloses that active areas include one or more protrusions extending upwardly from a semiconductor substrate. EX1011, ¶¶26, 6, 8, 14, Abstract, FIG. 1. In another example, as I discussed in Section VI.B above, Shieh discloses a method for forming FinFETs and explains that "an active region of the FinFET…includes the source/drain region and (semiconductor) fins for forming channel regions of the FinFET." EX1030, 2:40-42.

196. Chang discloses "*an isolation region*" consistent with how the term isolation region is used in the '909 patent. The '909 patent does not define the term "*isolation region*," and merely describes "*an isolation region*" with respect to the element contained therein—i.e., as including a trench deeper than the trenches included in the active region, as shown in Figure 10 of the '909 patent (reproduced and annotated) above. EX1001, 2:2-4, FIG. 10 (isolation region 402).

197. Referring to Figure 11 above, Chang discloses that the outermost trenches are deeper having a height $h_2$ and the inner trenches between the lower

portions 82 of adjacent protrusions 8 are shallower having a height $h_3$ "that is less than the height $h_2$" of the outermost trenches. EX1006, 4:3-5, 10:12-13, FIG. 5b. Chang's substrate therefore includes a region comprising a deep trench. Because this region of Chang's substrate comprises the same element as the "*isolation region*" in the '909 patent, in my opinion, a POSA would have understood that the region of Chang's substrate comprising the deep trench discloses, or renders obvious, the claimed "*isolation region*."

198. Another reason a POSA would have understood Chang's substrate region comprising the deep trench to disclose, or render obvious, the claimed "*isolation region*" is because Chang discloses filling its deep trenches with a dielectric layer 10 having "one or more suitable dielectric materials such as silicon oxide, silicon nitride, low-k dielectrics such as carbon doped oxides, extremely low-k dielectrics such as porous carbon doped silicon dioxide, a polymer such as polyimide, combinations of these, or the like." EX1006, 4:30-36, FIG. 8b. A POSA would have understood that the dielectric layer 10 is an insulator, and would thus function to electrically isolate Chang's different active regions. EX1004, 6:54-57, claim 12. Thus, in my opinion, Chang has the same arrangement of protrusions, isolation materials, and trenches as the '909 patent. As a result, Chang discloses the "*active region*" and "*isolation region*" limitations, even though it does not use those terms.

199. In my opinion, a POSA would have also understood that Chang's isolation region "*encompasses*" its active regions. Chang explains that "semiconductor substrate 4 may comprise bulk silicon," but that "[o]nly a portion of the semiconductor substrate 4 is illustrated in the figures." EX1006, 2:40-42. A POSA would have understood that bulk substrate 4 would include additional active regions surrounding the active region illustrated in Figure 5b. In such instances, a POSA would have understood that the illustrated active region should be electrically isolated from each of the surrounding active regions to prevent current leakage between adjacent active regions. To achieve the benefits of electrically isolating the active regions, it would have been obvious to a POSA that Chang's deep trench including dielectric layer 10 would not only be formed on two sides of the active region as illustrated in Figure 5b, but would naturally be formed on all four sides of the active region, thereby "*encompass[ing]*" the illustrated active region and electrically isolating it from the surrounding active regions. In my opinion, this is substantially the same viewpoint shown in Figures 8 and 13 of the '909 patent, which shows the same active region being encompassed by an isolation region. Therefore, in my opinion, a POSA would have understood that Chang's isolation region "*encompasses the active region*" to the same extent that this configuration is disclosed in the '909 patent.

200. Besides it was well-known prior to the '909 patent to fabricate

semiconductor devices with isolation regions surrounding active regions, similar to Chang. For example, Liaw discloses a method of forming a FinFET with its active region having protrusions that are "**surrounded** by the isolation region." EX1010, 1:39-44, claims 1 and 18. Liaw explains that it was known that a "FinFET comprises an isolation region formed in a substrate, a reverse T-shaped fin formed in the substrate, wherein a bottom portion of the reverse T-shaped **fin is enclosed by the isolation region**…." EX1010, Abstract.

201. In another example, as I discussed in Section VI.C above, Cho discloses forming a FinFET with active areas and forming isolation regions surrounding the active areas:

> An isolation hard mask is deposited and patterned overlying the plurality of fins and is used as an etch mask to **etch trenches in the substrate defining a plurality of active areas**, each of the plurality of active areas including at least a portion of at least one of the fins. The **trenches are filled with an insulating material** to isolate between adjacent active areas.

EX1011, Abstract, ¶¶6, 14.

202. In a further example, as I discussed in Section VI.C above, Shieh discloses forming a FinFET with an active region and forming an isolation region encircling the active region:

> The patterned hard mask 30 is then used to pattern substrate 20,

> resulting in trenches 34. The regions of substrate 20 covered by hard mask 30 are left un-recessed, forming active region 36 and large-pitch active region 38, while the uncovered portions are recessed. **The resulting trenches 34 may encircle (in the top view) active region 36** and large-pitch active region 38…. A dielectric material is then filled into trenches 34, followed by a chemical mechanical polish (CMP) to remove the excess dielectric material over silicon nitride layer 22, leaving insulation regions 40.

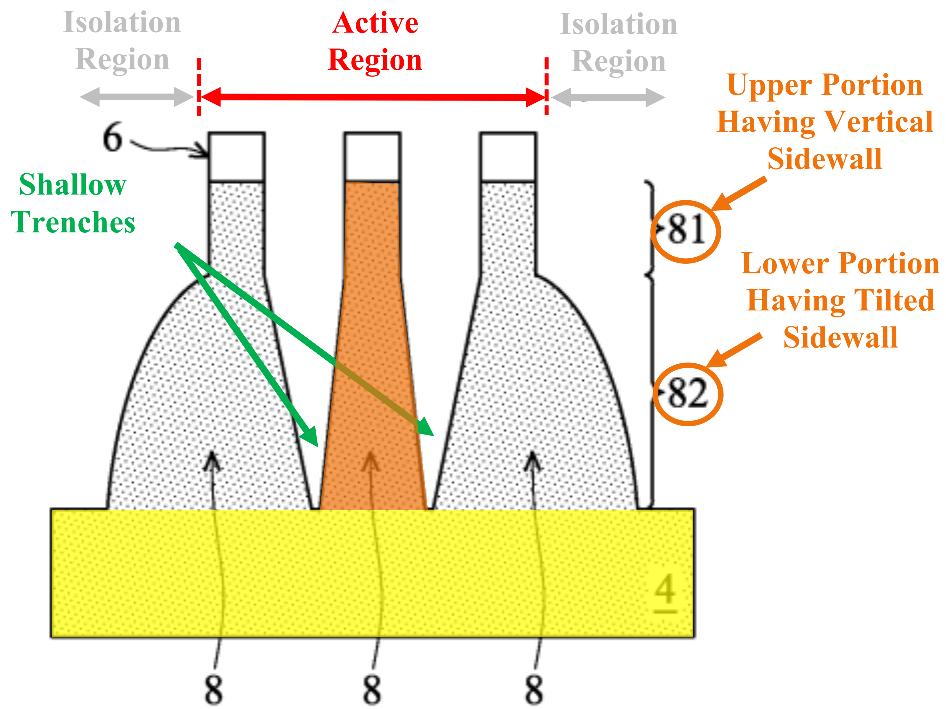
EX1030, 3:27-33, 3:40-43, FIGS. 4, 5B, 14B, 15.

203. Thus, in view of the above, in my opinion, a POSA would have understood that Chang discloses and/or renders obvious "*a substrate having an active region and an isolation region, wherein the isolation region encompasses the active region*."

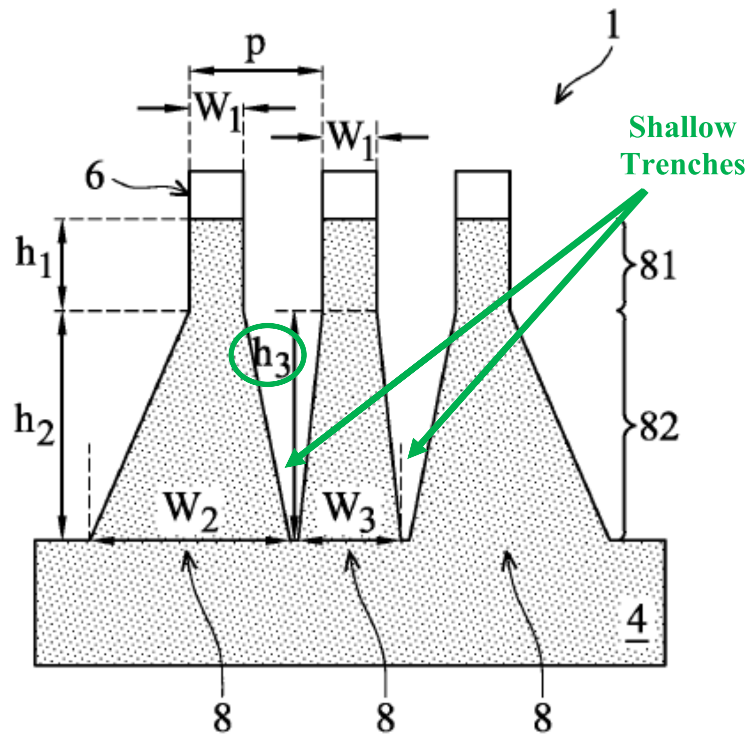
#### c. [1.b] a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall;

204. Below, I reproduce Figure 11 of Chang with the "*active region*" annotated with red arrows and texts, the "*plurality of shallow trenches*" annotated with green arrows and texts, and the "*protruding structure ha[ving] an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall*" highlighted in orange.

205. As I discussed in Section IX.C.1.b above, referring to Figure 11, Chang discloses an active region of semiconductor substrate 4 that includes a plurality of protrusions 8 over the semiconductor substrate 4 and trenches between the lower portions of the protrusions 8, where the outermost trenches are deeper having a height $h_2$ and the inner trenches between the lower portions 82 of adjacent protrusions 8 are shallower having a height $h_3$ "that is less than the height $h_2$" of the outermost trenches. EX1006, 4:3-5, 10:8-13, 11:3-5. Although not drawn to scale, Figure 5b is also annotated below showing the inner trenches ("*a plurality of shallow trenches*") having the lower height $h_3$ relative to the height of the outer trenches $h_2$. Also, as I discussed above in Section VIII.B, in several instances, Chang refers to each protrusion 8 as a "semiconductor fin." EX1006, Abstract, 3:26-40. Regardless of the terminology used, a POSA would have understood that each of Chang's protrusions 8 represents the claimed "*protruding structure*" and the upper portion 81 of each protrusion 8 represents the claimed "*fin structure*," as I explain for claim element [1.e] below. Thus, in my opinion, Chang discloses an active region that includes "*a plurality of shallow trenches … wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure*."




**EX1006, FIG. 11 (annotated).**




**EX1006, FIG. 5 (annotated).**

206. Chang also discloses that "*the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall*." Referring to Figure 11 above, Chang discloses that "the exposed areas of semiconductor substrate 4 are etched to form the **upper portions 81 of the fins 8**." EX1006, 3:26-28. Subsequently, a "second etch process is applied to the exposed areas of the semiconductor substrate 4 to form the **flared profile of the lower portions 82**." EX1006, 3:42-44, 6:38-51 ("FIG. 11 illustrates a third embodiment in which … [s]imilar to the embodiment in FIGS. 5*a* and 5*b* … the

width at the bottom of the lower portion 82 of the inner fin 8 (See width $w_3$ in FIG. 5*b*) may be greater than the width of the upper portion 81 (See width $w_1$ in FIG. 5*b*).”). Chang explains that “**[e]ach fin** of the plurality of fins 8 has a sidewall, **the upper portion of the sidewall being substantially orthogonal** to a top surface of the semiconductor substrate 4.” EX1006, 3:50-52, 6:52-55. This means that the upper portions 81 of the protrusions 8 are “*substantially vertical*.” Chang also explains, for at least the inner protrusion 8, a “**lower portion of the sidewall being non-orthogonal** to the top surface of the semiconductor substrate 4,” which can include the lower sidewall having “a **substantially constant slope**.” EX1006, 3:53-57, 6:38-51. This means that the lower portions 82 of the protrusions 8 are “*tilted*.”

207. Thus, in view of the above, in my opinion, a POSA would have understood that Chang discloses and/or renders obvious “*a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall*.”

**d. [1.c] a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion;**

208. Below, I reproduce Figure 11 of Chang with the “*isolation region*”

annotated with blue arrows and texts, the "*shallow trenches*" annotated with green arrows and texts, and the "*deep trench*" annotated with purple arrows and texts. As I discussed in Section IX.C.1.b above, Chang discloses an isolation region of semiconductor substrate 4 that includes the outermost trenches ("*a deep trench"*) having a height $h_2$ that are "*deeper than the shallow trenches*," which are the inner trenches between the lower portions 82 of adjacent protrusions having a height $h_3$ "that is less than the height $h_2$" of the outermost trenches. EX1006, 4:3-5, 10:8-13. Although not drawn to scale, Figure 5b is also again annotated below showing each outer trench ("*deep trench*") having the larger height $h_2$ relative to the height of the inner trenches $h_3$. Chang also discloses that its deep trench can be filled with dielectric layer 10. EX1006, 4:30-31, FIG. 8b. A POSA would have understood that that the dielectric layer 10 is an insulator, and would thus function to electrically isolate the protrusions 8. EX1004, 6:54-57, claim 12.

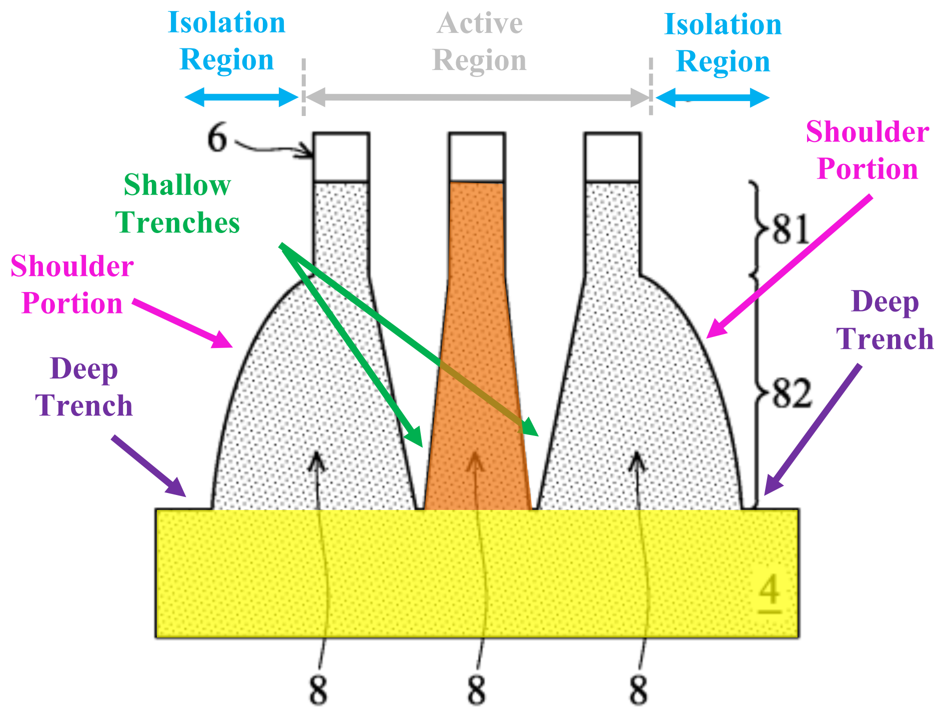
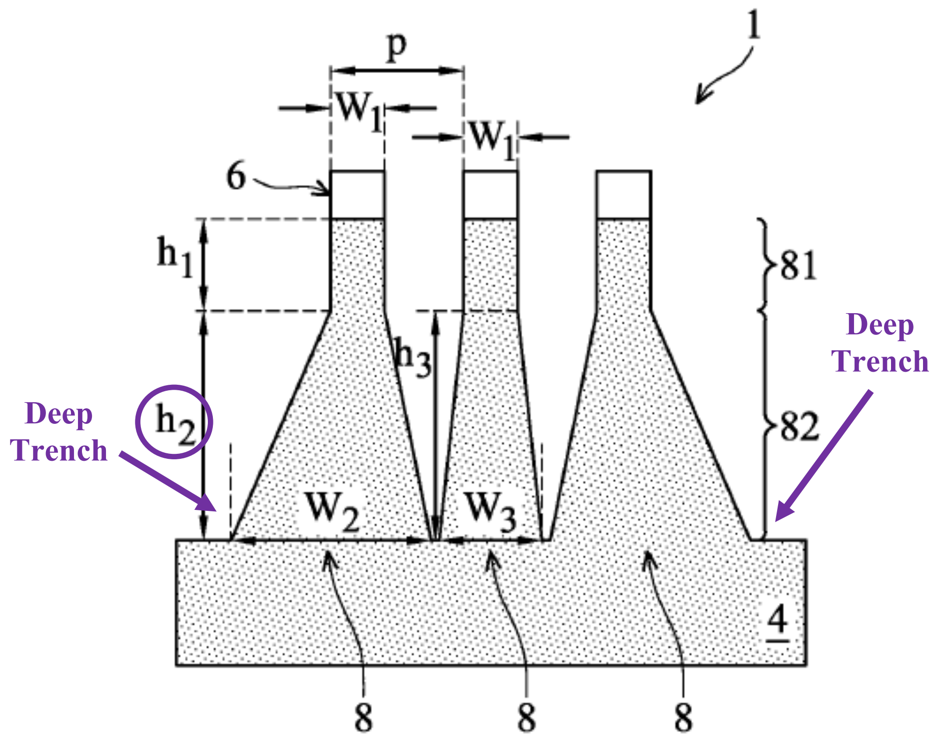



FIG. 11

**EX1006, FIG. 11 (annotated).**




**EX1006, FIG. 5 (annotated).**

209. Chang also discloses, and/or renders obvious that "*the deep trench … has a shoulder portion*." Referring to Figure 11 above, Chang discloses that "the outer sidewall of the lower portions 82 of the outermost fins 8 are formed to have a non-constant slope" and "the slope of the outer sidewall is smaller at the top of the lower portion 82 and gradually increases towards the bottom of the lower portion 82," which creates "the curved profile of the lower portions 82." EX1006, 6:38-43, 6:52-55. In my opinion, a POSA would have understood that the curved protrusion sidewalls of the outermost protrusions 8 form the boundaries of the outermost

trenches ("*deep trench*") and that the upper curved portion of the boundary disclose the claimed "*shoulder portion*," as annotated with pink arrows and texts in Figure 11 above.

210. The '909 patent does not mention the term "*shoulder portion*" of its deep trench outside of the claims themselves, let alone define the term. Based on Figure 10 (reproduced and annotated below) of the '909 patent, in my opinion, a POSA would have understood the upper curved portion of the '909 patent's deep trench 323 to represent the "*shoulder portion.*" And in my opinion, Chang's curved profiles of the lower portions 82 of the outermost protrusions 8 have the same shape and are located in the same location as the "*shoulder portion[s]*" illustrated in Figure 10 of the '909 patent.

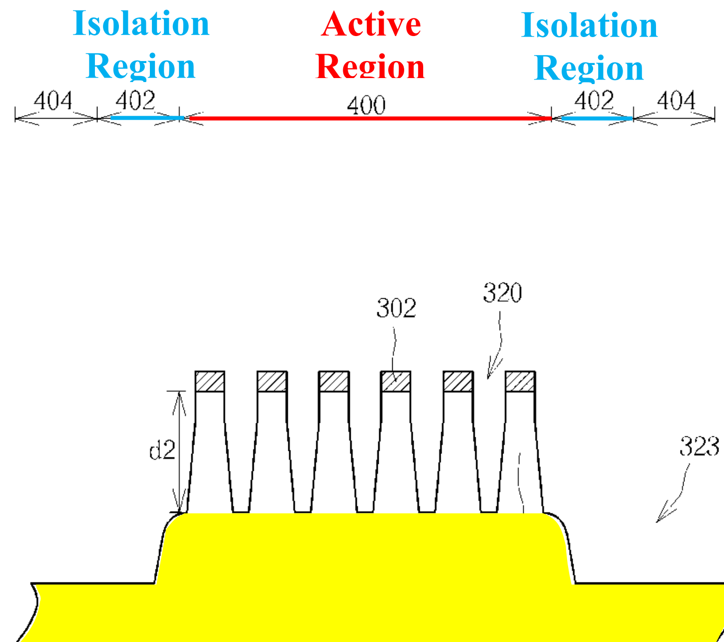



FIG. 10

**EX1001, FIG. 11 (annotated).**

211. Moreover, based on Chang's disclosure, a POSA would have understood that the location of the "*shoulder portion*" of Chang's outermost trench ("*deep trench*") with respect to the protrusions 8 is one of many possible design choices for deep trenches disclosed by Chang. For example, Chang discloses that any number of shoulder portions (e.g., "a stair-step profile") may be implemented along the lower portion 82 of the outermost protrusions, and that those shoulder portions can be implemented at various heights relative to the bottom of the shallow inner trenches ($h_2$). EX1006, FIG. 16, 9:28-30, 9:61-67. Chang also discloses that "the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments." EX1006, 2:4-6. Thus, in my opinion, a POSA would have recognized that the curved profiles of the lower portions 82 of the outermost protrusions in Figure 11 above (the claimed "*shoulder portion*") could similarly be implemented at different heights relative to the bottom of the shallow inner trenches.

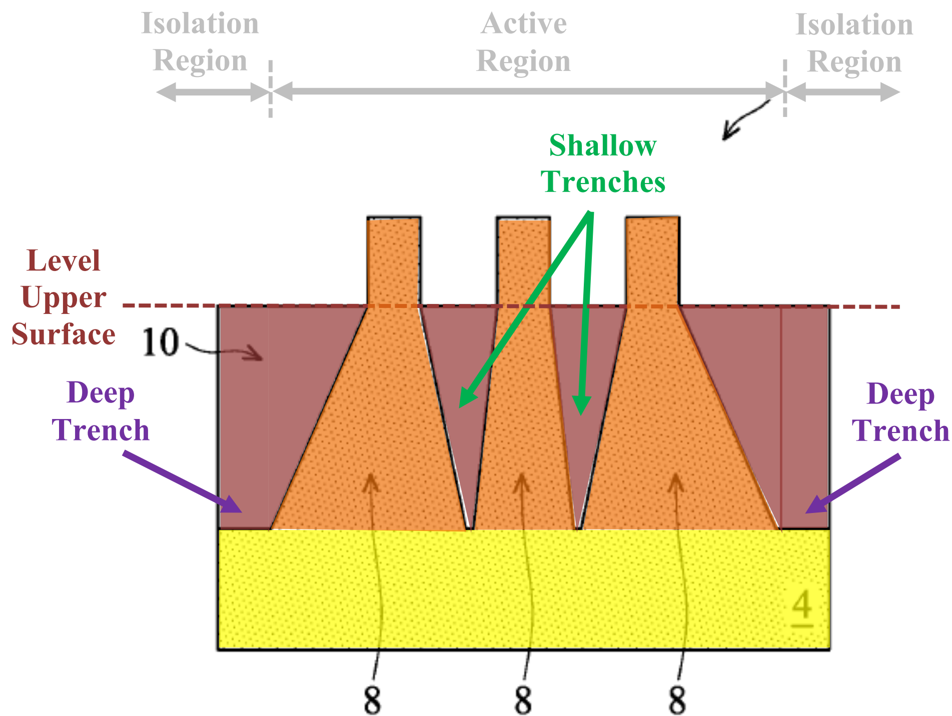
212. Thus, in view of the above, in my opinion, a POSA would have understood that Chang discloses and/or renders obvious "*a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion*."

**e. [1.d] an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench;**

213. As I discussed in Section IX.C.1.d, Chang's inner trenches between adjacent protrusions 8 represent the "*shallow trenches*" and the outermost trench represent the "*deep trench*." Chang discloses filling its deep trench with a dielectric layer 10 having "one or more suitable dielectric materials such as silicon oxide…." EX1006, 4:30-36, FIGS. 6b, 8b. As silicon oxide is well-known as an insulation material, a POSA would have understood that Chang's dielectric layer 10 represents "*an insulation layer*." EX1004, 4:56-61 ("depositing an insulator material, such as an oxide (preferably, silicon oxide)").

214. Moreover, Chang illustrates in Figure 8b that the upper surface of Chang's dielectric layer 10 "*in the shallow trenches is level with that in the deep trench*." Below, I reproduce Figure 8b of Chang with the "*shallow trenches*" annotated with green arrows and texts, the "*deep trench*" annotated with purple arrows and texts, and the "*isolation layer*" having a level upper surface highlighted in maroon. As discussed above, a POSA would have understood that the inner trenches are "*shallow trenches*," because they have a lower height $h_3$ relative to the height of the outer trenches $h_2$. EX1006, 10:8-13. A POSA would have further understood that dielectric layer 10 "*in the shallow trenches is level with that in the*

*deep trench*," because Chang discloses using a single etch processes to "thin[] the dielectric layer 10 below the tops of the fins 8." EX1006, 4:52-53. A POSA would have also understood that it was common practice to form the dielectric layer with a substantially uniform surface level when forming a FinFET device as non-uniformity in the upper surface of the dielectric layer can create challenges in forming reliable structures (e.g., gate dielectric layer and gate electrode layer) on the dielectric layer and/or the fin structures of the FinFET.




**EX1006, FIG. 8b (annotated).**

215. Though the dielectric layer 10 is illustrated for the structure of Figure 8b, a POSA would have recognized that the same dielectric layer 10 would have

also been formed on the structure illustrated in Figure 11 above to complete the fabrication of FinFET device 1 having the structural configuration of Figure 11. EX1006, 2:4-6 ("the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments"), 5:52-53 ("FIGS. 10 through 16 illustrate further embodiments of FinFET device 1 [illustrated in FIG. 8b]"), 6:52-53 ("The embodiment in FIG. 11 may begin formation as shown in FIGS. 1*a* through 4*b*"), 10:1-3 ("The embodiments in FIGS. 10 through 16 may continue processing to form a gate structure and source and drain regions [as illustrated in FIGS. 6*a* through 9*b*]").

216. Thus, in view of the above, in my opinion, a POSA would have understood that Chang discloses "*an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench*."

**f. [1.e] a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure;**

217. In my opinion, Chang discloses this limitation for the same reasons as I discussed above for claim limitations [1.b] and [1.d]. For example, as I discussed in Sections IX.C.1.c and IX.C.1.e above, each of protrusions 8 represents "*a protruding structure*" and a dielectric layer 10 ("*insulation layer*") deposited on the protrusions 8 is etched to expose the upper portion 81 of each protrusions 8.

EX1006, 3:26-28, 4:3-5, 4:52-53 ("FIGS. 8*a* and 8*b* illustrate the next step of thinning the dielectric layer 10 below the tops of the fins 8"), 6:38-51, 10:8-13, 11:3-5, FIGS. 8a, 8b. As the upper portion 81 ("*a portion*") of each protrusions 8 ("*the protruding structure*") "*protrudes over*" the dielectric layer 10 ("*insulation layer*"), the upper portion 81 of each protrusions 8 represents the claimed "*fin structure*." Therefore, in my opinion, Chang discloses "*a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure*."

**g. [1.f] a conductive layer disposed on the fin structure; and**

218. Chang discloses the "formation of the gate structure 12 **over the fins 8**" of FinFET device 1, where the gate structure 12 includes "a gate electrode [that] may comprise **a conductive material**…." EX1006, 4:61-64, 2:29-37, 5:6-8. Though the gate structure 12 is illustrated for the structure of Figure 9b, a POSA would have recognized that the same gate structure 12 would have also been formed on the structure illustrated in Figure 11 above to complete the fabrication of FinFET device 1 having the structural configuration of Figure 11. EX1006, 2:4-6 ("the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments"), 10:1-3 ("The embodiments in FIGS. 10 through 16 may continue processing to form a gate structure and source and drain regions [as illustrated in FIGS. 6*a* through 9*b*]").

219. Thus, in view of the above, in my opinion, a POSA would have understood that Chang's gate electrode is "*a conductive layer disposed on the fin structure*."

#### h. [1.g] a gate dielectric layer disposed between the fin structure and the conductive layer.

220. As I discussed above, Chang discloses that the gate structure 12 is formed "**over the fins 8**" and the gate structure 12 includes a gate electrode that represents the claimed "*conductive layer*." EX1006, 4:61-64, 2:29-37. Chang also discloses that "gate structure 12 may include **a gate dielectric layer**" (EX1006, 4:61-64), and that the "gate electrode layer … may be formed **over the gate dielectric layer**" (EX1006, 5:6-8). Thus, in view of the above, in my opinion, Chang discloses that its gate dielectric layer is "*disposed between the fin structure and the conductive layer*."

### 2. Dependent Claim 2: wherein the upper portion has a height between 200 and 400 angstroms.

221. Chang discloses that "the exposed areas of semiconductor substrate 4 are etched to **form the upper portions 81** of the fins 8. … The etch process may be a time-controlled process, and continue until the **upper portions 81 reach a predetermined height $h_1$ from about 5 nm to about 50 nm**," i.e., about 50 to about 500 angstroms, which overlaps the claimed range of "*between 200 and 400 angstroms.*" EX1006, 3:26-34.

222. Thus, in view of the above, in my opinion, Chang discloses claim 2.

**3. Dependent Claim 3: wherein the lower portion has a height between 1000 and 2000 angstroms.**

223. Chang discloses that "[t]he etch process may be a time-controlled process, and continue until the lower portions 82 reach a predetermined height $h_2$ from about 90 nm to about 250 nm," i.e., about 900 to about 2,500 angstroms, which overlaps the claimed range of "*between 1000 and 2000 angstroms.*" EX1006, 3:60-63.

224. Thus, in view of the above, in my opinion, Chang discloses claim 3.

**4. Dependent Claim 5: wherein the shoulder portion includes a round corner.**

225. In my opinion, Chang discloses, and/or renders obvious, claim 5 for the same reasons I discussed above for claim limitation [1.c]. For example, as I discussed in Section IX.C.1.d above, Chang discloses that "the outer sidewall of the lower portions 82 of the outermost fins 8 are formed to have a non-constant slope" and "the slope of the outer sidewall is smaller at the top of the lower portion 82 and gradually increases towards the bottom of the lower portion 82," which creates "the curved profile of the lower portions 82." EX1006, 6:38-43, 6:52-55. A POSA would have understood that the curved protrusion sidewalls of the outermost protrusions 8 form the boundaries of the outermost trenches ("*deep trench*") and that the upper curved portion of the boundary disclose the claimed

"*shoulder portion*."

226. Thus, in view of the above, in my opinion, Chang discloses, and/or renders obvious claim 5.

#### 5. Dependent Claim 6: wherein each of the fin structures has a same size.

227. In the '909 patent, the claimed "*fin structure[]*" is defined as the "*portion of the protruding structure that protrudes over the insulation layer*." EX1001, claim 1. Therefore, claim 6 merely requires that the portions of the protruding structures that protrude over the insulation layer have "*a same size*." In my opinion, Chang discloses such a structure. More specifically, Chang discloses and illustrates that each of the upper portions 81 of the protrusions 8 has the same height $h_1$, width $w_1$, and pitch p. EX1006, 3:30-37, FIGS. 4b, 5b, 8b, 11 (illustrating "*each of the fin structures has a same size*").

228. Thus, in view of the above, in my opinion, Chang discloses claim 6.

### D. Ground 4: The combination of Chang and Liu renders obvious claim 4.

#### 1. A POSA would have been motivated to combine Chang and Liu.

229. Referring to Figure 6b, reproduced below, Chang discloses that after the formation of its protrusions 8, "a dielectric layer 10 is blanket deposited on the FinFET device 1." EX1006, 4:30-39, FIGS. 6a, 6b. Referring to Figure 8b, reproduced below, Chang discloses "the next step of thinning the dielectric layer

10 below the tops of the fins 8." EX1006, 4:52-53, FIGS. 8a, 8b. Though Figures 8a and 8b of Chang illustrate the dielectric layer 10 to be thinned down to be in-line with the top surface of the lower portions 82 of protrusions 8, Chang does not explicitly explain the significance of choosing such a thickness for the dielectric layer 10. In fact, Chang discloses that "[t]he dielectric layer 10 may be thinned back in a variety of ways" (EX1006, 4:42-43), and that the "figures are merely intended for illustration" (EX1006, 2:6-8).

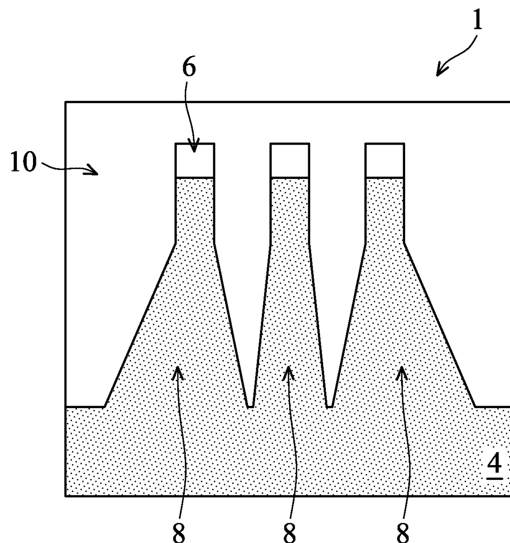



FIG. 6b

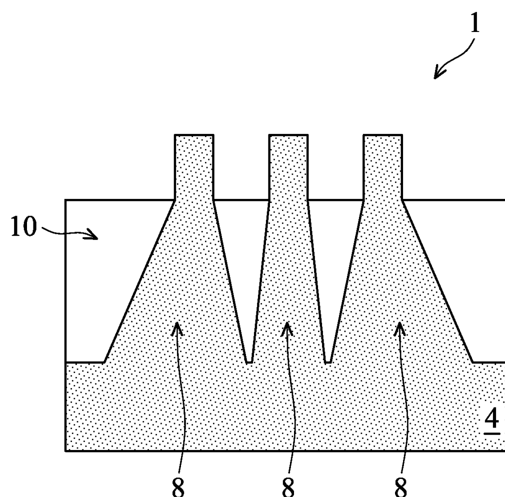



FIG. 8b

**EX1006, FIGS. 6b, 8b.**

230. As such, in my opinion, a POSA would have understood that thinning down the dielectric layer 10 to be in-line with the top surface of the lower portions 82 of protrusions 8 is merely a matter of design choice. This understanding is also supported by the '909 patent, which does not disclose why a POSA would choose

one insulation layer thickness over another. Thus, in my opinion, a POSA would have been motivated to look to other prior art references, such as Liu, for teachings on dielectric layer thicknesses used in FinFETs, and the significance of choosing one thickness over the other.

231. Similar to Chang, Liu discloses a FinFET fabrication process that includes blanket depositing a dielectric layer—an oxide layer 12—on protrusions 10 formed on a substrate 4, followed by an etching process to thin down the oxide layer 12:

> The resulting structure includes a **plurality of fins 10 formed in substrate 4**. Each fin of the plurality of fins 10 has a sidewall, a portion of the sidewall being substantially orthogonal to a major surface of the substrate 4, and a lower portion of the sidewall being non-orthogonal to the major surface of the substrate. These **fins 10 serve as the fin structure for the to-be-formed FinFET device 1**…. Turning now to FIG. 3**, an oxide layer 12 is blanket deposited on device 1** [followed by] … the next stage in the manufacturing process, wherein **oxide layer 12 is [] thinned back. Oxide layer 12 can be thinned back in a variety of ways**. In one embodiment, oxide layer 12 is thinned back by a diluted hydrofluoric acid (DHF) treatment or a vapor hydrofluoric acid (VHF) treatment for a suitable time.

EX1009, ¶¶8, 9, 11.

232. Liu further discloses that the dielectric layer can be thinned down to different thicknesses to expose different heights of the upper portions of

protrusions 10. EX1009, Abstract, ¶¶4, 14, 15. Specifically, Liu discloses multiple instances where the dielectric layer has an upper surface height that is above the lower portion of protrusion 10. EX1009, FIGS. 6*c*, 6*d*. Liu explains that "[b]y varying the thickness of oxide layer 12 between fins [10], and hence varying the height of fins 10 above the oxide layer [12], the overall channel width of the resulting finFET [1] can be modified." EX1009, ¶15. As channel width "impacts device performance, such as the driving current [($I_{Dsat}$)] of the device," adjusting the channel width by adjusting the dielectric layer thickness can fine-tune the drive current to meet the requirements of the FinFET device, thereby "overcoming the shortcomings in the conventional arts." EX1009, Abstract, ¶¶1, 15. As one example (illustrated in Figure 6d), Liu discloses that implementing the dielectric layer having an upper surface height that is above the lower portion of protrusions 10 can be beneficial in its relative ease of laying out the protrusion structure. EX1009, ¶16. Moreover, a POSA would have understood that such an implementation would ensure that Liu's gate structure 14 are wrapped only around the upper portions of protrusions 10, which are narrower than the lower portions of protrusions 10. A POSA would have known that having the gate structure 14 on the narrower upper portions would result in improved gate control for Liu's FinFET device. EX1034, 2 ("As [fin width] $W_{fin}$ shrinks, the gate control over the channel improves.")

233. Similar to Chang, Liu discloses that its fabrication method can be used to form a FinFET device structure, and can employ a photoresist and an etching process. *Compare* EX1006, Abstract, 2:9-20, 3:26-4:11 *with* EX1009, ¶¶6, 16. Thus, in my opinion, a POSA would have recognized that Liu's techniques are applicable to and compatible with Chang's fabrication process, and that modifying the FinFET device 1 of Chang to have the upper surface of Chang's dielectric layer 10 to be higher than the lower portions 82 of Chang's protrusions 8 would have required minimal modifications. In my opinion, in the combined Chang-Liu system, the Chang fabrication process would use Liu's etching process to thin down Chang's dielectric layer 10, as taught by Liu. This would result in the upper surface of Chang's dielectric layer 10 to be higher than the lower portions 82 of protrusions 8, as taught by Liu's Figure 6d.

234. In my opinion, a POSA would have found it obvious to implement the upper surface of Chang's dielectric layer 10 to be higher than the lower portions 82 of the protrusions 8, as taught by Liu, because such implementation represents selecting one of a finite number of identified, predictable upper surface heights (e.g., in-line with, above, or below the top surface of the lower portions 82 of the protrusions 8).

235. Furthermore, in my opinion, a POSA would have been motivated to combine Chang and Liu because they are in the same general field of FinFET

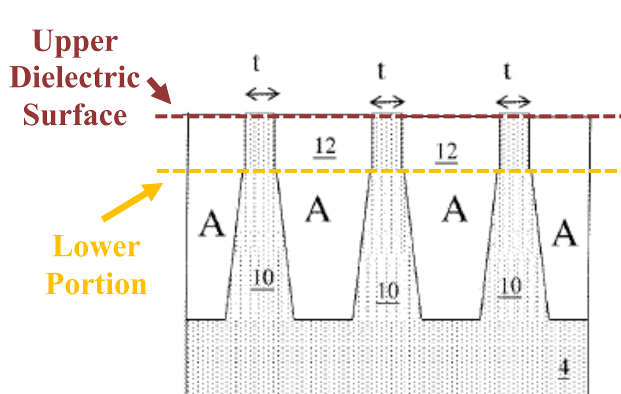
fabrication, and address the same problem—formation of a semiconductor device structure having dimensions that are closely controlled so as to produce efficient and reliable performance. EX1006, 1:6-20, 4:15-18; EX1009, Abstract, ¶1. Chang and Liu are thus analogous art to each other and to the '909 patent. A POSA would have had a reasonable expectation of success in modifying Chang's fabrication process to use techniques and processing steps to form the upper surface of Chang's dielectric layer 10 to be higher than the lower portions 82 of the protrusions 8, as taught by Liu.

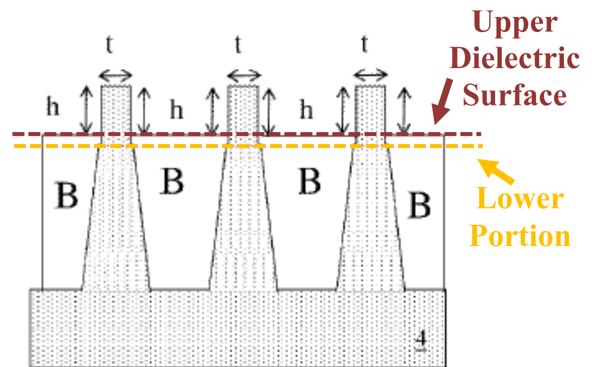
236. In my opinion, a POSA would not have experienced any unreasonable technical hurdles in implementing these modifications. And, a POSA would have understood that modifying Chang's fabrication process to use Liu's dielectric layer thinning process would merely amount to combining prior art elements (the Chang FinFET fabrication process and Liu's dielectric layer thinning process) according to known methods (implementing Liu's dielectric layer thinning process to form the upper surfaces of Chang's dielectric layer) to yield predictable results (e.g., causing the upper surface of Chang's dielectric layer to be higher than the lower portions 82 of the protrusions 8).

#### 2. Dependent Claim 4: wherein the upper surface of the insulation layer is higher than the lower portion.

237. As I discussed in Section IX.D.1 above, Liu discloses blanket

depositing a dielectric layer—an oxide layer 12—on protrusions 10, which is followed by a thinning process to thin down the dielectric layer to different thicknesses to expose different heights of the upper portions of protrusions 10. EX1009, Abstract, ¶¶4, 14, 15. EX1009, Abstract. Liu further discloses multiple instances where the dielectric layer is "*higher than the lower portion [of the protruding structure]*," including in Figure 6*c* (reproduced below) where the dielectric layer (oxide layer 12) "is not etched back at all," and in Figure 6*d* (reproduced below) where the dielectric layer (oxide layer 12) "is uniformly etched back" but only to a small degree. In each of these instances, the upper surface of the dielectric layer ("*insulation layer*") is "*higher than the lower portion [of the protruding structure]*."




**EX1009, FIGS. 6c-d (annotated).**

238. For at least the reasons discussed in Section IX.D.1 above, in my opinion, a POSA would have been motivated to implement Chang's dielectric

layer 10 with its upper surface "*higher than the lower portion [of the protruding structure]*," as taught by Liu.

239. Thus, in view of the above, in my opinion, the Chang-Liu combination renders obvious claim 4.

## X. CLAIMS APPENDIX

1. **[1.P]** A non-planar transistor, comprising:

**[1.a]** a substrate having an active region and an isolation region, wherein the isolation region encompasses the active region;

**[1.b]** a plurality of shallow trenches disposed in the substrate in the active region, wherein a portion of the substrate between each two shallow trenches is defined as a protruding structure, and the protruding structure has an upper portion having a substantially vertical sidewall and a lower portion having a tilted sidewall;

**[1.c]** a deep trench disposed in the substrate in the isolation region, wherein the deep trench is deeper than the shallow trenches and has a shoulder portion;

**[1.d]** an insulation layer disposed in the shallow trenches and the deep trench, wherein an upper surface of the insulation layer in the shallow trenches is level with that in the deep trench;

**[1.e]** a portion of the protruding structure that protrudes over the insulation layer defined as a fin structure;

**[1.f]** a conductive layer disposed on the fin structure; and

**[1.g]** a gate dielectric layer disposed between the fin structure and the conductive layer.

2. The non-planar transistor according to claim 1, wherein the upper portion has a height between 200 and 400 angstroms.

3. The non-planar transistor according to claim 1, wherein the lower portion has a height between 1000 and 2000 angstroms.

4. The non-planar transistor according to claim 1, wherein the upper surface of the insulation layer is higher than the lower portion.

5. The non-planar transistor according to claim 1, wherein the shoulder portion includes a round corner.

6. The non-planar transistor according to claim 1, wherein each of the fin structures has a same size.

## XI. CONCLUSION

In signing this declaration, I recognize that the declaration will be filed as evidence in an *inter partes* review before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 9th day of September 2025, in Lafayette, California.

Sayeef Salahuddin, Ph.D.