

# Improvement of High-Frequency FinFET Performance by Fin Width Engineering

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**Abstract**—Frequency dependent behaviour of MOSFETs arises from self-heating and source-to-drain coupling through the substrate. In this work the output conductance variation with frequency is experimentally investigated in FinFETs with various fin widths. We demonstrate that fin narrowing suppresses the output conductance degradation due to the substrate effect in the high-frequency range such that self-heating dominates the output conductance variation. The work thus emphasizes the importance of thermal management and device design in FinFETs.

## I. INTRODUCTION

FinFETs and UTBB SOI MOSFETs are widely being considered to satisfy ITRS requirements for device downscaling towards the 22 nm-node and below. Output conductance  $g_d$  variation is of prime importance for MOSFET technology as it translates into intrinsic gain, a key analogue figure of merit. The observed frequency dependent behaviour of SOI MOSFETs arises in particular from self-heating (SH) and source-to-drain coupling through the substrate, as well as from gate resistance [1]. Coupling through the substrate introduces  $g_d$  variation at low frequencies (1-10 Hz) due to the response of minority carriers in the substrate while at high frequencies ( $\sim$ GHz) the  $g_d$  response arises from majority carriers in the substrate [2]. The variation in  $g_d$  due to self-heating and substrate effects have previously been studied in FinFETs and UTBB MOSFETs [1], [3–5]. For UTBB MOSFETs without a ground plane,  $g_d$  variations are dominated by source-drain coupling [5]. However, the only literature addressing substrate effects in FinFETs used a low frequency range and suggested that at 0.1-10 kHz, substrate effects are negligible for FinFETs with the fin width smaller than 70 nm [2]. Smaller fin widths are beneficial due to improved electrostatic control. In this work we analyze FinFET device design requirements for minimising the  $g_d$  (and hence intrinsic gain) variation in the frequency range up to tens of GHz, focussing on the effect of fin width.

## II. EXPERIMENTAL DETAILS

The n-channel FinFETs were fabricated on 145 nm buried oxide (BOX). The devices used 40 nm gate length  $L_g$ , 10 parallel fins ( $N_{fin}$ ), 48 parallel fingers ( $N_{finger}$ ), 328 nm fin spacing  $S_{fin}$  and 60 nm fin height  $H_{fin}$ . The fin width  $W_{fin}$  was varied from 12 to 82 nm. Therefore, the total device gate width varied from 63  $\mu$ m to 97  $\mu$ m. Emphasis was given to  $W_{fin}$  as it is a critical FinFET parameter for both digital and analogue performance [6]. The FinFET parameters are schematically shown

in Fig 1.  $S$ -parameters were measured from 40 kHz to 110 GHz, de-embedded and converted to  $Y$ -parameters to obtain  $g_d$ .

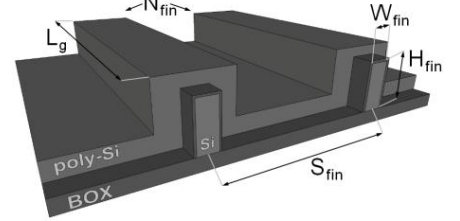


Fig. 1. Schematic FinFET drawing showing two fins.

## III. RESULTS AND DISCUSSION

Fig. 2 shows the  $g_d$  variation with frequency for the FinFETs. To evaluate the impact of the substrate effects, the frequency range has to be chosen carefully. In the 100 kHz to 4 GHz range, the observed  $g_d$  variation is dominated by self-heating and substrate effects [1]. Above 50-100 MHz dynamic self-heating is removed because device temperature cannot follow voltage oscillations [7]. At high frequencies (hundreds MHz-GHz), the  $g_d$  variation is governed by the substrate effect and the gate resistance  $R_g$  [1]. These effects obscure characteristic frequencies (inflection points) in Fig. 2 and the amplitudes of  $g_d$  transitions.

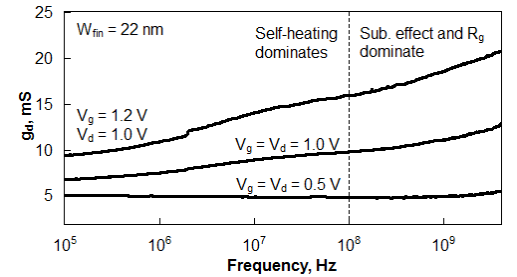


Fig. 2. Variation in  $g_d$  with frequency at various  $V_g$  and  $V_d$  in FinFETs

To identify the frequency range where substrate effects dominate  $g_d$  characteristics,  $g_d$  was corrected for  $R_g$  [8]. Fig. 3 shows  $g_d$  variation with and without  $R_g$ . Up to  $\sim$ 3 GHz  $R_g$  does not significantly affect  $g_d$ . Above  $\sim$ 3 GHz the two curves deviate, thus the  $g_d$  transition above 3 GHz appears dominated by  $R_g$ . This was further confirmed by analyzing  $g_d$  with self-heating and substrate effects suppressed. This was possible by selecting low  $V_g$  and  $V_d$ , since both self-heating and substrate effects are exasperated at high bias. In Fig. 2 the curve of  $g_d$  variation with frequency at  $V_g = V_d = 0.5$  V remains flat below

~1 GHz, which agrees with the results presented in Fig. 3. Thus, the frequency range from 100 MHz to 1 GHz was chosen for characterization of substrate-related effects.

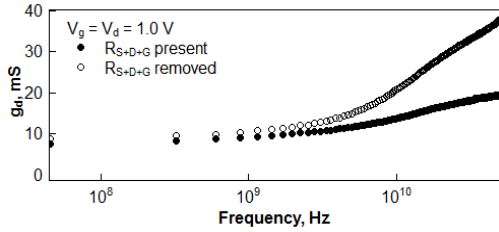


Fig. 3. Measured  $g_d$  frequency response with and without correction for parasitic series resistance,  $W_{fin} = 22$  nm.

To quantify the variation of the amplitudes of the high frequency transition  $\Delta g_{d-SUB}$  were extracted in FinFETs with different  $W_{fin}$ .  $\Delta g_{d-SUB}$  was obtained from  $g_d$  values at 100 MHz and 1 GHz. According to [2],  $\Delta g_{d-SUB}$  is proportional to the transconductance  $g_m$  and depends on the body factor  $n$  and the substrate capacitance  $C_{Sub}$  which is a function of frequency:

$$(1)$$

$C_{BGD}$ ,  $C_{SBG}$  and  $C_{GBG}$  are described in [2].

Fig. 4 shows  $\Delta g_{d-SUB}$  decreases for narrower  $W_{fin}$ . To the first order,  $g_m$  is proportional to the effective fin width ( $2H_{fin} + W_{fin}$ ), while  $C_{Sub}$  is proportional to  $W_{fin}$  only. Therefore, according to (1),  $\Delta g_{d-SUB}$  is normalized to  $(2H_{fin} + W_{fin})/W_{fin}$ . Fig. 4 also shows that this normalisation does not result in a flat line, indicating that  $g_m$  and  $C_{Sub}$  dependences on  $W_{fin}$  are not sufficient to explain the suppression of substrate effects for narrow fins. Another factor which causes the variation of normalized  $\Delta g_{d-SUB}$  with  $W_{fin}$  is  $n$  dependence on  $W_{fin}$ . As  $W_{fin}$  shrinks, the gate control over the channel improves and  $n$  approaches its ideal value of 1 [9]. Therefore,  $\Delta g_{d-SUB}$  reduces according to (1), reaching total suppression. A generalized model in [9] was modified for FinFETs with rectangular cross-sections to estimate  $n$ . The model accounts for vertical and lateral couplings as well as for the shielding distance  $d_s$  which indicates how far the gate extends under the fin. A large  $d_s$  is an indication of an  $\Omega$ -like fin cross-section.

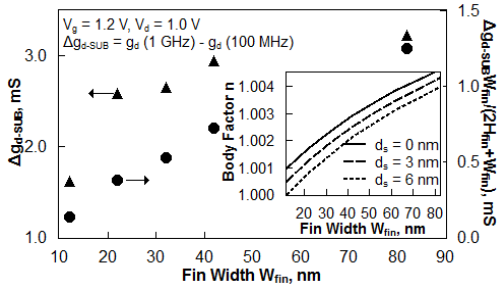


Fig. 4.  $\Delta g_{d-SUB}$  and normalized  $\Delta g_{d-SUB}$  variation with  $W_{fin}$ . Inset: calculated body factor  $n$  variation with  $W_{fin}$  using  $d_s = 0$  nm, 3 nm and 6 nm.

The inset in Fig. 4 shows the variation in  $n$  with  $W_{fin}$  for  $d_s = 0$  nm, 3 nm and 6 nm. As  $W_{fin}$  reduces from 82 to 12 nm, ( $n-1$ ) changes  $\sim 5x$  for  $d_s = 0$  nm. For larger  $d_s$  the difference is even greater,  $\sim 9x$  and  $\sim 40x$  for  $d_s$  of 3 nm and 6 nm, respectively. The normalized  $\Delta g_{d-SUB}$  changes  $\sim 9x$  for the same  $W_{fin}$  reduction (Fig. 4). Therefore, from (1)  $d_s \sim 3$  nm must be assumed to explain the experimental results. This is a realistic value using typical TEM images of FinFETs [10], [11].

Another contributing factor to the observed  $\Delta g_{d-SUB}$  variation may be a reduction in substrate depletion depth with fin narrowing. This arises from electric field lines penetration screening by the lateral gates which results in modification of  $C_{Sub}$  frequency response. Relative importance of this effect must be determined by simulations.

To understand the relative importance of self-heating and substrate effects on the  $g_d$  degradation, the frequency response of FinFETs with  $W_{fin}$  between 12 nm and 82 nm is presented in Fig. 5.  $\Delta g_{d-SUB}$  is only 20-30% of the total  $g_d$  variation in 100 kHz - 1GHz range for all devices with  $W_{fin}$  between 12 and 82 nm. The  $g_d$  transition due to self-heating ( $\Delta g_{d-SH}$ ) which occurs between 100 kHz and 100 MHz is the main source of the  $g_d$  variation. These results contrast with UTBB MOSFETs without a ground plane, where the  $g_d$  frequency response is affected by both self-heating and substrate effects, and at certain biases substrate effects dominate [5]. Conversely substrate effects are virtually eradicated in FinFETs with a few tens of nm wide fins. Their good high frequency performance can be further improved by optimisation of thermal properties, for example by optimising device geometry [1], BOX thinning [12] and source/drain engineering [12], [13].

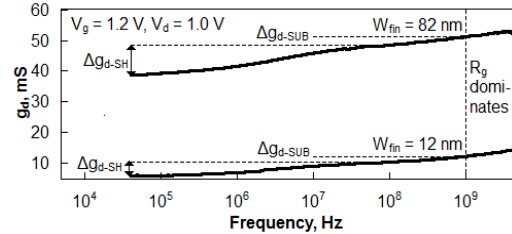


Fig. 5.  $g_d$  variation with frequency in devices with 12 and 82 nm-wide fins.

#### IV. CONCLUSIONS

It has been shown that substrate effects apparent in the  $g_d$  frequency response of FinFETs are effectively reduced where  $W_{fin}$  is reduced to a few tens of nm. This is mainly due to a reduction of the body factor with decreasing  $W_{fin}$  due to improved control from the gate. Consequently, self-heating dominates the observed  $g_d$  frequency variation. These results contrast with UTBB MOSFETs without a ground plane, equally affected by both self-heating and substrate effects. To further improve high frequency FinFET performance, optimisation of thermal properties is required.

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