UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

Case IPR2025-01527
U.S. Patent No. 9,117,909

PETITIONER'S OPPOSITION TO PATENT OWNER'S DISCRETIONARY DENIAL REQUEST

Mail Stop "PATENT BOARD"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

I. INTRODUCTION 1

II. INSTITUTION IS WARRANTED IN VIEW OF MATERIAL ERRORS BY THE EXAMINER. 2

A. The Examiner materially erred by overlooking teachings in the references cited during prosecution. 2

1. The Examiner overlooked teachings in the Shieh reference, applied during prosecution. 2

2. The Examiner overlooked teachings in the Dreeskornfeld reference, cited by Applicant in an IDS. 5

B. The Examiner also materially erred by conducting an inadequate search that failed to identify prior art disclosing the "shoulder" limitation. 7

III. INSTITUTION IS WARRANTED BECAUSE OF THE STRENGTH OF THE PETITION, WHICH INVALIDATES ALL CLAIMS OVER TWO SEPARATE PRIMARY REFERENCES..... 10

IV. MERITS CONSIDERATION IS WARRANTED BECAUSE THE SETTLED EXPECTATIONS OF PETITIONER AND OTHERS OUTWEIGH MARLIN'S ALLEGED EXPECTATIONS. 11

V. INSTITUTION IS AN EFFICIENT USE OF BOARD RESOURCES..... 16

VI. NATIONAL SECURITY, ECONOMIC, AND PUBLIC INTEREST CONSIDERATIONS STRONGLY FAVOR INSTITUTION. 17

VII. CONCLUSION..... 20

PETITIONER'S UPDATED EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 9,117,909 to Kuo et al. ("'909 patent")
1002	Prosecution History of U.S. Patent No. 9,117,909 to Kuo et al.
1003	Declaration of Dr. Sayeef Salahuddin [**Corrected**]
1004	U.S. Patent No. 7,994,020 to Lin et al. ("Lin")
1005	U.S. Patent No. 8,629,512 to Liaw ("Liaw")
1006	U.S. Patent No. 8,546,891 to Chang et al. ("Chang")
1007	*Intentionally Left Blank*
1008	*Intentionally Left Blank*
1009	U.S. Patent Application Pub. No. 2013/0056826 to Liu et al. ("Liu")
1010	U.S. Patent No. 9,368,388 to Liaw ("Liaw-388")
1011	U.S. Patent Application Pub. No. 2013/0045580 to Cho ("Cho")
1012	*Curriculum Vitae* of Dr. Sayeef Salahuddin
1013	U.S. Patent Application Pub. No. 2011/0068405 to Yuan et al. ("Yuan")
1014	Park, D., et al., "Present and Future of Si-based Transistor Technology for Memories," *ECS Transactions*, 2(11):11-26 (2006) ("Park")
1015	U.S. Patent No. 7,148,120 to Chen et al. ("Chen-120")
1016	U.S. Patent No. 7,611,950 to Kim ("Kim")
1017	U.S. Patent Application Pub. No. 2011/0298041 to Renn ("Renn")

Exhibit No.	Description
1018	U.S. Patent Application Pub. No. 2007/0148979 to Lee et al. ("Lee-979")
1019	U.S. Patent No. 6,413,802 to Hu et al. ("Hu")
1020	Chau, R., et al., "Silicon nano-transistors and breaking the 10 nm physical gate length barrier," 61st Device Research Conference. Conference Digest, Salt Lake City, UT, USA, 123-126 (2003) ("Chau")
1021	Colinge, J., et al.," FinFETs and Other Multi-Gate Transistors," Springer (2008) ("Colinge")
1022	Hu, C., "Modern Semiconductor Devices for Integrated Circuits," 1st ed. (2009) (Excerpt) ("Hu-2009")
1023	Huang, X., et al., "Sub 50-nm FinFET: PMOS," International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318), Washington, DC, USA, 67-70 (1999) ("Huang")
1024	Bohr, M. et al., "Intel's Revolutionary 22nm Transistor Technology," available at http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf (accessed through https://newsroom.intel.com/press-kits/intel-22nm-3-d-tri-gatetransistor-technology/), ("Bohr")
1025	Kundu, S., et al., "Nanoscale CMOS VLSI Circuits: Design for Manufacturability," 1st ed. (2010) ("Kundu")
1026	Huang, X., et al., "Sub-50 nm P-channel FinFET," IEEE Transactions on Electron Devices, 48(5):880-886 (2001) ("Huang-2001")
1027	U.S. Patent No. 7,172,943 to Yeo et al. ("Yeo")

Exhibit No.	Description
1028	Park, T., et al., "Fabrication of body-tied FinFETs (Omega MOSFETs) using bulk Si wafers," 2003 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, Japan, 135-136 (2003) ("Park-2003")
1029	Wolf, S. and Tauber, R., "Silicon Processing For The VLSI Era," Vol. 2, Lattice Press (1990) ("Wolf")
1030	U.S. Patent No. 8,110,466 to Shieh et al. ("Shieh")
1031	Shamiryan, D., et al. "Dry etching process for bulk finFET manufacturing," Microelectron. Engineering, 86(10):96-98 (2009) ("Shamiryan")
1032	U.S. Patent No. 2012/0049294 to Chen et al. ("Chen-294")
1033	Engelhardt, M., et al. "A new $CBrF_3$ process for etching tapered trenches in Silicon," Journal of Electrochemical Society: Solid-State Science and Technology, 134(8):1985-1988 (1987) ("Engelhardt")
1034	Makovejev, S., et al. "Improvement of high-frequency FinFET performance by fin width engineering," 2012 IEEE International SOI Conference (SOI), Napa, CA, USA, 2012, pp. 1-2
1035	Jan, C., et al. "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications," 2012 International Electron Devices Meeting, San Francisco, CA, USA, 2012, pp. 3.1.1-3.1.4
1036	U.S. Patent Application Pub. No. 2012/0001197 to Liaw et al. ("Liaw-197")
1037	U.S. Patent Application Pub. No. 2014/0131813 to Liaw et al. ("Liaw-813")

Exhibit No.	Description
1038	U.S. Patent Application Pub. No. 2007/0158756 to Dreeskornfeld et al. ("Dreeskornfeld")
1039	United States Securities and Exchange Commission, United Microelectronics Corporation Form 20-F Annual Report, Dec. 31, 2015
1040	Docket Navigator Case Search, Marlin Litigation Docket, captured Dec. 1, 2025
1041	USPTO Assignment Data for U.S. Patent No. 9,117,909
1042	Docket Navigator Case Search, U.S. Patent No. 9,117,909, captured Dec. 6, 2025
1043	Patent Assignment for U.S. Patent No. 9,117,909, Reel and Frame No. 56991/0292
1044	"16/12nm Technology" TSMC, captured Dec. 2, 2025 https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_16_12nm
1045	"Another Historic Investment Secured Under President Trump," The White House, Published Mar. 3, 2025 https://www.whitehouse.gov/articles/2025/03/another-historic-investment-secured-under-president-trump/
1046	"CNBC Transcript: United States Commerce Secretary Howard Lutnick Speaks with CNBC's Brian Sullivan on "The Exchange" Today," CNBC, Published Apr. 29, 2025 https://www.cnbc.com/2025/04/29/cnbc-transcript-united-states-commerce-secretary-howard-lutnick-speaks-with-cnbcs-brian-sullivan-on-the-exchange-today.html

Exhibit No.	Description
1047	"Removing Barriers To American Leadership In Artificial Intelligence," The White House, Published Jan. 23, 2025 https://www.whitehouse.gov/presidential-actions/2025/01/removing-barriers-to-american-leadership-in-artificial-intelligence/
1048	Excerpt of "TSMC Annual Report 2024," https://investor.tsmc.com/english/annual-reports
1049	Shilov, A., "Both Trump and Biden expected to attend TSMC's Arizona fab grand opening ceremony — Fab 21 opens in December," Yahoo! Finance – tom'sHardware, Published Nov. 8, 2024 https://finance.yahoo.com/news/both-trump-biden-expected-attend-151941592.html
1050	*Longitude Licensing Ltd. et al v. Apple Inc. et al*, Case No. WDTX-1-25-cv-00215, Docket Report, Docket Navigator, captured Dec. 2, 2025
1051	Docket Navigator Case Search, United Microelectronics Corporation (UMC) Litigation Docket, captured Dec. 2, 2025
1052	Nasdaq – This 1 Number May Ensure TSMC's Market Dominance https://www.nasdaq.com/articles/1-number-may-ensure-tsmcs-market-dominance, captured Dec. 5, 2025
1053	U.S. Patent No. 8,214,007 B2 to Baker et al. ("Baker")
1054	IDS Citation Sheet, Prosecution History of US 9,905,641 (Sept. 15, 2015)

Exhibit No.	Description
1055	"Ansys Strengthens Collaboration with TSMC on Advanced Node Processes Certification and 3D-IC Multiphysics Design Solutions," Published Apr. 23, 2025 https://investors.ansys.com/news-releases/news-release-details/ansys-strengthens-collaboration-tsmc-advanced-node-processes, captured Dec. 5, 2025
1056	TSMC-Cadence Press Release, Published Apr. 24, 2025 https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr/2025/cadence-and-tsmc-advance-ai-and-3d-ic-chip-design-with-certified.html, captured Dec. 5, 2025
1057	"TSMC's Resurgence: What Lies Ahead for the Architect of AI," Published June 11, 2025 https://www.cmcmarkets.com/en-au/market-news/tsmc-resurgence, captured Dec. 5, 2025
1058	Klearman, J., "Decoding TSMC's Contribution to the AI and 5G Ecosystem" Nov. 20, 2024 https://graniteshares.com/institutional/us/en-us/research/decoding-tsmc-s-contribution-to-the-ai-and-5g-ecosystem/, captured Dec. 5, 2025
1059	USPTO Class 438 Schedule, Apr. 2011
1060	He, A., "In the Global AI Chips Race, China is Playing Catch-Up," Centre for International Governance Innovation, Published Sept. 18, 2024 https://www.cigionline.org/articles/in-the-global-ai-chips-race-china-is-playing-catch-up/, captured Dec. 14, 2025
1061	"How Military Tensions Are Driving the Next Semiconductor Chip Race," Microchip USA, Published July 16, 2025 https://www.microchipusa.com/industry-news/how-military-tensions-are-driving-the-next-semiconductor-chip-race, captured Dec. 14, 2025

Exhibit No.	Description
1062	O'Brien, R., "Trump on China Putting - America First," available at: https://trumpwhitehouse.archives.gov/wp-content/uploads/2020/11/Trump-on-China-Putting-America-First.pdf

I. INTRODUCTION

A core purpose of the PTAB under the AIA is to strengthen the integrity of the U.S. patent system by ensuring that only valid and properly granted patents remain in force. The challenged patent, U.S. Patent No. 9,117,909 ("'909 patent"), issued as a result of an Examiner (1) overlooking critical teachings of cited prior art (e.g, the Shieh and Dreeskornfeld references) that disclose the limitation which led to allowance, and (2) conducting a deficient prior art search that missed critical prior art (e.g., Lin and Chang relied upon in the Petition). Institution is warranted to address these material Examiner errors.

Further, the settled expectations of TSMC and its customers outweigh any settled expectations of Marlin and warrant merits consideration. TSMC and its customers had a settled expectation of non-enforcement due to the lack of assertion by UMC, an alleged "primary" competitor of TSMC's, during the first 6 years of the '909 patent's life. During this time, TSMC invested billions of dollars to manufacture FinFET chips, including for American customers who expected to be able to integrate those chips into their own products without incident. Marlin, a foreign entity which only recently acquired the patent, has no comparable expectations.

Institution is also an efficient use of Board resources in view of *Fintiv* because the '909 patent is not currently asserted in a parallel litigation. There is,

however, a threat of enforcement, as evidenced by Marlin's claim of infringement and existing lawsuits in the ITC and district court. In response, TSMC diligently challenged the '909 patent's validity in the PTAB to provide a true alternative to district court or ITC litigation. Moreover, this case involves complicated semiconductor technologies, and trained PTAB judges are best suited to adjudicate the merits of the Petition and to correct the past errors of this Office.

Finally, compelling national security, economic, and public interests make review an appropriate use of the Board's resources. TSMC is the world's largest chip maker, by some accounts providing around 90% of the world's advanced chips (e.g., 7nm and smaller). EX1052, 2. Its advanced semiconductor technology is vital to the U.S. supply chain, with a wide range of applications including AI, 5G, health care, and national security and defense. Given TSMC's vital and strategic contribution to the U.S. supply chain, the Administration has a heightened interest in ensuring that the USPTO corrects its error in issuing this patent.

II. INSTITUTION IS WARRANTED IN VIEW OF MATERIAL ERRORS BY THE EXAMINER.

A. The Examiner materially erred by overlooking teachings in the references cited during prosecution.

1. The Examiner overlooked teachings in the Shieh reference, applied during prosecution.

The Examiner materially erred by failing to consider critical teachings of Shieh (EX1030) when allowing the '909 patent claims. EX1002, 66. Although

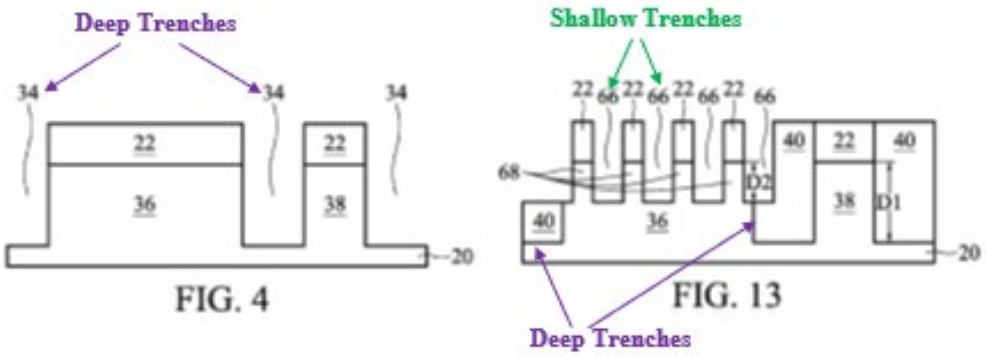
citing and applying Shieh, the Examiner failed to recognize that Shieh discloses the very claim limitation that formed the basis for allowance.

The Examiner issued two Office Actions prior to the issuance of a Notice of Allowance. In the first Office Action, the Examiner rejected independent claim 1 as being anticipated under § 102(a)(1) by each of King (*see* EX1002, 63-64) and Shieh (*see* EX1002, 64-65). In response, Applicant amended independent claim 1 and added new claim 6 (along with others); application claim 6 recited "each of the shallow trenches has a shoulder portion." EX1002, 75-76.

In the second Office Action, the Examiner dropped the rejection over Shieh and rejected the amended independent claim 1 as being obvious under §103 in view of King in combination with a secondary reference (Wann). *See* EX1002, 84-86. The Examiner further indicated that the features of new prosecution claim 6 would be "allowable over the prior art of record" if corrected to recite: "each of the *deep* trenches has a shoulder portion," instead of referring to "*shallow* trenches." *Id.* In response, Applicant canceled claim 6 and amended claim 1 to incorporate this allegedly allowable feature of claim 6, revising it per the Examiner's instruction to recite: "a deep trench … has a shoulder portion." EX1002, 90. The Examiner then allowed claim 1 as amended and the dependent claims. *See* EX1002, 97-101 (Notice of Allowance). In allowing the claims, the Examiner made a material error by overlooking Shieh's teaching, despite applying Shieh as

an anticipatory ground in the first rejection.

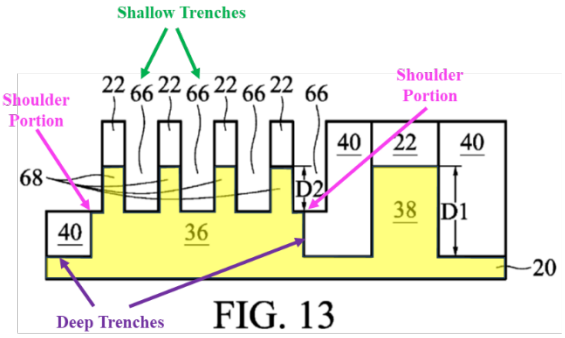
Shieh discloses "a deep trench … [that] has a shoulder portion." In the first Office Action, the Examiner specifically cited Figure 13 of Shieh, and mapped the claimed "[first] trenches" (later amended to "shallow trenches") to Shieh's trenches 66 (shown in Figure 13, annotated and reproduced below). *See* EX1002, 64-65. The Examiner further mapped the claimed "a [second] trench" (later amended to "a deep trench") to Shieh's trenches 34 (shown in Figure 4, annotated and reproduced below). The Examiner failed to appreciate that trenches 34 in Shieh's Figure 4 are subsequently formed into deep insulation regions 40 (shown in Figure 13). *See id.*



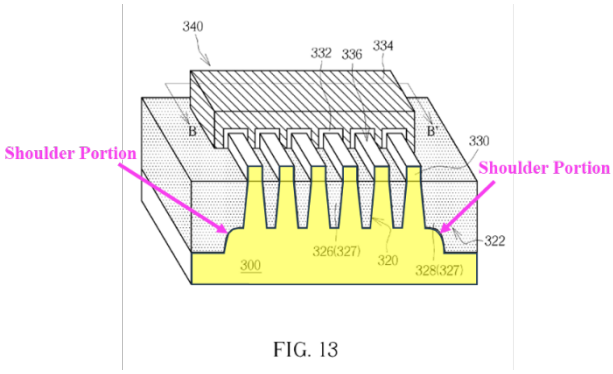
EX1030, FIGS. 4 and 13 (annotated).

Then faced with Applicant's amendment and addition of the "shoulder portion" feature, the Examiner overlooked Sheih's teachings that deep trenches 34 in fact have the claimed "shoulder portion," as shown in annotated Figure 13 below. Notably, Shieh's "shoulder portions" are located in the same location as the "shoulder portion[s]" depicted in Figure 13 of '909 patent (the figure identified by

Applicant during prosecution as allegedly providing support for the newly-added "shoulder portion," EX1002, 79-80), as shown below:



EX1030, FIG. 13 (annotated).



EX1001, FIG. 13 (annotated).

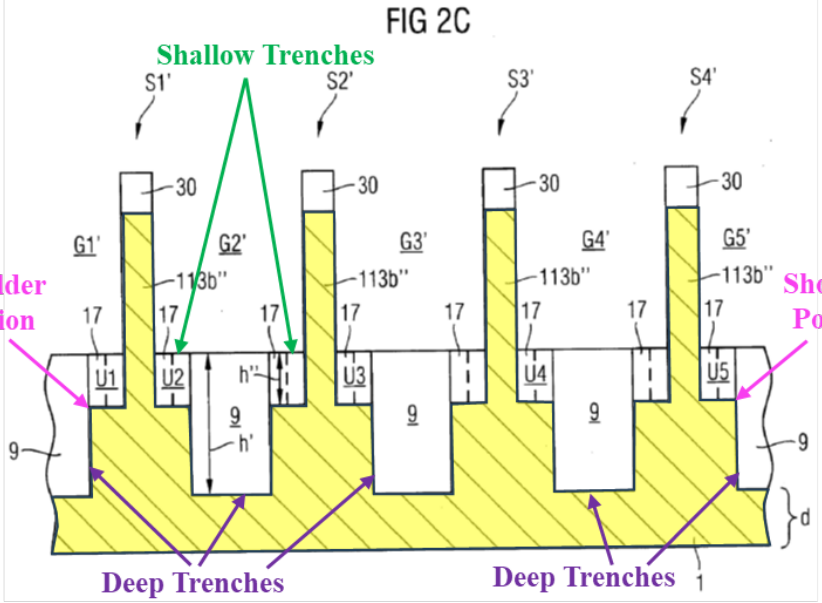
The Examiner materially erred in allowing the claims because the "deep trench … [that] has a shoulder portion" feature of issued claim 1, the exact feature that the Examiner identified as the allowable subject matter, was well established in Shieh cited during prosecution. The Examiner should have instead used Shieh to reject the proposed claims. Institution is warranted to correct this material Examiner error.

2. The Examiner overlooked teachings in the Dreeskornfeld reference, cited by Applicant in an IDS.

The Examiner also failed to address critical teachings of Dreeskornfeld (EX1038)—cited by Applicant in an information disclosure statement filed concurrently with the application. EX1002, 3. Indeed, like Shieh, Dreeskornfeld discloses the very claim limitation that formed the basis for allowance, i.e., that "a deep trench … has a shoulder portion."

Referring to Figure 2C (annotated and reproduced below), Dreeskornfeld

discloses deep trenches with oxide filling 9 having height h', which are deeper than shallow trenches (gap regions) U1-U5 with height h" and oxide layer 17. EX1038, ¶44.



EX1038, FIG. 2C (annotated).

The Examiner overlooked that Dreeskornfeld's deep trenches (with oxide filling 9) include the claimed "shoulder portion" at both the top left and top right corners, where the sidewalls of the trenches meet the upper surface of substrate 1. The "shoulder portion[s]" in Figure 2C of Dreeskornfeld are again in the same locations as the alleged shoulder portions in the '909 patent, as shown in annotated Figure 13 of the '909 patent below.

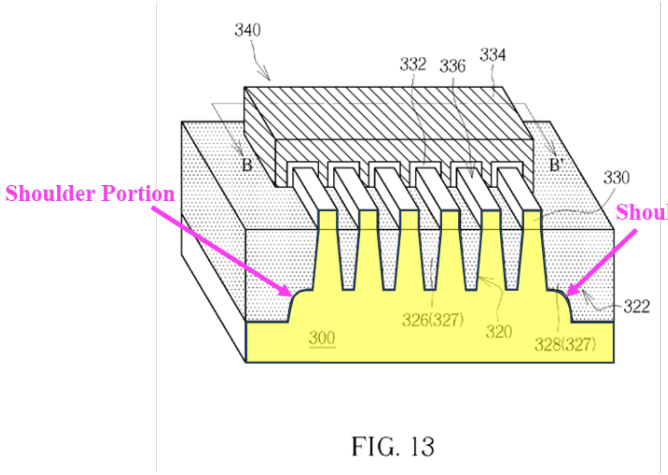


FIG. 13

EX1001, FIG. 13 (annotated).

Thus, the Examiner also materially erred in allowing the claims over the Dreeskornfeld art submitted by the Applicant in an IDS during prosecution. *See Carbyne, Inc. v. Tritech Software Sys.*, IPR2025-00959, Paper 11 at 2 (PTAB Oct. 3, 2025) (finding material error where petitioner showed a reference cited in an IDS discloses the limitations the examiner identified as not taught by the prior art); *Samsung Elecs. Co., Ltd. v. Wilus Inst. of Standards and Tech. Inc.*, IPR2025-00935, Paper 12 at 2-3 (PTAB Sept. 26, 2025) (finding material error where examiner overlooked teachings of a reference cited in IDS).

B. The Examiner also materially erred by conducting an inadequate search that failed to identify prior art disclosing the "shoulder" limitation.

Aside from Shieh and Dreeskornfeld, the art is replete with other teachings of the alleged missing shoulder limitation of the '909 patent's independent claim 1, including the references raised in the Petition, which clearly teach this feature. *See, e.g.*, Pet., 33-35, 62-66. The Examiner's failure to locate this art is the result of an

inadequate and sub-standard prior art search. Even a minimally adequate search would have uncovered the prior art applied in the petition (or art similar thereto) that discloses all limitations of claim 1 including the alleged missing limitation.

Indicative of the poor search quality, the Examiner's Search Notes do not even conform with the procedural guidance set out for Examiners in the MPEP. The MPEP indicates that "the examiner must record[,] in the appropriate sections of the Official Correspondence 'Search Notes' form[,] the areas in which the search for prior art was made," and that "[a]ny time that a limited electronic search was performed … a complete search history in the form of a printout must be included in the application file." *See* MPEP § 719.05. But, here, the Examiner did not comply with these requirements, providing only the broad classifications searched, providing no information regarding any search terms used, and including no search history printout. The Examiner's limited Search Notes confirm the improperly narrow scope of the search.

Moreover, the limited Search Notes indicate that the Examiner searched only within certain limited subclasses of a single USPC class (257). EX1002, 72, 88. As a result, the Examiner failed to search for and consider prior art classified in other relevant areas, leading the Examiner to miss critical prior art. For example, the Examiner failed to search the entirety of class 438, which not only covers semiconductor device manufacturing, including field effect devices (like FinFETs),

but is also the class that the ’909 patent itself is classified in. EX1059, 1. Additionally, Lin (one of the primary references used in the Petition) is also in class 438. Lin is clearly material because it discloses many of the limitations of claim 1 including the purportedly allowable “shoulder portion” limitation. *See* Pet., 16-43. By failing to search in this area, the Examiner missed critical prior art used in the Petition.

The deficiency of the Examiner’s searches is further underscored by the fact that the Examiner did not even search the very areas where the patent itself is classified. The Examiner’s Search Notes list various CPC symbols purportedly used to search the prior art: “H01L 29/66795, H01L 29/785” and “H01L 29/7853.” EX1002, 106 (search notes with notice of allowance indicating only an “update” of prior searched); *see id.* 72, 88 (prior searches). But these symbols completely leave out several of the CPC classifications applied to the ’909 patent (indicated with bolded italics): H01L 29/7851, ***H01L 21/76224***, ***H01L 27/0886***, ***H01L 29/0649***, H01L 29/66795, H01L 29/7853. EX1001, (52). Further, had the Examiner searched any of the IPC symbols listed on the ’909 patent, including e.g., H01L 29/78, the Examiner would have found Chang (another reference used in the Petition that renders obvious many of the ’909 patent claims). EX1001, (51); EX1006, (51); Pet., 53-71. Failure to even search the very areas where the patent itself is classified is emblematic of an inadequate search process that constitutes a

material error warranting review for merits and non-discretionary considerations.

The Examiner's flawed search is exactly the type of Examiner error IPRs are designed to address. Institution is warranted for this reason alone. *See, e.g.*, *Anthony, Inc. v. Control-Tec, LLC*, IPR2025-00559, Paper 12 (PTAB July 16, 2025) (finding material prosecution error where examiner failed to locate a petition reference); *Carbyne, Inc. v. Tritech Software Sys.*, IPR2025-00959, Paper 11, 2 (PTAB Oct. 3, 2025) (referring in part based on examiner's failure to apply reference cited on an IDS); *Taiwan Semiconductor Mfg. Co. Ltd. v. Marlin Semiconductor Ltd.*, IPR2025-00847, Paper 11, 3-4 (PTAB Sept. 3, 2025) (referring 15-year-old patent based on examiner's failure to apply reference cited during prosecution).

III. INSTITUTION IS WARRANTED BECAUSE OF THE STRENGTH OF THE PETITION, WHICH INVALIDATES ALL CLAIMS OVER TWO SEPARATE PRIMARY REFERENCES.

The merits are strong, well-supported, and well-reasoned, and the invalidity positions are straightforward. TSMC presents two obviousness grounds for the independent claim over (i) Lin in view of Liaw and (ii) Chang. Pet., 16-77. As set forth in the Petition, each asserted ground teaches all claim 1 limitations, including, the "shoulder portion" limitation allegedly not found in the prior art. Moreover, the Petition's compelling merits can be gleaned even just from the side-by-side figures below, which show, for example, the striking similarities between the alleged

invention and Lin, raised as Ground 1 in the Petition.

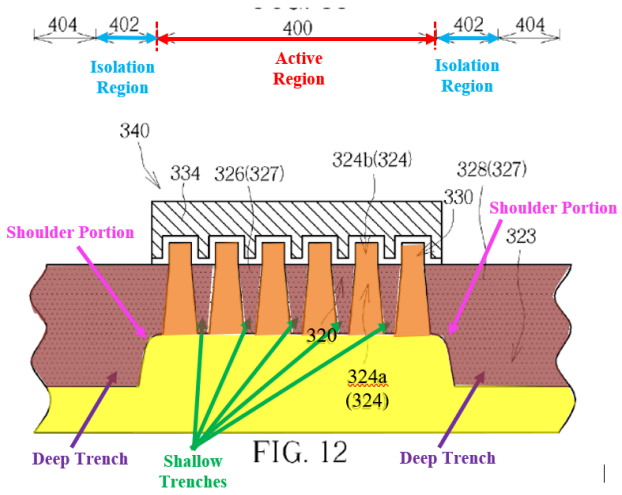
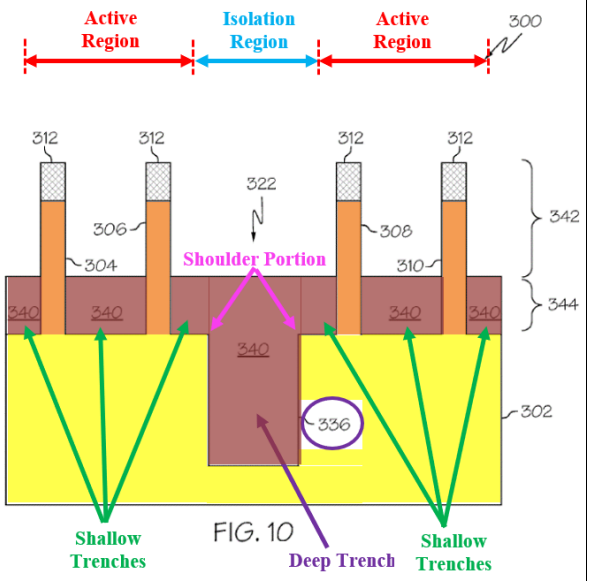
’909 patent, FIG. 12 (annotated)	Lin, FIG. 10 (annotated)
	

FIG. 12

FIG. 10

IV. MERITS CONSIDERATION IS WARRANTED BECAUSE THE SETTLED EXPECTATIONS OF PETITIONER AND OTHERS OUTWEIGH MARLIN’S ALLEGED EXPECTATIONS.

Marlin’s main contention in requesting denial is that the patent issued ten years ago, allegedly creating “settled expectations” that, alone, effectively trump all other considerations. DD Br. (Paper 7), 2-8. Focusing only on Marlin’s expectations, without regard for the expectations of TSMC, its customers, and the public, is not balanced or fair. TSMC, its customers, and the public have “settled expectations,” and they heavily outweigh Marlin’s expectations.

Since acquiring the ’909 patent in June 2021 (EX1041; EX1043), Marlin began an enforcement campaign against the semiconductor industry, including TSMC’s customers. EX2104. And Marlin has since asserted patents against TSMC

and its customers in the ITC, seeking an exclusion order. The Petition can resolve patentability of the '909 patent's claims before Marlin sues TSMC or its customers and disturbs the parties' well-settled expectations that the '909 patent remains dormant.

First, TSMC and its customers had settled expectations that the '909 patent would not be asserted due to the prior patent owner's (UMC's) inaction. TSMC has been engaged in FinFET manufacture since 2013. EX1044, 1. Since the issuance of the '909 patent, TSMC has invested billions of dollars in fabrication facilities to manufacture millions of wafers per year using the FinFET technology, and its customers similarly invested significant resources into designs based on that technology. *See* EX1045. During this time, UMC, who Marlin claims is "TSMC's main competitor," DD Br., 3, remained silent and inactive.

Indeed, UMC does not have a history of asserting its patents *at all*. In 2015 when the '909 patent issued, UMC had "4,673 U.S. patents." EX1039, 0040. And according to DocketNavigator, UMC has been involved in a *total* of 19 patent actions since 1992. EX1051. In most of those cases, UMC was the ITC *respondent* or district court *defendant*. UMC is a listed plaintiff/complainant in only 5 cases, and *none of these* are after 2009. Despite its large patent portfolio, UMC did not have a history of patent enforcement. UMC's inactivity created settled expectations for TSMC and its customers that the patent would remain dormant.

Marlin's activities cannot unwind the settled expectations of TSMC and its customers created by UMC's longstanding inaction with the patent. In analogous bodies of law, the expectations of others would exceed those of a new property owner under such circumstances. *See* Restatement (First) of Prop. § 459 cmt. a (1993) ("Through lapse of time old rights become obscure. A long continued use raises reasonable expectations of its continuance."); *Anaheim Gardens, L.P. v. United States*, 953 F.3d 1344, 1350-51 (Fed. Cir. 2020); *Nordlinger v. Hahn*, 505 U.S. 1, 12-13 (1992) ("[A]n existing owner rationally may be thought to have vested expectations in his property or home that are more deserving of protection than the anticipatory expectations of a new owner at the point of purchase.").

Second, Marlin has not presented persuasive evidence that '909 patent was ever "commercialized, asserted, marked, licensed, or otherwise applied" in the same "particular technology space" where it now seeks enforcement. *Shenzhen Tuozhu Tech. Co., Ltd. v. Stratasys, Inc.*, IPR2025-00531, Paper 10, 3 (PTAB July 17, 2025) (internal quotations omitted). This weighs against any claim by Marlin of "settled expectations." *Id.*; *Home Depot U.S.A., Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper 11, 2-3 (PTAB Sept. 4, 2025). The '909 patent has not been asserted in litigation in any venue, against any party. EX1042. Marlin alleges that UMC is "another Taiwanese semiconductor foundry" and "TSMC's main business competitor." DD Br., 1. Yet Marlin has not pointed to any evidence suggesting

UMC enforced or demanded a license for the '909 patent against TSMC (or anyone) during the 6 years UMC owned the patent.

Marlin also misleadingly argues that the '909 patent has "been commercialized, at least in the form of licensing" with Intel and Samsung.[1] DD Br., 4-5. Marlin's sole support for this argument is a bare assertion by its corporate representative Paul Ahern (EX2104) that fails to provide *any details* regarding this license by which to assess its relevance or significance. Moreover, Marlin fails to put forth any evidence its purported licensees marked their products in any way to evidence commercialization that would disturb TSMC's settled expectations. At bottom, when Marlin acquired patents (including the '909 patent) that had never been asserted with the intention of enforcing them, the only reasonable expectation it could have is that their validity would be challenged. *See Anaheim Gardens*, 953 F.3d at 1350-51 ("timing" of property purchase and "knowledge of the purchaser" are relevant in determining whether purchaser had reasonable investment-backed expectations); *Celgene Corp. v. Peter*, 931 F.3d 1342, 1361-63 (Fed. Cir. 2019) (owners know patents may be subject to post-issuance reconsideration)

[1] The parties have recently reached agreement that Marlin will provide the same discovery of these licenses as authorized by the Board in IPR2025-01054. TSMC intends to request additional briefing when Marlin produces these licenses.

Relying on *iRhythm Tech., Inc. v. Welch Allyn, Inc.*, IPR2025-00363, Marlin argues that TSMC's alleged knowledge of the '909 patent through prosecution of its own patent applications favors denial. DD Br., 4. But Marlin's argument is distinguishable. In the only citation to the '909 patent[2], unlike *iRhythm*, where the patent owner in the IPR proceeding owned the patent at the time of issuance, the citation here occurred before Marlin acquired the patent. EX1053 (U.S. Patent No. 8,214,007 issued to Welch Allyn, Inc.); EX1054 (IDS citation of '909 patent in U.S. 9,905,641). As described above, TSMC has settled expectations, based on UMC's conduct, that the '909 patent would not be asserted. A petitioner's expectation of non-enforcement has been deemed sufficient to overcome any alleged settled expectations based on the age of the patent. *See, e.g.*, *Globus Medical, Inc. v. Spinelogik, Inc.*, IPR2025-00225, Paper 8 (PTAB June 12, 2025) (patent expired for failure to pay maintenance fees prior to enforcement); *Home Depot USA, Inc. v. H2 Intellect LLC*, IPR2025-00480, Paper 11 (PTAB Sept. 4, 2025) (no expectation of enforcement against hardware store); *Apple v. Ferid Allani*, IPR2025-00856, Paper 11 (PTAB Sept. 5, 2025) (delay of enforcement of 11 years; after patent expired).

[2] The other application does not refer to the '909 patent at all, but rather to family members. EX2103, 5.

Finally, Marlin argues that licensing negotiations between the parties beginning in 2024 weigh against any claim of settled expectations by TSMC. DD Br., 6-7 (citing *DataDome S.A. v. Arkose Labs Holdings, Inc*. IPR2025-00693, Paper 13 (PTAB Aug. 14, 2025)). Marlin's reliance on *DataDome* is unavailing. First, in *DataDome*, there was a parallel proceeding and no argument regarding material error by the Examiner. *DataDome*, Paper 8 at 7-8; Paper 12 at 26-31. Both of these factors differ here and weigh in favor of institution. Moreover, TSMC filed this Petition just over a year after receiving a licensing proposal, which was followed by a period of evaluation and good faith negotiations, and less than 7 months after those negotiations discontinued due to Marlin asserting patents against TSMC in court. TSMC was far more diligent than the *DataDome* Petitioner who waited over two years after receiving an initial demand and 15 months after refusing a license to file its Petition. *DataDome*, Paper 13 at 7; *DataDome*, EX1013 (Jan. 11, 2023 letter seeking license on one challenged patent).

V. INSTITUTION IS AN EFFICIENT USE OF BOARD RESOURCES.

Institution here is an efficient use of Board resources in view of *Fintiv* because there is no parallel litigation involving the '909 patent. *See, e.g.*, *Intas Pharms. Ltd. v. Atossa Therapeutics, Inc.*, IPR2025-00799, Paper 12, 2-3 (PTAB Aug. 12, 2025); *Azurity Pharms., Inc. v. Helsinn Healthcare S.A.*, IPR IPR2025-00945, Paper 11, 2-3 (PTAB Sept. 19, 2025) (no parallel proceeding and Examiner

error outweigh patent owner settled expectations (age of patent and commercialization)). No other tribunal is set to resolve the merits; therefore, no risk of duplicated efforts, inconsistent decisions, or unnecessary expense exists.

Marlin argues this fact is not dispositive because the petitions in *Intel Corp. v. Proxense LLC* were discretionarily denied despite having no *trial date*. DD Br., 7 (citing IPR2025-00327, Paper 12, 2 (PTAB June 26, 2025)). However, in *Intel*, the Acting Director explained the discretionary denial decision was based upon Petitioner's failure to "provide any persuasive reasoning as to why an *inter partes* review is an appropriate use of Board resources." *Intel*, Paper 12 at 2. Here, TSMC presents several compelling reasons why IPR is an appropriate use of resources, e.g., to address the Examiner's material errors and to resolve the parties' dispute in an efficient manner avoiding "unnecessary and counterproductive litigation costs" before Marlin asserts this patent in a court against TSMC.

Marlin has already alleged infringement of the '909 patent and shown a willingness to bring TSMC to court. Institution before litigation promotes the very ideals that underlie the IPR process and is an appropriate use of Board resources.

VI. NATIONAL SECURITY, ECONOMIC, AND PUBLIC INTEREST CONSIDERATIONS STRONGLY FAVOR INSTITUTION.

Marlin acknowledges it has alleged infringement of the '909 patent by TSMC. EX2104. Given Marlin's chosen forum for enforcement is the ITC, this threat to weaponize the '909 patent undermines the U.S. semiconductor supply

chain, harming priorities this Administration has made clear are vital to U.S. economic interests and national security. EX1046, 3; EX1047, 1. This makes IPR of the '909 patent an appropriate use of the Office's resources—indeed a compelling one. TSMC's FinFET fabrication capabilities are vital to leading U.S. companies (such as Apple, NVIDIA, Amazon, Broadcom, Qualcomm, and AMD). More specifically, TSMC's 5 nm processing node supports U.S. advanced semiconductor research and development in industries including AI, health care, and national security/defense. EX1048, 18-19. Meanwhile, the semiconductor chips that drive artificial intelligence systems, such as NVIDIA's H100, are manufactured with TSMC's 4nm process. EX1060, 2. And NVIDIA's latest B100 and B200 chips can only be manufactured using TSMC's world-leading 3 nm process. *See id.* Promoting these emerging industries is an important step in advancing the Administration's priorities. EX1046, 3; EX1047, 1.

Indeed, the U.S. government has recognized AI's importance to national security, and TSMC is an important part of the American AI-dominance strategy. EX1055; EX1056. The semiconductor chips manufactured by TSMC are vital to U.S. industries and to the U.S. military. As Secretary Lutnick explained in April 2025, "national security" is the "key" reason to "bring semiconductors home." EX1046, 3. That has been a key principle of President Trump's agenda: "Our national security depends on bringing our supply chain home. This is especially

true when we are dealing with critical technology, computer chips that are not only important to our civilian world … but also to our military." EX1062, 40.

Moreover, TSMC "produces the advanced processors that Nvidia [] and Apple [] rely on to bring AI to life," including, NVIDIA's next-generation Blackwell AI chips for NVIDIA's AI supercomputers. EX1057, 2. Moreover, healthcare is a key area of projected growth in the AI semiconductor market, where the demand for "advanced chips—TSMC's specialty—will continue to surge." EX1058, 5. Further, as industry publications report, TSMC's "3nm and 5nm nodes power everything from smartphones to stealth fighters." EX1061, 3-4. And the U.S. Air Force estimates "90% of its precision-guided munitions rely on TSMC chips." *Id.*, 4. And a similar calculus applies to warships, satellites, and communication systems. *Id.* And, Blocking or burdening access to TSMC-made advanced semiconductors could create a catastrophic single-point failure for medical R&D, causing direct effects on future patient care and far-reaching consequences for the development of life-saving technology.

Marlin does not dispute the serious impact a ban on importing FinFET products into the United States would have to vital U.S. national security, public health, or economic interests. Instead, Marlin sets up a strawman—painting itself as protector of local industries. DD Br., 10. The facts belie Marlin's pronouncement. Marlin does not practice the '909 patent, nor any patent it holds.

There is no evidence that Marlin, a foreign entity, has invested in the U.S. semiconductor technology space, except by trying to assert its recently acquired patents. Given Marlin's assertion of its patents in the ITC against U.S.-based companies (e.g., Apple, Qualcomm, Broadcom), *see* EX1050, Marlin's arguments that it is a protector of "local industry" ring hollow.

Finally, trying to cast TSMC as a "foreign entity" that "import[s] infringing products" and must be protected against twists the facts beyond recognition. There is zero evidence, other than a bare, unsupported statement from an interested party, Mr. Ahern, that any product of TSMC infringes any patent in Marlin's portfolio, including the '909 patent. Additionally, Marlin ignores TSMC's commitment to invest $165 billion in building manufacturing facilities in the United States in support of this Administration's goal to onshore advanced semiconductor manufacturing to bolster U.S. economic and national security interests. EX1046, 3. Indeed, TSMC's Arizona facilities are already producing 4nm chips for American customers. EX1049, 2. Marlin's enforcement campaign against TSMC seeks to damage the core supply chain of semiconductor chips from TSMC to the United States These considerations therefore warrant institution.

VII. CONCLUSION

For these reasons, the Director should deny Marlin's request to discretionarily deny this IPR and should institute review of the challenged claims.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX PLLC

/Ryan C. Richardson, Reg. No., 67,254/

Ryan C. Richardson
Registration No. 67,254
Attorney for Petitioner Taiwan Semiconductor Manufacturing Company Ltd.

Date: December 18, 2025

1101 K Street, NW, 10th Floor
Washington, DC 20005
(202) 371-2600

CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that, on December 18, 2025, true and correct copies of the foregoing **PETITIONER'S OPPOSITION TO PATENT OWNER'S DISCRETIONARY DENIAL REQUEST** and **EXHIBITS 1038-1062** were served electronically via e-mail in their entirety on the following counsel for Patent Owner:

William A. Meunier (Lead counsel) WAMeunier@mintz.com
Adam S. Rizk (Back-up Counsel) ARizk@mintz.com
Michael T. Renaud (Back-up Counsel) MTRenaud@mintz.com
Reza Dokhanchy (Back-up Counsel) RDokhanchy@mintz.com
Tawfik Goma (Back-up Counsel) TAGoma@mintz.com
MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND POPEO, P.C.
MINTZ-MARLIN-IPRS@MINTZ.COM

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX PLLC

/Ryan C. Richardson, Reg. No., 67,254/

Ryan C. Richardson
Registration No. 67,254
Attorney for Petitioner Taiwan Semiconductor Manufacturing Company Ltd.

Date: December 18, 2025

1101 K Street, NW, 10th Floor
Washington, DC 20005
(202) 371-2600