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Dry etching process for bulk finFET manufacturing

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ABSTRACT

This paper describes a method to manufacture bulk fins for finFET. The bulk fins consist of two parts: the straight top of 125 nm height which is used as a fin and a sloped bottom of 200 nm one that facilitates the trench filling. The method is based on a conventional shallow trench isolation (STI) process flow with an additional α-C hard mask of 90 nm (with antireflective SiOC coating of 35 nm) on top of the STI stack (70 nm nitride on top of 8 nm oxide). The nitride layer and the top straight part of the fin is patterned using $CH_2F_2/SF_6/N_2$ chemistry and α-C as a mask, while the bottom sloped part is patterned using $Cl_2/O_2/N_2$ chemistry and the nitride layer as a mask. After the etching, the STI process flow remains almost unchanged.

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1. Introduction

Continuous downscaling of the device sizes resulted in emergence of new device architectures. One of the new device architectures is so-called fin field-effect transistor (finFET), where the gate wraps a fin-like transistor channel from three sides [1]. First finFETs were fabricated using silicon-on-insulator (SOI) technology where the fins (usually 50–100 nm high) were patterned stopping on thick insulating SiO_2. The schematic drawing of such type fin is presented in Fig. 1a. SOI fins are relatively easy to make, but they have some disadvantages: SOI wafers are much more expensive, have higher defect density and lower heat conductivity as compared to bulk Si wafers.

In order to overcome those issues a bulk (or body-tied) finFET has been proposed [2,3]. In this architecture, the fins are made out of the bulk Si substrate using shallow trench isolation (STI)-like technology. The performance of the bulk finFET devices is similar to that of the conventional SOI finFETs [4,5]. Moreover, the presence of a contact to the fin body allows fabrication of both NOR and NAND flash memory devices [6]. The body contact also makes possible study of negative bias temperature instability [7] by providing possibility to apply body bias as a manner of stress and to monitor body current. There are reports on other studies of bulk finFETs, such us device characteristic simulations [8] or hot carrier-induced degradation [9] showing advantages of bulk finFETs.

There are several bulk finFET process flows reported in literature. The simplest one from the technological point of view is based on STI process [10]. In this approach, after the completion of the STI process flow, the field oxide is recessed below the active area level to the desired fin depth. The main disadvantage of this approach is that the fin walls are nonparallel as the sidewalls of active areas in the STI technology are sloped at 70°–85° in order to facilitate top corner rounding and trench filling.

Another approach is to make a straight fin from top to bottom as shown in Fig. 1b. The disadvantage of this approach is patterning of high aspect ratio fins (fin width should be in the range of 10–30 nm [1] while bulk fin depth should be 300–400 nm in order to provide enough isolation from the substrate) [2]. Another difficulty of this approach is filling the space between fins with conventional dielectric used for STI (although aspect ratio in bulk finFET is smaller than STI of the same technology node – narrower lines for same pitch and depth – trench filling is more challenging in bulk finFET because of its trench shape with vertical walls).

In order to facilitate bulk fin fabrication, we propose a combination of vertical fin (top part) and sloped STI-like bottom as illustrated in Fig. 1c. The top vertical part provides the desired electrical performance, while the sloped bottom facilitates the filling.

2. Experimental

The following stack was used for the bulk fin patterning. At the bottom, a typical STI stack was present (from top to bottom):

- 70 nm CVD silicon nitride.
- 8 nm thermally grown silicon dioxide.
- Si substrate.

On top of the STI stack, an amorphous carbon (α-C) hard mask (HM) was deposited with an SiOC antireflective coating on top:

- 35 nm SiOC.
- 90 nm α-C.

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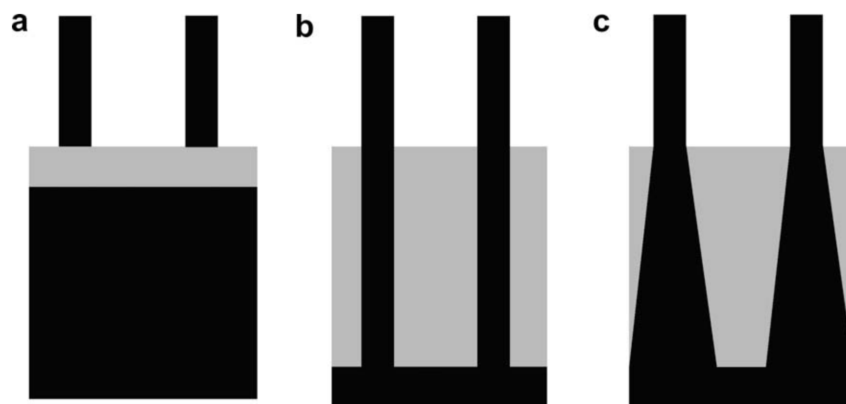

Fig. 1. Schematic representation of different fin types. Crystalline Si is in black, insulating SiO_2 is gray. (a) SOI fin, (b) straight bulk fin and (c) double-sloped bulk fin.

Both layers were deposited by CVD. The SiOC layer is inserted in order to facilitate lithography. One hundred and ninety three nanometer immersion lithography with organic BARC was used to print the pattern.

All etching was performed in Lam Research Versys 2300 Kiyo reactors. This is a transformer-coupled plasma (TCP) reactor that allows separate control of plasma power and substrate bias.

After the patterning the wafers underwent conventional STI processing:

- Silicon dioxide deposition (high-aspect ratio process [HARP] using O_3/TEOS based sub-atmospheric chemical vapor deposition process at 540 °C) [11].
- Chemical mechanical polishing (CMP).
- Nitride removal.
- SiO_2 level adjustment using HF solution.

After the processing the bulk fins were inspected using cross-sectional scanning electron microscopy (X-SEM) using Philips Nova 200 SEM tool.

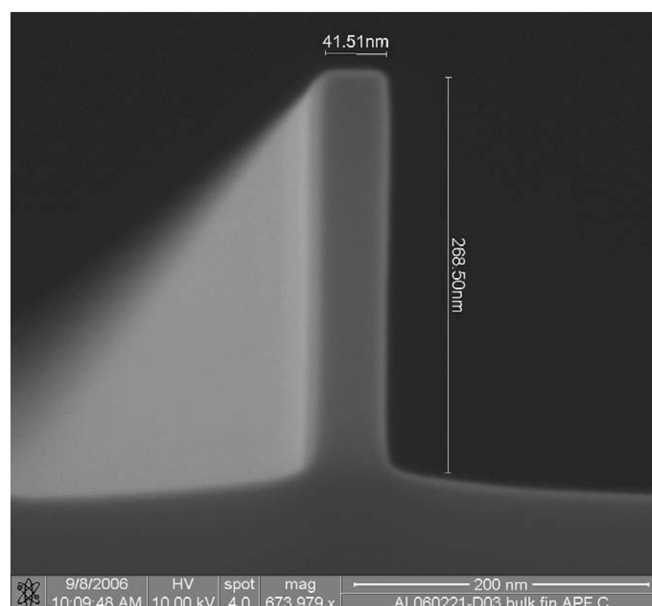

Fig. 2. X-SEM image of a vertical fin etched with $CH_2F_2/SF_6/N_2$ chemistry.

3. Results and discussion

Patterning of double-sloped bulk fins could be easily achieved using double hard mask – α-C and Si_3N_4 (it should be noted that the latter is also used as a CMP stopping layer). Patterning of straight Si fins could be rather straightforward with α-C HM and appropriate chemistry ($CH_2F_2/SF_6/N_2$) as can be seen in Fig. 2. It might be possible to tune the etch recipe in order to get a slope of the fin walls after certain depth without using nitride, but in that case the further STI processing must be redeveloped for α-C HM (factors such as resistance of α-C to thermal cycles required for trench filling and efficiency of this material as CMP stop layer would require considerable development effort). It would be easier to insert a nitride layer between α-C and Si in order to keep the rest of the STI processing unchanged. In that case, α-C could be used as a mask for patterning of nitride and the top straight part of the fin while the nitride layer can be used as mask for patterning the bottom sloped part of the fin. In our experiments, we targeted the straight part to be at 125 nm deep and the sloped part to be around 200 nm deep, so the total depth is 325 nm which is standard depth of STI in our process flows.

The introduction of nitride into the Si/α-C stack requires some adaptations of the etch process. Nitride itself could be etched with the same chemistry as Si fin ($CH_2F_2/SF_6/N_2$) – that's why nitride alone cannot be used as mask for patterning the straight fins with that chemistry. However, as nitride is opened and Si is started to be etched, a severe Si profile distortion is observed as can be seen in

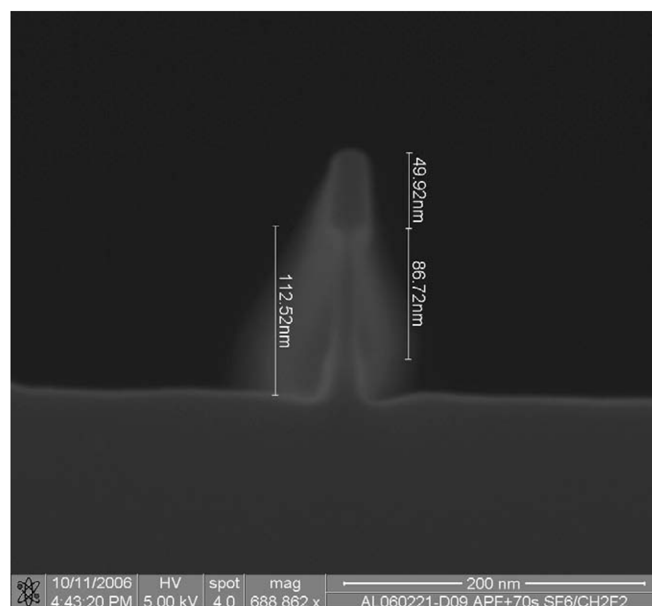

Fig. 3. X-SEM image of a fin with nitride mask, etched with the same conditions as for Fig. 1.

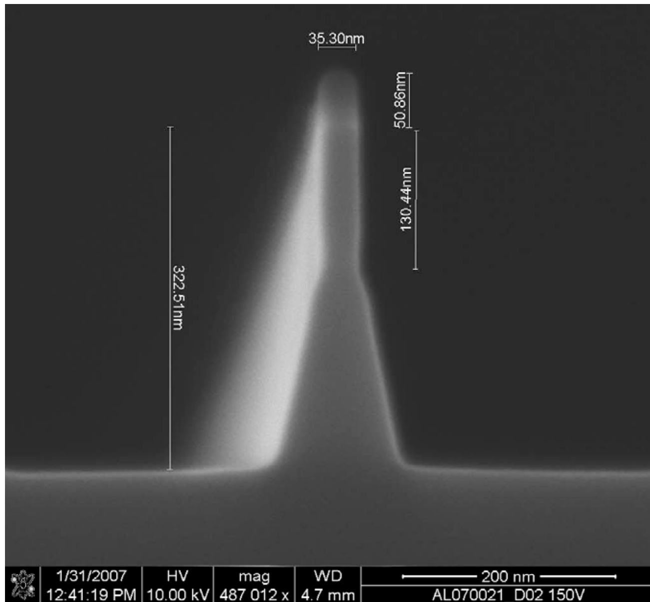

Fig. 4. X-SEM image of a fin after full patterning.

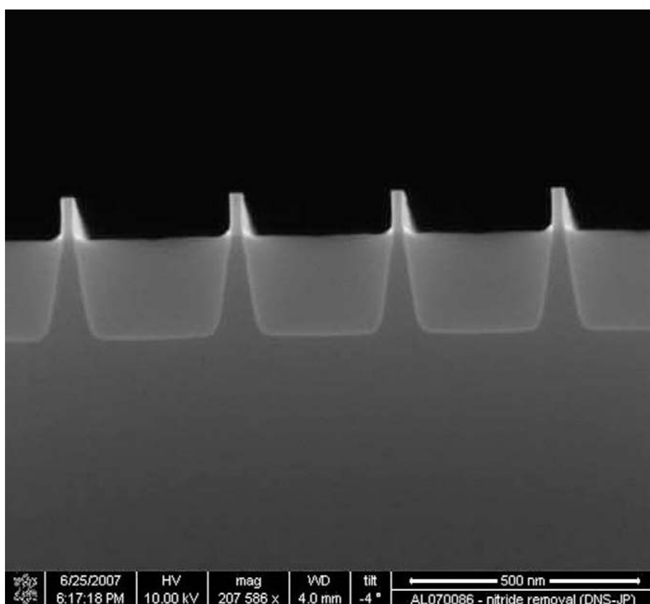

Fig. 5. X-SEM image of a fin after full processing.

Fig. 2. It should be noted that the etch condition used to obtain results shown in Figs. 2 and 3 are the same, the only difference is presence of nitride in the stack where profile distortion was observed. The distortion could be explained by charging effects. Silicon nitride is known for easy charging and a charged layer in the stack can deflect incoming ions to the walls beneath the nitride layer if the ion energy is low. A similar effect is described in details elsewhere [12]. An obvious adaptation for the etch recipe is increasing the substrate bias in order to increase ion energy so the ions are not deflected anymore by the charged nitride layer. Indeed, after increasing the substrate bias from −70 to −200 V the profile distortion disappeared.

When the top straight part is patterned, the remaining α-C is removed (stripped) using O_2/Cl_2 (10% Cl_2) chemistry before switching to the STI-like etching. The α-C strip is required in order to prevent uneven damage to the nitride during the STI etch. As the STI chemistry contains oxygen (we use $Cl_2/O_2/N_2$ mixture) it easily removes the remaining α-C. Since the top surface of the α-C mask that was exposed to the plasma during nitride and top fin patterning is likely to be uneven (faceted) this faceting could be transferred to the nitride that will be detrimental for the stopping of CMP. If the remaining α-C is stripped before nitride is reached, then the nitride surface is exposed uniformly to the STI etch plasma that results in uniform loss of the nitride without faceting.

After the α-C stripping the remaining of the bulk fin is patterned using typical STI etch plasma ($Cl_2/O_2/N_2$) that produces sloped walls. It should be noted that nitride is relatively resistant to such type of plasma that allows any reasonable depth (typical depth for the STI trenches is 200–400 nm) to be achieved. The SEM image of the bulk fin after patterning is shown in Fig. 4.

After the patterning, the wafers underwent our standard STI processing as described in the experimental section, with adapted trench fill and CMP targets. Field recess was done in HF solution to target 70 nm fin height before gate fabrication (standard STI targets a flat surface at gate level). The SEM image of bulk fins after the full processing is shown in Fig. 5.

4. Conclusions

We propose a method to manufacture bulk fins for finFET. The bulk fins consist of two parts: the straight top one which is used as a fin and a sloped bottom one that facilitates the trench filling. The method is based on a conventional STI process flow with an additional α-C hard mask on top of the STI stack. The nitride layer and the top straight part of the fin is patterned using $CH_2F_2/SF_6/N_2$ chemistry and α-C as a mask, while the bottom sloped part is patterned using $Cl_2/O_2/N_2$ chemistry and the nitride layer as a mask. After the etching, the STI process flow remains unchanged.

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