

1	HAVING BIOMATERIAL COMPONENT OR INTEGRATED WITH LIVING ORGANISM	30	..Liquid crystal component
		31	..Optical waveguide structure
		32	..Optical grating structure
2	HAVING SUPERCONDUCTIVE COMPONENT	33	.Substrate dicing
3	HAVING MAGNETIC OR FERROELECTRIC COMPONENT	34	.Making emissive array
		35	..Multiple wavelength emissive
4	REPAIR OR RESTORATION	36	.Ordered or disordered
5	INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION	37	.Graded composition
	..Interconnecting plural devices on semiconductor substrate	38	.Passivating of surface
	..Optical characteristic sensed	39	.Mesa formation
8	..Chemical etching	40	..Tapered etching
9	...Plasma etching	41	..With epitaxial deposition of semiconductor adjacent mesa
10	..Electrical characteristic sensed	42	.Groove formation
11	..Utilizing integral test element	43	..Tapered etching
12	..And removal of defect	44	..With epitaxial deposition of semiconductor in groove
13	..Altering electrical property by material removal	45	.Dopant introduction into semiconductor region
14	WITH MEASURING OR TESTING	46	.Compound semiconductor
15	..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor	47	..Heterojunction
	..Optical characteristic sensed	48	MAKING DEVICE OR CIRCUIT RESPONSIVE TO NONELECTRICAL SIGNAL
16	..Electrical characteristic sensed	49	.Chemically responsive
17	..Utilizing integral test element	50	.Physical stress responsive
18	HAVING INTEGRAL POWER SOURCE (E.G., BATTERY, ETC.)	51	..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
20	ELECTRON EMITTER MANUFACTURE		
21	MANUFACTURE OF ELECTRICAL DEVICE CONTROLLED PRINTHEAD	52	..Having cantilever element
		53	..Having diaphragm element
22	MAKING DEVICE OR CIRCUIT EMISSIVE OF NONELECTRICAL SIGNAL	54	.Thermally responsive
	..Having diverse electrical device	55	..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor
24	..Including device responsive to nonelectrical signal		
25	...Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor	56	.Responsive to corpuscular radiation (e.g., nuclear particle detector, etc.)
	..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor	57	.Responsive to electromagnetic radiation
26	..Having additional optical element (e.g., optical fiber, etc.)	58	..Gettering of substrate
28	..Plural emissive devices	59	..Having diverse electrical device
29	..Including integrally formed optical element (e.g., reflective layer, luminescent material, contoured surface, etc.)	60	...Charge transfer device (e.g., CCD, etc.)
		61	..Continuous processing
		62	...Using running length substrate
		63	..Particulate semiconductor component

64	..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor	88	..Direct application of electric current
65	...Having additional optical element (e.g., optical fiber, etc.)	89	..Fusion or solidification of semiconductor region
66	...Plural responsive devices (e.g., array, etc.)	90	..Including storage of electrical charge in substrate
67	...Assembly of plural semiconductor substrates	91	..Avalanche diode
68	..Substrate dicing	92	..Schottky barrier junction
69	..Including integrally formed optical element (e.g., reflective layer, luminescent layer, etc.)	93	..Compound semiconductor
70	...Color filter	94	...Heterojunction
71	...Specific surface topography (e.g., textured surface, etc.)	95	...Chalcogen (i.e., oxygen (O), sulfur (S), selenium (Se), tellurium (Te)) containing
72	...Having reflective or antireflective component	96	..Amorphous semiconductor
73	..Making electromagnetic responsive array	97	..Polycrystalline semiconductor
74	...Vertically arranged (e.g., tandem, stacked, etc.)	98	..Contact formation (i.e., metallization)
75	...Charge transfer device (e.g., CCD, etc.)	99	HAVING ORGANIC SEMICONDUCTIVE COMPONENT
76	...Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)	100	MAKING POINT CONTACT DEVICE
77	...Compound semiconductor	101	..Direct application of electrical current
78	...Having structure to improve output signal (e.g., exposure control structure, etc.)	102	HAVING SELENIUM OR TELLURIUM ELEMENTAL SEMICONDUCTOR COMPONENT
79	...Having blooming suppression structure (e.g., antiblooming drain, etc.)	103	..Direct application of electrical current
80	...Lateral series connected array	104	HAVING METAL OXIDE OR COPPER SULFIDE COMPOUND SEMICONDUCTOR COMPONENT
81	...Specified shape junction barrier (e.g., V-grooved junction, etc.)	105	HAVING DIAMOND SEMICONDUCTOR COMPONENT
82	..Having organic semiconductor component	106	PACKAGING (E.G., WITH MOUNTING, ENCAPSULATING, ETC.) OR TREATMENT OF PACKAGED SEMICONDUCTOR
83	..Forming point contact	107	..Assembly of plural semiconductive substrates each possessing electrical device
84	..Having selenium or tellurium elemental semiconductor component	108	..Flip-chip-type assembly
85	..Having metal oxide or copper sulfide compound semiconductive component	109	..Stacked array (e.g., rectifier, etc.)
86	...And cadmium sulfide compound semiconductive component	110	..Making plural separate devices
87	..Graded composition	111	..Using strip lead frame
		112	...And encapsulating
		113	..Substrate dicing
		114	...Utilizing a coating to perfect the dicing
		115	..Including contaminant removal or mitigation
		116	..Having light transmissive window
		117	..Incorporating resilient component (e.g., spring, etc.)
		118	..Including adhesive bonding step

119	..Electrically conductive adhesive	146	..Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)
120	.With vibration step	147	..Changing width or direction of channel (e.g., meandering channel, etc.)
121	.Metallic housing or support	148	..Substantially incomplete signal charge transfer (e.g., bucket brigade, etc.)
122	..Possessing thermal dissipation structure (i.e., heat sink)	149	.On insulating substrate or layer (e.g., TFT, etc.)
123	..Lead frame	150	..Specified crystallographic orientation
124	..And encapsulating	151	..Having insulated gate
125	.Insulative housing or support	152	...Combined with electrical device not on insulating substrate or layer
126	..And encapsulating	153	...Complementary field effect transistors
127	.Encapsulating	154	...Complementary field effect transistors
128	MAKING DEVICE ARRAY AND SELECTIVELY INTERCONNECTING	155	...And additional electrical device on insulating substrate or layer
129	.With electrical circuit layout	156	...Vertical channel
130	.Rendering selected devices operable or inoperable	157	...Plural gate electrodes (e.g., dual gate, etc.)
131	.Using structure alterable to conductive state (i.e., antifuse)	158	...Inverted transistor structure
132	.Using structure alterable to nonconductive state (i.e., fuse)	159	...Source-to-gate or drain-to-gate overlap
133	MAKING REGENERATIVE-TYPE SWITCHING DEVICE (E.G., SCR, IGBT, THYRISTOR, ETC.)	160	...Utilizing backside irradiation
134	.Bidirectional rectifier with control electrode (e.g., triac, diac, etc.)	161	...Including source or drain electrode formation prior to semiconductor layer formation (i.e., staggered electrodes)
135	.Having field effect structure	162	...Introduction of nondopant into semiconductor layer
136	..Junction gate	163	...Adjusting channel dimension (e.g., providing lightly doped source or drain region, etc.)
137	...Vertical channel	164	...Semiconductor islands formed upon insulating substrate or layer (e.g., mesa formation, etc.)
138	..Vertical channel	165	...Including differential oxidation
139	.Altering electrical characteristic	166	...Including recrystallization step
140	.Having structure increasing breakdown voltage (e.g., guard ring, field plate, etc.)	167	.Having Schottky gate (e.g., MESFET, HEMT, etc.)
141	MAKING CONDUCTIVITY MODULATION DEVICE (E.G., UNIJUNCTION TRANSISTOR, DOUBLE BASE DIODE, CONDUCTIVITY-MODULATED TRANSISTOR, ETC.)	168	..Specified crystallographic orientation
142	MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS	169	..Complementary Schottky gate field effect transistors
143	.Gettering of semiconductor substrate		
144	.Charge transfer device (e.g., CCD, etc.)		
145	..Having additional electrical device		

170	..And bipolar device	201Including insulated gate field effect transistor having gate surrounded by dielectric (i.e., floating gate)
171	..And passive electrical device (e.g., resistor, capacitor, etc.)	202Including bipolar transistor (i.e., BiCMOS)
172	..Having heterojunction (e.g., HEMT, MODFET, etc.)	203Complementary bipolar transistors
173	..Vertical channel	204Lateral bipolar transistor
174	..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)	205Plural bipolar transistors of differing electrical characteristics
175	..Buried channel	206Vertical channel insulated gate field effect transistor
176	..Plural gate electrodes (e.g., dual gate, etc.)	207Including isolation structure
177	..Closed or loop gate	208Isolation by PN junction only
178	..Elemental semiconductor	209	...Including additional vertical channel insulated gate field effect transistor
179	..Asymmetric	210	...Including passive device (e.g., resistor, capacitor, etc.)
180	..Self-aligned	211	..Having gate surrounded by dielectric (i.e., floating gate)
181	...Doping of semiconductive region	212	..Vertical channel
182T-gate	213	..Common active region
183Dummy gate	214	..Having underpass or crossunder
184Utilizing gate sidewall structure	215	..Having fuse or integral short
185Multiple doping steps	216	..Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound
186	..Having junction gate (e.g., JFET, SIT, etc.)	217	...Doping of semiconductor channel region beneath gate insulator (e.g., threshold voltage adjustment, etc.)
187	..Specified crystallographic orientation	218	...Including isolation structure
188	..Complementary junction gate field effect transistors	219Total dielectric isolation
189	..And bipolar transistor	220Isolation by PN junction only
190	..And passive device (e.g., resistor, capacitor, etc.)	221Dielectric isolation formed by grooving and refilling with dielectric material
191	..Having heterojunction	222With epitaxial semiconductor layer formation
192	..Vertical channel	223Having well structure of opposite conductivity type
193	..Multiple parallel current paths (e.g., grid gate, etc.)	224Plural wells
194	..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)	225	...Recessed oxide formed by localized oxidation (i.e., LOCOS)
195	..Plural gate electrodes	226With epitaxial semiconductor layer formation
196	..Including isolation structure		
197	..Having insulated gate (e.g., IGFET, MISFET, MOSFET, etc.)		
198	..Specified crystallographic orientation		
199	..Complementary insulated gate field effect transistors (i.e., CMOS)		
200	...And additional electrical device		

227Having well structure of opposite conductivity type	257	..Having additional gate electrode surrounded by dielectric (i.e., floating gate)
228Plural wells		
229	...Self-aligned		
230	...Utilizing gate sidewall structure	258	...Including additional field effect transistor (e.g., sense or access transistor, etc.)
231Plural doping steps		
232Plural doping steps	259	...Including forming gate electrode in trench or recess in substrate
233	...And contact formation		
234	..Including bipolar transistor (i.e., BiMOS)	260	...Textured surface of gate insulator or gate electrode
235	..Heterojunction bipolar transistor	261	...Multiple interelectrode dielectrics or nonsilicon compound gate insulator
236	...Lateral bipolar transistor		
237	..Including diode	262	...Including elongated source or drain region disposed under thick oxide regions (e.g., buried or diffused bitline, etc.)
238	..Including passive device (e.g., resistor, capacitor, etc.)		
239	...Capacitor	263Tunneling insulator
240Having high dielectric constant insulator (e.g., Ta2O5, etc.)	264	...Tunneling insulator
241And additional field effect transistor (e.g., sense or access transistor, etc.)	265	...Oxidizing sidewall of gate electrode
242Including transistor formed on trench sidewalls	266	...Having additional, nonmemory control electrode or channel portion (e.g., for accessing field effect transistor structure, etc.)
243Trench capacitor		
244Utilizing stacked capacitor structure (e.g., stacked trench, buried stacked capacitor, etc.)	267	...Including forming gate electrode as conductive sidewall spacer to another electrode
245With epitaxial layer formed over the trench		
246Including doping of trench surfaces	268	..Vertical channel
247Multiple doping steps	269	...Utilizing epitaxial semiconductor layer grown through an opening in an insulating layer
248Including isolation means formed in trench		
249Doping by outdiffusion from a dopant source layer (e.g., doped oxide, etc.)	270	...Gate electrode in trench or recess in semiconductor substrate
250Planar capacitor	271V-gate
251Including doping of semiconductive region	272Totally embedded in semiconductive layers
252Multiple doping steps	273	...Having integral short of source and base regions
253Stacked capacitor		
254Including selectively removing material to undercut and expose storage node layer	274Short formed in recess in substrate
255Including texturizing storage node layer	275	..Making plural insulated gate field effect transistors of differing electrical characteristics
256Contacts formed by selective growth or deposition	276	...Introducing a dopant into the channel region of selected transistors

277Including forming overlapping gate electrodes	302Oblique implantation
278After formation of source or drain regions and gate electrode (e.g., late programming, encoding, etc.)	303Utilizing gate sidewall structure
279	..Making plural insulated gate field effect transistors having common active region	304Conductive sidewall component
280	..Having underpass or crossunder	305Plural doping steps
281	..Having fuse or integral short	306Plural doping steps
282	..Buried channel	307Using same conductivity-type dopant
283	..Plural gate electrodes (e.g., dual gate, etc.)	308	..Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)
284	..Closed or loop gate		
285	..Utilizing compound semiconductor	309	FORMING BIPOLAR TRANSISTOR BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS
286	..Asymmetric		
287	..Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound	310	.Gettering of semiconductor substrate
288	..Having step of storing electrical charge in gate dielectric	311	.On insulating substrate or layer (i.e., SOI type)
289	..Doping of semiconductive channel region beneath gate insulator (e.g., adjusting threshold voltage, etc.)	312	.Having heterojunction
290	...After formation of source or drain regions and gate electrode	313	..Complementary bipolar transistors
291	...Using channel conductivity dopant of opposite type as that of source and drain	314	..And additional electrical device
292	..Direct application of electrical current	315	..Forming inverted transistor structure
293	..Fusion or solidification of semiconductor region	316	..Forming lateral transistor structure
294	..Including isolation structure	317	..Wide bandgap emitter
295	...Total dielectric isolation	318	..Including isolation structure
296	..Dielectric isolation formed by grooving and refilling with dielectric material	319	...Air isolation (e.g., mesa, etc.)
297	...Recessed oxide formed by localized oxidation (i.e., LOCOS)	320	..Self-aligned
298Doping region beneath recessed oxide (e.g., to form chanstop, etc.)	321	...Utilizing dummy emitter
299	..Self-aligned	322	.Complementary bipolar transistors
300	..Having elevated source or drain (e.g., epitaxially formed source or drain, etc.)	323	..Having common active region (i.e., integrated injection logic (I ² L), etc.)
301	...Source or drain doping	324	...Including additional electrical device
		325	...Having lateral bipolar transistor
		326	..Including additional electrical device
		327	..Having lateral bipolar transistor
		328	.Including diode
		329	.Including passive device (e.g., resistor, capacitor, etc.)
		330	..Resistor

331	...Having same doping as emitter or collector	361	...Including deposition of polysilicon or noninsulative material into groove
332	...Lightly doped junction isolated resistor	362	..Recessed oxide by localized oxidation (i.e., LOCOS)
333	..Having fuse or integral short	363	...With epitaxial semiconductor layer formation
334	..Forming inverted transistor structure	364	.Self-aligned
335	..Forming lateral transistor structure	365	..Forming active region from adjacent doped polycrystalline or amorphous semiconductor
336	..Combined with vertical bipolar transistor	366	...Having sidewall
337	..Active region formed along groove or exposed edge in semiconductor	367	...Including conductive component
338	..Having multiple emitter or collector structure	368	...Simultaneously outdiffusing plural dopants from polysilicon or amorphous semiconductor
339	..Self-aligned	369	..Dopant implantation or diffusion
340	..Making plural bipolar transistors of differing electrical characteristics	370	...Forming buried region (e.g., implanting through insulating layer, etc.)
341	..Using epitaxial lateral overgrowth	371	...Simultaneous introduction of plural dopants
342	..Having multiple emitter or collector structure	372Plural doping steps
343	..Mesa or stacked emitter	373Multiple ion implantation steps
344	..Washed emitter	374Using same conductivity-type dopant
345	..Walled emitter	375Forming partially overlapping regions
346	..Emitter dip prevention or utilization	376Single dopant forming regions of different depth or concentrations
347	..Permeable or metal base	377Through same mask opening
348	..Sidewall base contact	378	..Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)
349	..Pedestal base	379	VOLTAGE VARIABLE CAPACITANCE DEVICE MANUFACTURE (E.G., VARACTOR, ETC.)
350	..Forming base region of specified dopant concentration profile (e.g., inactive base region more heavily doped than active base region, etc.)	380	AVALANCHE DIODE MANUFACTURE (E.G., IMPATT, TRAPPAT, ETC.)
351	..Direct application of electrical current	381	MAKING PASSIVE DEVICE (E.G., RESISTOR, CAPACITOR, ETC.)
352	..Fusion or solidification of semiconductor region	382	.Resistor
353	..Including isolation structure	383	..Lightly doped junction isolated resistor
354	..Having semi-insulative region	384	..Deposited thin film resistor
355	..Total dielectrical isolation	385	...Altering resistivity of conductor
356	..Isolation by PN junction only		
357	...Including epitaxial semiconductor layer formation		
358Up diffusion of dopant from substrate into epitaxial layer		
359	..Dielectric isolation formed by grooving and refilling with dielectrical material		
360	...With epitaxial semiconductor formation in groove		

386	.Trench capacitor	415	..Thermomigration
387	..Having stacked capacitor structure (e.g., stacked trench, buried stacked capacitor, etc.)	416	..With epitaxial semiconductor formation
		417	...And simultaneous polycrystalline growth
388	..With epitaxial layer formed over the trench	418	...Dopant addition
		419Plural doping steps
389	..Including doping of trench surfaces	420	..Plural doping steps
		421	.Having air-gap dielectric (e.g., groove, etc.)
390	..Multiple doping steps		
391	..Including isolation means formed in trench	422	..Enclosed cavity
		423	.Implanting to form insulator
392	..Doping by outdiffusion from a dopant source layer (e.g., doped oxide)	424	.Grooved and refilled with deposited dielectric material
		425	..Combined with formation of recessed oxide by localized oxidation
393	.Planar capacitor		
394	..Including doping of semiconductive region	426	...Recessed oxide laterally extending from groove
		427	..Refilling multiple grooves of different widths or depths
395	..Multiple doping steps	428	...Reflow of insulator
396	.Stacked capacitor	429	..And epitaxial semiconductor formation in groove
397	..Including selectively removing material to undercut and expose storage node layer	430	..And deposition of polysilicon or noninsulative material into groove
398	..Including texturizing storage node layer		
399	..Having contacts formed by selective growth or deposition	431	...Oxidation of deposited material
400	FORMATION OF ELECTRICALLY ISOLATED LATERAL SEMICONDUCTIVE STRUCTURE	432Nonoxidized portions remaining in groove after oxidation
401	.Having substrate registration feature (e.g., alignment mark)	433	..Dopant addition
402	.And gettering of substrate	434	..From doped insulator in groove
403	.Having semi-insulating component	435	..Multiple insulative layers in groove
404	.Total dielectric isolation		
405	..And separate partially isolated semiconductor regions	436	...Reflow of insulator
406	..Bonding of plural semiconductive substrates	437	...Conformal insulator formation
		438	..Reflow of insulator
407	..Nondopant implantation	439	.Recessed oxide by localized oxidation (i.e., LOCOS)
408	..With electrolytic treatment step	440	..Including nondopant implantation
		441	..With electrolytic treatment step
409	...Porous semiconductor formation	442	..With epitaxial semiconductor layer formation
410	..Encroachment of separate locally oxidized regions	443	..Etchback of recessed oxide
411	..Air isolation (e.g., beam lead supported semiconductor islands, etc.)	444	..Preliminary etching of groove
		445	...Masking of groove sidewall
412	...Semiconductor islands formed upon insulating substrate or layer (e.g., mesa isolation, etc.)	446Polysilicon containing sidewall
		447Dopant addition
413	..With epitaxial semiconductor formation	448	..Utilizing oxidation mask having polysilicon component
414	.Isolation by PN junction only		

449	..Dopant addition	480	..Including implantation of ion which reacts with semiconductor substrate to form insulating layer
450	...Implanting through recessed oxide		
451	...Plural doping steps		
452	..Plural oxidation steps to form recessed oxide	481	..Utilizing epitaxial lateral overgrowth
453	..And electrical conductor formation (i.e., metallization)	482	.Amorphous semiconductor
454	.Field plate electrode	483	..Compound semiconductor
455	BONDING OF PLURAL SEMICONDUCTOR SUBSTRATES	484	..Running length (e.g., sheet, strip, etc.)
456	.Having enclosed cavity	485	..Deposition utilizing plasma (e.g., glow discharge, etc.)
457	.Warping of semiconductor substrate	486	..And subsequent crystallization
458	.Subsequent separation into plural bodies (e.g., delaminating, dicing, etc.)	487	...Utilizing wave energy (e.g., laser, electron beam, etc.)
459	.Thinning of semiconductor substrate	488	.Polycrystalline semiconductor
460	SEMICONDUCTOR SUBSTRATE DICING	489	..Simultaneous single crystal formation
461	.Beam lead formation	490	..Running length (e.g., sheet, strip, etc.)
462	.Having specified scribe region structure (e.g., alignment mark, plural grooves, etc.)	491	..And subsequent doping of polycrystalline semiconductor
463	.By electromagnetic irradiation (e.g., electron, laser, etc.)	492	.Fluid growth step with preceding and subsequent diverse operation
464	.With attachment to temporary support or carrier	493	.Plural fluid growth steps with intervening diverse operation
465	.Having a perfecting coating	494	..Differential etching
466	DIRECT APPLICATION OF ELECTRICAL CURRENT	495	..Doping of semiconductor
467	.To alter conductivity of fuse or antifuse element	496	..Coating of semiconductive substrate with nonsemiconductive material
468	.Electromigration	497	.Fluid growth from liquid combined with preceding diverse operation
469	.Utilizing pulsed current	498	..Differential etching
470	.Fusion of semiconductor region	499	..Doping of semiconductor
471	GETTERING OF SUBSTRATE	500	.Fluid growth from liquid combined with subsequent diverse operation
472	.By vibrating or impacting		
473	.By implanting or irradiating		
474	..Ionized radiation (e.g., corpuscular or plasma treatment, etc.)	501	..Doping of semiconductor
475	...Hydrogen plasma (i.e., hydrogenization)	502	..Heat treatment
476	.By layers which are coated, contacted, or diffused	503	.Fluid growth from gaseous state combined with preceding diverse operation
477	.By vapor phase surface reaction	504	..Differential etching
478	FORMATION OF SEMICONDUCTIVE ACTIVE REGION ON ANY SUBSTRATE (E.G., FLUID GROWTH, DEPOSITION)	505	..Doping of semiconductor
479	.On insulating substrate or layer	506	...Ion implantation
		507	.Fluid growth from gaseous state combined with subsequent diverse operation
		508	..Doping of semiconductor
		509	..Heat treatment

510	INTRODUCTION OF CONDUCTIVITY MODIFYING DOPANT INTO SEMICONDUCTIVE MATERIAL	540	..Including plural controlled heating or cooling steps or nonuniform heating
511	..Ordering or disordering	541	...Including diffusion after fusing step
512	..Involving nuclear transmutation doping	542	..Diffusing a dopant
513	..Plasma (e.g., glow discharge, etc.)	543	..To control carrier lifetime (i.e., deep level dopant)
514	..Ion implantation of dopant into semiconductor region	544	..To solid-state solubility concentration
515	..Ionized molecules	545	..Forming partially overlapping regions
516	..Including charge neutralization	546	..Plural dopants in same region (e.g., through same mask opening, etc.)
517	..Of semiconductor layer on insulating substrate or layer	547	...Simultaneously
518	..Of compound semiconductor	548	..Plural dopants simultaneously in plural regions
519	...Including multiple implantation steps	549	..Single dopant forming plural diverse regions (e.g., forming regions of different concentrations or of different depths, etc.)
520Providing nondopant ion (e.g., proton, etc.)	550	..Nonuniform heating
521Using same conductivity-type dopant	551	..Using multiple layered mask
522	...Including heat treatment	552	...Having plural predetermined openings in master mask
523	..And contact formation (i.e., metallization)	553	..Using metal mask
524	..Into grooved semiconductor substrate region	554	..Outwardly
525	..Using oblique beam	555	..Laterally under mask opening
526	..Forming buried region	556	..Edge diffusion by using edge portion of structure other than masking layer to mask
527	..Including multiple implantation steps	557	..From melt
528	...Providing nondopant ion (e.g., proton, etc.)	558	..From solid dopant source in contact with semiconductor region
529	...Using same conductivity-type dopant	559	...Using capping layer over dopant source to prevent out-diffusion of dopant
530	..Including heat treatment	560	...Plural diffusion stages
531	..Using shadow mask	561	...Dopant source within trench or groove
532	..Into polycrystalline region	562	...Organic source
533	..And contact formation (i.e., metallization)	563	...Glassy source or doped oxide
534	...Rectifying contact (i.e., Schottky contact)	564	...Polycrystalline semiconductor source
535	..By application of corpuscular or electromagnetic radiation (e.g., electron, laser, etc.)	565	..From vapor phase
536	..Recoil implantation	566	...Plural diffusion stages
537	..Fusing dopant with substrate (i.e., alloy junction)	567	...Solid source in operative relation with semiconductor region
538	..Using additional material to improve wettability or flow characteristics (e.g., flux, etc.)	568	...In capsule-type enclosure
539	..Application of pressure to material during fusion	569	...Into compound semiconductor region

570	FORMING SCHOTTKY JUNCTION (I.E., SEMICONDUCTOR-CONDUCTOR RECTIFYING JUNCTION CONTACT)	595	..Having sidewall structure
		596	...Portion of sidewall structure is conductive
571	..Combined with formation of ohmic contact to semiconductor region	597	..To form ohmic contact to semiconductive material
572	..Compound semiconductor	598	..Selectively interconnecting (e.g., customization, wafer scale integration, etc.)
573	..Multilayer electrode		
574	...T-shaped electrode	599	...With electrical circuit layout
575	...Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)	600	...Using structure alterable to conductive state (i.e., antifuse)
576	..Into grooved or recessed semiconductor region	601	...Using structure alterable to nonconductive state (i.e., fuse)
577	...Utilizing lift-off	602	..To compound semiconductor
578	...Forming electrode of specified shape (e.g., slanted, etc.)	603	...II-VI compound semiconductor
579	...T-shaped electrode	604	...III-V compound semiconductor
580	..Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)	605	...Multilayer electrode
581	..Silicide	606	...Ga and As containing semiconductor
582	..Using refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)	607	..With epitaxial conductor formation
583	..Silicide	608	..Oxidic conductor (e.g., indium tin oxide, etc.)
584	COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL	609	...Transparent conductor
585	..Insulated gate formation	610	..Conductive macromolecular conductor (including metal powder filled composition)
586	..Combined with formation of ohmic contact to semiconductor region	611	..Beam lead formation
587	..Forming array of gate electrodes	612	..Forming solder contact or bonding pad
588	...Plural gate levels	613	...Bump electrode
589	..Recessed into semiconductor substrate	614	...Plural conductive layers
590	..Compound semiconductor	615	...Including fusion of conductor
591	..Gate insulator structure constructed of plural layers or nonsilicon containing compound	616By transcription from auxiliary substrate
592	..Possessing plural conductive layers (e.g., polycide)	617By wire bonding
593	...Separated by insulator (i.e., floating gate)	618	..Contacting multiple semiconductive regions (i.e., interconnects)
594	...Tunnelling dielectric layer	619	...Air bridge structure
		620	...Forming contacts of differing depths into semiconductor substrate
		621	...Contacting diversely doped semiconductive regions (e.g., p-type and n-type regions, etc.)
		622	...Multiple metal levels, separated by insulating layer (i.e., multiple level metallization)
		623	...Including organic insulating material between metal levels

624Separating insulating layer is laminate or composite of plural insulating materials	650Having noble group metal (i.e., silver (Ag), gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)
625At least one metallization level formed of diverse conductive layers	651Silicide
626Planarization	652	..Plural layered electrode or conductor
627At least one layer forms a diffusion barrier	653	...At least one layer forms a diffusion barrier
628Having adhesion promoting layer	654	...Having adhesion promoting layer
629Diverse conductive layers limited to viahole/plug	655	...Silicide
630Silicide formation	656	...Having refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)
631	...Having planarization step	657	...Having electrically conductive polysilicon component
632Utilizing reflow	658	..Altering composition of conductor
633Simultaneously by chemical and mechanical means	659	...Implantation of ion into conductor
634Utilizing etch-stop layer	660	..Including heat treatment of conductive layer
635	...Insulator formed by reaction with conductor (e.g., oxidation, etc.)	661	...Subsequent fusing conductive layer
636	...Including use of antireflective layer	662	...Utilizing laser
637	...With formation of opening (i.e., viahole) in insulative layer	663	...Rapid thermal anneal
638Having viaholes of diverse width	664	...Forming silicide
639Having viahole with sidewall component	665	..Utilizing textured surface
640Having viahole of tapered shape	666	..Specified configuration of electrode or contact
641	...Selective deposition	667	...Conductive feedthrough or through-hole in substrate
642	...Diverse conductors	668	...Specified aspect ratio of conductor or viahole
643	...At least one layer forms a diffusion barrier	669	..And patterning of conductive layer
644	...Having adhesion promoting layer	670	...Utilizing lift-off
645	...Having planarization step	671	...Utilizing multilayered mask
646Utilizing reflow	672	...Plug formation (i.e., in viahole)
647	...Having electrically conductive polysilicon component	673	...Tapered etching
648	...Having refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)	674	..Selective deposition of conductive layer
649Silicide	675	...Plug formation (i.e., in viahole)
		676	..Utilizing electromagnetic or wave energy

677	...Pretreatment of surface to enhance or retard deposition	699	...Plural coating steps
678	..Electroless deposition of conductive layer	700	..Formation of groove or trench
679	..Evaporative coating of conductive layer	701	...Tapered configuration
680	..Utilizing chemical vapor deposition (i.e., CVD)	702	...Plural coating steps
681	...Of organo-metallic precursor (i.e., MOCVD)	703	..Plural coating steps
682	..Silicide	704	..Having liquid and vapor etching steps
683	..Of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)	705	..Altering etchability of substrate region by compositional or crystalline modification
684	..Electrically conductive polysilicon	706	..Vapor phase etching (i.e., dry etching)
685	..Refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)	707	..Utilizing electromagnetic or wave energy
686	..Noble group metal (i.e., silver (Ag), gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)	708	...Photo-induced etching
687	..Copper or copper alloy conductor	709Photo-induced plasma etching
688	..Aluminum or aluminum alloy conductor	710	...By creating electric field (e.g., plasma, glow discharge, etc.)
689	CHEMICAL ETCHING	711Utilizing multiple gas energizing means
690	..Combined with the removal of material by nonchemical means (e.g., ablating, abrading, etc.)	712Reactive ion beam etching (i.e., RIBE)
691	..Combined mechanical and chemical material removal	713Forming tapered profile (e.g., tapered etching, etc.)
692	...Simultaneous (e.g., chemical-mechanical polishing, etc.)	714Including change in etch influencing parameter (e.g., energizing power, etchant composition, temperature, etc.)
693Utilizing particulate abradant	715With substrate heating or cooling
694	..Combined with coating step	716With substrate handling (e.g., conveying, etc.)
695	..Simultaneous etching and coating	717Utilizing multilayered mask
696	..Coating of sidewall	718Compound semiconductor
697	..Planarization by etching and coating	719Silicon
698	...Utilizing reflow	720Electrically conductive material (e.g., metal, conductive oxide, etc.)
		721Silicide
		722Metal oxide
		723Silicon oxide or glass
		724Silicon nitride
		725Organic material (e.g., resist, etc.)
		726Having microwave gas energizing
		727Producing energized gas remotely located from substrate
		728Using magnet (e.g., electron cyclotron resonance, etc.)

729Using specified electrode/ susceptor configuration (e.g., of multiple substrates using barrel-type susceptor, planar reactor configuration, etc.) to generate plasma	754	..Electrically conductive material (e.g., metal, conductive oxide, etc.)
730Producing energized gas remotely located from substrate	755	...Silicide
731Using intervening shield structure	756	..Silicon oxide
732	...Using magnet (e.g., electron cyclotron resonance, etc.)	757	..Silicon nitride
733	...Using or orientation dependent etchant (i.e., anisotropic etchant)	758	COATING OF SUBSTRATE CONTAINING SEMICONDUCTOR REGION OR OF SEMICONDUCTOR SUBSTRATE
734	..Sequential etching steps on a single layer	759	.Combined with the removal of material by nonchemical means
735	..Differential etching of semiconductor substrate	760	.Utilizing reflow (e.g., planarization, etc.)
736	...Utilizing multilayered mask	761	.Multiple layers
737	..Substrate possessing multiple layers	762	..At least one layer formed by reaction with substrate
738Selectively etching substrate possessing multiple layers of differing etch characteristics	763	..Layers formed of diverse composition or by diverse coating processes
739Lateral etching of intermediate layer (i.e., undercutting)	764	.Formation of semi-insulative polycrystalline silicon
740Utilizing etch stop layer	765	.By reaction with substrate
741PN junction functions as etch stop	766	..Implantation of ion (e.g., to form ion amorphousized region prior to selective oxidation, reacting with substrate to form insulative region, etc.)
742Electrically conductive material (e.g., metal, conductive oxide, etc.)	767	..Compound semiconductor substrate
743Silicon oxide or glass	768	..Reaction with conductive region
744Silicon nitride	769	..Reaction with silicon semiconductive region (e.g., oxynitride formation, etc.)
745	.Liquid phase etching	770	...Oxidation
746	..Utilizing electromagnetic or wave energy	771	...Using electromagnetic or wave energy
747	..With relative movement between substrate and confined pool of etchant	772Microwave gas energizing
748	..Projection of etchant against a moving substrate or controlling the angle or pattern of projected etchant	773	...In atmosphere containing water vapor (i.e., wet oxidation)
749	..Sequential application of etchant	774	...In atmosphere containing halogen
750	...To same side of substrate	775	...Nitridation
751Each etch step exposes surface of an adjacent layer	776	...Using electromagnetic or wave energy
752	..Germanium	777Microwave gas energizing
753	..Silicon	778	.Insulative material deposited upon semiconductive substrate
		779	..Compound semiconductor substrate
		780	..Depositing organic material (e.g., polymer, etc.)
		781	...Subsequent heating modifying organic coating composition

782	..With substrate handling during coating (e.g., immersion, spinning, etc.)	904	CHARGE CARRIER LIFETIME CONTROL
		905	CLEANING OF REACTION CHAMBER
		906	CLEANING OF WAFER AS INTERIM STEP
783	..Insulative material having impurity (e.g., for altering physical characteristics, etc.)	907	CONTINUOUS PROCESSING
		908	.Utilizing cluster apparatus
		909	CONTROLLED ATMOSPHERE
784	...Introduction simultaneous with deposition	910	CONTROLLING CHARGING STATE AT SEMICONDUCTOR-INSULATOR INTERFACE
785	..Insulative material is compound of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)	911	DIFFERENTIAL OXIDATION AND ETCHING
		912	DISPLACING PN JUNCTION
		913	DIVERSE TREATMENTS PERFORMED IN UNITARY CHAMBER
		914	DOPING
		915	.Amphoteric doping
786	..Tertiary silicon containing compound formation (e.g., oxynitride formation, etc.)	916	.Autodoping control or utilization
		917	.Deep level dopants (e.g., gold (Au), chromium (Cr), iron (Fe), nickel (Ni), etc.)
787	..Silicon oxide formation	918	.Special or nonstandard dopant
788	...Using electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)	919	.Compensation doping
		920	.Controlling diffusion profile by oxidation
789	...Organic reactant	921	.Nonselective diffusion
790	...Organic reactant	922	.Diffusion along grain boundaries
791	..Silicon nitride formation	923	.Diffusion through a layer
792	..Utilizing electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)	924	.To facilitate selective etching
		925	.Fluid growth doping control (e.g., delta doping, etc.)
793	...Organic reactant	926	DUMMY METALLIZATION
794	...Organic reactant	927	ELECTROMIGRATION RESISTANT METALLIZATION
795	RADIATION OR ENERGY TREATMENT MODIFYING PROPERTIES OF SEMICONDUCTOR REGION OF SUBSTRATE (E.G., THERMAL, CORPUSCULAR, ELECTROMAGNETIC, ETC.)	928	FRONT AND REAR SURFACE PROCESSING
		929	EUTECTIC SEMICONDUCTOR
		930	TERNARY OR QUATERNARY SEMICONDUCTOR COMPRISED OF ELEMENTS FROM THREE DIFFERENT GROUPS (E.G., I-III-V, ETC.)
796	.Compound semiconductor	931	SILICON CARBIDE SEMICONDUCTOR
797	..Ordering or disordering	932	BORON NITRIDE SEMICONDUCTOR
798	.Ionized irradiation (e.g., corpuscular or plasma treatment, etc.)	933	GERMANIUM OR SILICON OR GE-SI ON III-V
799	.By differential heating	934	SHEET RESISTANCE (I.E., DOPANT PARAMETERS)
800	MISCELLANEOUS	935	GAS FLOW CONTROL
		936	GRADED ENERGY GAP
		937	HILLOCK PREVENTION
		938	LATTICE STRAIN CONTROL OR UTILIZATION
		939	LANGMUIR-BLODGETT FILM UTILIZATION
		940	LASER ABLATIVE MATERIAL REMOVAL
		941	LOADING EFFECT MITIGATION
<u>CROSS-REFERENCE ART COLLECTIONS</u>			
900	BULK EFFECT DEVICE MAKING		
901	CAPACITIVE JUNCTION		
902	CAPPING LAYER		
903	CATALYST AIDED DEPOSITION		

942	MASKING	982	VARYING ORIENTATION OF DEVICES IN ARRAY
943	.Movable		
944	.Shadow	983	ZENER DIODES
945	.Special (e.g., metal, etc.)		
946	.Step and repeat		
947	.Subphotolithographic processing		
948	.Radiation resist		
949	..Energy beam treating radiation resist on semiconductor		
950	..Multilayer mask including nonradiation sensitive layer		
951	..Lift-off		
952	..Utilizing antireflective layer		
953	MAKING RADIATION RESISTANT DEVICE		
954	MAKING OXIDE-NITRIDE-OXIDE DEVICE		
955	MELT-BACK		
956	MAKING MULTIPLE WAVELENGTH EMISSIVE DEVICE		
957	MAKING METAL-INSULATOR-METAL DEVICE		
958	PASSIVATION LAYER		
959	MECHANICAL POLISHING OF WAFER		
960	POROUS SEMICONDUCTOR		
961	ION BEAM SOURCE AND GENERATION		
962	QUANTUM DOTS AND LINES		
963	REMOVING PROCESS RESIDUES FROM VERTICAL SUBSTRATE SURFACES		
964	ROUGHENED SURFACE		
965	SHAPED JUNCTION FORMATION		
966	SELECTIVE OXIDATION OF ION-AMORPHOUSIZED LAYER		
967	SEMICONDUCTOR ON SPECIFIED INSULATOR		
968	SEMICONDUCTOR-METAL-SEMICONDUCTOR		
969	SIMULTANEOUS FORMATION OF MONOCRYSTALLINE AND POLYCRYSTALLINE REGIONS		
970	SPECIFIED ETCH STOP MATERIAL		
971	STOICHIOMETRIC CONTROL OF HOST SUBSTRATE COMPOSITION		
972	STORED CHARGE ERASURE		
973	SUBSTRATE ORIENTATION		
974	SUBSTRATE SURFACE PREPARATION		
975	SUBSTRATE OR MASK ALIGNING FEATURE		
976	TEMPORARY PROTECTIVE LAYER		
977	THINNING OR REMOVAL OF SUBSTRATE		
978	FORMING TAPERED EDGES ON SUBSTRATE OR ADJACENT LAYERS		
979	TUNNEL DIODES		
980	UTILIZING PROCESS EQUIVALENTS OR OPTIONS		
981	UTILIZING VARYING DIELECTRIC THICKNESS		
			FOREIGN ART COLLECTIONS
			FOR 000 CLASS-RELATED FOREIGN DOCUMENTS
			Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.
			METHODS (156/1)
		FOR 100	.Etching of semiconductor precursor, substrates, and devices used in an electrical function (156/625.1)
		FOR 101	..Measuring, testing, or inspecting (156/626.1)
		FOR 102	...By electrical means or of electrical property (156/627.1)
		FOR 103	..Altering the etchability of a substrate by alloying, diffusing, or chemical reacting (156/628.1)
		FOR 104	..With uniting of preforms (e.g., laminating, etc.) (156/629.1)
		FOR 105	...Prior to etching (156/630.1)
		FOR 106	...Delamination subsequent to etching (156/631.1)
		FOR 107	...With coating (156/632.1)
		FOR 108	...Differential etching (156/633.1)
		FOR 109	...Metal layer etched (156/634.1)
		FOR 110	..With in situ activation or combining of etching components on surface (156/635.1)
		FOR 111	..With thin film of etchant between relatively moving substrate and conforming surface (e.g., chemical lapping, etc.) (156/636.1)

- FOR 112 ..With relative movement between the substrate and a confined pool of etchant (156/637.1)
- FOR 113 ...With removal of adhered reaction product from substrate (156/638.1)
- FOR 114 ...With substrate rotation, repeated dipping, or advanced movement (156/639.1)
- FOR 115 ..Projection of etchant against a moving substrate or controlling the angle or pattern of projected etchant (156/640.1)
- FOR 116 ..Recycling or regenerating etchant (156/642.1)
- FOR 117 ..With treatment by high energy radiation or plasma (e.g., ion beam, etc.) (156/643.1)
- FOR 118 ..Forming or increasing the size of an aperture (156/644.1)
- FOR 119 ..With mechanical deformation, severing, or abrading of a substrate (156/ 645.1)
- FOR 120 ..Etchant is a gas (156/646.1)
- FOR 121 ..Etching according to crystalline planes (156/647.1)
- FOR 122 ..Etching isolates or modifies a junction in a barrier layer (156/648.1)
- FOR 123 ...Discrete junction isolated (e.g., mesa formation, etc.) (156/649.1)
- FOR 124 ..Sequential application of etchant material (156/650.1)
- FOR 125 ...Sequentially etching the same surface of a substrate (156/ 651.1)
- FOR 126Each etching exposes surface of an adjacent layer (156/ 652.1)
- FOR 127Etched layer contains silicon (e.g., oxide, nitride, etc.) (156/653.1)
- FOR 128 ..Differential etching of a substrate (156/654.1)
- FOR 129 ..Composite substrate (156/ 655.1)
- FOR 130Substrate contains metallic element or compound (156/ 656.1)
- FOR 131Substrate contains silicon or silicon compound (156/657.1)
- FOR 132 ...Resist coating (156/659.11)
- FOR 133Plural resist coating (156/ 661.11)
- FOR 134 ..Silicon, germanium, or gallium containing substrate (156/ 662.1)
- FOR 135 **MAKING DEVICE HAVING ORGANIC SEMICONDUCTOR COMPONENT (437/ 1)**
- FOR 136 **MAKING DEVICE RESPONSIVE TO RADIATION (437/2)**
- FOR 137 ..Radiation detectors, e.g., infrared, etc. (437/3)
- FOR 138 ..Composed of polycrystalline material (437/4)
- FOR 139 ..Having semiconductor compound (437/5)
- FOR 140 **MAKING THYRISTOR, E.G., DIAC, TRIAC, ETC. (437/6)**
- FOR 141 **INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION (437/7)**
- FOR 142 **INCLUDING TESTING OR MEASURING (437/8)**
- FOR 143 **INCLUDING APPLICATION OF VIBRATORY FORCE (437/9)**
- FOR 144 **INCLUDING GETTERING (437/10)**
- FOR 145 ..By ion implanting or irradiating (437/11)
- FOR 146 ..By layers which are coated, contacted, or diffused (437/ 12)
- FOR 147 ..By vapor phase surface reaction (437/13)
- FOR 148 **THERMOMIGRATION (437/14)**
- FOR 149 **INCLUDING FORMING A SEMICONDUCTOR JUNCTION (437/15)**
- FOR 150 ..Using energy beam to introduce dopant or modify dopant distribution (437/ 16)
- FOR 151 ..Neutron, gamma ray or electron beam (437/17)
- FOR 152 ..Ionized molecules (437/18)
- FOR 153 ..Coherent light beam (437/19)
- FOR 154 ..Ion beam implantation (437/20)
- FOR 155 ..Of semiconductor on insulating substrate (437/21)
- FOR 156 ...Of semiconductor compound (437/22)
- FOR 157Light emitting diode (LED) (437/23)
- FOR 158 ...Providing nondopant ion including proton (437/24)
- FOR 159 ...Providing auxiliary heating (437/25)
- FOR 160 ...Forming buried region (437/26)

- FOR 161 ...Including multiple implantations of same region (437/27)
- FOR 162 ...Through insulating layer (437/28)
- FOR 163Forming field effect transistor (FET) type device (437/29)
- FOR 164 ...Using same conductivity type dopant (437/30)
- FOR 165 ...Forming bipolar transistor (NPN/PNP) (437/31)
- FOR 166Lateral bipolar transistor (437/32)
- FOR 167Having dielectric isolation (437/33)
- FOR 168 ...Forming complementary MOS (metal oxide semiconductor) (437/34)
- FOR 169 ...Using oblique beam (437/35)
- FOR 170 ...Using shadow mask (437/36)
- FOR 171 ...Having projected range less than thickness of dielectrics on substrate (437/37)
- FOR 172 ...Into shaped or grooved semiconductor substrate (437/38)
- FOR 173 ...Involving Schottky contact formation (437/39)
- FOR 202 ...Gate structure constructed of diverse dielectrics (437/42)
- FOR 203Gate surrounded by dielectric layer, e.g., floating gate, etc. (437/43)
- FOR 204Adjusting channel dimension (437/44)
- FOR 205Active step for controlling threshold voltage (437/45)
- FOR 185Self-aligned (437/41 R)
- FOR 186With bipolar (437/41 RBP)
- FOR 187CMOS (437/41 RCM)
- FOR 188Lightly doped drain (437/41 RLD)
- FOR 189Memory devices (437/41 RMM)
- FOR 190Asymmetrical FET (437/41 AS)
- FOR 191Channel specifics (437/41 CS)
- FOR 192DMOS/vertical FET (437/41 DM)
- FOR 193Gate specifics (437/41 GS)
- FOR 194Junction FET/static induction transistor (437/41 JF)
- FOR 195Layered channel (437/41 LC)
- FOR 196Specifics of metallization/contact (437/41 SM)
- FOR 197Recessed gate (Schottky falls below in SH) (437/41 RG)
- FOR 198Schottky gate/MESFET (437/41 SH)
- FOR 199Sidewall (437/41 SW)
- FOR 200Thin film transistor, inverted (437/41 TFI)
- FOR 201Thin film transistor (437/41 TFT)
- FOR 174 ...Forming pair of device regions separated by gate structure, i.e., FET (437/40 R)
- FOR 175 ...Asymmetrical FET (any asymmetry in S/D profile, gate spacing, etc.) (437/40 AS)
- FOR 176 ...DMOS/vertical FET (437/40 DM)
- FOR 177 ...Gate specific (specifics of gate insulator/structure/material/contact) (437/40 GS)
- FOR 178 ...Junction FET/static induction transistor (437/40 JF)
- FOR 179 ...Layered channel (e.g., HEMT, MODFET, 2DEG, heterostructure FETS) (437/40 LC)
- FOR 180 ...Recessed gate (437/40 RG)
- FOR 181 ...Schottky gate/MESFET (controls over RG) (437/40 SH)
- FOR 182 ...Sidewall (not LDDs) (437/40 SW)
- FOR 183 ...Thin film transistor inverted/staggered (437/40 TFI)
- FOR 184 ...Thin film transistor (437/40 TFT)
- FOR 206 ...Into polycrystalline or polyamorphous regions (437/46)
- FOR 207 ...Integrating active with passive devices (437/47)
- FOR 208 ...Forming plural active devices in grid/array, e.g., RAMS/ROMS, etc. (437/48)
- FOR 209 ...Having multiple-level electrodes (437/49)
- FOR 210 ...Forming electrodes in laterally spaced relationships (437/50)
- FOR 211 ..Making assemblies of plural individual devices having community feature, e.g., integrated circuit, electrical connection, etc. (437/51)
- FOR 212 ..Memory devices (437/52)

- FOR 213 ..Charge coupled devices (CCD) (437/53)
- FOR 214 ..Diverse types (437/54)
- FOR 215 ...Integrated injection logic (I2L) circuits (437/55)
- FOR 216 ...Plural field effect transistors (CMOS) (437/56)
- FOR 217Complementary metal oxide having diverse conductivity source and drain regions (437/57)
- FOR 218Having like conductivity source and drain regions (437/58)
- FOR 219 ...Including field effect transistor (437/59)
- FOR 220 ...Including passive device (437/60)
- FOR 221 ..Including isolation step (437/61)
- FOR 222 ..By forming total dielectric isolation (437/62)
- FOR 223 ..By forming vertical isolation combining dielectric and PN junction (437/63)
- FOR 224 ..Using vertical dielectric (air-gap/insulator) and horizontal PN junction (437/64)
- FOR 225 ...Grooved air-gap only (437/65)
- FOR 226V-groove (437/66)
- FOR 227 ...Grooved and refilled with insulator (437/67)
- FOR 228V-groove (437/68)
- FOR 229 ...Recessed oxide by localized oxidation (437/69)
- FOR 230Preliminary formation of guard ring (437/70)
- FOR 231Preliminary anodizing (437/71)
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- FOR 233Using overhanging oxidation mask and pretreatment of recessed walls (437/73)
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- FOR 235 ...By diffusion from upper surface only (437/75)
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- FOR 237Substrate and epitaxial regions of same conductivity type, i.e., P or N (437/77)
- FOR 238 ...By etching and refilling with semiconductor material having diverse conductivity (437/78)
- FOR 239 ...Using polycrystalline region (437/79)
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- FOR 243 ..Growing single crystal on amorphous substrate (437/83)
- FOR 244 ..Growing single crystal on single crystal insulator (SOS) (437/84)
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- FOR 246 ..Using transitory substrate (437/86)
- FOR 247 ..Using inert atmosphere (437/87)
- FOR 248 ..Using catalyst to alter growth process (437/88)
- FOR 249 ..Growth through opening (437/89)
- FOR 250 ...Forming recess in substrate and refilling (437/90)
- FOR 251By liquid phase epitaxy (437/91)
- FOR 252 ...By liquid phase epitaxy (437/92)
- FOR 253 ..Specified crystal orientation other than (100) or (111) planes (437/93)
- FOR 254 ..Introducing minority carrier life time reducing dopant during growth, i.e., deep level dopant Au (Gold), Cr (Cromium), Fe (Iron), Ni (Nickel), etc. (437/94)
- FOR 255 ..Autodoping control (437/95)
- FOR 256 ...Compound formed from Group III and Group V elements (437/96)
- FOR 257 ..Forming buried regions with outdiffusion control (437/97)
- FOR 258 ...Plural dopants simultaneously outdiffused (437/98)
- FOR 259 ..Growing mono and polycrystalline regions simultaneously (437/99)
- FOR 260 ..Growing silicon carbide (SiC) (437/100)
- FOR 261 ..Growing amorphous semiconductor material (437/101)
- FOR 262 ..Source and substrate in close-space relationship (437/102)

- FOR 263 ...Group IV elements (437/103)
FOR 264 ...Compound formed from Group III and Group V elements (437/104)
FOR 265 ..Vacuum growing using molecular beam, i.e., vacuum deposition (437/105)
FOR 266 ...Group IV elements (437/106)
FOR 267 ...Compound formed from Group III and Group V elements (437/107)
FOR 268 ..Growing single layer in multi-steps (437/108)
FOR 269 ...Polycrystalline layers (437/109)
FOR 270 ..Using modulated dopants or materials, e.g., superlattice, etc. (437/110)
FOR 271 ...Using preliminary or intermediate metal layer (437/111)
FOR 272 ...Growing by varying rates (437/112)
FOR 273 ..Using electric current, e.g., Peltier effect, glow discharge, etc. (437/113)
FOR 274 ..Using seed in liquid phase (437/114)
FOR 275 ...Pulling from melt (437/115)
FOR 276 ...And diffusing (437/116)
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FOR 279 ..Sliding liquid phase epitaxy (437/119)
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FOR 281 ...Controlling volume or thickness of growth (437/121)
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FOR 283 ...With nonlinear slide movement (437/123)
FOR 284 ...One melt simultaneously contacting plural substrates (437/124)
FOR 285 ..Tipping liquid phase epitaxy (437/125)
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FOR 287 ...Multi-color light emitting diode (LED) (437/127)
FOR 288 ...Graded composition (437/128)
FOR 289 ...Forming laser (437/129)
FOR 290 ...By liquid phase epitaxy (437/130)
FOR 291 ...Si (Silicon on Ge (Germanium) or Ge (Germanium) on Si (Silicon) (437/131)
FOR 292 ...Either Si (Silicon) or Ge (Germanium) layered with or on compound formed from Group III and Group V elements (437/132)
FOR 293 ...Compound formed from Group III and Group V elements on diverse Group III and Group V including substituted Group III and Group V compounds (437/133)
FOR 294 ..By fusing dopant with substrate, e.g., alloying, etc. (437/134)
FOR 295 ..Using flux (437/135)
FOR 296 ..Passing electric current through material (437/136)
FOR 297 ..With application of pressure to material during fusing (437/137)
FOR 298 ..Including plural controlled heating or cooling steps (437/138)
FOR 299 ..Including diffusion after fusion step (437/139)
FOR 300 ..Including additional material to improve wettability or flow characteristics (437/140)
FOR 301 ..Diffusing a dopant (437/141)
FOR 302 ..To control carrier lifetime, i.e., deep level dopant Au (Gold), Cr (Chromium), Fe (Iron), Ni (Nickel), etc. (437/142)
FOR 303 ..Al (Aluminum) dopant (437/143)
FOR 304 ..Li (Lithium) dopant (437/144)
FOR 305 ..Including nonuniform heating (437/145)
FOR 306 ..To solid state solubility concentration (437/146)
FOR 307 ..Using multiple layered mask (437/147)
FOR 308 ...Having plural predetermined openings in master mask (437/148)
FOR 309 ..Forming partially overlapping regions (437/149)
FOR 310 ..Plural dopants in same region, e.g., through same mask opening, etc. (437/150)
FOR 311 ...Simultaneously (437/151)
FOR 312 ..Plural dopants simultaneously in plural region (437/152)

- FOR 313 ..Single dopant forming plural diverse regions (437/153)
- FOR 314 ...Forming regions of different concentrations or different depths (437/154)
- FOR 315 ..Using metal mask (437/155)
- FOR 316 ..Outwardly (437/156)
- FOR 317 ..Laterally under mask (437/157)
- FOR 318 ..Edge diffusion by using edge portion of structure other than masking layer to mask (437/158)
- FOR 319 ..From melt (437/159)
- FOR 320 ..From solid dopant source in contact with substrate (437/160)
- FOR 321 ...Using capping layer over dopant source to prevent outdiffusion of dopant (437/161)
- FOR 322 ...Polycrystalline semiconductor source (437/162)
- FOR 323 ...Organic source (437/163)
- FOR 324 ...Glassy source or doped oxide (437/164)
- FOR 325 ..From vapor phase (437/165)
- FOR 326 ...In plural stages (437/166)
- FOR 327 ...Zn (Zinc) dopant (437/167)
- FOR 328 ...Solid source is operative relation with semiconductor material (437/168)
- FOR 329In capsule type enclosure (437/169)
- FOR 330 **DIRECTLY APPLYING ELECTRICAL CURRENT (437/170)**
- FOR 331 ..And regulating temperature (437/171)
- FOR 332 ..Alternating or pulsed current (437/172)
- FOR 333 **APPLYING CORPUSCULAR OR ELECTROMAGNETIC ENERGY (437/173)**
- FOR 334 ..To anneal (437/174)
- FOR 335 **FORMING SCHOTTKY CONTACT (437/175)**
- FOR 336 ..On semiconductor compound (437/176)
- FOR 337 ..Multi-layer electrode (437/177)
- FOR 338 ..Using platinum group silicide, i.e., silicide of Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium) (437/178)
- FOR 339 ..Using metal, i.e., Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium), Au (Gold), Ag (Silver) (437/179)
- FOR 340 **MAKING OR ATTACHING ELECTRODE ON OR TO SEMICONDUCTOR, OR SECURING COMPLETED SEMICONDUCTOR TO MOUNTING OR HOUSING (437/180)**
- FOR 341 ..Forming transparent electrode (437/181)
- FOR 342 ..Forming beam electrode (437/182)
- FOR 343 ..Forming bump electrode (437/183)
- FOR 344 ..Electrode formed on substrate composed of elements of Group III and Group V semiconductor compound (437/184)
- FOR 345 ..Electrode formed on substrate composed of elements of Group II and Group VI semiconductor compound (437/185)
- FOR 346 ..Single polycrystalline electrode layer on substrate (437/186)
- FOR 347 ..Single metal layer electrode on substrate (437/187)
- FOR 348 ..Subsequently fusing, e.g., alloying, sintering, etc. (437/188)
- FOR 349 ..Forming plural layered electrode (437/189)
- FOR 350 ..Including central layer acting as barrier between outer layers (437/190)
- FOR 351 ..Of polysilicon only (437/191)
- FOR 352 ..Including refractory metal layer of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten) (437/192)
- FOR 353 ..Including polycrystalline silicon layer (437/193)
- FOR 354 ..Including Al (Aluminum) layer (437/194)
- FOR 355 ..Including layer separated by insulator (437/195)
- FOR 356 ..Forming electrode of alloy or electrode of a compound of Si (Silicon) (437/196)
- FOR 357 ..Al (Aluminum) alloy (437/197)
- FOR 358 ...Including Cu (Copper) (437/198)

- FOR 359 ...Including Si (Silicon) (437/199)
- FOR 360 ..Silicide of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten), (437/200)
- FOR 361 ..Of platinum metal group Ru (Ruthenium), Rh (Rhodium), Pd (Palladium), Os (Osmium), Ir (Iridium), Pt (Platinum) (437/201)
- FOR 362 ..By fusing metal with semiconductor (alloying) (437/202)
- FOR 363 .Depositing electrode in preformed recess in substrate (437/203)
- FOR 364 .Including positioning of point contact (437/204)
- FOR 365 .Making plural devices (437/205)
- FOR 366 ..Using strip lead frame (437/206)
- FOR 367 ...And encapsulating (437/207)
- FOR 368 ..Stacked array, e.g., rectifier, etc. (437/208)
- FOR 369 .Securing completed semiconductor to mounting, housing or external lead (437/209)
- FOR 370 ..Including contaminant removal (437/210)
- FOR 371 ..Utilizing potting or encapsulating material only to surround leads and device to maintain position, i.e. without housing (437/211)
- FOR 372 ...Including application of pressure (437/212)
- FOR 373 ...Glass material (437/213)
- FOR 374 ..Utilizing header (molding surface means) (437/214)
- FOR 375 ..Insulating housing (437/215)
- FOR 376 ...Including application of pressure (437/216)
- FOR 377 ...And lead frame (437/217)
- FOR 378 ..Ceramic housing (437/218)
- FOR 379 ...Including encapsulating (437/219)
- FOR 380 ..Lead frame (437/220)
- FOR 381 ..Metallic housing (437/221)
- FOR 382 ...Including application of pressure (437/222)
- FOR 383 ...Including glass support base (437/223)
- FOR 384 ...Including encapsulating (437/224)
- FOR 385 **INCLUDING COATING OR MATERIAL REMOVAL, E.G., ETCHING, GRINDING, ETC. (437/ 225)**
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- FOR 387 ..With a perfecting coating (437/227)
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